CYPRESS SEMICONDUCTOR

Reprogrammable CMOS PAL® Device

Features

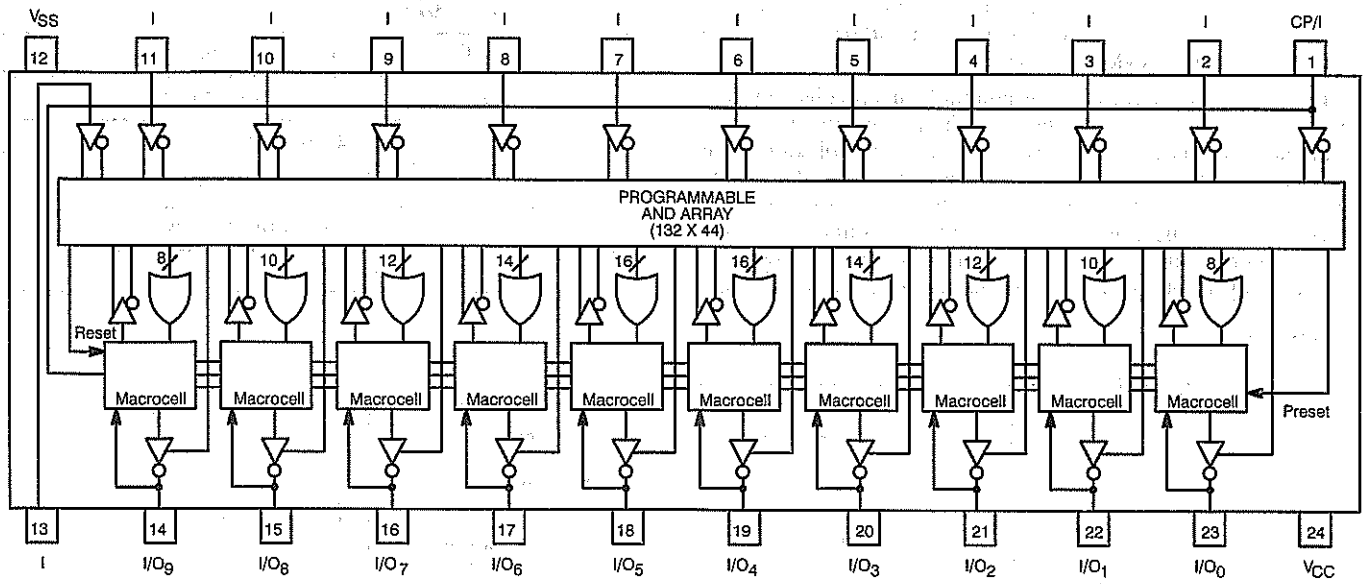
- Advanced second generation PAL architecture
- Low power
  - 90 mA max. standard
  - 100 mA max. military
- CMOS EPROM technology for reprogrammability
- Variable product terms
  - 2 x (8 through 16) product terms
- User-programmable macrocell
  - Output polarity control
  - Individually selectable for registered or combinatorial operation
  - "15" commercial and industrial
    10 ns t_{CO}
    10 ns t_S
    15 ns t_{PD}
    50 MHz
  - "15" and "20" military
    10/15 ns t_{CO}
    10/17 ns t_S
    15/20 ns t_{PD}
    50/31 MHz
- Up to 22 input terms and 10 outputs
- Enhanced test features
  - Phantom array
  - Top test
  - Bottom test
  - Preload
- High reliability
  - Proven EPROM technology
  - 100% programming and functional testing
- Windowed DIP, windowed LCC, DIP, LCC, PLCC available

Functional Description

The Cypress PALC22V10B is a CMOS second-generation programmable logic array device. It is implemented with the familiar sum-of-products (AND-OR) logic structure and a new concept, the "Programmable Macrocell."

The PALC22V10B is executed in a 24-pin 300-mil molded DIP, a 300-mil windowed cerDIP, a 28-lead square ceramic leadless chip carrier, a 28-lead square plastic leaded chip carrier, and provides up to 22 inputs and 10 outputs. When the windowed cerDIP is exposed to UV light, the 22V10B is erased and can then be reprogrammed. The programmable macrocell provides the capability of defining the architecture of each output individually. Each of the 10 potential outputs may be specified as "registered" or "combinatorial." Polarity of each output may also be

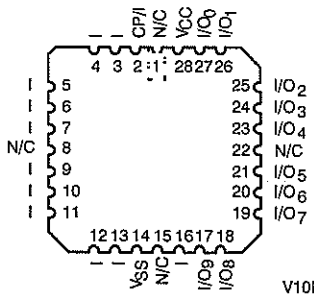
Logic Block Diagram (PDIP/CDIP)



V10B-1

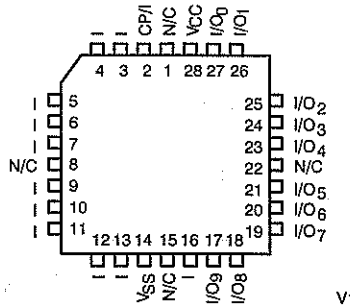
Pin Configurations

LCC
Top View



V10B-2

PLCC
Top View



V10B-3

PAL is a registered trademark of Monolithic Memories Inc.

Functional Description (continued)

individually selected, allowing complete flexibility of output configuration. Further configurability is provided through "array" configurable "output enable" for each potential output. This feature allows the 10 outputs to be reconfigured as inputs on an individual basis, or alternately used as a combination I/O controlled by the programmable array.

PALC22V10B features a "variable product term" architecture. There are 5 pairs of product terms beginning at 8 product terms per output and incrementing by 2 to 16 product terms per output. By providing this variable structure, the PALC22V10B is optimized to the configurations found in a majority of applications without creating devices that burden the product term structures with unusable product terms and lower performance.

Additional features of the Cypress PALC22V10B include a synchronous preset and an asynchronous reset product term. These product terms are common to all macrocells, eliminating the need to dedicate standard product terms for initialization function. The device automatically resets upon power-up.

For testing of programmed functions, a preload feature allows any or all of the registers to be loaded with an initial value for testing. This is accomplished by raising pin 8 to a supervoltage V_{PP}, which puts the output drivers in a high-impedance state. The data to be loaded is then placed on the I/O pins of the device and is loaded into the registers on the positive edge of the clock on pin 1. A 0 on the I/O pin preloads the register with a 0 and a 1 preloads the register with a 1. The actual signal on the output pin will be the inversion of the input data. The data on the I/O pins is then removed, and pin 8 returned to a normal TTL voltage. Care should be exercised to power sequence the device properly.

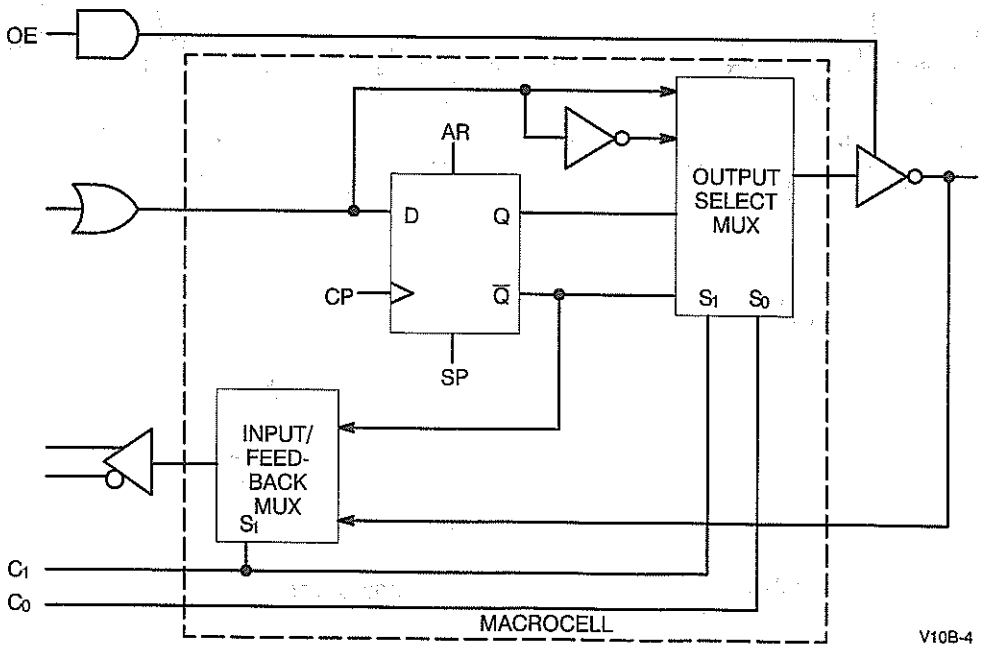
The PALC22V10B featuring programmable macrocells and variable product terms provides a device with the flexibility to implement logic functions in the 500 to 800 gate array complexity. Since each of the 10 output pins may be individually configured as inputs on a temporary or permanent basis, functions requiring up to 21 inputs and only a single output and down to 12 inputs and 10 outputs are possible. The 10 potential outputs are enabled using product terms. Any output pin may be permanently selected as an output or arbitrarily enabled as an output and an input through the selective use of individual product terms associated with each output. Each of these outputs is achieved through an individual programmable macrocell. These macrocells are programmable to provide a combinatorial or registered inverting or non-inverting output. In a registered mode of operation, the output of the register is fed back into the array, providing current status information to the array. This information is available for establishing the next result in applications such as control-state-machines. In a combinatorial configuration, the combinatorial output or, if the output is disabled, the signal present on the I/O pin is made available to the array. The flexibility provided by both programmable macrocell product term control of the outputs and variable product terms allows a significant gain in functional density through the use of a programmable logic.

Along with this increase in functional density, the Cypress PALC22V10B provides lower-power operation through the use of CMOS technology, increased testability with a register preload feature, and guaranteed AC performance through the use of a phantom array. This phantom array ($P_0 - P_3$) and the "top test" and "bottom test" features allow the 22V10B to be programmed with a test pattern and tested prior to shipment for full AC specifications without using any of the functionality of the device specified for the product application. In addition, this same phantom array may be used to test the PALC22V10B at incoming inspection before committing the device to a specific function through programming. Preload facilitates testing programmed devices by loading initial values into the registers.

Configuration Table 2

Registered/Combinatorial		
C_1	C_0	Configuration
0	0	Registered/Active LOW
0	1	Registered/Active HIGH
1	0	Combinatorial/Active LOW
1	1	Combinatorial/Active HIGH

Macrocell



Selection Guide

Generic Part Number	I_{CC1} mA		t_{PD} ns		t_S ns		t_{CO} ns	
	Com/Ind	Mil	Com/Ind	Mil	Com/Ind	Mil	Com/Ind	Mil
22V10B–15	90	100	15	15	10	10	10	10
22V10B–20	–	100	–	20	–	17	–	15

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

Output Current into Outputs (Low) ..... 16 mA

UV Exposure ..... 7258 Wsec/cm^2

DC Programming Voltage 13.0V

Latch-Up Current ..... >200 mA

Static Discharge Voltage (per MIL–STD 883 Method 3015) ..... >2001V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±10%
Military[1]	– 55°C to +125°C	5V ±10%
Industrial	–40°C to +85°C	5V ±10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions			Min.	Max.	Units
V_{OH1}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3.2 mA	Com'l/Ind	2.4		V
			I_{OH} = –2 mA	Mil			
V_{OH2}	HIGH Level CMOS Output Voltage[3]	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100 µA		V_{CC} – 1.0V		
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA	Com'l/Ind		0.5	V
			I_{OL} = 12 mA	Mil			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[4]			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[4]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$, V_{CC} = Max.			–10	10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			–40	40	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3, 5]			–30	–90	mA
I_{CC1}	Standby Power Supply Current	V_{CC} = Max., V_{IN} = GND Outputs Open for Unprogrammed Device		Com'l/Ind		90	mA
				Mil		100	mA
I_{CC2}	Operating Power Supply Current	f_{toggle} = F_{MAX}[3] Device Programmed with Worst Case Pattern, Outputs Three-Stated		Com'l/Ind		90	mA
				Mil		100	mA

Notes:

1. t_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Tested initially and after any design or process changes that may affect these parameters.
4. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
5. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

Capacitance[3]

Parameters	Description	Typical	Max.	Units
C_{IN}	Input Capacitance	11		pF
C_{OUT}	Output Capacitance	9		pF

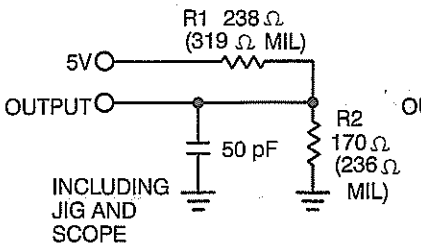
Switching Characteristics PALC22V10[2, 6]

Parameters	Description	Commercial & Industrial B–15		Military B–15		Military B–20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[7]		15		15		20	ns
t_{EA}	Input to Output Enable Delay		15		15		20	ns
t_{ER}	Input to Output Disable Delay[8]		15		15		20	ns
t_{CO}	Clock to Output Delay[9]		10		10		15	ns
t_S	Input or Feedback Set-Up Time	10		10		17		ns
t_H	Input Hold Time	0		0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	20		20		32		ns
t_{WH}	Clock Width HIGH[3]	6		6		12		ns
t_{WL}	Clock Width LOW[3]	6		6		12		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[10]	50.0		50		31.2		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[3, 11]	83.3		83.3		41.6		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[12]	80.0		80		33.3		MHz
t_{CF}	Register Clock to Feedback Input[13]		2.5		2.5		13	ns
t_{AW}	Asynchronous Reset Width	15		15		20		ns
t_{AR}	Asynchronous Reset Recovery Time	10		12		20		ns
t_{AP}	Asynchronous Reset to Registered Output Delay		20		20		25	ns
t_{SPR}	Synchronous Preset Recovery Time	10		20		20		ns
t_{PR}	Power-Up Reset Time[14]	1.0		1.0		1.0		µs

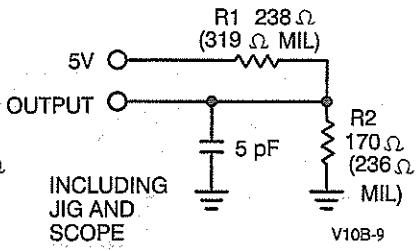
Notes:

6. Part (a) of AC Test Loads and Waveforms used for all parameters except t_{EA}, t_{ER}, t_{PZX}, and t_{PXZ}. Part (b) of AC Test Loads and Waveforms used for t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}.
7. This specification is guaranteed for all device outputs changing state in a given access cycle. See part (d) of AC Test Loads and Waveforms for the minimum guaranteed negative correction which may be subtracted from t_{PD} for cases in which fewer outputs are changing state per access cycle.
8. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max. Please see part (e) of AC Test Loads and Waveforms for enable and disable test waveforms and measurement reference levels.
9. This specification is guaranteed for all device outputs changing state in a given access cycle. See part (d) of AC Test Loads and Waveforms for the minimum guaranteed negative correction which may be subtracted from t_{CO} for cases in which fewer outputs are changing state per access cycle.
10. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
11. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
12. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate. This parameter is tested periodically by sampling production product.
13. This parameter is calculated from the clock period at f_{MAX} internal ($1/f_{MAX3}$) as measured (see Note 12 above) minus t_S.
14. The registers in the PALC22V10B has been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in V_{CC} must be monotonic and the timing constraints depicted in Power-Up Reset Waveform must be satisfied.

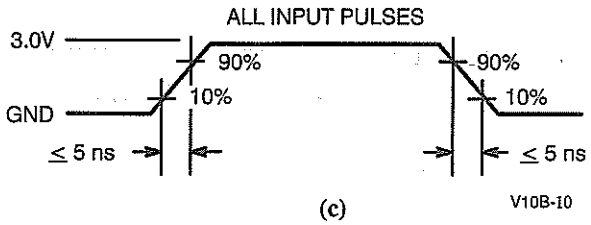
AC Test Loads and Waveforms (Commercial)



(a)

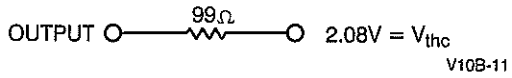


(b)

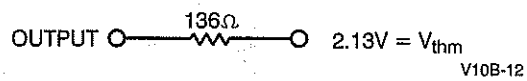


(c)

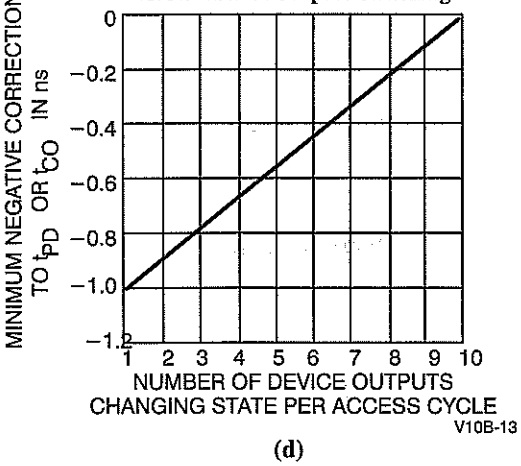
Equivalent to: THÉVENIN EQUIVALENT (Commercial)



Equivalent to: THÉVENIN EQUIVALENT (Military)



Minimum Negative Correction to t_{PD} and t_{CO} vs. Number of Outputs Switching

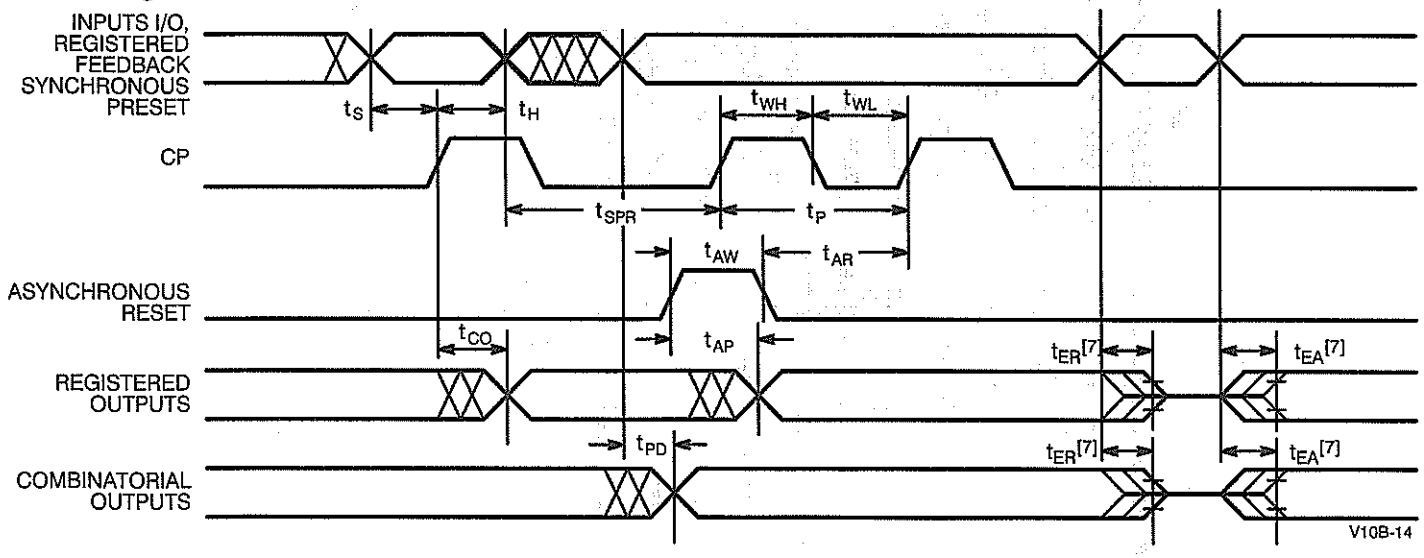


(d)

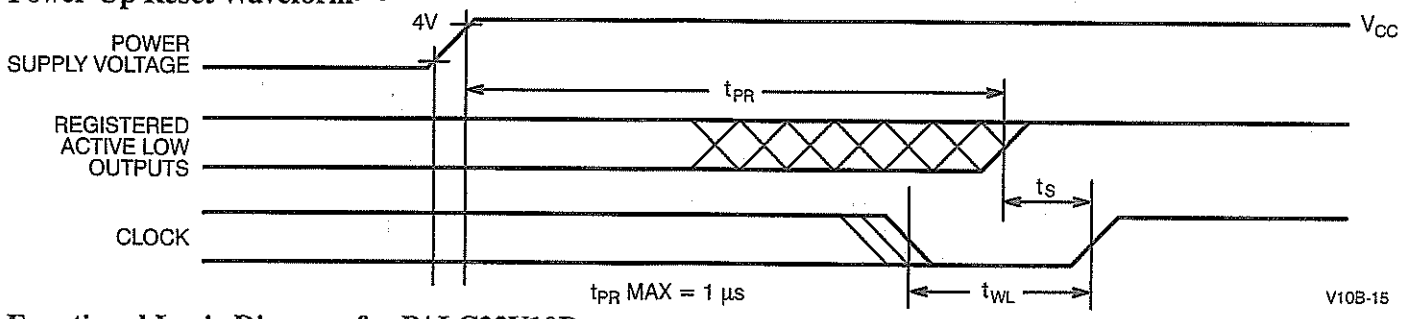
Parameter	V_X	Output Waveform—Measurement Level
t_{ER} (−)	1.5V	V_{OH} 0.5V V_X V10B-5
t_{ER} (+)	2.6V	V_{OL} 0.5V V_X V10B-6
t_{EA} (+)	V_{thc}	V_X 0.5V V_{OH} V10B-7
t_{EA} (−)	V_{thc}	V_X 0.5V V_{OL} V10B-8

(e) Test Waveforms

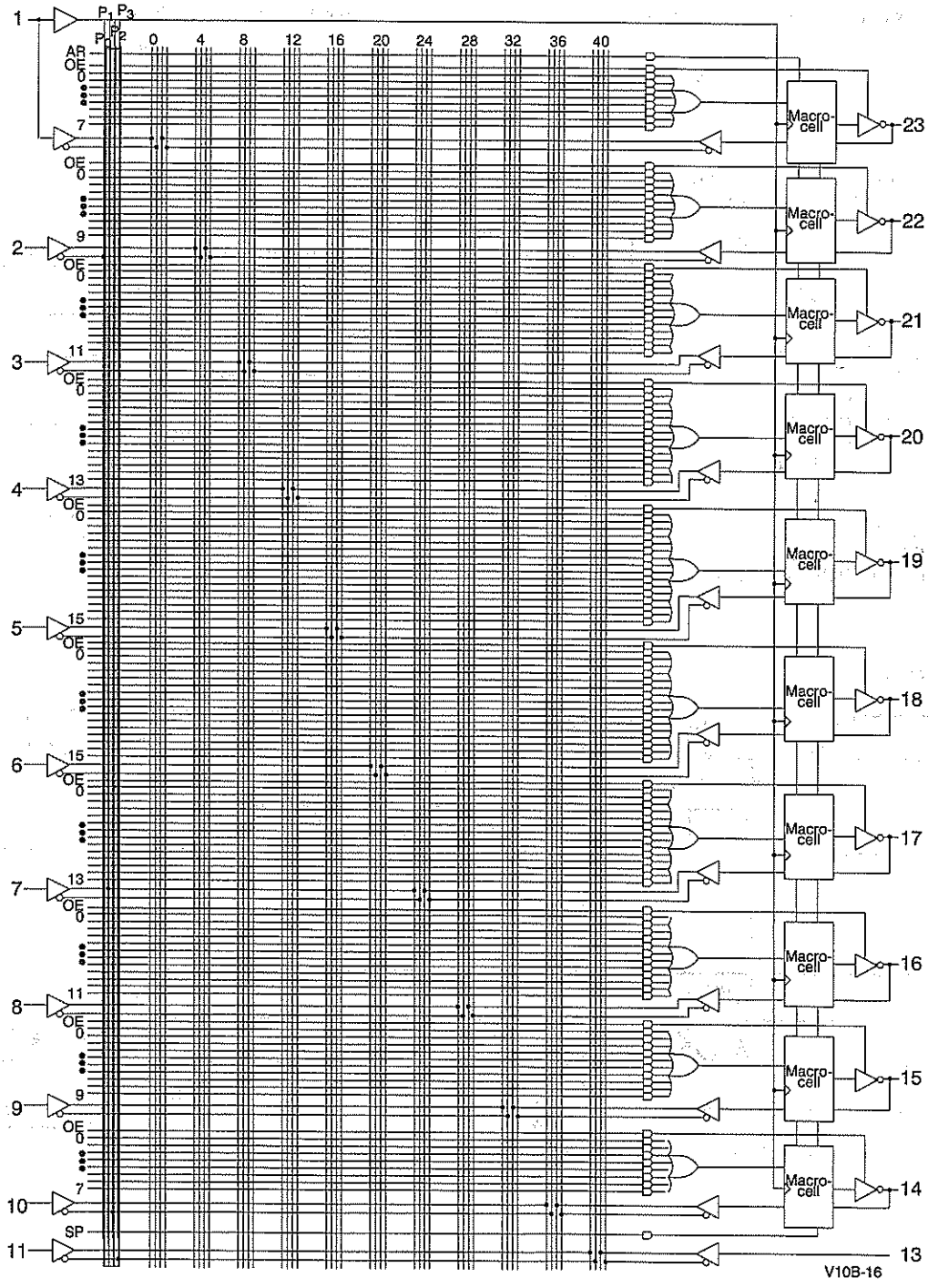
Switching Waveform



Power-Up Reset Waveform[14]

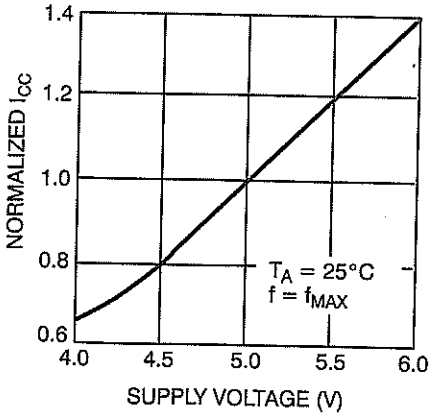


Functional Logic Diagram for PALC22V10B

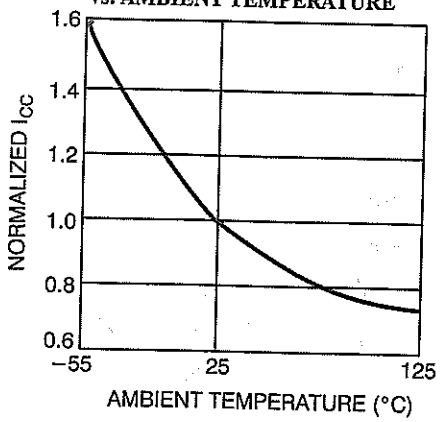


Typical DC and AC Characteristics

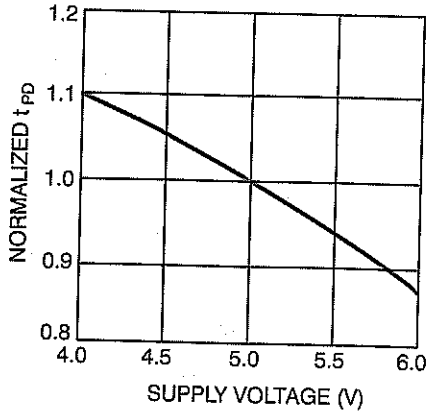
NORMALIZED STANDBY SUPPLY CURRENT (I_{CC1}) vs. SUPPLY VOLTAGE



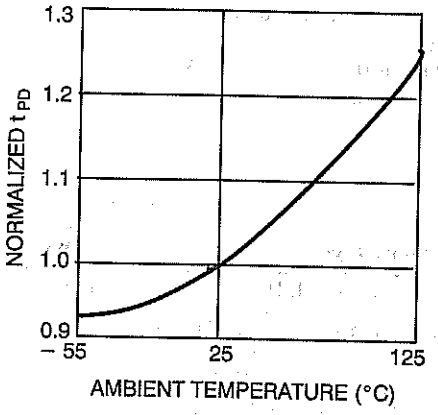
NORMALIZED STANDBY SUPPLY CURRENT (I_{CC1}) vs. AMBIENT TEMPERATURE



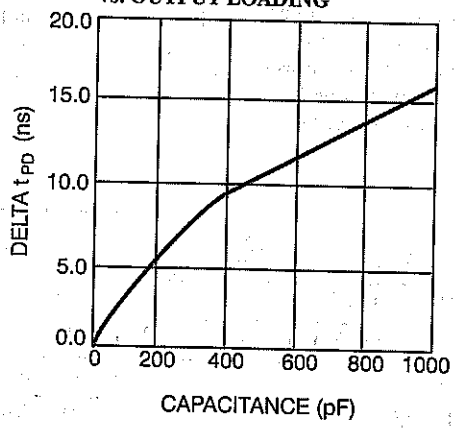
NORMALIZED PROPAGATION DELAY vs. SUPPLY VOLTAGE



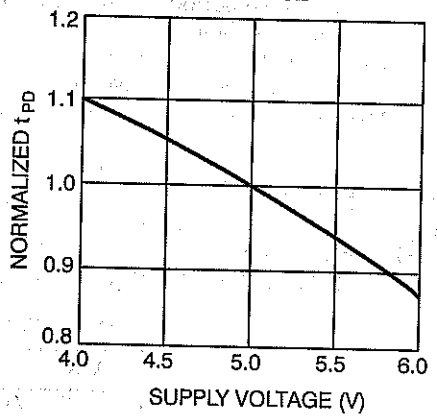
NORMALIZED PROPAGATION DELAY vs. TEMPERATURE



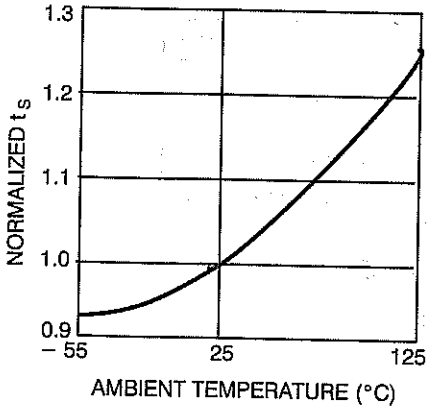
DELTA PROPAGATION TIME vs. OUTPUT LOADING



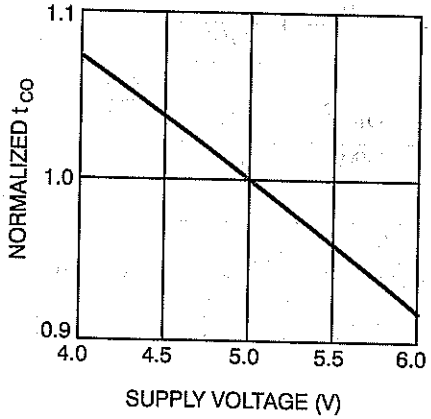
NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE



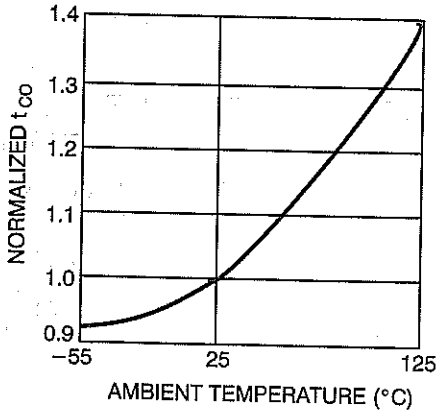
NORMALIZED SET-UP TIME vs. TEMPERATURE



NORMALIZED CLOCK TO OUTPUT TIME vs. SUPPLY VOLTAGE



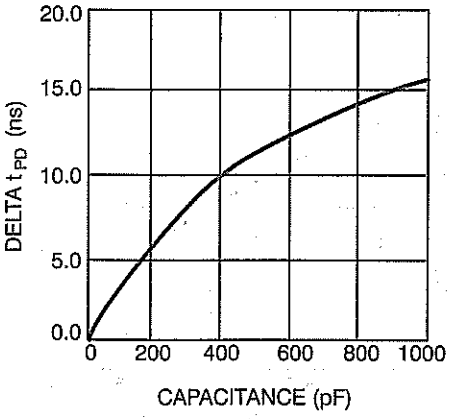
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



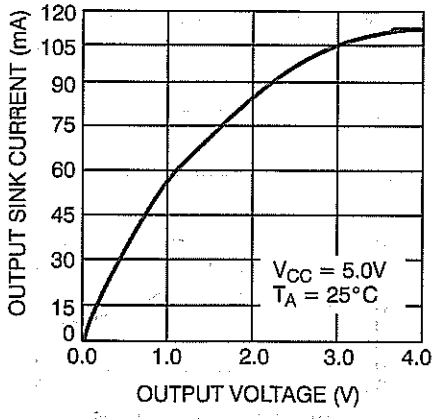
V10B-17

Typical DC and AC Characteristics (continued)

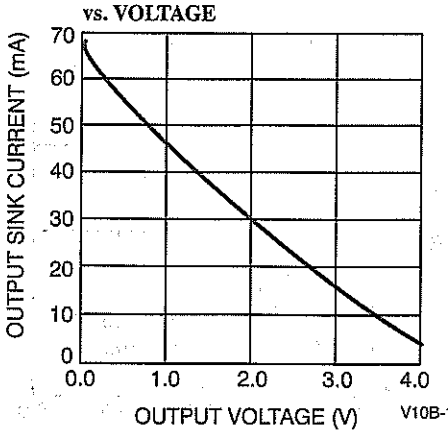
DELTA CLOCK TO OUTPUT TIME vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. VOLTAGE



V10B-18

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the PALC22V10B. For this reason, an opaque label should be placed over the window if the device is exposed to sunlight or fluorescent lighting for extended periods of time. In addition, high ambient light levels can create hole-electron pairs that may cause "blank" check failures or "verify errors" when programming windowed parts. This phenomenon can be avoided by use of an opaque label over the window during programming in high ambient light environments.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure would be approximately 35 minutes. The PALC22V10B needs to be placed within 1 inch of the lamp during erasure. Permanent damage may result if the device is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Ordering Information

I_{CC} (mA)	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package Name	Package Type	Operating Range
90	15	10	10	PALC22V10B–15PC/PI	P13	24-Lead (300-Mil) Molded DIP	Commercial/ Industrial
				PALC22V10B–15WC/WI	W14	24-Lead (300-Mil) Windowed CerDIP	
				PALC22V10B–15JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
				PALC22V10B–15HC	H64	28-Pin Windowed Leaded Chip Carrier	
100	15	10	10	PALC22V10B–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PALC22V10B–15WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
				PALC22V10B–15HMB	H64	28-Pin Windowed Leaded Chip Carrier	
				PALC22V10B–15LMB	L64	28-Square Leadless Chip Carrier	
				PALC22V10B–15QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
				PALC22V10B–15KMB	K73	24-Lead Rectangular Cerpack	
100	20	17	15	PALC22V10B–20DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PALC22V10B–20WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
				PALC22V10B–20HMB	H64	28-Pin Windowed Leaded Chip Carrier	
				PALC22V10B–20LMB	L64	28-Square Leadless Chip Carrier	
				PALC22V10B–20QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
				PALC22V10B–20KMB	K73	24-Lead Rectangular Cerpack	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{PD}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_S	7, 8, 9, 10, 11
t_H	7, 8, 9, 10, 11

Document #: 38−00195