Data Sheet

PAW3335DB-TZDU: Low Power Optical Gaming Navigation Chip

General Description

PAW3335DB-TZDU is PixArt Imaging's new low power gaming navigation chip suitable for wired and wireless gaming application. It has the latest state-of-the-art low-power architecture and automatic power management modes, making it ideal for battery-operated, power-sensitive cordless gaming devices. It provides excellent gaming experience with the features of high speed and high resolution even in low power mode to fulfill gamers' need. It is packaged in an 8pin staggered dual-in-line package (DIP) and designed to be used with L0AC-LSG1 lens to achieve optimum performance.

Key Features

- Low power consumption of typical 1.7mA @ run mode
- Programmable rest modes
- Small form factor PDIP 8L molded lead-frame package
- Operating Voltage: 1.80V - 2.10V
- High speed motion detection 400ips and acceleration 40g
- Selectable resolutions up to 16000cpi
- Three-wire serial port interface (SDIO)
- Internal oscillator — no clock input needed
- Customizable response time and downshift time for rest modes
- Angle snapping
- Lift detection options
  - 1mm setting
  - 2mm setting

Applications

- Wired and wireless Gaming Optical Mouse
- Trackball application

Key Parameters

Parameter	Value
Power Supply Voltage (V)	VDD: 1.80 – 2.10V
Interface	3-wire Serial Peripheral Interface
Supply Current @ VDD = 1.9V *Note: includes LED current*	Run: 1.7 mA Power Down: 3uA
Resolution (cpi)	Up to 16000
Tracking Speed (ips)	400
Acceleration (g)	40
Package Type (mm)	8L PDIP, 9.9 x 12.85 x 6.1

Ordering Information

Part Number	Package Type
PAW3335DB-TZDU	8L PDIP
L0AC-LSG1	Small Trim Lens

RoHS compliant

For any additional inquiries, please contact us at http://www.pixart.com

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1.0 Introduction

1.1 Overview

PAW3335DB-TZDU is based on Optical Navigation Technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement. PAW3335DB-TZDU contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP), and a three-wire serial port. The IAS acquires microscopic surface images via the lens and illumination system. These images are processed by the DSP to determine the direction and distance of motion. The DSP calculates the ΔX and ΔY relative displacement values. An external microcontroller reads and translates the ΔX and ΔY information from the chip serial port into PS2, USB, or RF signals before sending them to the host PC.

Note: Throughout this document PAW3335DB-TZDU is referred to as the chip.

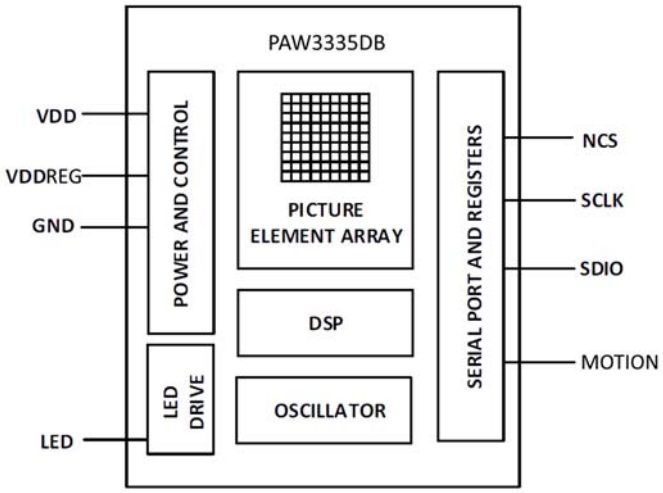


Figure 1. Functional Block Diagram

1.2 Terminology

Term	Description
DSP	Digital Signal Processing
LED	Light Emitting Diode
NCS	Chip Select
VDDREG	LDO output for digital core
VDD	Supply voltage
SCLK	Serial Clock
SDIO	Serial Data In & Out
SPI	Serial Peripheral Interface
GND	Ground
MOTION	Motion Detect

Pins Description

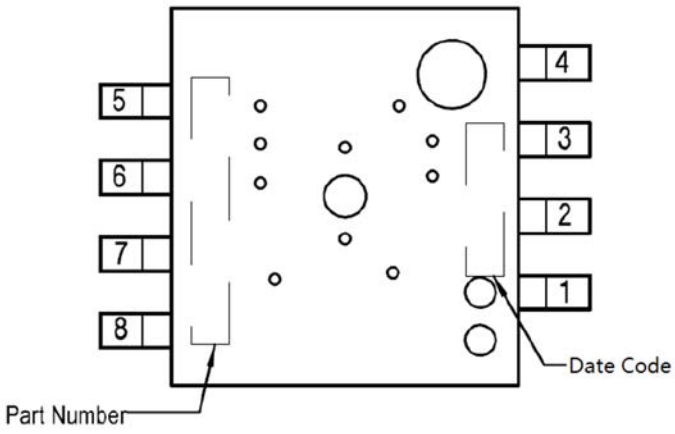


Figure 2. Pin Configuration

Table 1. PAW3335DB-TZDU Pins Description

Pin No.	Name	Type	Description
1	LED	Input	LED Illumination Control input
2	VDDREG	Power	LDO output (only for sensor internal usage).
3	VDD	Power	Power supply
4	SCLK	Input	Serial clock input
5	MOTION	Output	Motion Detect
6	GND	Gnd	Ground
7	SDIO	Input/Output	Serial data in/out
8	NCS	Input	Chip select (active low)

2.0 Operating Specifications

2.1 Regulatory Requirements

- Passes FCC "Part15 Subpart, Class B", "ICES-003:2016 Issue 6, Class B" and "ANSI C63.4:2014" when assembled into a mouse with shielded USB cable using ferrite bead and following PixArt's recommendations.
- Passes IEC 62471:2006 Photo biological safety of lamps and lamp systems.

2.2 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	T_S	-40	85	°C	
Lead Solder Temperature	T_{SOLDER}		260	°C	For 10 seconds, 1.6mm below seating plane
Supply Voltage	V_{DD}	-0.5	2.1	V	Including V_{NA} of 100 mV_{pp}
ESD	ESD_{HBM}		2	kV	All pins, Human Body Model
Input Voltage	V_{IN}	-0.5	VDD	V	All I/O pins

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are the stress ratings only and functional operation of the device at these or any other condition beyond those indicated for extended period of time may affect device reliability.
2. The maximum ratings do not reflect eye-safe operation.
3. The inherent design of this component causes it to be sensitive to electrostatic discharge. The ESD threshold is listed above. To prevent ESD induced damage, take adequate ESD precautions when handling this product

2.3 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Temperature	T_A	0		40	°C	
Power Supply Voltage	V_{DD}	1.8	1.9	2.1	V	Including V_{NA} of 100 mV_{pp}
Power Supply Rise Time	t_{RT}	0.15		20	ms	0 to Min. VDD
Supply Noise	V_{NA}			100	mV_{p-p}	10kHz – 75MHz
Serial Port Clock Frequency	f_{SCLK}			8	MHz	Active drive, 50% duty cycle
Distance from Lens Reference Plane to Tracking Surface	Z	2.20	2.40	2.60	mm	
Speed	S	400			ips	PixArt standard gaming surfaces
Acceleration	A	40			g	In run mode PixArt standard gaming surfaces
Load Capacitance	C_L			20	pF	SDIO, MOTION
Lift Cutoff 1mm setting	$Lift_{1mm}$		1		mm	L0AC-LSG1
Lift Cutoff 2mm setting	$Lift_{2mm}$		2		mm	L0AC-LSG1

Note: PixArt does not guarantee the chip performance if the operating temperature is beyond the specified limit.

2.4 Thermal Specifications

Table 4. Thermal Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	T_S	-25	-	80	°C	
Lead-free Solder Temperature	T_P	-	-	260	°C	For 10 seconds, 1.6mm below seating plane for wave soldering

2.5 DC Characteristics

Table 5. DC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
DC Supply Current in various modes Note: Includes I_{LED}	I_{DD_RUN}		1.7		mA	Average Run current
	I_{DD_REST1}		610		uA	
	I_{DD_REST2}		25		uA	
	I_{DD_REST3}		5		uA	No load on SDIO & MOTION
Power Down Current	I_{PD}		3		uA	
Input Low Voltage	V_{IL}			0.3* VDD	V	SCLK, SDIO, NCS
Input High Voltage	V_{IH}	0.7* VDD			V	SCLK, SDIO, NCS
Input Hysteresis	V_{I_HYS}		100		mV	SCLK, SDIO, NCS,
Input Leakage Current	I_{LEAK}		± 1	± 10	uA	Vin=VDD or 0V, SCLK, SDIO, NCS
Output Low Voltage	V_{OL}			0.45	V	I_{OUT} = 1mA, SDIO, MOTION
Output High Voltage	V_{OH}	VDD-0.45			V	I_{OUT} = -1mA, SDIO, MOTION
Input Capacitance	C_{in}		10		pF	SCLK, SDIO, NCS

Note: All the parameters are tested under recommended operating conditions. Typical values at 25 °C, V_{DD} = 1.9 V & LED current = 24mA

2.6 AC Characteristics

Table 6. AC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Motion Delay After Reset	$t_{MOT-RST}$	50			ms	From reset to valid motion, assuming motion is present
Shutdown	t_{STDWN}			500	ms	From Shutdown mode active to low current This timing could be affected by Rest3 period
Wake up from Shutdown	t_{WAKEUP}	50			ms	From Shutdown mode inactive to valid motion. Notes: A RESET must be asserted after a shutdown. Refer to section "5.2 Power Down Sequence", also note $t_{MOT-RST}$.
SDIO Output Rise Time	t_{r-SDIO}		6		ns	C_L = 20pF
SDIO Output Fall Time	t_{f-SDIO}		6		ns	C_L = 20pF
SDIO Output Delay After SCLK	$t_{DLY-SDIO}$			38	ns	From SCLK falling edge to SDIO output data valid C_L = 20pF
SDIO Output Hold Time	$t_{hold-SDIO}$	31.25			ns	Data held until next falling SCLK edge
SDIO input Hold Time	$t_{hold-SDIO\ input}$	31.25			ns	Amount of time data is valid after SCLK rising edge
SDIO input Setup Time	$t_{setup-SDIO\ input}$	31.25			ns	From data valid to SCLK rising edge
SPI Time Between Write Commands	t_{SWW}	5			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte.
SPI Time Between Write And Read Commands	t_{SWR}	5			µs	From rising SCLK for last bit of the 1st data byte, to rising SCLK for last bit of the second address byte
SPI Time Between Read And Subsequent Commands	t_{SRW} t_{SRR}	2			µs	From rising SCLK for last bit of the 1st data byte, to falling SCLK for the 1st bit of data being read.
SPI Read Address-Data Delay	t_{SRAD}	2			µs	From rising SCLK for last bit of the address byte, to falling SCLK for the 1st bit of data being read.
NCS Inactive After Motion Burst	t_{BEXIT}	500			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS To SCLK Active	$t_{NCS-SCLK}$	120			ns	From last NCS falling edge to 1st SCK rising edge.

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
SCLK To NCS Inactive SDIO Read	$t_{SCLK-NCS\ read}$	120			ns	From last SCLK rising edge to NCS rising edge, for valid SDIO data transfer
SCLK To NCS Inactive SDIO Write	$t_{SCLK-NCS\ write}$	1			µs	From last SCLK rising edge to NCS rising edge, for valid SDIO data transfer
NCS To SDIO High-Z	$t_{NCS-SDIO}$			500	ns	From NCS rising edge to SDIO high-Z state
Transient Supply Current	IDDT		70		mA	Max supply current during the supply ramp from 0V to V_{DD} with min 150us and max 20ms rise time. (Does not include charging currents of bypass capacitors)

Note: All the parameters are tested under recommended operating conditions. Typical values at 25 °C & VDD=1.9V

3.0 Mechanical Specifications

3.1 Mechanical Dimension

Table 7. Package Dimensions

Parameters	Nominal	Min.	Max.	Unit
Package Body Dimension X	9.90	9.80	10.00	mm
Package Body Dimension Y	9.10	9.00	9.20	mm
Package Width (inclusive pins)	12.85	12.35	13.35	mm
Lead Length	5.15	5.05	5.25	mm
Lead Pitch	2.00	1.85	2.15	mm
Total Lead Count	8	-	-	-
Lead Offset	1.00	-	-	mm
Lead Width	0.50	0.40	0.60	mm
Hole Diameter	0.70	0.65	0.75	mm
Center of Hole from edge of body X	4.55	4.45	4.65	mm
Center of Hole from edge of body Y	3.92	3.82	4.02	mm

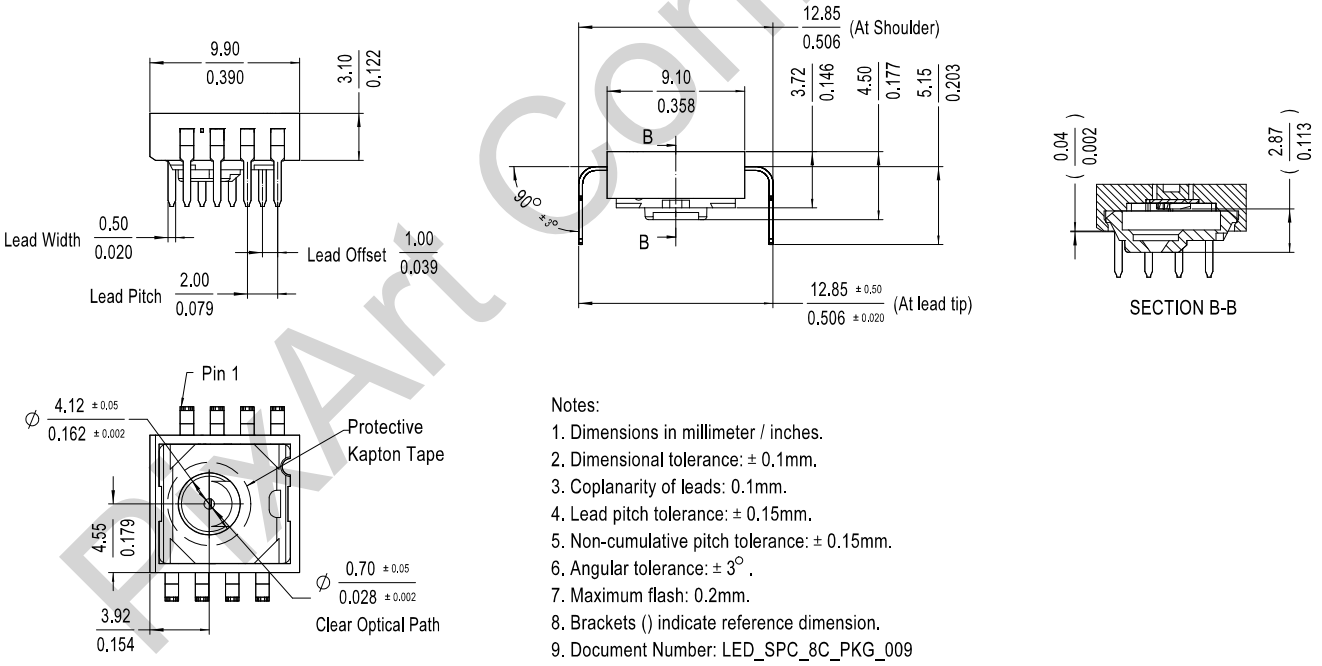


Figure 3. Package Drawing Outline

3.2 Assembly Drawings

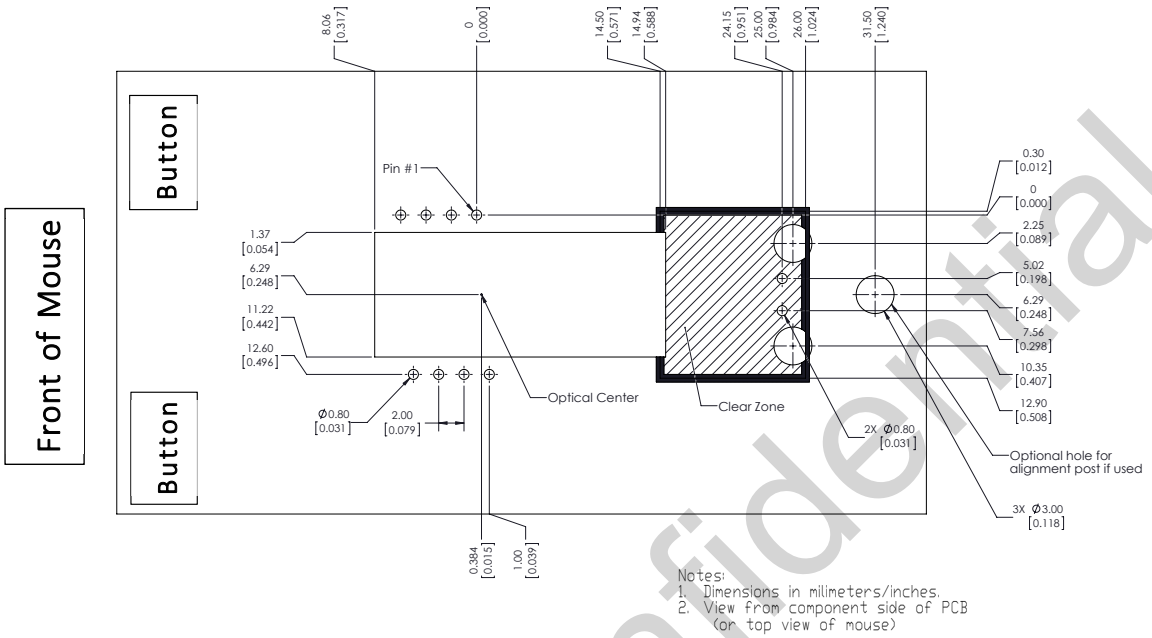


Figure 4. Recommended chip orientation, mechanical cutouts & spacing (Top View)

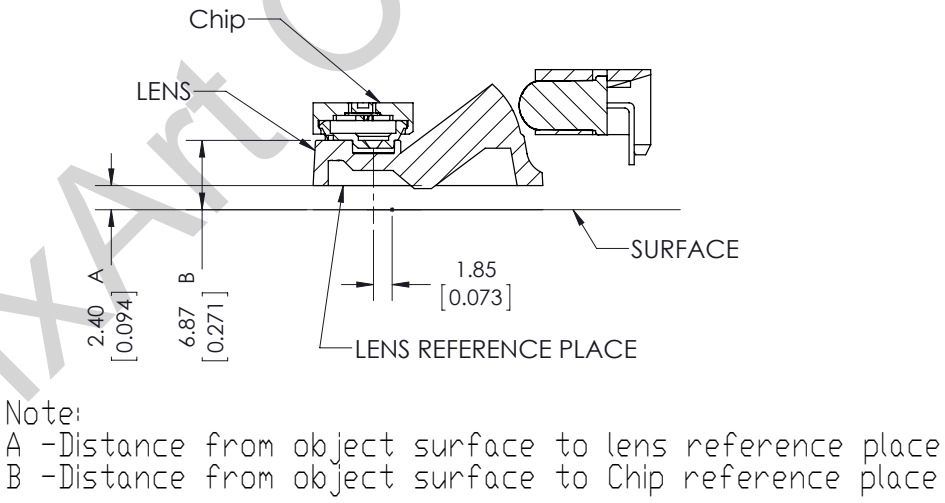


Figure 5. Distance from Lens Reference Plane to Surface

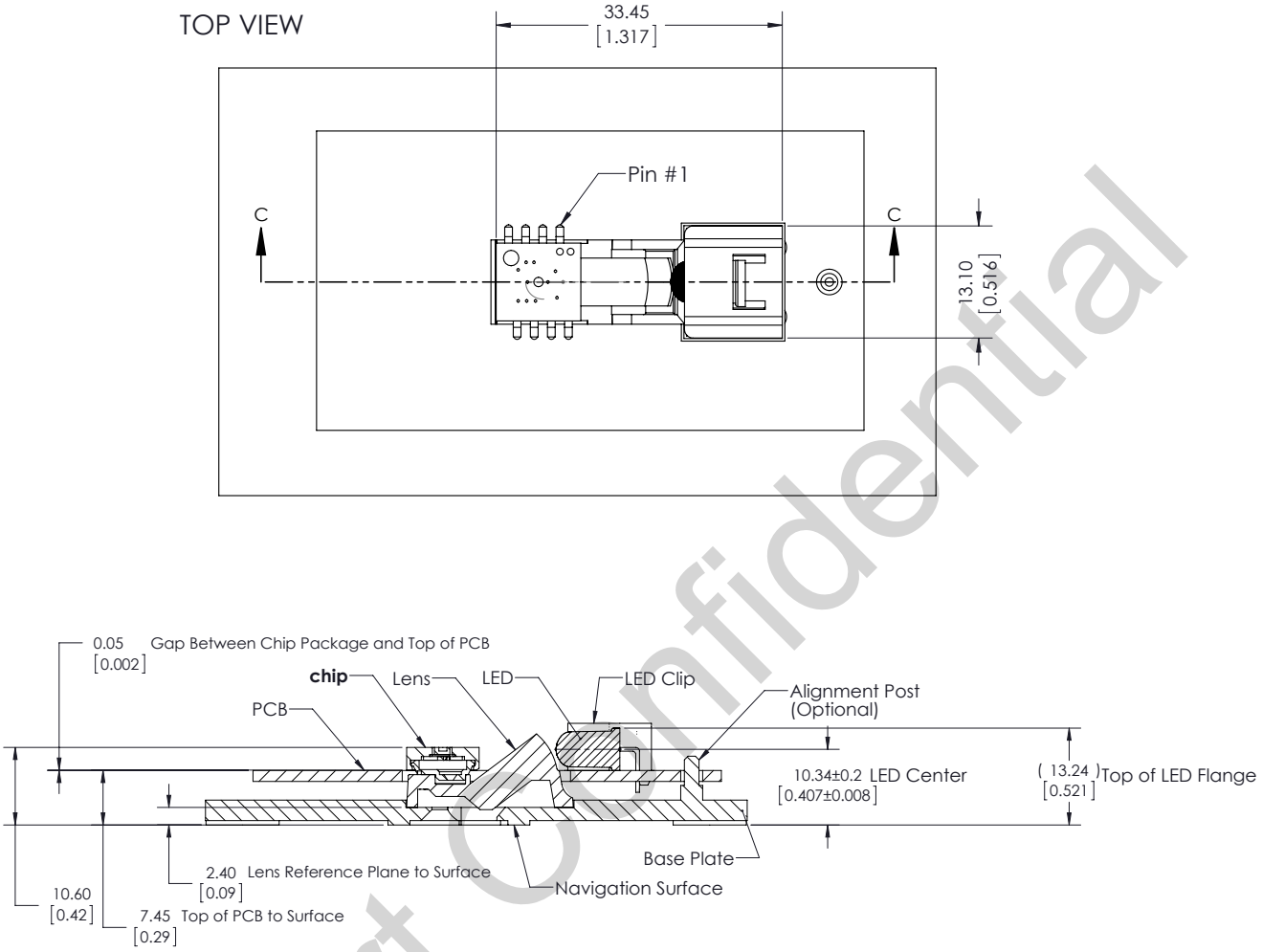


Figure 6. 2D Assembly

Note: The LED should be bent 90 degree with LED flange touching the PCB.

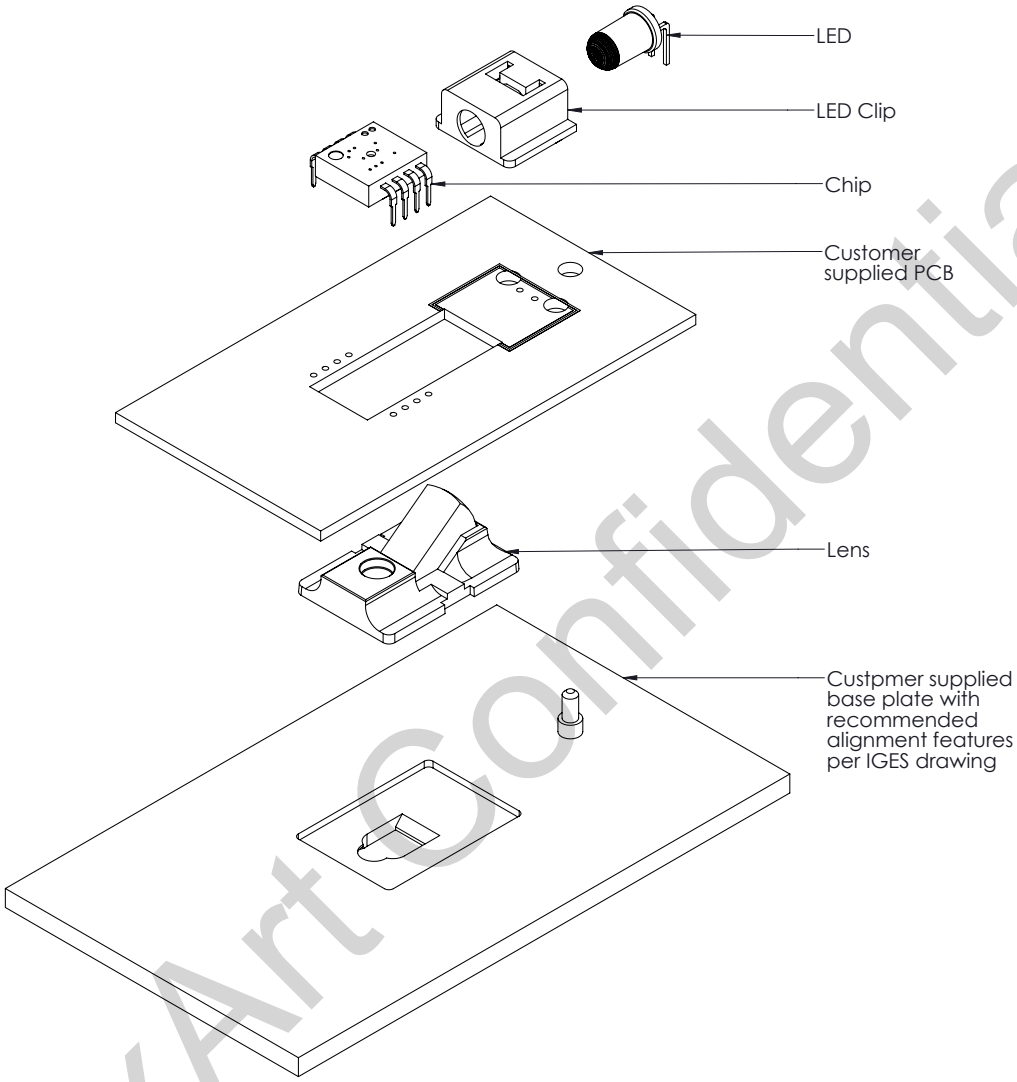
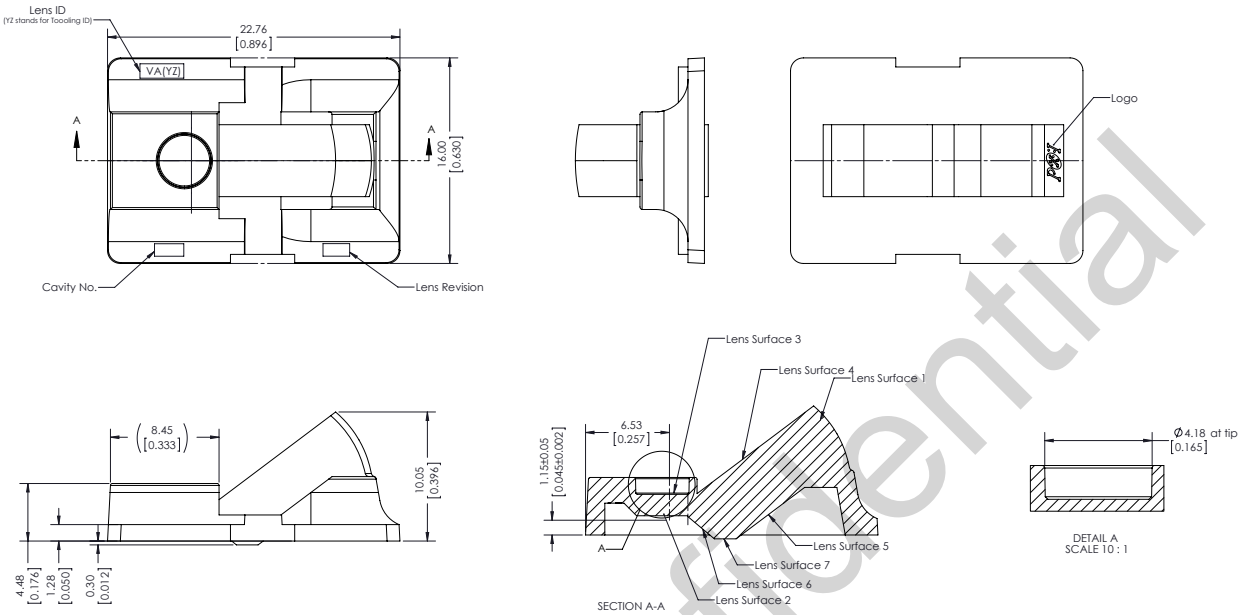


Figure 7. 2D Mouse Assembly



Notes:
1.0 Dimension in milimeters [inches]
2.0 General dimension tolerance: ±0.10mm
unless specified otherwise
3.0 Angular tolerance: ±3.0°
4.0 Maximum flash: 0.20mm
5.0 Bracket ( ) indicates reference dimension
6.0 Optical details removed
7.0 Document Number: L0AC-LSG-G8_003

Figure 8. L0AC-LSG1 Lens Outline Drawing

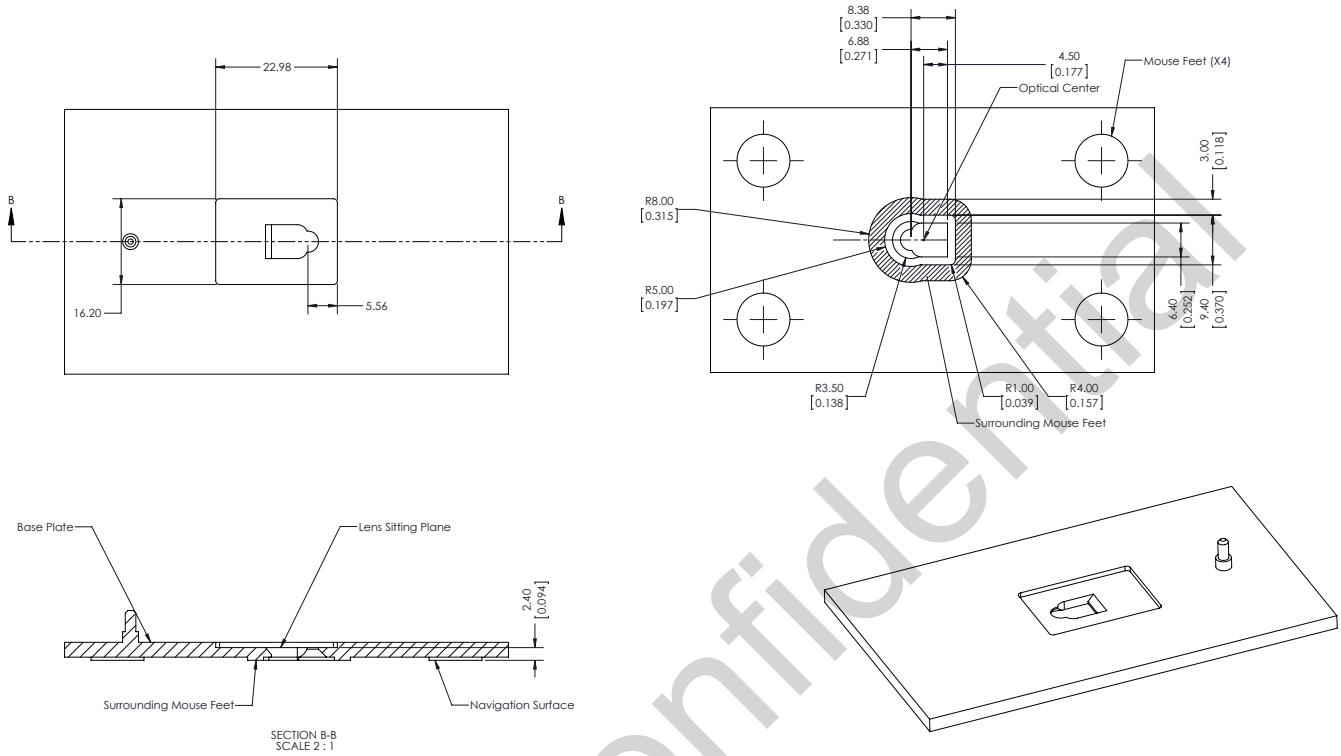


Figure 9. Recommended Base Plate Design with L0AC-LSG1 Lens

3.3 Package Marking

Refer to Figure 2. Pin Configuration

Table 8. Code Identification

Code	Marking	Description
Product Number	PAW3335DB-TZDU	Part number label
Lot Code	YYWWXXXXX	YYWW=Date code XXXXX= PixArt Reserved

4.0 System Level Description

4.1 Reference Application Schematic Diagram

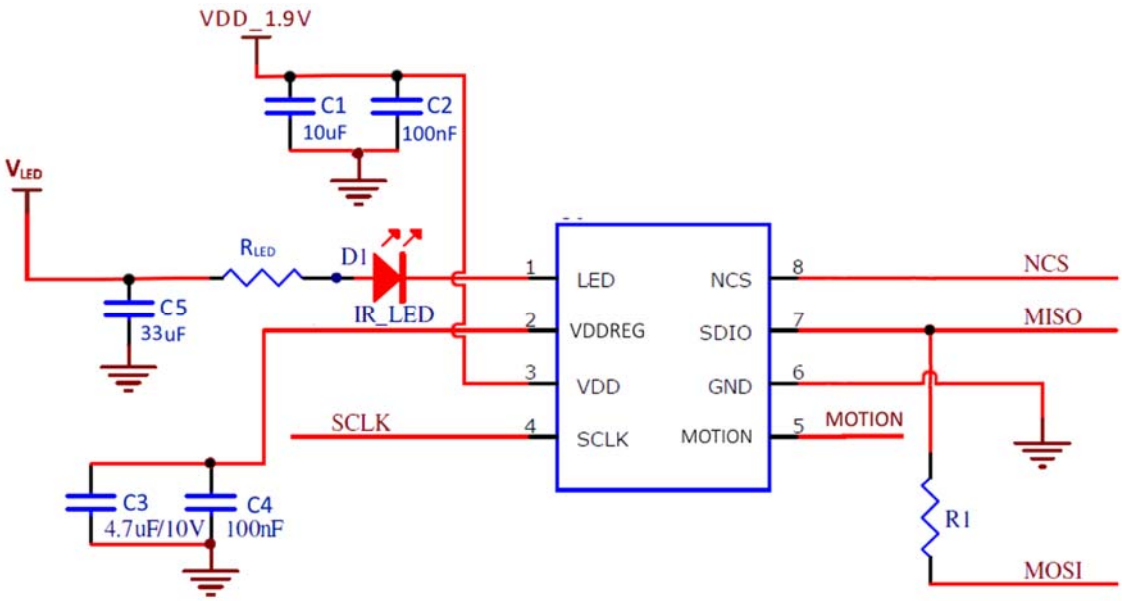


Figure 10. PAW3335DB-TZDU Reference Mouse Schematic

PixArt recommends to use HSDL-4261IR LED with the PAW3335DB-TZDU chip. Table 9 shows the recommended value of R_{LED} and V_{LED} to obtain 24mA current for LED. Recommend to use R_{LED} with 1% tolerance.

Table 9. Recommended R_{LED}

V_{LED} (V)	Recommended R_{LED} (Ω)
1.9	18

Table 10 shows the recommended value of R1 for 2MHz, 4MHz and 8MHz of serial port clock frequency. Recommend to use R1 with 1% tolerance.

Table 10. Recommended R1

Serial Port Clock Frequency (MHz)	Recommended R1 (Ω)
2	3.3k
4	1.0k
8	240

4.2 PCB Assembly Recommendation

1. Insert the integrated chip and all other electrical components into PCB.
2. Wave-solder the entire assembly in a no-wash solder process utilizing solder-fixture. A solder-fixture is required to protect the chip from flux spray and wave solder.
3. Avoid getting any solder flux onto the chip body as there is potential for flux to seep into the chip package. The solder fixture should be designed to expose only the chip leads to flux spray & molten solder while shielding the chip body and optical apertures. The fixture should also set the chip at the correct position and height on the PCB.
4. Place the lens onto the base plate. Care must be taken to avoid contamination on the optical surfaces.
5. Remove the protective kapton tapes from optical apertures of the chip. Care must be taken to prevent contaminants from entering the apertures. Do not place the PCB with the chip facing up during the entire product assembly process. Hold the PCB vertically when removing kapton tape.
6. Remove the protective kapton tapes from optical apertures of the chip. Care must be taken to prevent contaminants from entering the apertures. Do not place the PCB with the chip facing up during the entire mouse assembly process. Hold the PCB vertically when removing kapton tape.
7. Insert PCB assembly over the lens onto the base plate aligning post to retain PCB assembly. The chip package will self-align to the lens via the guide posts. The optical position reference for the PCB is set by the base plate and lens. Note that the PCB motion due to button presses must be minimized to maintain optical alignment.
8. Install mouse top case. There must be a feature in the top case to press down onto the PCB assembly to ensure all components are stacked or interlocked to the correct vertical height

5.0 Power States & Sequence

5.1 Power-Up Sequence

Although the sensor performs an internal power up self-reset, it is still recommend that the Power_Up_Reset register is written every time power is applied. The appropriate sequence is as follows:

1. Apply power to VDD.
2. Wait for 50ms.
3. Drive NCS high, and then low to reset the SPI port.
4. Write 0x5A to Power_Up_Reset register.
5. Wait for at least 5ms.
6. Load Power-up initialization register setting.
7. Read from registers 0x02, 0x03, 0x04, 0x05 and 0x06 one time regardless of the motion bit state.

5.2 Power-Up Initialization Register Setting

- Write register 0x40 with value 0x80
- Write register 0x55 with value 0x01
- Wait for at least 1ms
- Write register 0x7F with value 0x0E
- Write register 0x43 with value 0x1D
- Read register 0x46 and store in Var“R1”
- Write register 0x43 with value 0x1E
- Read register 0x46 and store in Var“R2”
- Write register 0x7F with value 0x14
- Write register 0x6A with value “R1”
- Write register 0x6C with value “R2”
- Write register 0x7F with value 0x00
- Write register 0x55 with value 0x00
- Write register 0x4E with value 0x23
- Write register 0x77 with value 0x18
- Write register 0x7F with value 0x05
- Write register 0x53 with value 0x0C
- Write register 0x5B with value 0xEA
- Write register 0x61 with value 0x13
- Write register 0x62 with value 0x0B
- Write register 0x64 with value 0xD8
- Write register 0x6D with value 0x86
- Write register 0x7D with value 0x84
- Write register 0x7E with value 0x00
- Write register 0x7F with value 0x06
- Write register 0x60 with value 0xB0
- Write register 0x61 with value 0x00
- Write register 0x7E with value 0x40
- Write register 0x7F with value 0x0A

- Write register 0x4A with value 0x23
- Write register 0x4C with value 0x28
- Write register 0x49 with value 0x00
- Write register 0x4F with value 0x02
- Write register 0x7F with value 0x07
- Write register 0x42 with value 0x16
- Write register 0x7F with value 0x09
- Write register 0x40 with value 0x03
- Write register 0x7F with value 0x0C
- Write register 0x54 with value 0x00
- Write register 0x44 with value 0x44
- Write register 0x56 with value 0x40
- Write register 0x42 with value 0x0C
- Write register 0x43 with value 0xA8
- Write register 0x4E with value 0x8B
- Write register 0x59 with value 0x63
- Write register 0x7F with value 0x0D
- Write register 0x5E with value 0xC3
- Write register 0x4F with value 0x02
- Write register 0x7F with value 0x14
- Write register 0x4A with value 0x67
- Write register 0x6D with value 0x82
- Write register 0x73 with value 0x83
- Write register 0x74 with value 0x00
- Write register 0x7A with value 0x16
- Write register 0x63 with value 0x14
- Write register 0x62 with value 0x14
- Write register 0x7F with value 0x10
- Write register 0x48 with value 0x0F
- Write register 0x49 with value 0x88
- Write register 0x4C with value 0x1D
- Write register 0x4F with value 0x08
- Write register 0x51 with value 0x6F
- Write register 0x52 with value 0x90
- Write register 0x54 with value 0x64
- Write register 0x55 with value 0XF0
- Write register 0x5C with value 0x40
- Write register 0x61 with value 0xEE
- Write register 0x62 with value 0xE5
- Write register 0x7F with value 0x00
- Write register 0x5B with value 0x40
- Write register 0x61 with value 0xAD
- Write register 0x51 with value 0xEA
- Write register 0x19 with value 0x9F

- Read register 0x20 at 1ms interval until 0x0F is obtained of read up to 55ms, this register read interval must be carried out at 1ms interval with timing tolerance of +/- 1%.
- Write register 0x19 with value 0x10
- Write register 0x61 with value 0xD5
- Write register 0x40 with value 0x00
- Write register 0x7F with value 0x00
- Write register 0x77 with value 0x2F
- Write register 0x7F with value 0x0D
- Write register 0x4E with value 0x6B
- Write register 0x7F with value 0x05
- Write register 0x44 with value 0xA8
- Write register 0x4A with value 0x14
- Write register 0x7F with value 0x00
- Write register 0x4F with value 0x46
- Write register 0x4D with value 0xD0

During power-up there will be a period of time after the power supply is high but before any clocks are available. The table below shows the state of the various pins during power-up and reset.

Table 11. State of Signal Pins after VDD is Valid

Pin	After Reset
NCS	Functional
SCLK	Depends on NCS
SDIO	Depends on NCS
XYLED	Functional

5.3 Power-Down Sequence

PAW3335DB-TZDU can be set in Shutdown mode by writing to Shutdown register 0x3B with value 0xB6. The SPI port should not be accessed when Shutdown mode is asserted, except the power-up command (writing 0x5A to register 0x3A). Other ICs on the same SPI bus can be accessed, as long as the chip's NCS pin is not asserted.

To de-assert Shutdown mode:

1. Drive NCS high, and then low to reset the SPI port.
2. Write 0x5A to Power_Up_Reset register.
3. Wait for at least 5ms.
4. Load power up initialization register setting as per Section 5.0, step 6.
5. Read from registers 0x02, 0x03, 0x04, 0x05 and 0x06 one time regardless of the motion bit state.

Table 12. Status during Shutdown Mode

Pin	Status during Shutdown Mode
NCS	High *1
SCLK	Ignore if NCS = 1 *2
SDIO	Ignore if NCS = 1*3
XYLED	High

*1. NCS pin must be held to 1 (high) if SPI bus is shared with other devices. It must be held to 1 (high) during Shutdown unless powering up the chip. It must be held to 0 (low) if the chip is to be re-powered up from shutdown (writing 0x5A to register 0x3A).
*2. SCLK is ignored if NCS is 1 (high). It is functional if NCS is 0 (low).
*3. SDIO should be pulled up during Shutdown in order to meet the low power consumption specification in the data sheet.

6.0 Serial Peripheral Interface Communication

6.1 Signal Description

The synchronous serial port is used to write and read parameters in the chip. The port is a three wire serial port. The host micro-controller always initiates communication and the chip never initiates communication. SCLK, SDIO & NCS may be driven directly by a micro-controller. The port pins cannot be shared with other SPI slave devices. When the NCS pin is high, the inputs are ignored.

The lines that comprise the SPI port:

Pin	Description
SCLK	Clock input, generated by the master (microcontroller).
SDIO	Input/output data
NCS	Chip select input (active low). NCS can also be used to reset the serial port in the event of an error

6.2 Motion Bit Timing

The motion bit is an output that signals the micro-controller when motion has occurred. The motion bit turns to “1” whenever the motion is detected; in other words, whenever there is non-zero data in the Delta_X_L, Delta_X_H, Delta_Y_L or Delta_Y_H registers. Clearing the motion bit by reading MOTION registers will set the Motion bit back to “0”.

6.3 Chip Select Operation

The serial port is activated after NCS goes low. If NCS is raised during a transaction, the entire transaction is aborted and the serial port will reset. After a transaction is aborted, the normal address-to-data or transaction-to-transaction delay is still required before beginning the next transaction. In order to improve communication reliability, all serial transactions should be framed by NCS.

In other words, the port should not remain enabled during periods of non-use because ESD and EFT/B events could be interpreted as serial communication and set the chip into unknown state. In addition, NCS must be raised after each burst-mode transaction is complete to terminate burst-mode. The port is not available for further use until burst-mode is terminated.

6.4 Write Operation

Write operation is defined as data going from the micro-controller to the chip. It is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate write sequence. The second byte contains the data. The chip reads SDIO on the rising edges of SCLK.

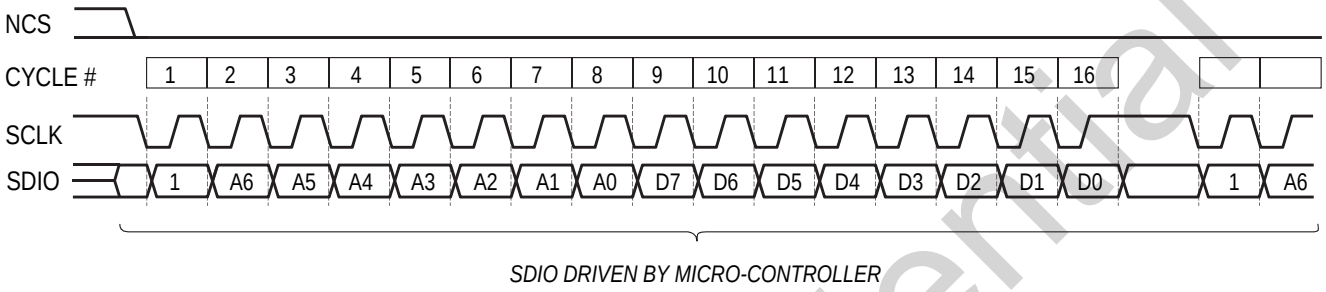


Figure 11. Write Operation

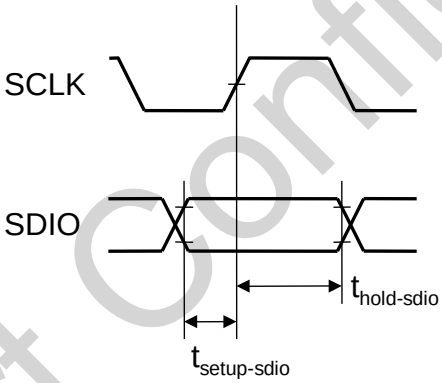


Figure 12. SDIO Setup & Hold Time during write operation

6.5 Read Operation

A read operation is defined as data going from the chip to the microcontroller. It is always initiated by the microcontroller and consists of two bytes. The first byte contains the address, is sent by the microcontroller over SDIO and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the chip over SDIO. The chip outputs SDIO bits on falling edges of SCLK and samples SDIO bits on every rising edge of SCLK.

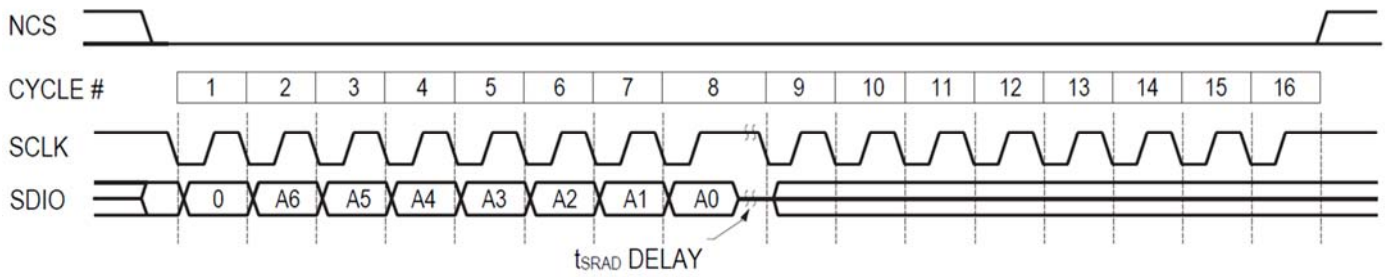


Figure 13. Read Operation

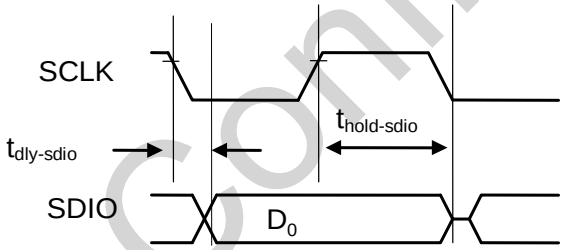


Figure 14. SDIO Delay & Hold Time during read operation

Note: The high state of SCLK is also the SDIO data hold time of the chip. The falling edge of SCLK is the start of the next read or write command, the chip will hold the state of data on SDIO until the falling edge of SCLK.

6.6 Required Timing between Read and Write Commands

Required timing between Read and Write Commands (t_{SXX}).

There are minimum timing requirements between read and write commands on the serial port.

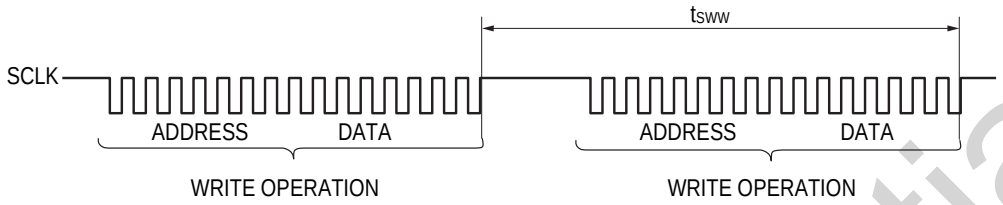


Figure 15. Timing between two Write commands

If the rising edge of the SCLK for the last data bit of the second write command occurs before the required delay (t_{SWW}), then the first write command may not complete correctly.

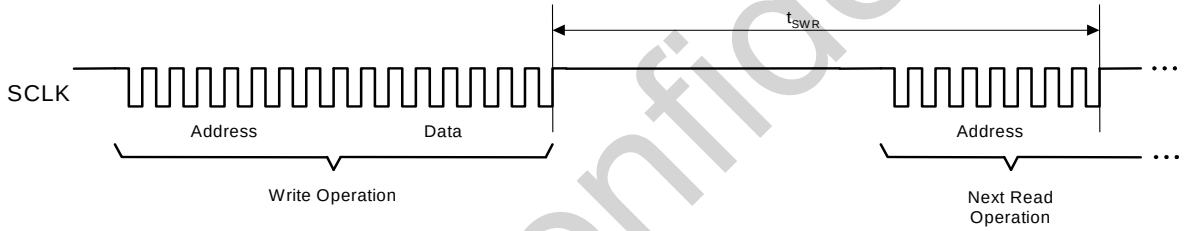


Figure 16. Timing between Write & Read commands

If the rising edge of SCLK for the last address bit of the read command occurs before the required delay (t_{SWR}), the write command may not complete correctly.

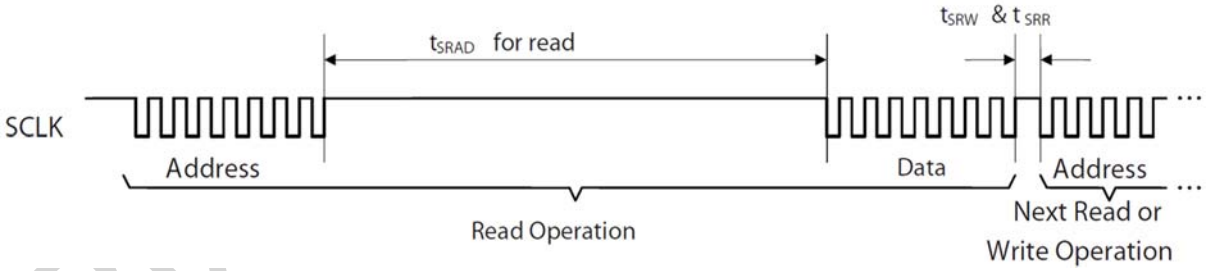


Figure 17. Timing between Read & Subsequent Write or Read commands

If the rising edge of SCLK for the last address bit of the read command occurs before the t_{SWR} required delay, the write command may not be completed correctly. During a read operation SCLK should be delayed at least t_{SRAD} after the last address data bit to ensure that the chip has sufficient time to prepare the requested data.

The falling edge of SCLK for the first address bit of either the read or write command must be at least 2us after the last SCLK rising edge of the last data bit of the previous read operation. In addition, during a read operation SCLK should be delayed after the last address data bit to ensure that the chip has sufficient time to prepare the requested data.

6.7 Burst Mode Operation

Burst mode is a special serial port operation mode which may be used to reduce the serial transaction time for predefined registers. The speed improvement is achieved by continuous data clocking to or from multiple registers without the need to specify the register address and by not requiring the normal delay period between data bytes.

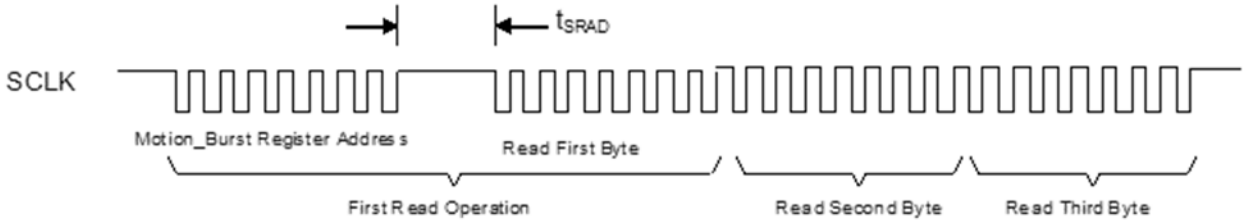


Figure 18. Motion Burst Timing

Motion Burst Read

Reading the Burst_Motion_Read register activates this mode. The chip will respond with the following motion burst report in order. Motion burst report:
BYTE[00] = Motion
BYTE[01] = Chip_Observation
BYTE[02] = Delta_X_L
BYTE[03] = Delta_X_H
BYTE[04] = Delta_Y_L
BYTE[05] = Delta_Y_H
BYTE[06] = SQUAL
BYTE[07] = Raw_Data_Sum
BYTE[08] = Maximum_Raw_Data
BYTE[09] = Minimum_Raw_Data
BYTE[10] = Shutter_Upper
BYTE[11] = Shutter_Lower

After sending the register address, the microcontroller must wait for t_{SRAD}, and then begin reading data. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data are latched into the output buffer after the last address bit is received. After the burst transmission is complete, the microcontroller must raise the NCS line for at least t_{BEXIT} to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

Procedure to start motion burst as below.

1. Pull NCS line to low.
2. Read Motion_Burst register (address 0x16).
3. Wait for t_{SRAD}.
4. Start reading SPI Data continuously up to 12 bytes.
   Motion burst may be terminated by pulling NCS high for at least t_{BEXIT}.
5. To read new motion burst data, start again from step 1.

Burst mode must be terminated by the micro-controller by raising the NCS line for at least t_{BEXIT}. The serial port is not available for use until it is reset with NCS signal, even for a second Burst transmission.

Note: Motion burst data can be read from Motion_Burst register even in rest modes.

7.0 RawData Grab

Rawdata grab is the way to download a full array of rawdata values from a single frame. Once rawdata grab is enabled, the next complete frame image will be stored to memory. In order to stream out the RawData values, register read operation is used.

Procedure to start frame capture burst mode is listed as below:

1. Write register 0x7F with value 0x00
2. Write register 0x40 with value 0x80
3. Write register 0x7F with value 0x13
4. Write register 0x47 with value 0x30
5. Write register 0x7F with value 0x00
6. Write register 0x55 with value 0x04
7. Continuously read register 0x02 until getting both OP_Mode_1 and OP_Mode_0 equal to 0.
8. Write register 0x58 with value 0xFF
9. Continuously read register 0x59 until getting PG_FIRST as "1"
10. Continuously read register 0x59 until getting PG_VALID as "1".
11. Read register 0x58 for 7 bit ADC data (RAWDATA 6-0). Repeat (10) and (11) for 900 times to form a complete picture element array information.
12. Write register 0x55 with value 0x00
13. Write register 0x40 with value 0x00
14. Write register 0x7F with value 0x13
15. Write register 0x47 with value 0x20
16. Write register 0x7F with value 0x00

Last RawData

29	59	89	119	149	179	209	239	269	299	329	359	389	419	449	479	509	539	569	599	629	659	689	719	749	779	809	839	869	899
28	58	88	118	148	178	208	238	268	298	328	358	388	418	448	478	508	538	568	598	628	658	688	718	748	778	808	838	868	898
27	57	87	117	147	177	207	237	267	297	327	357	387	417	447	477	507	537	567	597	627	657	687	717	747	777	807	837	867	897
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
2	32	62	92	122	152	182	212	242	272	302	332	362	392	422	452	482	512	542	572	602	632	662	692	722	752	782	812	842	872
1	31	61	91	121	151	181	211	241	271	301	331	361	391	421	451	481	511	541	571	601	631	661	691	721	751	781	811	841	871
0	30	60	90	120	150	180	210	240	270	300	330	360	390	420	450	480	510	540	570	600	630	660	690	720	750	780	810	840	870

First RawData

+Y

Top X-ray View of Mouse

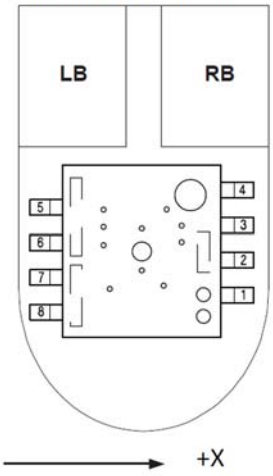


Figure 19. RawData Address Map for 30x30 (Chip looking on the navigation surface through the lens)

***Note**: The X/Y reporting direction shown above follows all the power up initialization sequence in the Power Up section.*

8.0 Power Management for Wireless Mode

PAW3335DB-TZDU has three power-saving modes. Each mode has a different motion detection period with its respective response time to mouse motion. Response time is the time taken for the chip to 'wake up' from rest mode when motion is detected. When left idle, the chip automatically changes or downshift from Run mode to Rest1, then to Rest2 and finally to Rest3 which consumes the least amount of current.

The current consumption is lowest at Rest3 and highest at Rest1. However the time required for chip to respond to motion from Rest1 is the shortest and longest from Rest3. Downshift time is the elapsed time (under no motion condition) from an existing mode to the next mode. For example, it takes 20s for the chip which is in Rest1 mode to change (downshift) to Rest2. The response time and downshift time for each mode is shown in the following table.

However user can change the timing setting for each mode via register 0x77 through 0x7C.

Table 13. Rest Modes Response & Downshift Time

Mode	Response Time	Downshift Time
Rest1	1ms	512ms
Rest2	32ms	20s
Rest3	500ms	600s

Note: These timings are based on Power-Up Initialization Register Setting in section 5.0 and subjected to change if any of the register 0x77 to 0x7C value is updated

9.0 Universal Lift Cut Off Setting

The Universal Lift Cut Off setting applies to all PixArt Standard Gaming Surfaces. The lift-cut off can be set to 1mm and 2mm when mated with the L0AC lens, per the register settings in the table below.

Please note that upon sensor start-up per the recommended Power-Up Sequence, the lift cut off is set to 1mm as default.

Table 14. Lift Cut Off Setting for L0AC-LSG1

Lens	Lift Cut Off Setting	Register Setting
L0AC-LSG1	1mm setting (Default in Power Up Sequence)	- Write register 0x7F with value 0x0C - Write register 0x40 with value 0xA0 - Write register 0x41 with value 0x70 - Write register 0x42 with value 0x0C - Write register 0x43 with value 0xA8 - Write register 0x44 with value 0x44 - Write register 0x45 with value 0x04 - Write register 0x4A with value 0x19 - Write register 0x4B with value 0x18 - Write register 0x4C with value 0x60 - Write register 0x4E with value 0x8B - Write register 0x54 with value 0x00 - Write register 0x56 with value 0x40 - Write register 0x59 with value 0x63 - Write register 0x6D with value 0x7F - Write register 0x7F with value 0x00
	2mm setting	- Write register 0x7F with value 0x0C - Write register 0x40 with value 0x14 - Write register 0x41 with value 0x14 - Write register 0x42 with value 0x20 - Write register 0x43 with value 0x18 - Write register 0x44 with value 0xC7 - Write register 0x45 with value 0x05 - Write register 0x4A with value 0x0A - Write register 0x4B with value 0x08 - Write register 0x4C with value 0x45 - Write register 0x4E with value 0x0F - Write register 0x54 with value 0x00 - Write register 0x56 with value 0x2A - Write register 0x59 with value 0x93 - Write register 0x6D with value 0x5F - Write register 0x7F with value 0x00

10.0 Registers

10.1 Registers List

The chip registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Table 15. Register List

Address	Register Name	Access	Reset Value
0x00	Product_ID	R	0x4E
0x02	Motion	RW	0x20
0x03	Delta_X_L	R	0x00
0x04	Delta_X_H	R	0x00
0x05	Delta_Y_L	R	0x00
0x06	Delta_Y_H	R	0x00
0x07	SQUAL	R	0x00
0x08	Raw_Data_Sum	R	0x00
0x09	Maximum_ Raw_Data	R	0x00
0x0A	Minimum_ Raw_Data	R	0x7F
0x0B	Shutter_Lower	R	0x00
0x0C	Shutter_Upper	R	0x01
0x15	Chip_Observation	RW	0x40
0x16	Burst_Motion_Read	R	0x00
0x3A	Power_Up_Reset	W	0x00
0x3B	Shutdown	W	0x00
0x40	Performance	RW	0x00
0x4E	Resolution	RW	0x12
0x56	Angle_Snap	RW	0x04
0x58	Raw_Data _Grab	RW	0x00
0x59	Raw_Data _Grab_Status	R	0x00
0x5A	Ripple_Control	RW	0x10
0x5B	Axis_Control	RW	0x60
0x5F	Inv_Product_ID	R	0xB1
0x77	Run_DownShift	RW	0x0C
0x78	Rest1_Period	RW	0x01
0x79	Rest1_Downshift	RW	0x4F
0x7A	Rest2_Period	RW	0x08
0x7B	Rest2_Downshift	RW	0x4A
0x7C	Rest3_Period	RW	0x3F
0x7D	Run_Downshift_Mult	RW	0x07
0x7E	Rest_Downshift_Mult	RW	0x77

10.2 Register Descriptions

Register Name	Product_ID							
Address	0x00							
Access	Read			Reset Value		0x4E		
Bit	7	6	5	4	3	2	1	0
Field	PID_{7-0}							
Description	This register contains a unique identification assigned to the PAW3335DB-TZDU. The value in this register does not change; it can be used to verify that the serial communications link is functional.							

Register Name	Motion							
Address	0x02							
Access	Read/Write			Reset Value		0x20		
Bit	7	6	5	4	3	2	1	0
Field	MOT	Reserved	1	Reserved	Reserved	Reserved	OP_Mode_1	OP_Mode_0

Description

This register allows the user to determine if motion has occurred since the last time it was read.

The procedure to read the motion registers (Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H) is as follows:

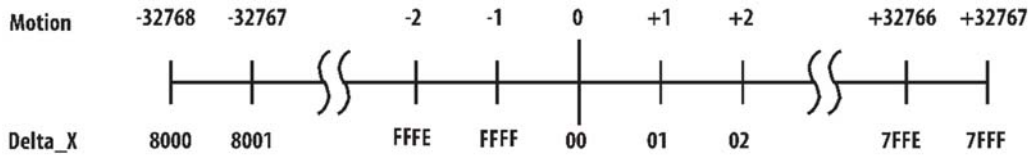
1. Read the Motion register. This will freeze the Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H register values.

2. If the MOT bit is set, Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers should be read in the given sequence to get the accumulated motion. Note: if Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers are not read before the motion register is read for the second time, the data in Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H will be lost.

3. To read a new set of motion data (Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H), repeat from Step 1.

Field Name	Description
MOT	Motion since last report **0 = No motion** 1 = Motion occurred, data ready for reading in Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers
$OP\_Mode_{1:0}$	00 – Run Mode 01 - Rest 1 10 - Rest 2 11 - Rest 3

Write any value to this register will clear all motion data.

Register Name	DELTA_X_L							
Address	0x03							
Access	Read			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0
Description	16 bits 2's complement number. Lower 8 bits of Delta_X. X movement is counts since last report. Absolute value is determined by resolution.  							

Register Name	DELTA_X_H							
Address	0x04							
Access	Read			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	X_{15}	X_{14}	X_{13}	X_{12}	X_{111}	X_{10}	X_9	X_8
Description	16 bits 2's complement number. Upper 8 bits of Delta_X. Delta_X_H must be read after Delta_X_L to have the full motion data. ***Note:*** *It is recommended that register 0x02, 0x03, 0x04, 0x05 and 0x06 to be read sequentially.*							

Register Name	DELTA_Y_L							
Address	0x05							
Access	Read			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
Description	16 bits 2's complement number. Lower 8 bits of Delta_Y. Y movement is counts since last report. Absolute value is determined by resolution.  							

Register Name	DELTA_Y_H							
Address	0x06							
Access	Read			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8
Description	16 bits 2's complement number. Upper 8 bits of Delta_Y. Delta_Y_H must be read after Delta_Y_L to have the full motion data. ***Note:*** *It is recommended that register 0x02, 0x03, 0x04, 0x05 and 0x06 to be read sequentially.*							

Register Name	SQUAL							
Address	0x07							
Access	Read			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	SQ_7	SQ_6	SQ_5	SQ_4	SQ_3	SQ_2	SQ_1	SQ_0
Description	The SQUAL (Surface quality) register is a measure of the number of valid features visible by the chip in the current frame. Use the following formula to find the total number of valid features. Number of Features = SQUAL Register Value * 4 The maximum SQUAL register value is 0xB6. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface is expected. SQUAL values are only valid when chip is in run mode. Disable Rest mode before measuring SQUAL.							

Register Name	RAWDATA_SUM							
Address	0x08							
Access	Read			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	RDS_7	RDS_6	RDS_5	RDS_4	RDS_3	RDS_2	RDS_1	RDS_0
Description	This register is used to find the chip average rawdata value. It reports the upper byte of a 17-bit counter which sums all 900 rawdata in the current frame. To find the average rawdata value follows the formula below: Average pixel value = PIX_ACCUM*512/900 The maximum register value is 0xDF(hex) or 223(dec) and the minimum register value is 0. The rawdata sum value can change every frame. Disable rest mode before reading RawData sum value.							

Register Name	MAXIMUM_RAWDATA							
Address	0x09							
Access	Read			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	MRD_7	MRD_6	MRD_5	MRD_4	MRD_3	MRD_2	MRD_1	MRD_0
Description	Maximum RawData value in current frame. Minimum value = 0, maximum value = 127. The maximum rawdata value can change every frame.							

Register Name	MINIMUM_RAWDATA							
Address	0x0A							
Access	Read			Reset Value		0x7F		
Bit	7	6	5	4	3	2	1	0
Field	$MinRD_7$	$MinRD_6$	$MinRD_5$	$MinRD_4$	$MinRD_3$	$MinRD_2$	$MinRD_1$	$MinRD_0$
Description	Minimum Rawdata value in current frame. Minimum value = 0, maximum value = 127. The minimum rawdata value can change every frame.							

Register Name	SHUTTER_LOWER							
Address	0x0B							
Access	Read			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0
Description	Lower byte of the 12-bit Shutter register.							

Register Name	SHUTTER_UPPER							
Address	0x0C							
Access	Read			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	S_{11}	S_{10}	S_9	S_8
Description	Upper 4-bit of the 12-bit Shutter register. Units are clock cycles of the internal oscillator. Read Shutter_Upper first, then Shutter_Lower. They should be read consecutively. The shutter is adjusted to keep the average rawdata values within normal operating ranges. The shutter value is checked and automatically adjusted to a new value if needed on every frame when operating in default mode.							

Register Name	CHIP_OBSERVATION							
Address	0x15							
Access	Read/Write			Reset Value		0x40		
Bit	7	6	5	4	3	2	1	0
Field	CO_7	CO_6	CO_5	CO_4	CO_3	CO_2	CO_1	CO_0
Description	The user must clear the register by writing 0x00, wait for a minimum T_{dly_obs} ms & read the register. The value of CO_{7-0} should be **0x77** or **0x7F** if the chip is working correctly. The register may be used as part of recovery scheme to detect a problem caused by EFT/B or ESD event. T_{dly_obs} is defined as the longest frame period + 10% variation. The longest frame period is when chip is in Rest3 mode. Clock frequency tolerance value need to be taken into account. For example if the default Rest3 period of 500ms is used, then T_{dly_obs} = 500ms + 50ms							

Register Name	BURST_MOTION_READ							
Address	0x16							
Access	Read			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	MB_7	MB_6	MB_5	MB_4	MB_3	MB_2	MB_1	MB_0
Description	The Burst_Motion_Read register is used for high-speed access to the Motion, Observation, Delta_X_L, Delta_X_H, Delta_Y_L, Delta_Y_H, SQUAL, RawData_Sum, Maximum_RawData, Minimum_RawData, Shutter_Upper and Shutter_Lower registers. See Burst Mode-Motion Read section 6.7 for use details.							

Register Name	POWER_UP_RESET							
Address	0x3A							
Access	Write			Reset Value		NA		
Bit	7	6	5	4	3	2	1	0
Field	$PRST_7$	$PRST_6$	$PRST_5$	$PRST_4$	$PRST_3$	$PRST_2$	$PRST_1$	$PRST_0$
Description	Write 0x5A to this register to reset the chip and all settings will revert to default values. Reset is required after recovering from Shutdown mode.							

Register Name	SHUTDOWN							
Address	0x3B							
Access	Write			Reset Value		NA		
Bit	7	6	5	4	3	2	1	0
Field	SD_7	SD_6	SD_5	SD_4	SD_3	SD_2	SD_1	SD_0
Description	Write 0xB6 to set the chip to Shutdown mode. Refer to the Shutdown section for more details on recovery procedure.							

Register Name	PERFORMANCE							
Address	0x40							
Access	Read/Write			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AWAKE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Description	This register configures the operating mode of the chip.							

Field Name	Description
AWAKE	**0: Enable Rest Mode** 1: Disable Rest Mode

Register Name	RESOLUTION							
Address	0x4E							
Access	Read/Write			Reset Value		0x12		
Bit	7	6	5	4	3	2	1	0
Field	RES_7	RES_6	RES_5	RES_4	RES_3	RES_2	RES_1	RES_0

Description

This register set the resolution XY of the chip. The resolution value for each register setting are shown below.

Note:

1. Recommend to set bit-7 in RIPPLE_CONTROL register to enable the ripple control when select resolution of 5000cpi and above.
2. * - Actual 85 CPI step for 400 CPI and below.

Field Name	Description
$RES_{7:0}$	Set the chip resolution with 100cpi step of approximately, starting from minimum of 100cpi. (Preliminary)

Hex	Target	Hex	Target	Hex	Target
0	100*	1F	2700	3F	5300
2	200*	20	2800	40	5400
3	300*	21	2900	41	5500
4	400*	**23**	**3000**	42	5600
5	500	25	3100	44	5700
6	600	26	3200	45	5800
7	700	27	3300	46	5900
9	800	28	3400	47	6000
A	900	29	3500	48	6100
B	1000	2A	3600	4A	6200
C	1100	2C	3700	4B	6300
D	1200	2D	3800	4C	6400
E	1300	2E	3900	4D	6500
10	1400	2F	4000	4E	6600
11	1500	30	4100	50	6700
12	1600	32	4200	51	6800
13	1700	33	4300	52	6900
14	1800	34	4400	53	7000
16	1900	35	4500	54	7100
17	2000	36	4600	56	7200
18	2100	38	4700	57	7300
19	2200	39	4800	58	7400
1A	2300	3A	4900	59	7500
1B	2400	3B	5000	5A	7600
1D	2500	3C	5100	5C	7700
1E	2600	3E	5200	5D	7800

Hex	Target	Hex	Target	Hex	Target
5E	7900	82	10900	A6	13900
5F	8000	83	11000	A7	14000
60	8100	84	11100	A8	14100
62	8200	86	11200	AA	14200
63	8300	87	11300	AB	14300
64	8400	88	11400	AC	14400
65	8500	89	11500	AD	14500
66	8600	8A	11600	AE	14600
68	8700	8C	11700	B0	14700
69	8800	8D	11800	B1	14800
6A	8900	8E	11900	B2	14900
6B	9000	8F	12000	B3	15000
6C	9100	90	12100	B4	15100
6E	9200	92	12200	B5	15200
6F	9300	93	12300	B6	15300
70	9400	94	12400	B7	15400
71	9500	95	12500	B8	15500
72	9600	96	12600	B9	15600
74	9700	98	12700	BA	15700
75	9800	99	12800	BB	15800
76	9900	9A	12900	BC	15900
77	10000	9B	13000	BD	16000
78	10100	9C	13100		
7A	10200	9E	13200		
7B	10300	9F	13300		
7C	10400	A0	13400		
7D	10500	A1	13500		
7E	10600	A2	13600		
80	10700	A4	13700		
81	10800	A5	13800		

Register Name	ANGLE_SNAP							
Address	0x56							
Access	Read/Write			Reset Value		0x04		
Bit	7	6	5	4	3	2	1	0
Field	EN	0	0	0	0	1	0	0
Description	Write to this register to enable angle snap feature. Field Name: EN — Description: 0: Angle snap disable; 1: Angle snap enable							

Register Name	RAWDATA_GRAB							
Address	0x58							
Access	Read/Write			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	$RAWDATA_6$	$RAWDATA_5$	$RAWDATA_4$	$RAWDATA_3$	$RAWDATA_2$	$RAWDATA_1$	$RAWDATA_0$
Description	This register contains the rawdata levels when the RawData Grab process is enabled. For details of the RawData Grab process please refer to section 7.0.							

Register Name	RAWDATA_GRAB_STATUS							
Address	0x59							
Access	Read			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	RDG_VALID	RDG_FIRST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Description	This register provides additional information for user to monitor the chip navigation status.							

Field Name	Description
RDG_VALID	1 = RawData Grab valid
RDG_FIRST	1 = RawData Grab first

Register Name	RIPPLE_CONTROL							
Address	0x5A							
Access	Read/Write			Reset Value		0x10		
Bit	7	6	5	4	3	2	1	0
Field	EN	Reserved	Reserved	1	Reserved	Reserved	Reserved	Reserved
Description	Set bit-7 to enable ripple control.							

Field Name	Description
EN	**0: Ripple Control Disable.** 1: Ripple Control Enable.

Register Name	AXIS_CONTROL							
Address	0x5B							
Access	Read/Write			Reset Value		0x60		
Bit	7	6	5	4	3	2	1	0
Field	Swap_XY	INV_Y	INV_X	Reserved	Reserved	Reserved	Reserved	Reserved

Description

The register set the axis direction of the chip reporting.

Field Name	Description
Swap_XY	1: Swap XY directions
INV_Y	1: Invert Y direction
INV_X	1: Invert X direction

Register Name	INV_PROD_ID							
Address	0x5F							
Access	Read			Reset Value		0xB1		
Bit	7	6	5	4	3	2	1	0
Field	$IPID_{7-0}$							
Description	This register value is the inverse of the Product_ID register value. It is used to test the SPI port hardware.							

Register Name	RUN_DOWNSHIFT							
Address	0x77							
Access	Read/Write			Reset Value		0x0C		
Bit	7	6	5	4	3	2	1	0
Field	RD_7	RD_6	RD_5	RD_4	RD_3	RD_2	RD_1	RD_0

Description

This register set the Run to Rest1 downshift time. Use the formula below for calculation.

Run Downshift time (ms) = RD[7:0] x RUN_DOWNSHIFT_MULT (default 256) x VFR1 (default 1ms)
Example for 12k FPS = 24 x 256 x 83.33us = 512ms (default)

Max Downshift time is 189 x 256 x 83.33us = 4s
Min value is 0x01. A value of 0x00 will be internally clipped to 0x01.

All the above values are expected to have +/- 10% tolerance.

Register Name	REST1_PERIOD							
Address	0x78							
Access	Read/Write			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	$R1R_7$	$R1R_6$	$R1R_5$	$R1R_4$	$R1R_3$	$R1R_2$	$R1R_1$	$R1R_0$
Description	This register set the Rest1 period Rest1 period = R1P[7:0] x 1ms Default Rest1 period = 1 x 1ms = 1ms Min value is 0x01. A value of 0x00 is invalid. All the above values are expected to have +/- 10% tolerance.							

Register Name	REST1_DOWNSHIFT							
Address	0x79							
Access	Read/Write			Reset Value		0x4F		
Bit	7	6	5	4	3	2	1	0
Field	$R1D_7$	$R1D_6$	$R1D_5$	$R1D_4$	$R1D_3$	$R1D_2$	$R1D_1$	$R1D_0$
Description	This register set the Rest1 to Rest2 downshift time. Use the formula below for calculation. Rest1 Downshift time (ms) = R1D[7:0] x REST1_DOWNSHIFT_MULT (default 256) x REST1 period (default 1ms) Default = 79 x 256 x 1ms = 20224ms = 20s Min value is 0x01. A value of 0x00 will be internally clipped to 0x01. All the above values are expected to have +/- 10% tolerance.							

Register Name	REST2_PERIOD							
Address	0x7A							
Access	Read/Write			Reset Value		0x08		
Bit	7	6	5	4	3	2	1	0
Field	$R2P_7$	$R2P_6$	$R2P_5$	$R2P_4$	$R2P_3$	$R2P_2$	$R2P_1$	$R2P_0$
Description	This register set the Rest2 period Rest2 period = R2P[7:0] x slow clock (1ms) x4 Default Rest2 period = 8 x 1ms x4= 32ms Min value is 0x01. A value of 0x00 is invalid. All the above values are expected to have +/- 10% tolerance.							

Register Name	REST2_DOWNSHIFT							
Address	0x7B							
Access	Read/Write			Reset Value		0x4A		
Bit	7	6	5	4	3	2	1	0
Field	$R2D_7$	$R2D_6$	$R2D_5$	$R2D_4$	$R2D_3$	$R2D_2$	$R2D_1$	$R2D_0$
Description	This register set the Rest2 to Rest3 downshift time. Use the formula below for calculation. Rest2 Downshift time (ms) = R2D[7:0] x REST2_DOWNSHIFT_MULT (default 256) x rest2_period (default 32ms) Default = 74 x 256 x 32ms = 606.208s = 10 min Min value is 0x01. A value of 0x00 will be internally clipped to 0x01. All the above values are expected to have +/- 10% tolerance.							

Register Name	REST3_PERIOD							
Address	0x7C							
Access	Read/Write			Reset Value		0x3F		
Bit	7	6	5	4	3	2	1	0
Field	$R3P_7$	$R3P_6$	$R3P_5$	$R3P_4$	$R3P_3$	$R3P_2$	$R3P_1$	$R3P_0$
Description	This register set the Rest3 period Rest3 period = R3P[7:0] x slow clock (1ms) x8 Default Rest3 period = 63 x 1ms x8 = 504ms Min value is 0x01. A value of 0x00 is invalid. All the above values are expected to have +/- 10% tolerance.							

Register Name	RUN_DOWNSHIFT_MULT							
Address	0x7D							
Access	Read/Write			Reset Value		0x07		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	RUN_M_3	RUN_M_2	RUN_M_1	RUN_M_0

Description

This register set the Run Downshift Multiplier. (Refer to the formula in Register RUN_DOWNSHIFT)

Field Name	Description	
$RUN\_M_{0:3}$	**Hex**	**RUN_DOWNSHIFT_MULT**
	0x0	2
	0x1	4
	0x2	8
	0x3	16
	0x4	32
	0x5	64
	0x6	128
	0x7	**256 (default)**
	0x8	512
	0x9	1024
	0xA	2048

Register Name	REST_DOWNSHIFT_MULT							
Address	0x7E							
Access	Read/Write			Reset Value		0x77		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	REST_M_6	REST_M_5	REST_M_4	Reserved	REST_M_2	REST_M_1	REST_M_0

Description

This register set the REST Downshift Multiplier. (Refer to the formula in Register REST1_DOWNSHIFT and REST2_DOWNSHIFT)

Field Name	Description	
REST_$M_{0:2}$	**Hex**	**REST2_DOWNSHIFT_MULT**
	0x0	2
	0x1	4
	0x2	8
	0x3	16
	0x4	32
	0x5	64
	0x6	128
	0x7	**256 (default)**
REST_$M_{4:6}$	**Hex**	**REST1_DOWNSHIFT_MULT**
	0x0	2
	0x1	4
	0x2	8
	0x3	16
	0x4	32
	0x5	64
	0x6	128
	0x7	**256 (default)**

10.3 Bit Masks for Register Write

Special precaution needs to be taken for some of the registers have “Reserved” bit. In order to overwrite specific bits in the register, one need to read and store its current value first, then apply bit masking and write back the new value into the register. This is accomplished by using bitwise operators such as AND(&), OR(|), or INVERSE(~).

Example:

To disable the Rest Mode in Register 0x40 (set bit-7 to 1)

Read register 0x40 and store in VarA

VarA |= 0x80

Write register 0x40 with value VarA

To enable the Rest Mode in Register 0x40 (set bit-7 to 0)

Read register 0x40 and store in VarA

VarA &= ~ 0x80

Write register 0x40 with value VarA

11.0 Document Revision History

Revision Number	Date	Description
1.0	26 Oct 2018	Official release version
1.1	27 Nov 2018	- Update lens part number from “L0AC-LSG” to “L0AC-LSG1” pg20-22 – update power up initialization setting
1.11	10 Dec 2018	Pg20-22 – update power up initialization setting
1.12	27 June 2019	Pg8 – added section 2.1 Regulatory Requirement Pg20-22 – update power up initialization setting Pg41 – update note and description in Register 0x4E (Resolution)