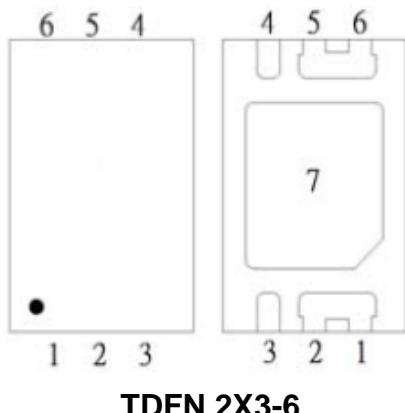


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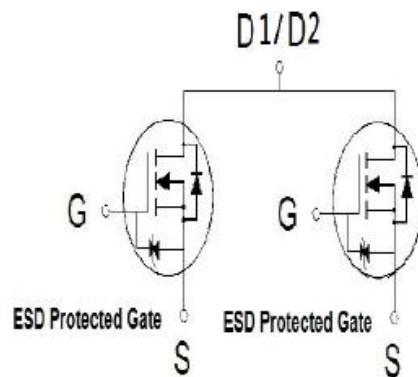
Dual N-Channel Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
20V	8mΩ @ $V_{GS} = 4.5V$	12.9A



1,2:S1
3:G1
4:G2
5,6:S2
7:D1/D2



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 10	V
Continuous Drain Current	I_D	12.9	A
$T_A = 70^\circ C$		10	
Pulsed Drain Current ¹	I_{DM}	42	
Avalanche Current	I_{AS}	23	
Avalanche Energy ³	E_{AS}	26	mJ
Power Dissipation	P_D	2.4	W
$T_A = 25^\circ C$		1.5	
Junction & Storage Temperature Range	T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient ²	$R_{\theta JA}$		52	°C / W

¹Pulse width limited by maximum junction temperature.

²The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper,in a still air environment with $T_A = 25^\circ C$.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

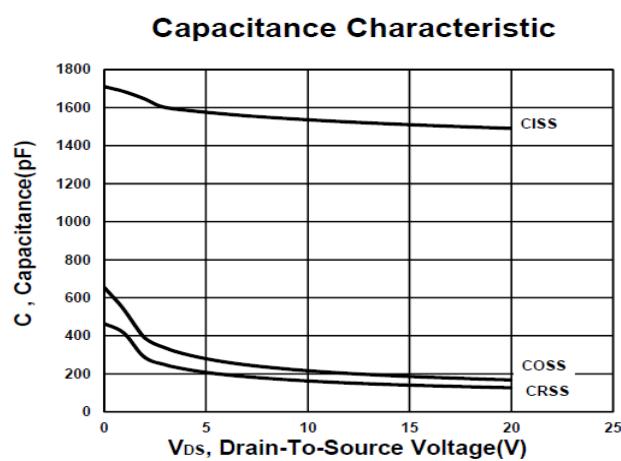
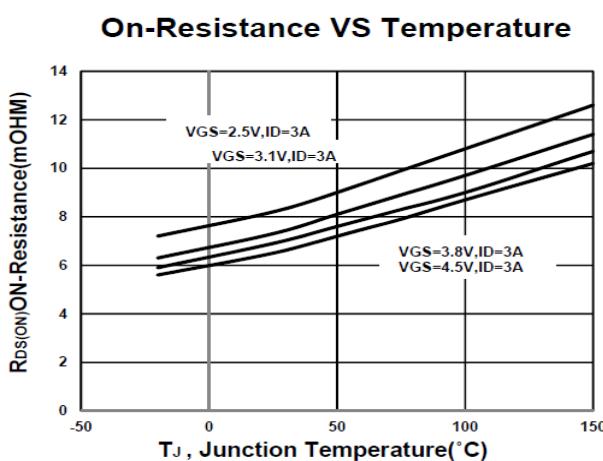
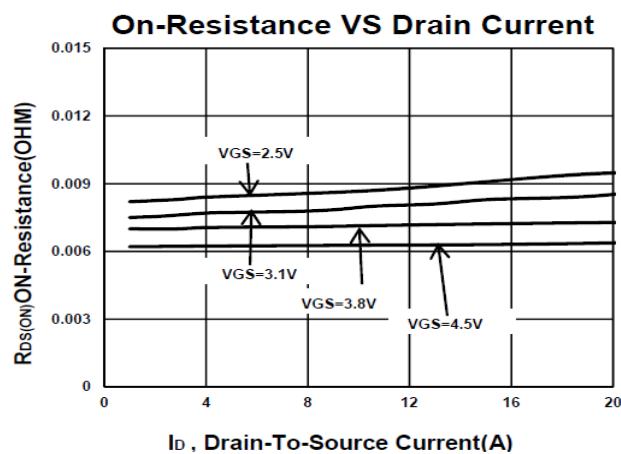
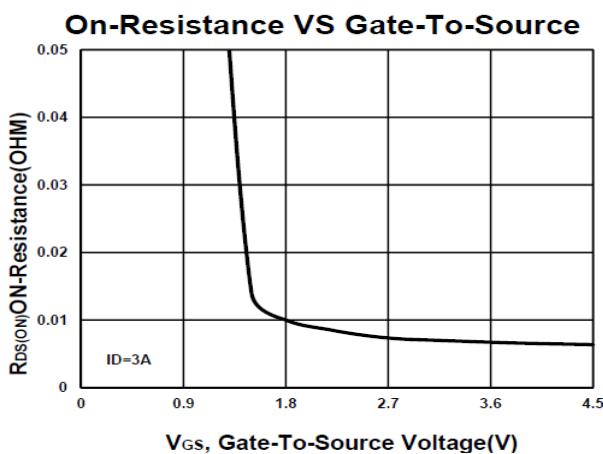
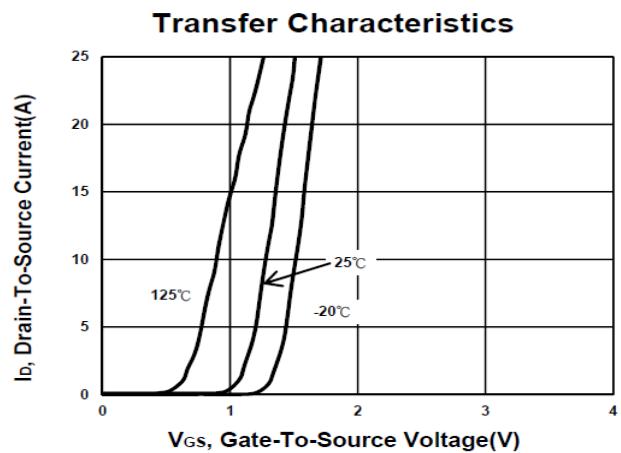
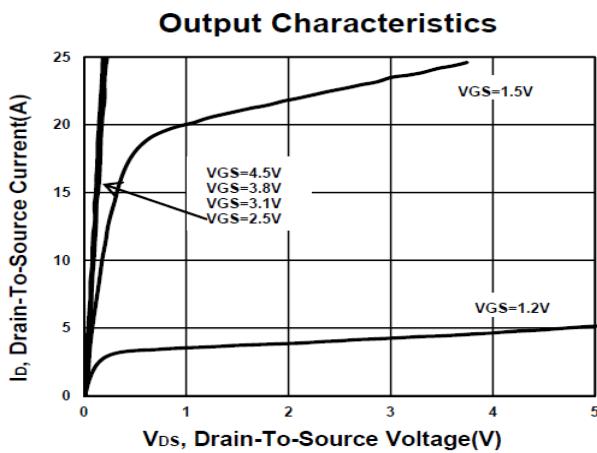
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	20			V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	0.4	0.66	1	
Gate-Body Leakage	I_{GSS}	$V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = \pm 8\text{V}$			± 10	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 16\text{V}, V_{\text{GS}} = 0\text{V}$			1	μA
		$V_{\text{DS}} = 10\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 125^\circ\text{C}$			10	
Drain-Source On-State Resistance ¹	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}} = 4.5\text{V}, I_D = 3\text{A}$	5.1	6.3	8	$\text{m}\Omega$
		$V_{\text{GS}} = 3.8\text{V}, I_D = 3\text{A}$	5.4	7.2	8.4	
		$V_{\text{GS}} = 3.1\text{V}, I_D = 3\text{A}$	5.7	7.6	9.5	
		$V_{\text{GS}} = 2.5\text{V}, I_D = 3\text{A}$	6.3	8.4	10.5	
		$V_{\text{GS}} = 1.8\text{V}, I_D = 3\text{A}$	7	11	15	
Forward Transconductance ¹	g_{fs}	$V_{\text{DS}} = 5\text{V}, I_D = 3\text{A}$		32		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 10\text{V}, f = 1\text{MHz}$		1584		pF
Output Capacitance	C_{oss}			215		
Reverse Transfer Capacitance	C_{rss}			164		
Total Gate Charge ²	Q_g	$V_{\text{DS}} = 10\text{V}, I_D = 3\text{A}$ $V_{\text{GS}} = 4.5\text{V}$		18.4		nC
Gate-Source Charge ²	Q_{gs}			1.8		
Gate-Drain Charge ²	Q_{gd}			4.4		
Turn-On Delay Time ²	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 10\text{V}$ $I_D \geq 3\text{A}, V_{\text{GS}} = 4.5\text{V}, R_{\text{GS}} = 6\Omega$		38		nS
Rise Time ²	t_r			42		
Turn-Off Delay Time ²	$t_{\text{d}(\text{off})}$			60		
Fall Time ²	t_f			25		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_J = 25^\circ\text{C}$)						
Continuous Current	I_S				2	A
Forward Voltage ¹	V_{SD}	$I_F = 3\text{A}, V_{\text{GS}} = 0\text{V}$			1.2	V
Reverse Recovery Time	t_{rr}	$I_F = 3\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$		20		nS
Reverse Recovery Charge	Q_{rr}			9		nC

¹Pulse test : Pulse Width $\leq 300\ \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

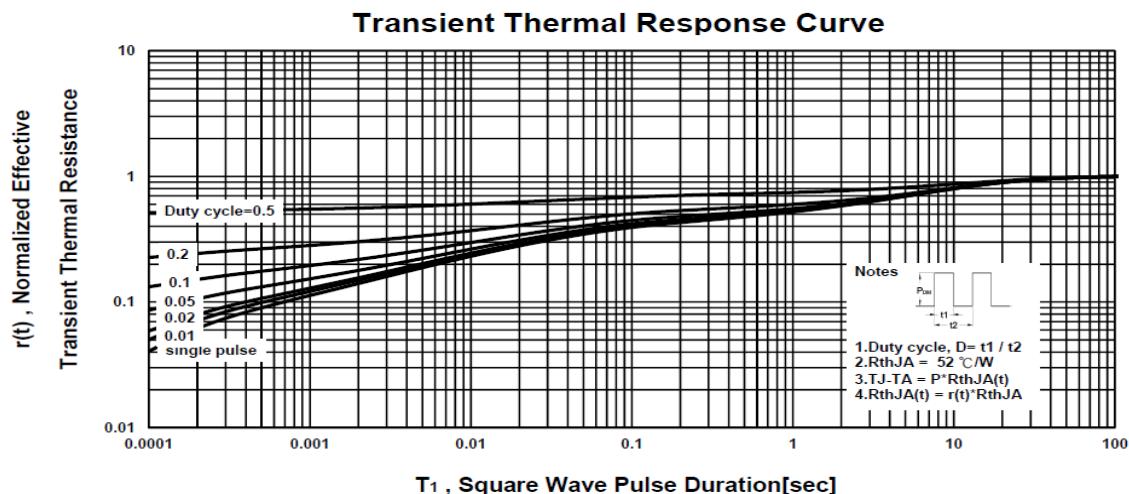
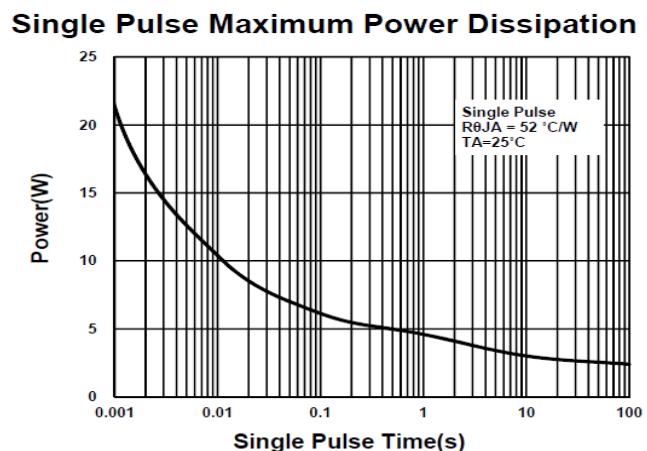
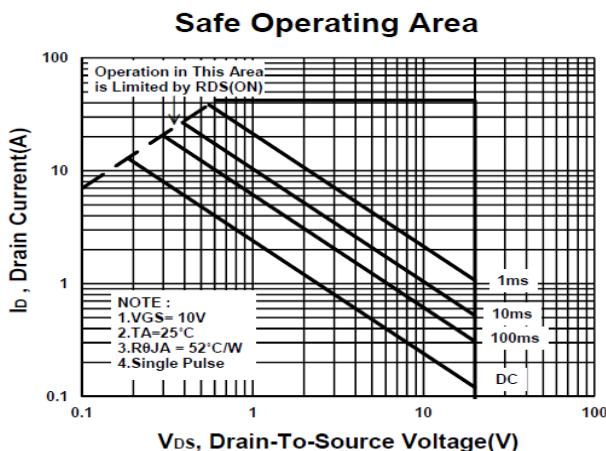
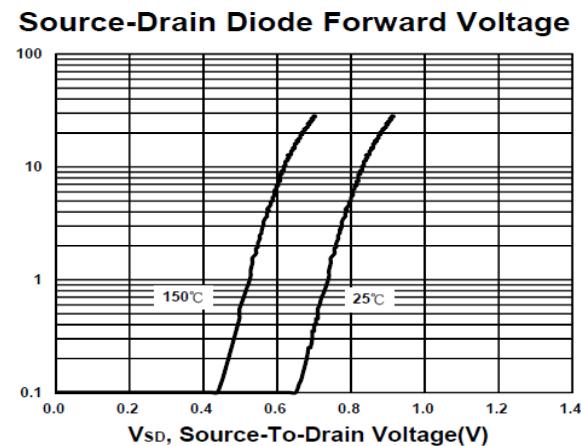
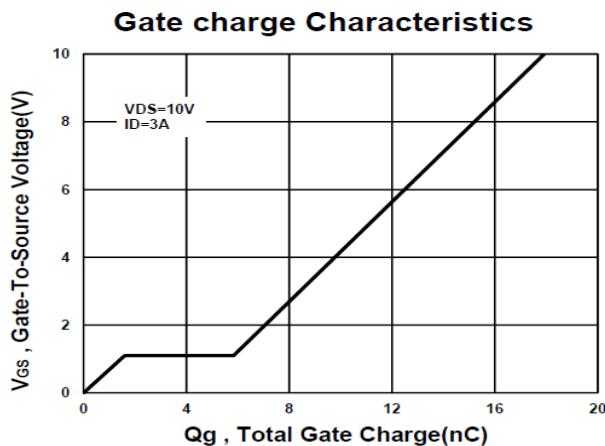
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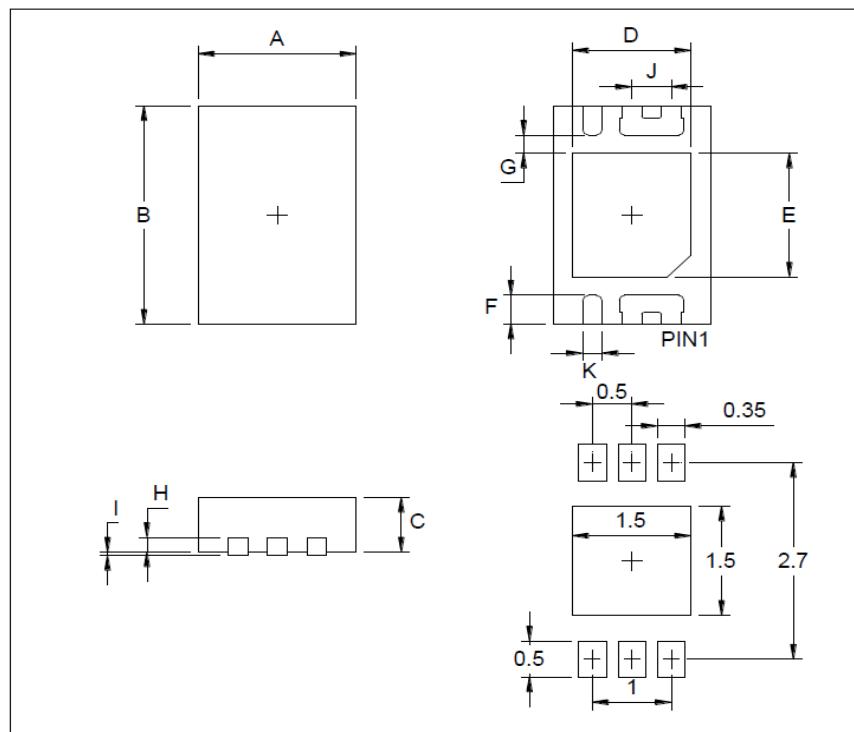
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Dual N-Channel Enhancement Mode MOSFET

Package Dimension

TDFN 2x3-6 MECHANICAL DATA

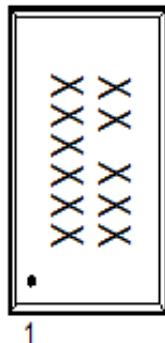
Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	1.95	2.00	2.05	H	0.195	0.203	0.211
B	2.95	3.00	3.05	I	0		0.05
C	0.70	0.75	0.8	J		0.50	
D	1.45	1.50	1.55	K	0.20	0.25	0.30
E	1.65	1.70	1.75				
F	0.35	0.40	0.45				
G	0.25						



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A. Marking Information (此产品代码为：D6)

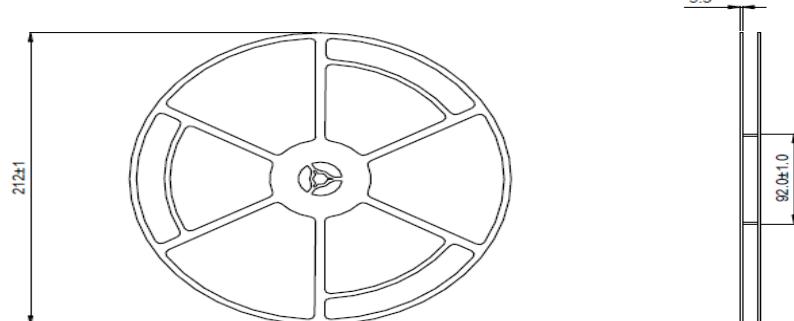
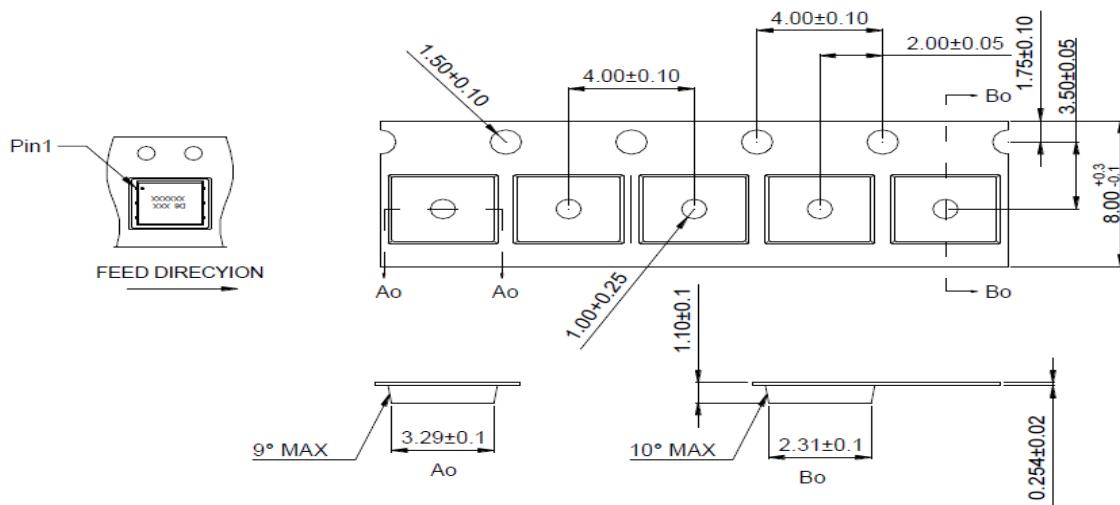


XX(前两码):产品代码

XXX

XXXXXX(后九码): LOT NO

B. Tape&Reel Information:3000pcs/Reel



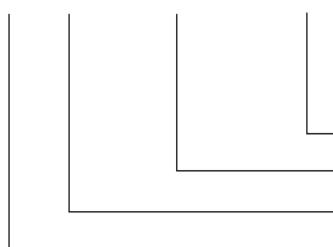
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Dual N-Channel Enhancement Mode MOSFET

C. Lot.No. & Date Code rule

1.LOT.NO.

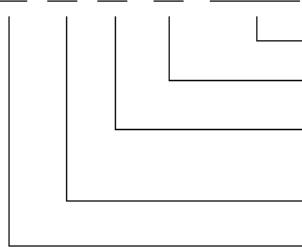
M N 15M21 03



- #8~9 Sub-lot No
- Order series no.
- Foundry site
- Assembly site

2.Date Code

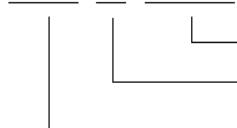
D Y M X XXX



- Order series no. & Sub-lot No
- Week
- M : Month (A:Jan , B:Feb , C:Mar ,D :Apr ,E:May ,F:Jun,G:Jul,H:Aug,I:Sep,J:Oct,K:Nov,L:Dec.)
- Y : Year (N : 2011, O : 2012 ...)
- Assembly site

3.Date Code (for Small package)

XX Y WW



- Week
- Y : Year (9: 2009,A : 2010, B : 2011 ...)
- Device Name

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D.Label rule

标签内容(Label content)



1	Label Size	30 * 90 mm
2	Font style	Times New Roman or Arial (或可区分英文“0”和数字“0”，“G”和“Q”的字型即可)
3	Great Power	Height: 4 mm
4	Package	Height: 2 mm
5	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12
6	Device	Height: 3 mm (Max: 16 Digit)
7	Lot	Height: 3 mm (Max: 9 Digit) Sub lot
8	D/C	Height: 3 mm (Max: 7 Digit)
9	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed
10	Pb Free label	 Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
11	Halogen Free label	 Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
12	Scan info	Device / Lot / D/C / QTY , Insert “ / ” between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least