PBL 403 10

3.5 V GSM 900 MHz Power Amplifier

Description.

The PBL 40310 is a highly integrated single-ended silicon MMIC power amplifier intended for use in GSM terminals. It delivers 35 dBm at 900 MHz with 55 % power added efficiency into a 50 Ω unbalanced load using a single 3.5 V supply.

The circuit has an analog ramp signal to control output power level and a logical on/off signal for power down mode. It can be used in dual-band amplifiers using the band select logical signal. It can be operated up to 50 % duty cycle with minimum performance degradation. The circuit is housed in a specially designed QSOP16 (150 mil body) package and the implementation requires only few external components.

25 GHz f_t state-of-the-art deep trench isolated double-poly silicon bipolar process with additional features for improved wireless performance has been used. On-chip capacitors and inductors are used for the integrated internal matching network. Special front-side metallized substrate contacts provide excellent ground paths from active devices to the highly doped semiconductor substrate and package ground.

Key features.

- 2.7 to 5.0 V single supply operation
- 35 dBm output power at 3.5 V
- 55 % Power Added Efficiency
- Input matched to 50 Ω
- Complete on chip input and interstage matching
- Analog power control
- Less than 10 µA current consumption in power down mode
- Proven RF Silicon Technology Reliability
- Minimum number of external components for low overall solution cost

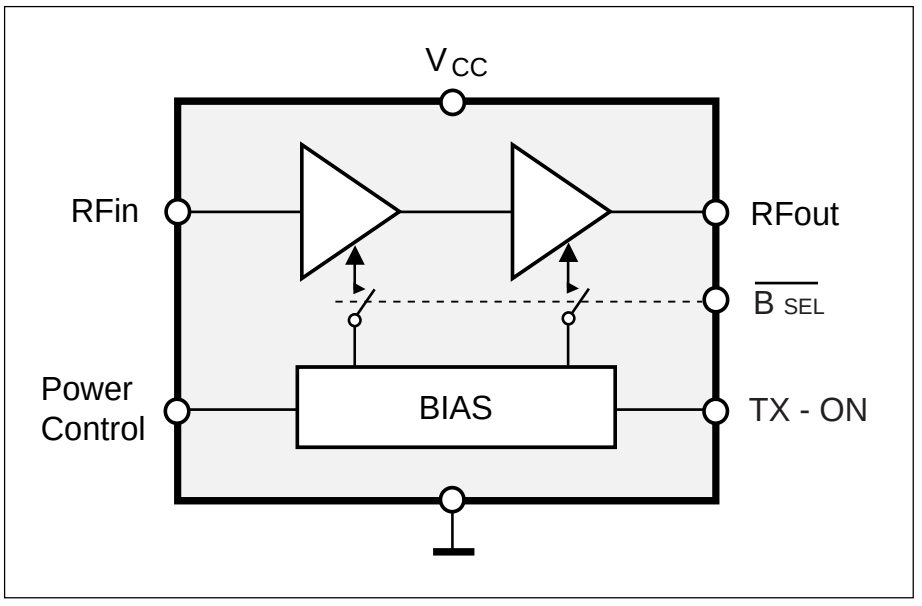


Figure 1. Block diagram.

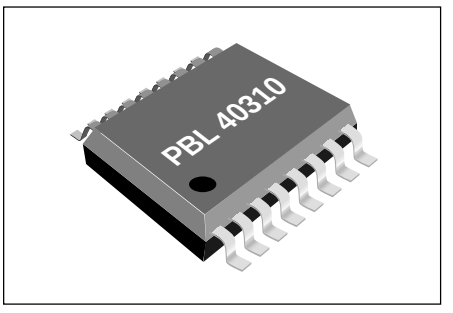


Figure 2. Package outlook.

Maximum Ratings

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply voltage, continuous		V_{CC}	-0.5		6.0	V
Power control voltage		V_{APC}	-0.5		6.0	V
Input power		P_{IN}			+20	dBm
Operating Case Temperature		T_{OP}	-40		+85	°C
Storage Temperature Range		$T_{STORAGE}$	-30		+100	°C

DC Electrical Characteristics

V_{CC} = 3.5 V, T_A= + 25°C unless otherwise stated.

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply voltage range		V_{CC}	2.7		5.0	V
Supply current	V_{APC}= 2.5 V, no RF signal applied	I_{CC}		150		mA
Standby supply current	V_{APC}<=0.5 V, TX-ON=HIGH	I_{STBY}			3.0	mA
Power down leakage current	V_{APC}<= 0.5 V, TX-ON=LOW	I_{LEAK}			5.0	µA
Input current, V_{APC}	0 < V_{APC} < 3.5 V			2.0	3.0	mA

AC Electrical Characteristics

V_{CC} = 3.5 V, f_{IN} = 900 MHz, P_{IN} = 8 dBm, V_{APC} = 2.5 V, TX-ON = high (V_{CC}), $\overline{B_{SEL}}$ = low (GND), duty cycle = 12.5 %, pulse width = 577 µs, T_A = +25°C unless otherwise stated. All data measured on evaluation board.

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Frequency range		f_{IN}	880		915	MHz
Input impedance		Z_{IN}		50		Ω
Input VSWR	P_{IN} = -10 to +20 dBm	VSWR		2:1		
Recommended input power		P_{IN}	8.0		12.0	dBm
Power gain	P_{IN} = 0 dBm	G_P	30	31		dB
Output power		P_{OUT}	34.5	35		dBm
Power added efficiency		η	50	55		%
Output power	V_{CC} = 2.9 V	P_{OUT}		33		dBm
2 nd harmonic		2 fo		**tbd**		dBc
3 rd harmonic		3 fo		**tbd**		dBc
Output Noise	RBW=100 kHz, f=925 to 935 MHz			**tbd**		dBm
Output Noise	RBW=100 kHz, f=925 to 960 MHz			**tbd**		dBm
Forward isolation	V_{APC}< 0.5 V, P_{IN} = -10 to + 10 dBm			-25		dB
Stability, load VSWR	All phases, no oscillations.	VSWR			6:1	
Ruggedness, load VSWR	All phases, no damage.	VSWR			10:1	
Power control for max. P_{OUT}		V_{APC}	2.5			V
Power control for min. P_{OUT}	P_{OUT}< -30 dBm	V_{APC}			0.5	V
Power control slope	-10 dBm < P_{OUT}< 35 dBm			**tbd**	**tbd**	dB/V

This document contains advance information of a new product. Data given in this document shall be considered as preliminary and may be changed without notice.

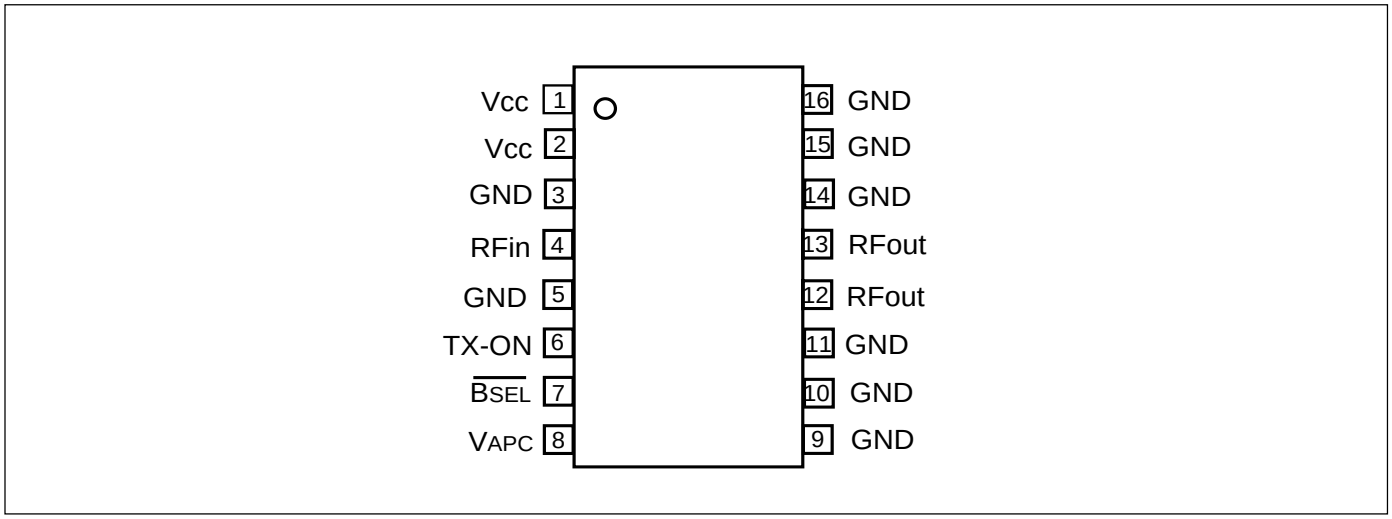


Figure 3. Pin configuration.

Pin Descriptions:

Refer to pin configuration.

SO	Name	Function	SO	Name	Function
1	Vcc	Supply voltage	9	GND	Common ground
2	Vcc	Supply voltage	10	GND	Common ground
3	GND	Common ground	11	GND	Common ground
4	RFin	RF input	12	RFout	RF output
5	GND	Common ground	13	RFout	RF output
6	TX-ON	Transmit ON	14	GND	Common ground
7	$\overline{\text{BSEL}}$	Band select	15	GND	Common ground
8	VAPC	Power control voltage	16	GND	Common ground

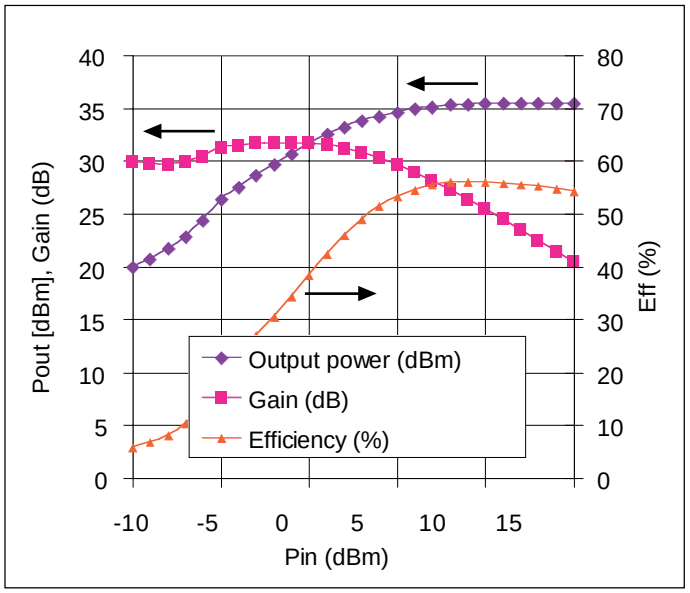


Figure 4. RF performance.

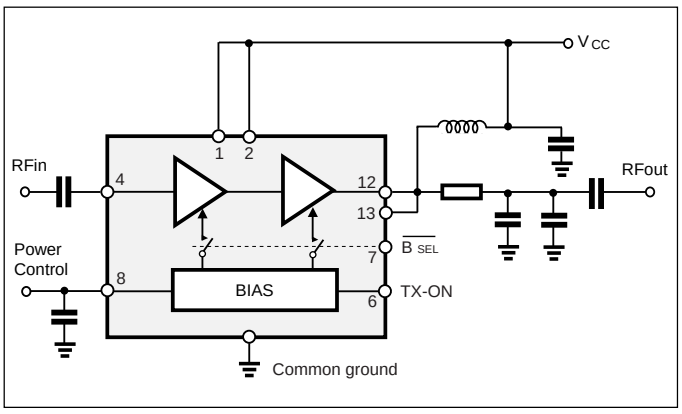
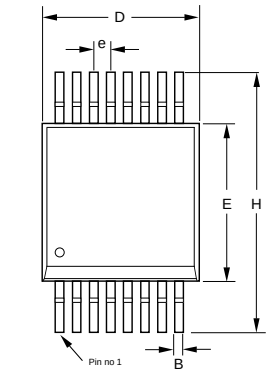
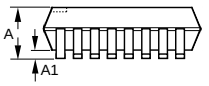


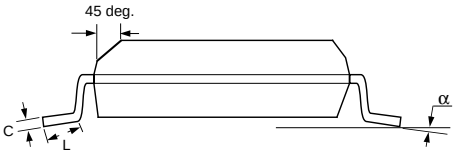
Figure 5. Evaluation setup including network for unbalanced input/output.

Package drawing, QSOP 16

Dim.	millimeters min.	max.	inches min.	max.
A	1.35	1.75	0.532	0.688
A1	0.10	0.25	0.004	0.0098
B	0.21	0.31	0.008	0.012
C	0.19	0.25	0.0075	0.0098
D	9.80	9.98	0.386	0.393
E	3.81	3.99	0.150	0.157
e	0.635mm		0.025 inch ref.	
H	5.70	6.20	0.2284	0.2240
L	0.41	1.27	0.016	0.050
$\alpha = 0–8$ deg.				







Note: This package has been chosen as a preliminary package. It will possibly be changed to a smaller solution.

This document contains advance information of a new product. Data given in this document shall be considered as preliminary and may bechanged without notice.

Specifications subject to change without notice.
1522-PBL 403 10 Uen Rev.A

March 2001

Ericsson Microelectronics AB
S-164 81 Kista-Stockholm, Sweden
Telephone: (08) 757 50 00
www.ericsson.se/microe