

# PBSS4112PAN

120 V, 1 A NPN/NPN low  $V_{CEsat}$  (BISS) transistor

29 November 2012

Product data sheet

## 1. Product profile

### 1.1 General description

NPN/NPN low  $V_{CEsat}$  Breakthrough In Small Signal (BISS) transistor in a leadless medium power DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package. NPN/PNP complement: PBSS4112PANP. PNP/PNP complement: PBSS5112PAP.

### 1.2 Features and benefits

- Very low collector-emitter saturation voltage  $V_{CEsat}$
- High collector current capability  $I_C$  and  $I_{CM}$
- High collector current gain  $h_{FE}$  at high  $I_C$
- Reduced Printed-Circuit Board (PCB) requirements
- High energy efficiency due to less heat generation
- AEC-Q101 qualified

### 1.3 Applications

- Load switch
- Battery-driven devices
- Power management
- Charging circuits
- Power switches (e.g. motors, fans)

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
$V_{CEO}$	collector-emitter voltage	open base	-	-	120	V
$I_C$	collector current		-	-	1	A
$I_{CM}$	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	1.5	A
<b>Per transistor</b>						
$R_{CEsat}$	collector-emitter saturation resistance	$I_C = 500$ mA; $I_B = 50$ mA; pulsed; $t_p \leq 300$ $\mu$ s; $\delta \leq 0.02$ ; $T_{amb} = 25$ °C	-	-	240	m $\Omega$

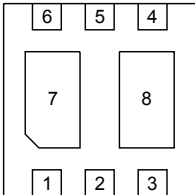
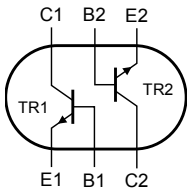


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## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 <p>Transparent top view <b>DFN2020-6 (SOT1118)</b></p>	 <p>sym140</p>
2	B1	base TR1		
3	C2	collector TR2		
4	E2	emitter TR2		
5	B2	base TR2		
6	C1	collector TR1		
7	C1	collector TR1		
8	C2	collector TR2		

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBSS4112PAN	DFN2020-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1118

## 4. Marking

Table 4. Marking codes

Type number	Marking code
PBSS4112PAN	2R

## 5. Limiting values

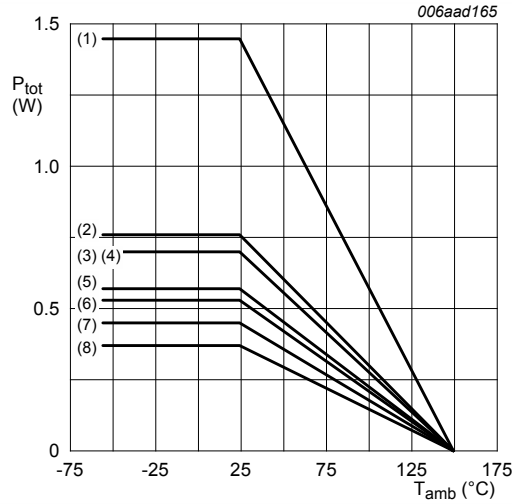
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Per transistor</b>					
V <sub>CBO</sub>	collector-base voltage	open emitter	-	120	V
V <sub>CEO</sub>	collector-emitter voltage	open base	-	120	V
V <sub>EBO</sub>	emitter-base voltage	open collector	-	7	V
I <sub>C</sub>	collector current		-	1	A
I <sub>CM</sub>	peak collector current	single pulse; t <sub>p</sub> ≤ 1 ms	-	1.5	A
I <sub>B</sub>	base current		-	0.3	A

Symbol	Parameter	Conditions		Min	Max	Unit
I <sub>BM</sub>	peak base current	single pulse; t <sub>p</sub> ≤ 1 ms		-	1	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	370	mW
			[2]	-	570	mW
			[3]	-	530	mW
			[4]	-	700	mW
			[5]	-	450	mW
			[6]	-	760	mW
			[7]	-	700	mW
			[8]	-	1450	mW
<b>Per device</b>						
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	510	mW
			[2]	-	780	mW
			[3]	-	730	mW
			[4]	-	960	mW
			[5]	-	620	mW
			[6]	-	1040	mW
			[7]	-	960	mW
			[8]	-	2000	mW
T <sub>j</sub>	junction temperature			-	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C

- [1] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [3] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated and standard footprint.
- [4] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [5] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated and standard footprint.
- [6] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [7] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated and standard footprint.
- [8] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.



- (1) 4-layer PCB 70 μm, mounting pad for collector 1 cm<sup>2</sup>
- (2) FR4 PCB 70 μm, mounting pad for collector 1 cm<sup>2</sup>
- (3) 4-layer PCB 70 μm, standard footprint
- (4) 4-layer PCB 35 μm, mounting pad for collector 1 cm<sup>2</sup>
- (5) FR4 PCB 35 μm, mounting pad for collector 1 cm<sup>2</sup>
- (6) 4-layer PCB 35 μm, standard footprint
- (7) FR4 PCB 70 μm, standard footprint
- (8) FR4 PCB 35 μm, standard footprint

Fig. 1. Per transistor: power derating curves

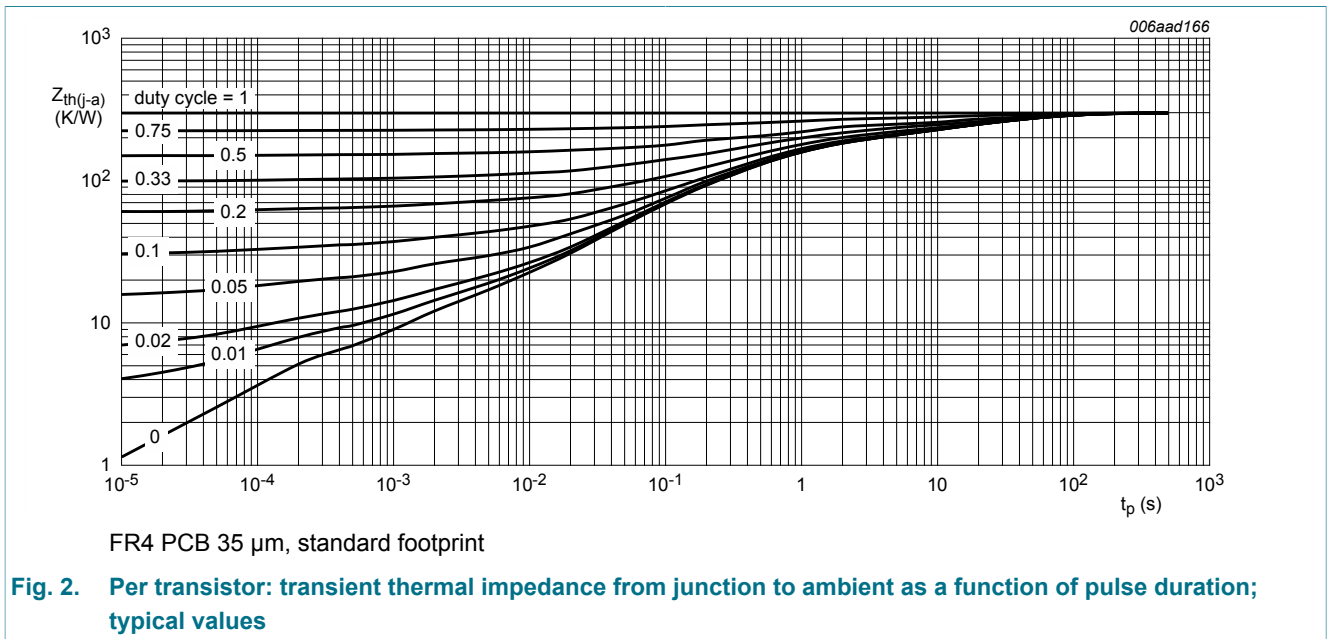
## 6. Thermal characteristics

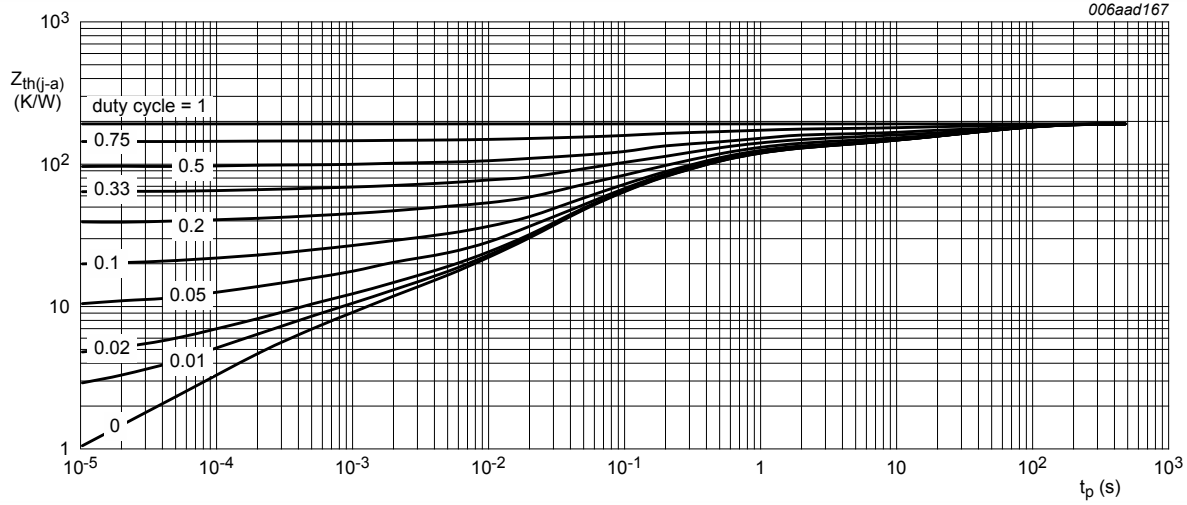
Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Per transistor</b>							
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	-	338	K/W
			[2]	-	-	219	K/W
			[3]	-	-	236	K/W
			[4]	-	-	179	K/W
			[5]	-	-	278	K/W
			[6]	-	-	164	K/W
			[7]	-	-	179	K/W
			[8]	-	-	86	K/W
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point		-	-	30	K/W	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per device</b>							
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	-	245	K/W
			[2]	-	-	160	K/W
			[3]	-	-	171	K/W
			[4]	-	-	130	K/W
			[5]	-	-	202	K/W
			[6]	-	-	120	K/W
			[7]	-	-	130	K/W
			[8]	-	-	63	K/W

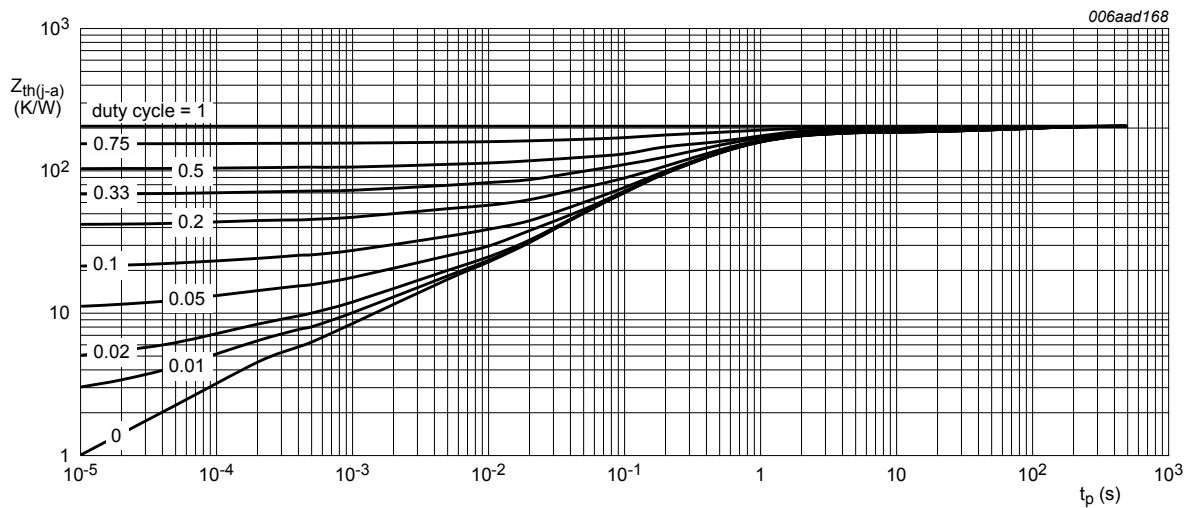
- [1] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [3] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated and standard footprint.
- [4] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [5] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated and standard footprint.
- [6] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [7] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated and standard footprint.
- [8] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.





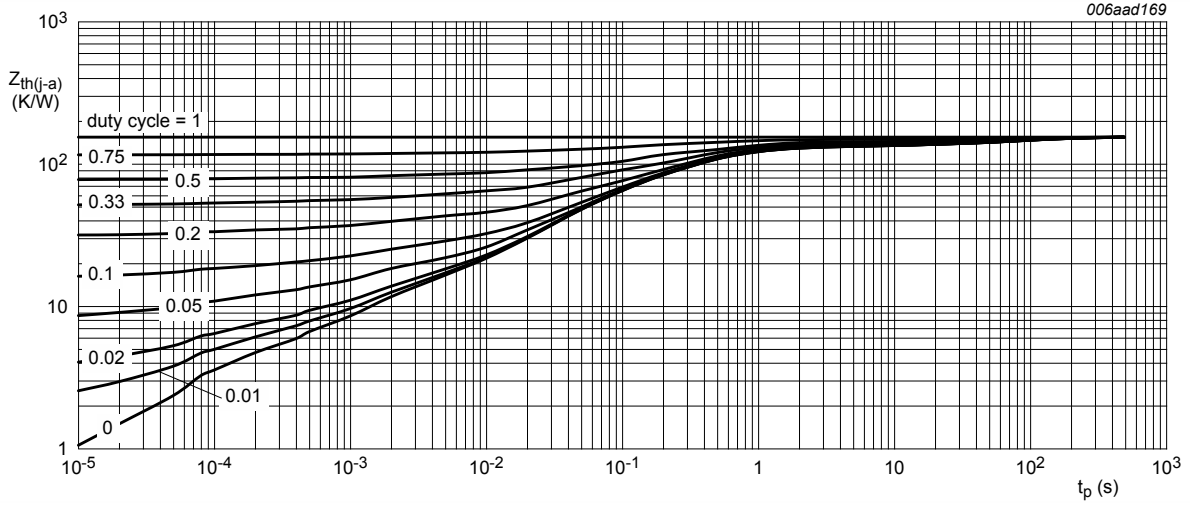
FR4 PCB 35 μm, mounting pad for collector 1 cm<sup>2</sup>

**Fig. 3. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



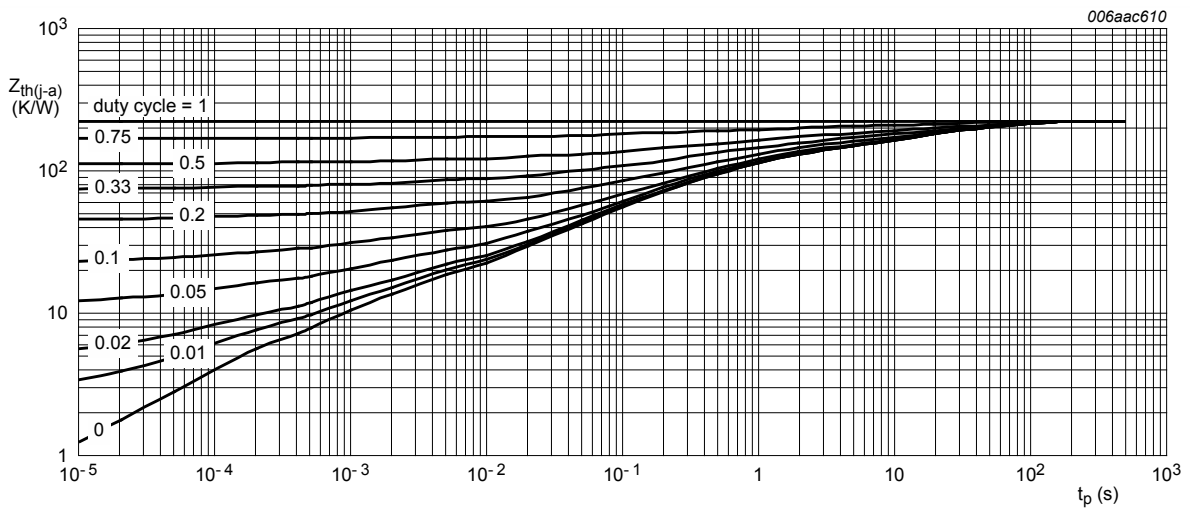
4-layer PCB 35 μm, standard footprint

**Fig. 4. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



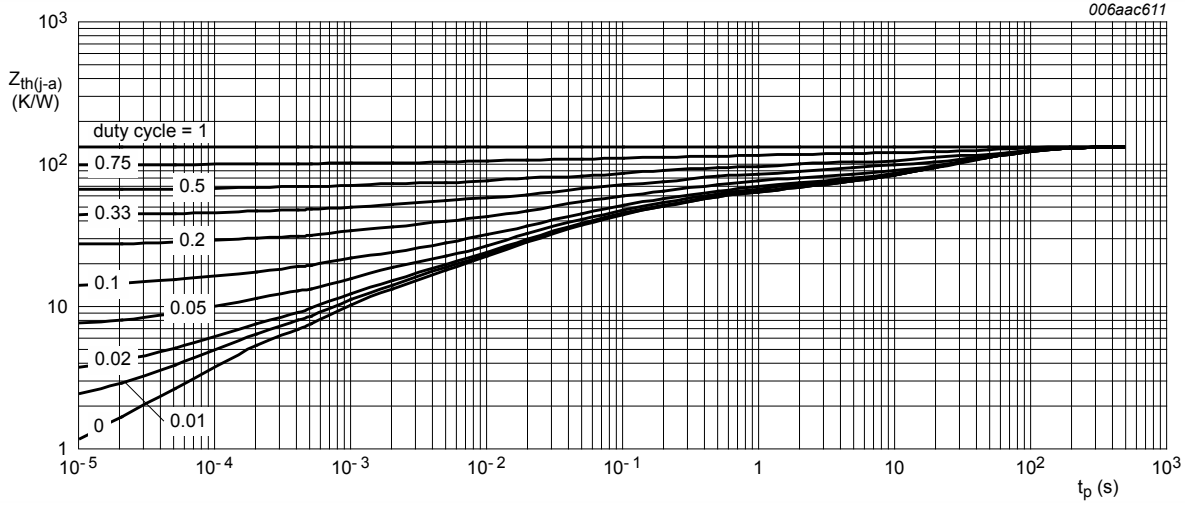
4-layer PCB 35  $\mu$ m, mounting pad for collector 1 cm<sup>2</sup>

Fig. 5. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



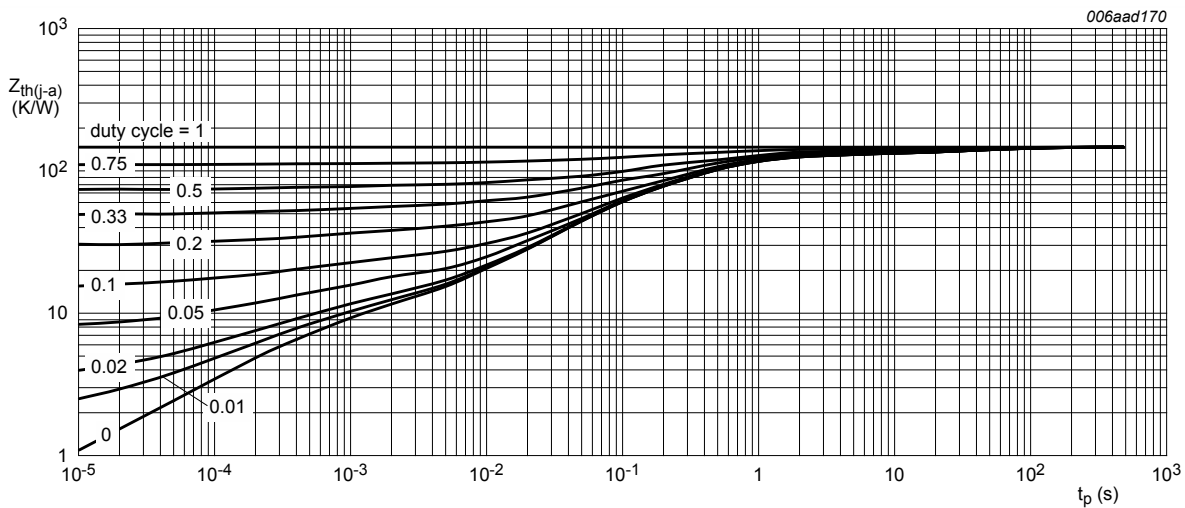
FR4 PCB 70  $\mu$ m, standard footprint

Fig. 6. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB 70 μm, mounting pad for collector 1 cm<sup>2</sup>

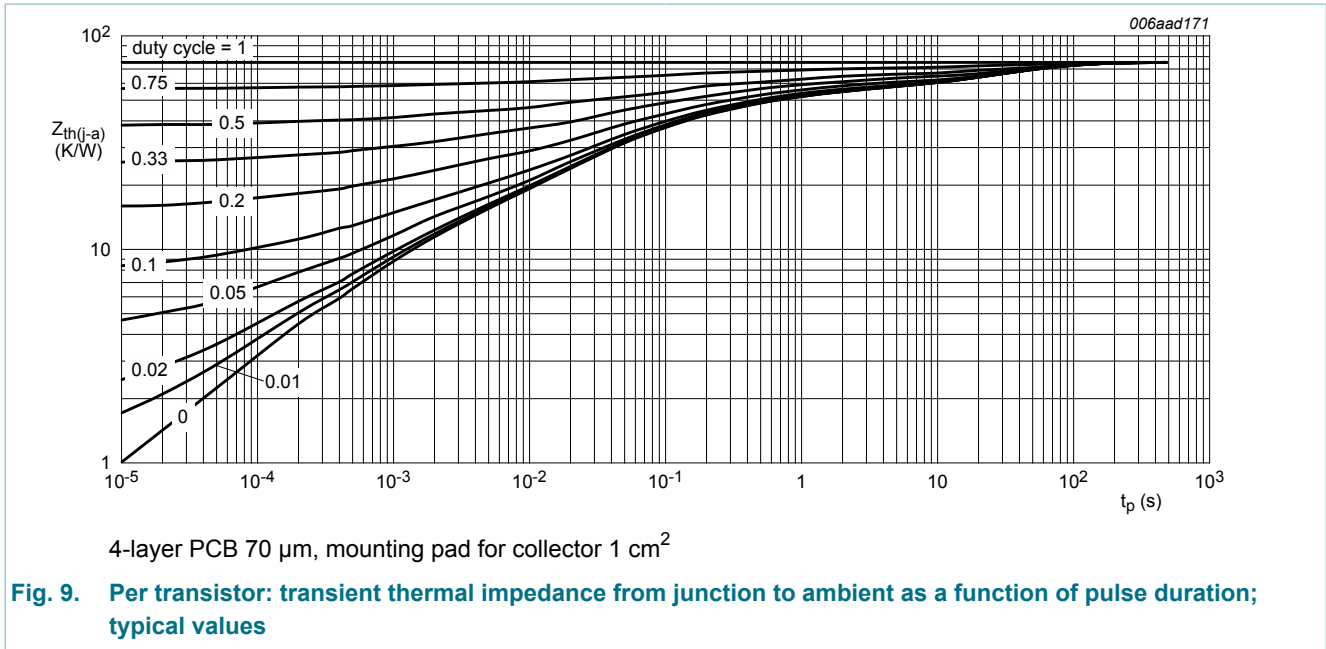
Fig. 7. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



4-layer PCB 70 μm, standard footprint

Fig. 8. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



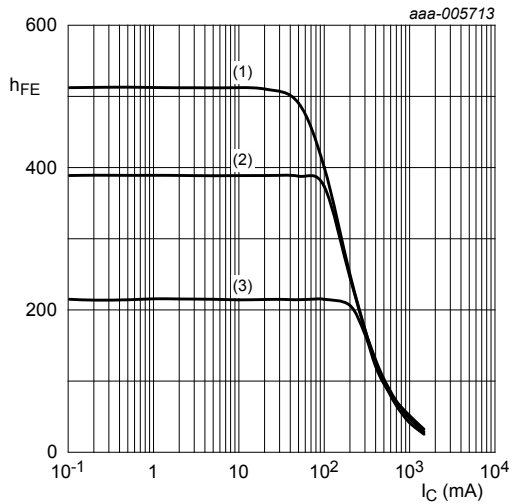


## 7. Characteristics

Table 7. Characteristics

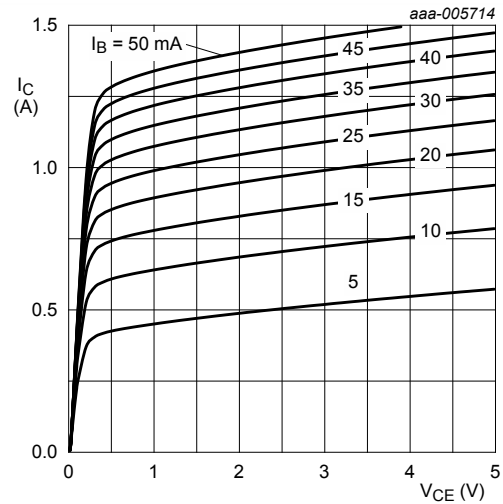
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = 96 V; I <sub>E</sub> = 0 A; T <sub>amb</sub> = 25 °C	-	-	100	nA
		V <sub>CB</sub> = 96 V; I <sub>E</sub> = 0 A; T <sub>j</sub> = 150 °C	-	-	50	μA
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 5 V; I <sub>C</sub> = 0 A; T <sub>amb</sub> = 25 °C	-	-	100	nA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 2 V; I <sub>C</sub> = 100 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	240	375	-	
		V <sub>CE</sub> = 2 V; I <sub>C</sub> = 500 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	60	100	-	
		V <sub>CE</sub> = 2 V; I <sub>C</sub> = 1 A; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	30	45	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = 500 mA; I <sub>B</sub> = 50 mA; T <sub>amb</sub> = 25 °C	-	90	120	mV
		I <sub>C</sub> = 1 A; I <sub>B</sub> = 50 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	-	205	260	mV
		I <sub>C</sub> = 1 A; I <sub>B</sub> = 100 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	-	170	220	mV
R <sub>CEsat</sub>	collector-emitter saturation resistance	I <sub>C</sub> = 500 mA; I <sub>B</sub> = 50 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	-	-	240	mΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{BEsat}$	base-emitter saturation voltage	$I_C = 500 \text{ mA}; I_B = 50 \text{ mA}; T_{amb} = 25 \text{ }^\circ\text{C}$	-	-	1	V
		$I_C = 1 \text{ A}; I_B = 50 \text{ mA}; \text{pulsed}; t_p \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^\circ\text{C}$	-	-	1.1	V
		$I_C = 1 \text{ A}; I_B = 100 \text{ mA}; \text{pulsed}; t_p \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^\circ\text{C}$	-	-	1.1	V
$V_{BEon}$	base-emitter turn-on voltage	$V_{CE} = 2 \text{ V}; I_C = 0.5 \text{ A}; \text{pulsed}; t_p \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^\circ\text{C}$	-	-	0.9	V
$t_d$	delay time	$V_{CC} = 10 \text{ V}; I_C = 500 \text{ mA}; I_{B(on)} = 25 \text{ mA}; I_{B(off)} = -25 \text{ mA}; T_{amb} = 25 \text{ }^\circ\text{C}$	-	20	-	ns
$t_r$	rise time		-	440	-	ns
$t_{on}$	turn-on time		-	460	-	ns
$t_s$	storage time		-	615	-	ns
$t_f$	fall time		-	390	-	ns
$t_{off}$	turn-off time		-	1005	-	ns
$f_T$	transition frequency		$V_{CE} = 10 \text{ V}; I_C = 50 \text{ mA}; f = 100 \text{ MHz}; T_{amb} = 25 \text{ }^\circ\text{C}$	60	120	-
$C_c$	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = 0 \text{ A}; i_e = 0 \text{ A}; f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ\text{C}$	-	4.5	7	pF



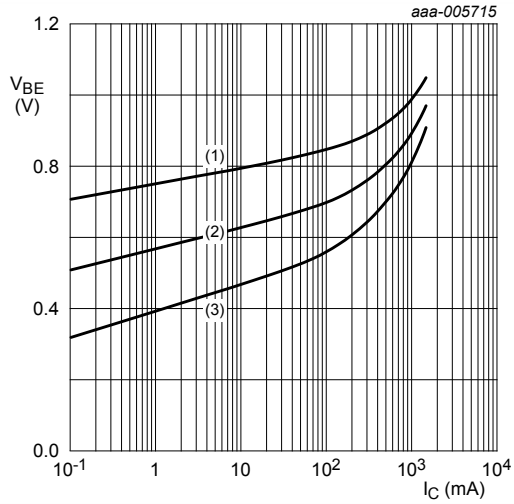
$V_{CE} = 2 \text{ V}$   
 (1)  $T_{amb} = 100 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$   
 (3)  $T_{amb} = -55 \text{ }^\circ\text{C}$

**Fig. 10. DC current gain as a function of collector current; typical values**



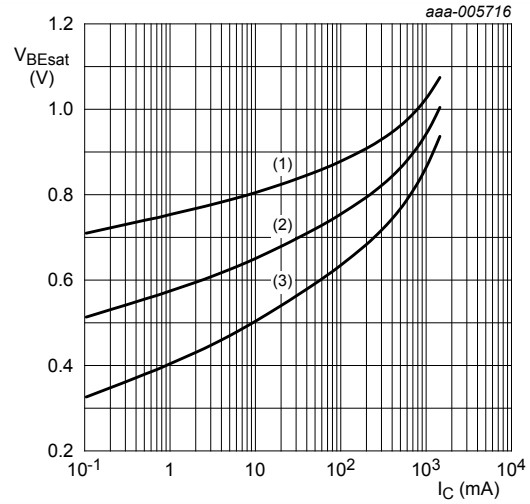
$T_{amb} = 25 \text{ }^\circ\text{C}$

**Fig. 11. Collector current as a function of collector-emitter voltage; typical values**



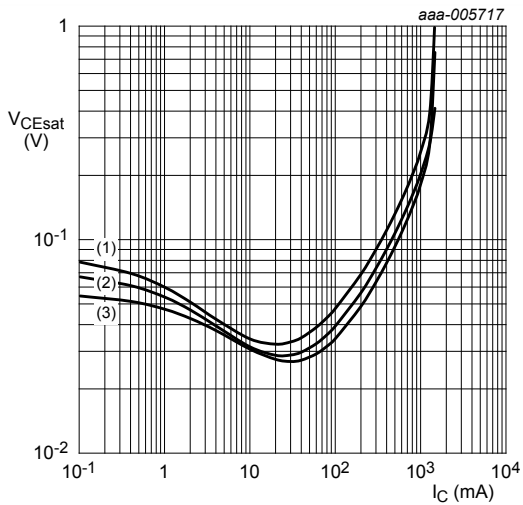
$V_{CE} = 2\text{ V}$   
 (1)  $T_{amb} = -55\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = 100\text{ °C}$

**Fig. 12. Base-emitter voltage as a function of collector current; typical values**



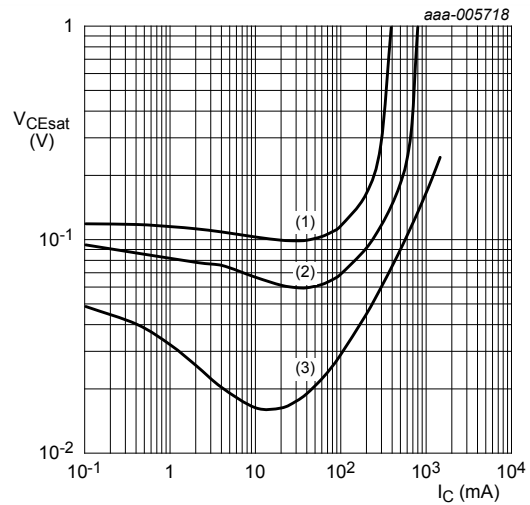
$I_C/I_B = 20$   
 (1)  $T_{amb} = -55\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = 100\text{ °C}$

**Fig. 13. Base-emitter saturation voltage as a function of collector current; typical values**



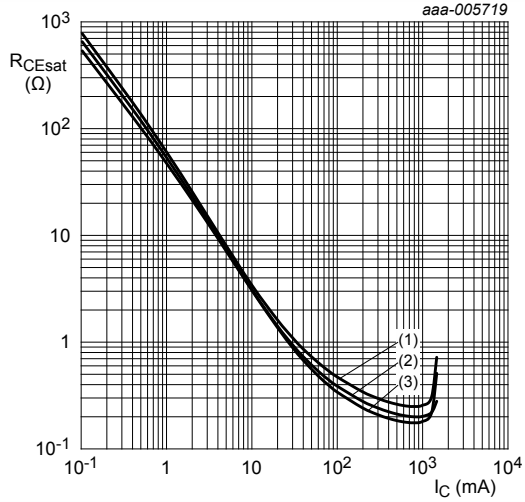
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -55\text{ °C}$

**Fig. 14. Collector-emitter saturation voltage as a function of collector current; typical values**



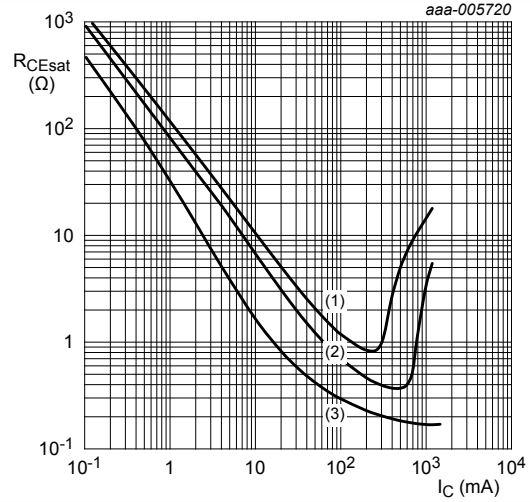
$T_{amb} = 25\text{ °C}$   
 (1)  $I_C/I_B = 100$   
 (2)  $I_C/I_B = 50$   
 (3)  $I_C/I_B = 10$

**Fig. 15. Collector-emitter saturation voltage as a function of collector current; typical values**



$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -55\text{ °C}$

Fig. 16. Collector-emitter saturation resistance as a function of collector current; typical values



$T_{amb} = 25\text{ °C}$   
 (1)  $I_C/I_B = 100$   
 (2)  $I_C/I_B = 50$   
 (3)  $I_C/I_B = 10$

Fig. 17. Collector-emitter saturation resistance as a function of collector current; typical values

### 8. Test information

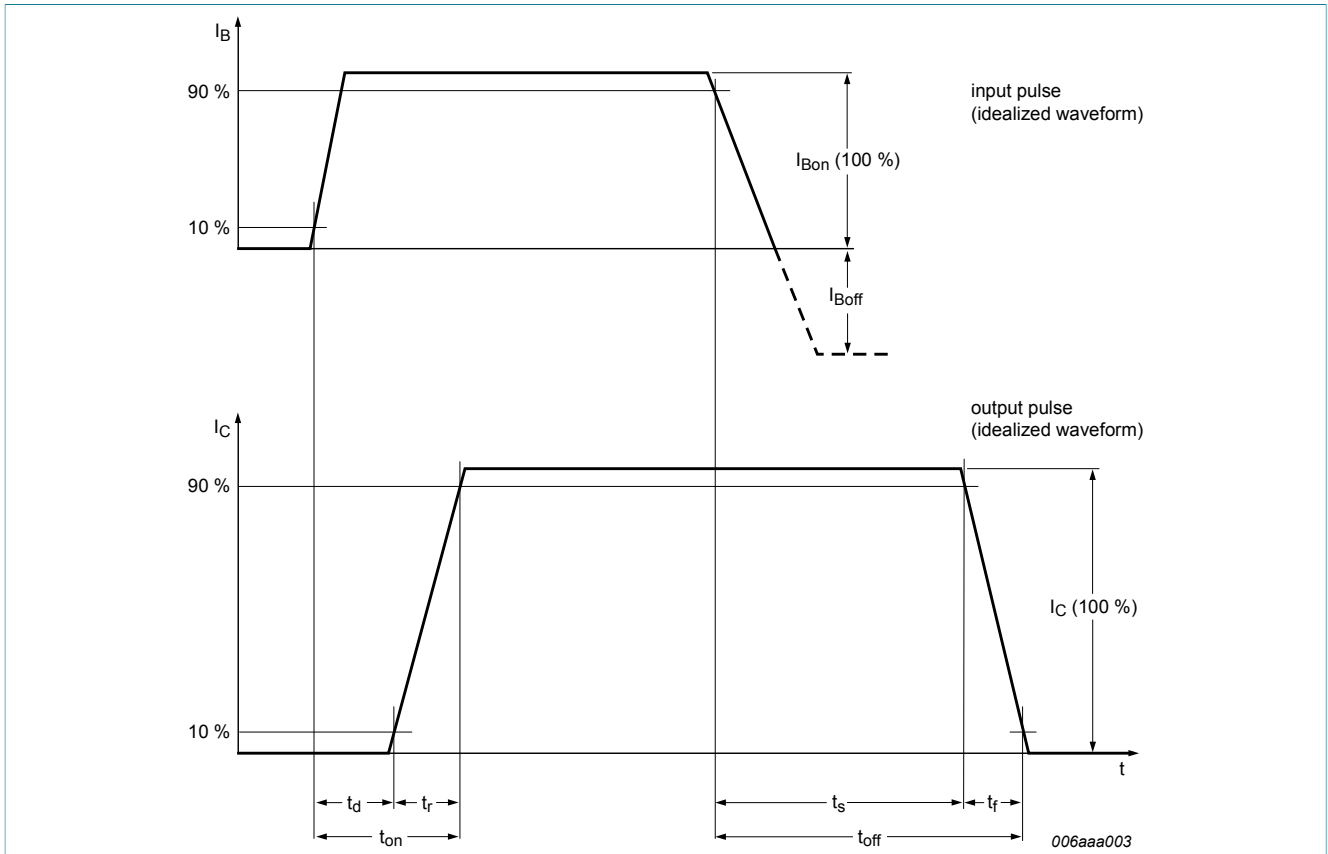


Fig. 18. BISS transistor switching time definition

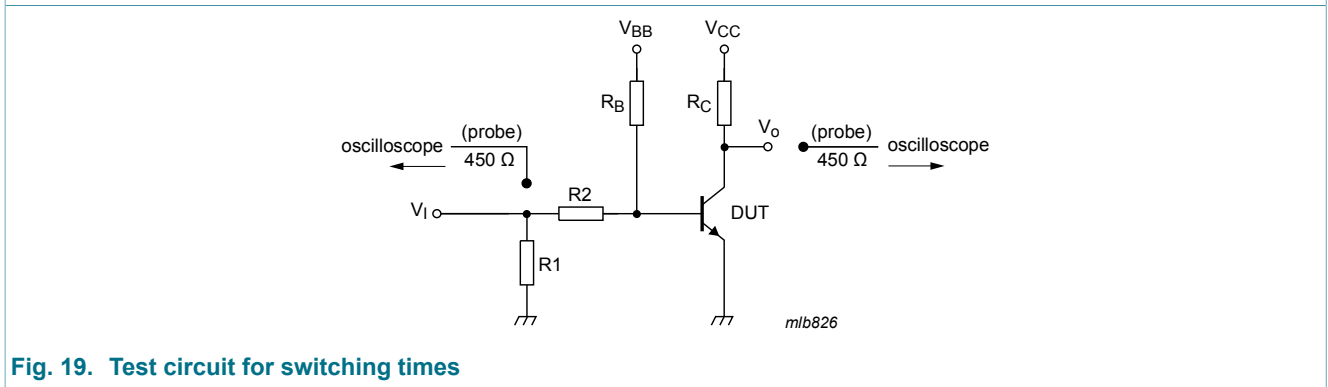


Fig. 19. Test circuit for switching times

#### 8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

### 9. Package outline

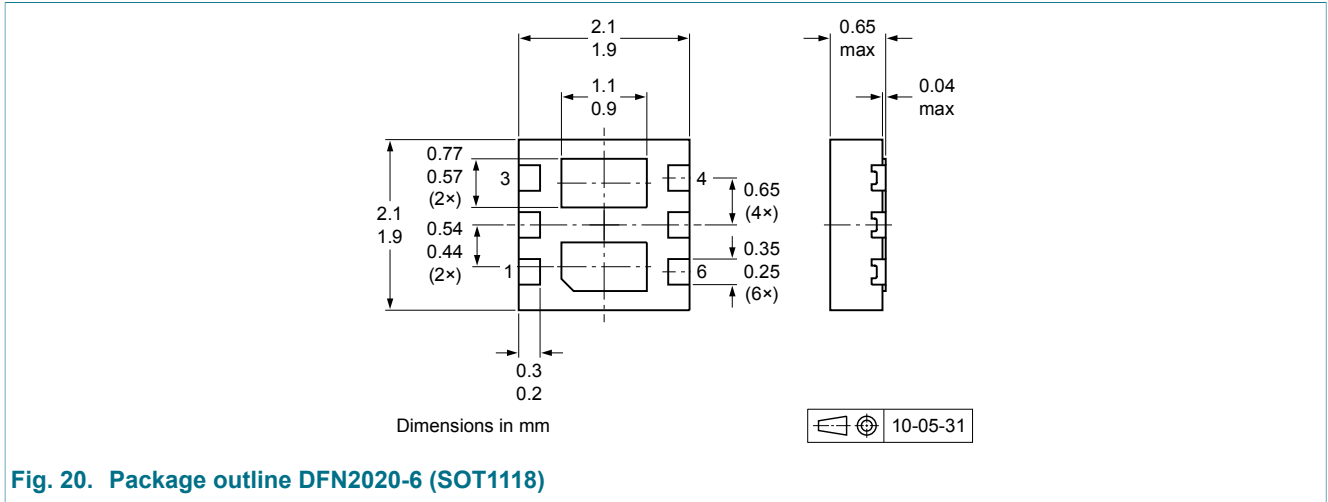


Fig. 20. Package outline DFN2020-6 (SOT1118)

### 10. Soldering

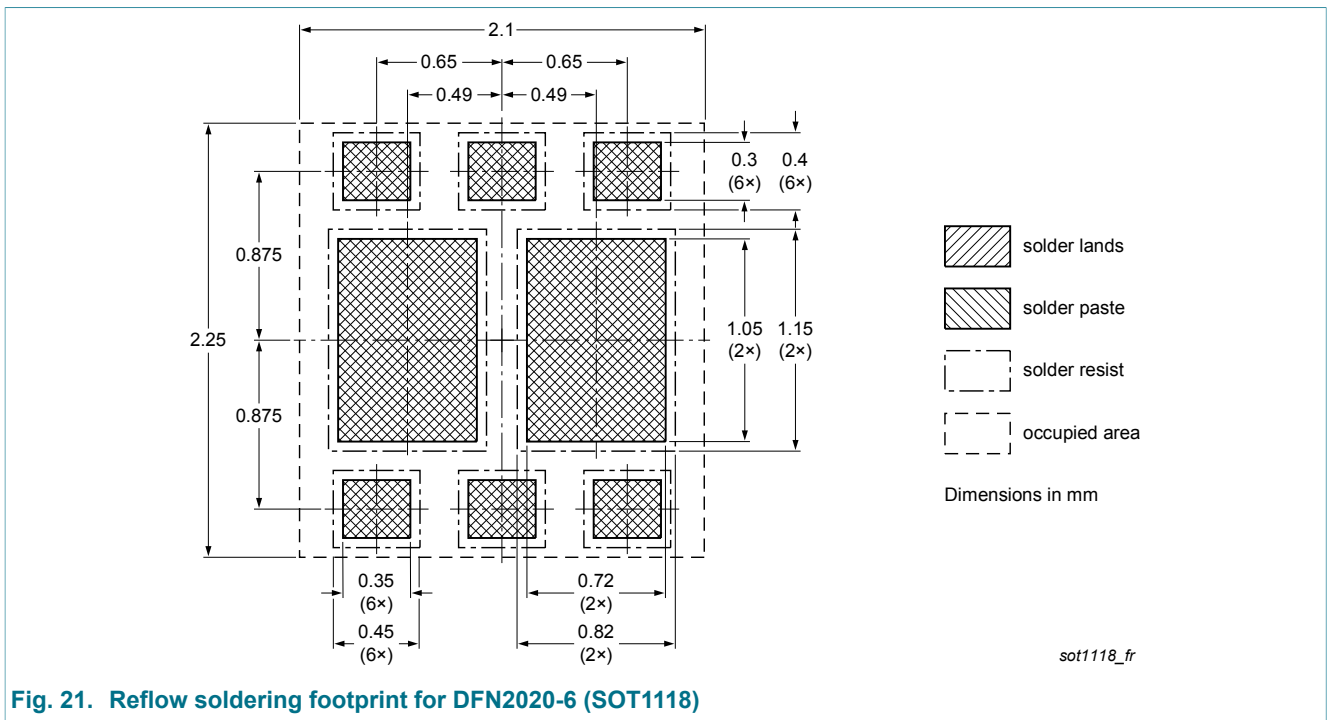


Fig. 21. Reflow soldering footprint for DFN2020-6 (SOT1118)

### 11. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBSS4112PAN v.N	20121129	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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