

# PBSS4230PANP

30 V, 2 A NPN/PNP low  $V_{CEsat}$  (BISS) transistor

14 December 2012

Product data sheet

## 1. General description

NPN/PNP low  $V_{CEsat}$  Breakthrough In Small Signal (BISS) transistor in a leadless medium power DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: PBSS4230PAN. PNP/PNP complement: PBSS5230PAP.

## 2. Features and benefits

- Very low collector-emitter saturation voltage  $V_{CEsat}$
- High collector current capability  $I_C$  and  $I_{CM}$
- High collector current gain  $h_{FE}$  at high  $I_C$
- Reduced Printed-Circuit Board (PCB) requirements
- High efficiency due to less heat generation
- AEC-Q101 qualified

## 3. Applications

- Load switch
- Battery-driven devices
- Power management
- Charging circuits
- Power switches (e.g. motors, fans)

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor; for the PNP transistor with negative polarity</b>						
$V_{CEO}$	collector-emitter voltage	open base	-	-	30	V
$I_C$	collector current		-	-	2	A
$I_{CM}$	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	3	A
<b>TR1 (NPN)</b>						
$R_{CEsat}$	collector-emitter saturation resistance	$I_C = 1$ A; $I_B = 100$ mA; pulsed; $t_p \leq 300$ $\mu$ s; $\delta \leq 0.02$ ; $T_{amb} = 25$ °C	-	-	145	m $\Omega$



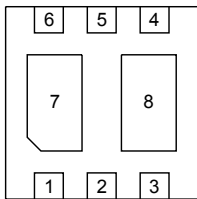
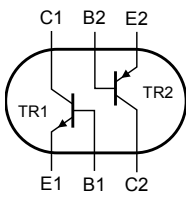
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>TR2 (PNP)</b>						
R <sub>CEsat</sub>	collector-emitter saturation resistance	I <sub>C</sub> = -1 A; I <sub>B</sub> = -100 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	-	-	195	mΩ

## 5. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 <p>Transparent top view <b>DFN2020-6 (SOT1118)</b></p>	 <p>sym139</p>
2	B1	base TR1		
3	C2	collector TR2		
4	E2	emitter TR2		
5	B2	base TR2		
6	C1	collector TR1		
7	C1	collector TR1		
8	C2	collector TR2		

## 6. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
PBSS4230PANP	DFN2020-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1118

## 7. Marking

**Table 4. Marking codes**

Type number	Marking code
PBSS4230PANP	2J

## 8. Limiting values

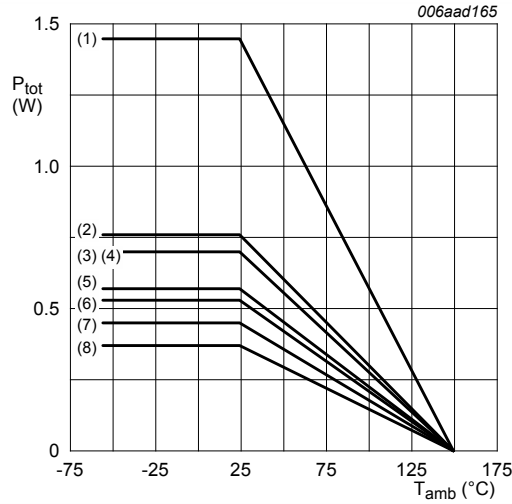
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Per transistor; for the PNP transistor with negative polarity</b>					
V <sub>CBO</sub>	collector-base voltage	open emitter	-	30	V
V <sub>CEO</sub>	collector-emitter voltage	open base	-	30	V

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>EBO</sub>	emitter-base voltage	open collector		-	7	V
I <sub>C</sub>	collector current			-	2	A
I <sub>CM</sub>	peak collector current	single pulse; t <sub>p</sub> ≤ 1 ms		-	3	A
I <sub>B</sub>	base current			-	0.3	A
I <sub>BM</sub>	peak base current	single pulse; t <sub>p</sub> ≤ 1 ms		-	1	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	370	mW
			[2]	-	570	mW
			[3]	-	530	mW
			[4]	-	700	mW
			[5]	-	450	mW
			[6]	-	760	mW
			[7]	-	700	mW
			[8]	-	1450	mW
<b>Per device</b>						
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	510	mW
			[2]	-	780	mW
			[3]	-	730	mW
			[4]	-	960	mW
			[5]	-	620	mW
			[6]	-	1040	mW
			[7]	-	960	mW
			[8]	-	2000	mW
T <sub>j</sub>	junction temperature			-	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C

- [1] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [3] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated and standard footprint.
- [4] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [5] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated and standard footprint.
- [6] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [7] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated and standard footprint.
- [8] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.



- (1) 4-layer PCB 70 μm, mounting pad for collector 1 cm<sup>2</sup>
- (2) FR4 PCB 70 μm, mounting pad for collector 1 cm<sup>2</sup>
- (3) 4-layer PCB 70 μm, standard footprint
- (4) 4-layer PCB 35 μm, mounting pad for collector 1 cm<sup>2</sup>
- (5) FR4 PCB 35 μm, mounting pad for collector 1 cm<sup>2</sup>
- (6) 4-layer PCB 35 μm, standard footprint
- (7) FR4 PCB 70 μm, standard footprint
- (8) FR4 PCB 35 μm, standard footprint

Fig. 1. Per transistor: power derating curves

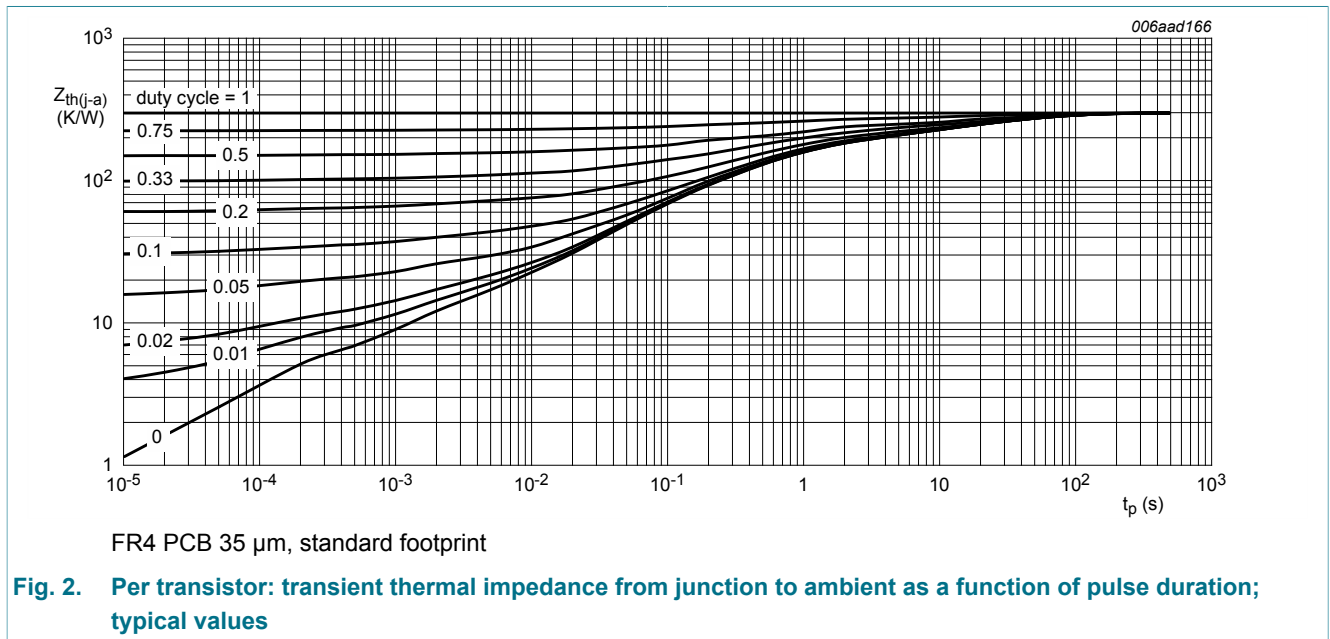
## 9. Thermal characteristics

Table 6. Thermal characteristics

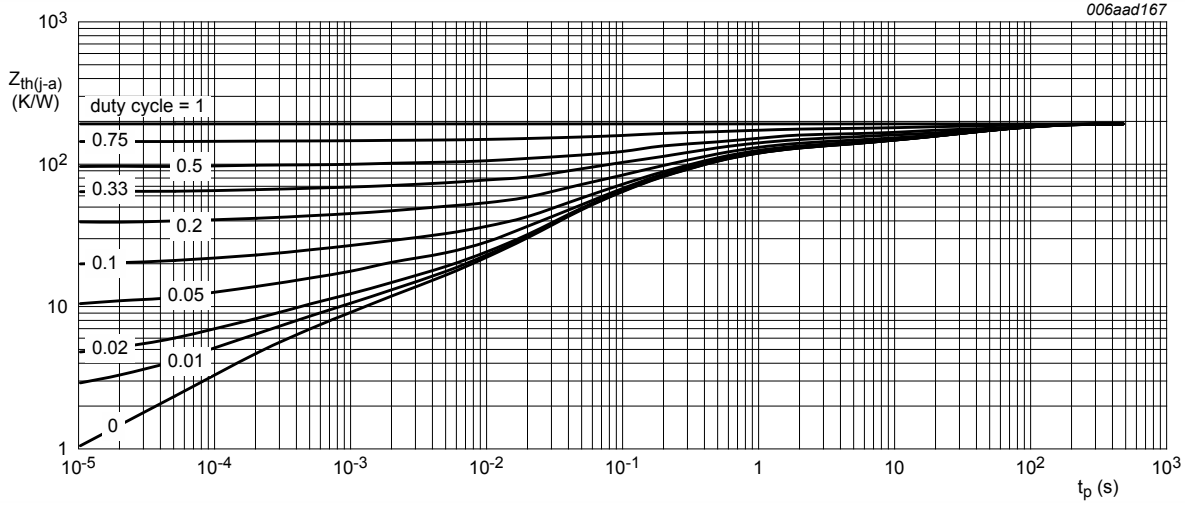
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	-	338	K/W
			[2]	-	-	219	K/W
			[3]	-	-	236	K/W
			[4]	-	-	179	K/W
			[5]	-	-	278	K/W
			[6]	-	-	164	K/W
			[7]	-	-	179	K/W
			[8]	-	-	86	K/W
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point			-	-	30	K/W

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per device</b>							
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	-	245	K/W
			[2]	-	-	160	K/W
			[3]	-	-	171	K/W
			[4]	-	-	130	K/W
			[5]	-	-	202	K/W
			[6]	-	-	120	K/W
			[7]	-	-	130	K/W
			[8]	-	-	63	K/W

- [1] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [3] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated and standard footprint.
- [4] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [5] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated and standard footprint.
- [6] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [7] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated and standard footprint.
- [8] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.

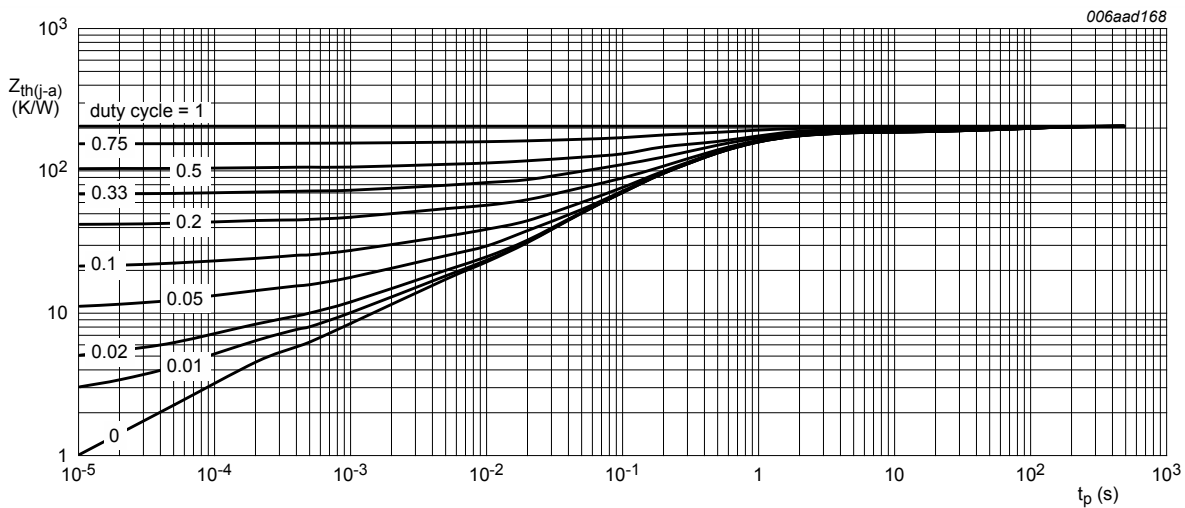


**Fig. 2. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



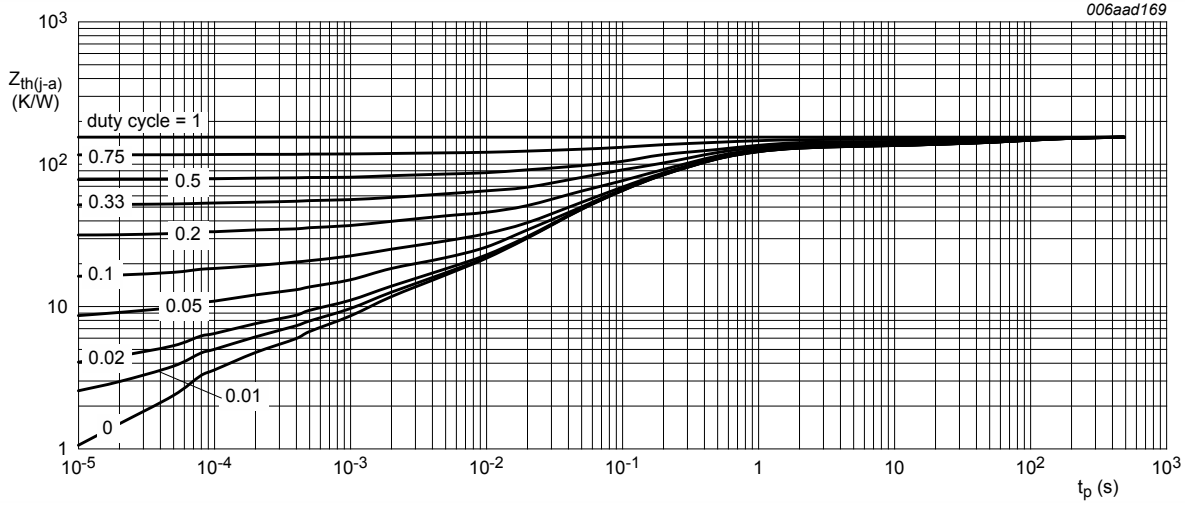
FR4 PCB 35 μm, mounting pad for collector 1 cm<sup>2</sup>

**Fig. 3. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



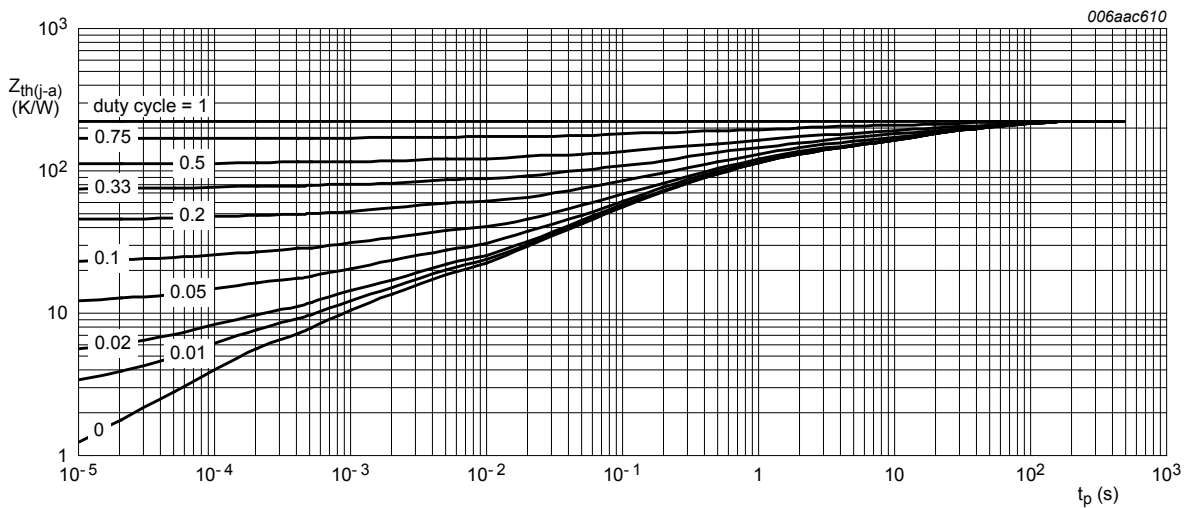
4-layer PCB 35 μm, standard footprint

**Fig. 4. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



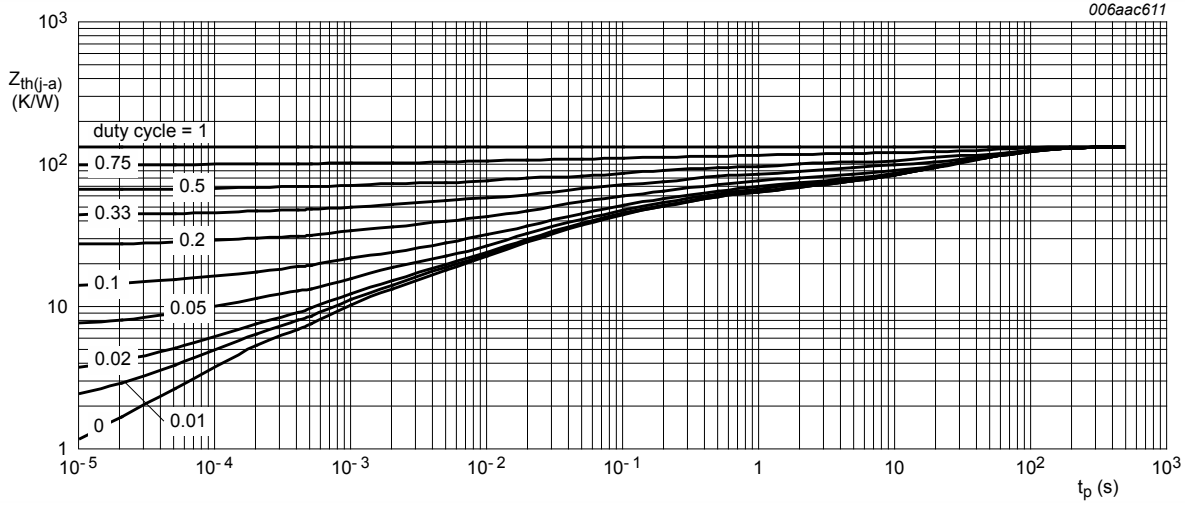
4-layer PCB 35  $\mu$ m, mounting pad for collector 1 cm<sup>2</sup>

Fig. 5. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



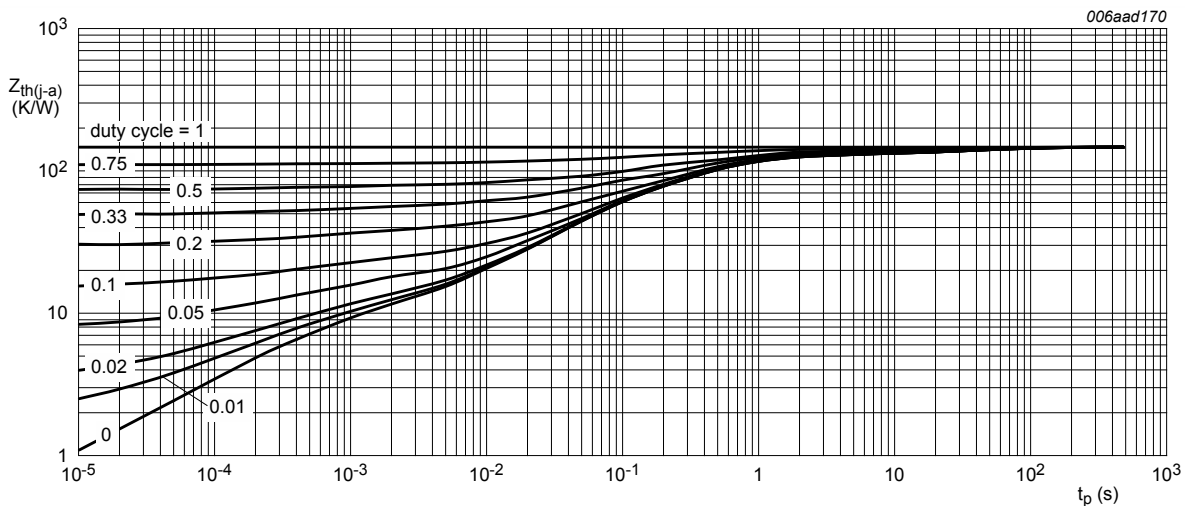
FR4 PCB 70  $\mu$ m, standard footprint

Fig. 6. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB 70  $\mu$ m, mounting pad for collector 1 cm<sup>2</sup>

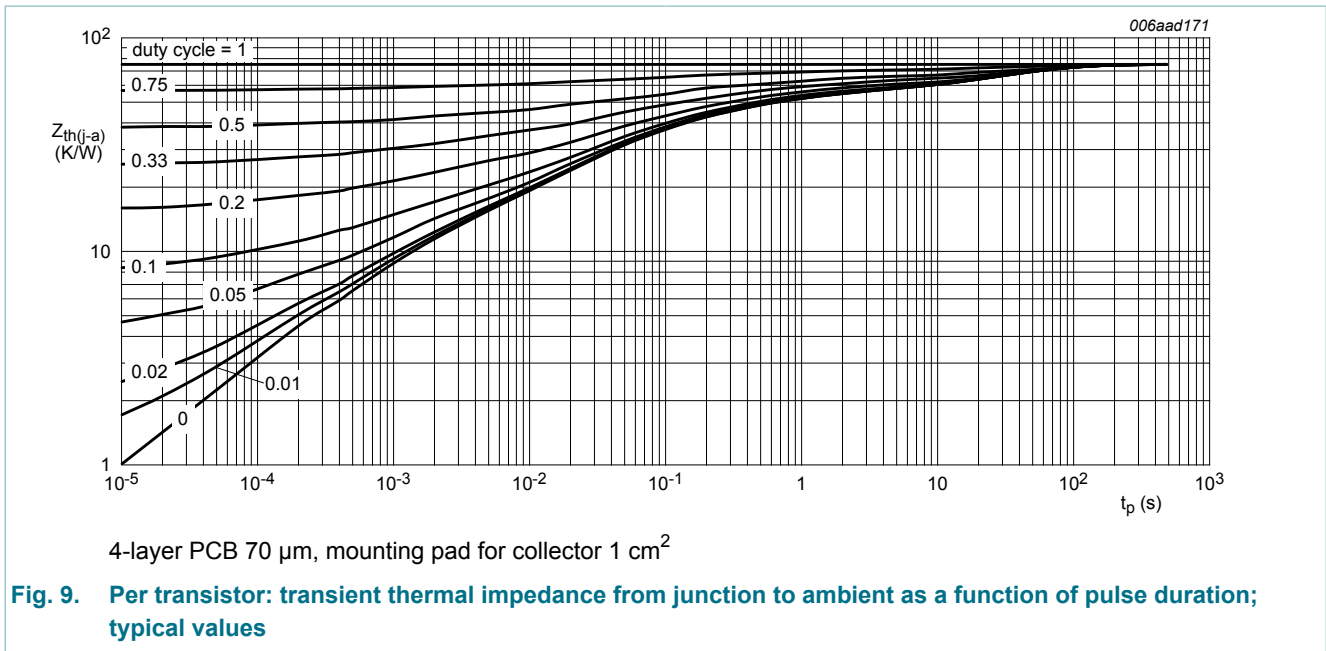
**Fig. 7. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



4-layer PCB 70  $\mu$ m, standard footprint

**Fig. 8. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**





## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>TR1 (NPN)</b>						
$I_{CBO}$	collector-base cut-off current	$V_{CB} = 24 \text{ V}; I_E = 0 \text{ A}; T_{amb} = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{CB} = 24 \text{ V}; I_E = 0 \text{ A}; T_j = 150 \text{ }^\circ\text{C}$	-	-	50	$\mu\text{A}$
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = 5 \text{ V}; I_C = 0 \text{ A}; T_{amb} = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$h_{FE}$	DC current gain	$V_{CE} = 2 \text{ V}; I_C = 100 \text{ mA}; \text{pulsed}; t_p \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^\circ\text{C}$	250	380	-	
		$V_{CE} = 2 \text{ V}; I_C = 500 \text{ mA}; \text{pulsed}; t_p \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^\circ\text{C}$	230	350	-	
		$V_{CE} = 2 \text{ V}; I_C = 1 \text{ A}; \text{pulsed}; t_p \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^\circ\text{C}$	200	310	-	
		$V_{CE} = 2 \text{ V}; I_C = 2 \text{ A}; \text{pulsed}; t_p \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^\circ\text{C}$	150	230	-	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 500 \text{ mA}; I_B = 50 \text{ mA}; T_{amb} = 25 \text{ }^\circ\text{C}$	-	60	80	mV
		$I_C = 1 \text{ A}; I_B = 50 \text{ mA}; \text{pulsed}; t_p \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^\circ\text{C}$	-	120	160	mV
		$I_C = 2 \text{ A}; I_B = 100 \text{ mA}; \text{pulsed}; t_p \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^\circ\text{C}$	-	230	300	mV
		$I_C = 2 \text{ A}; I_B = 200 \text{ mA}; \text{pulsed}; t_p \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{amb} = 25 \text{ }^\circ\text{C}$	-	220	290	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>CEsat</sub>	collector-emitter saturation resistance	I <sub>C</sub> = 1 A; I <sub>B</sub> = 100 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02 ; T <sub>amb</sub> = 25 °C	-	-	145	mΩ
V <sub>BEsat</sub>	base-emitter saturation voltage	I <sub>C</sub> = 500 mA; I <sub>B</sub> = 50 mA; T <sub>amb</sub> = 25 °C	-	-	1	V
		I <sub>C</sub> = 1 A; I <sub>B</sub> = 50 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02 ; T <sub>amb</sub> = 25 °C	-	-	1	V
		I <sub>C</sub> = 2 A; I <sub>B</sub> = 100 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02 ; T <sub>amb</sub> = 25 °C	-	-	1.1	V
		I <sub>C</sub> = 2 A; I <sub>B</sub> = 200 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02 ; T <sub>amb</sub> = 25 °C	-	-	1.2	V
V <sub>BEon</sub>	base-emitter turn-on voltage	V <sub>CE</sub> = 2 V; I <sub>C</sub> = 0.5 A; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02 ; T <sub>amb</sub> = 25 °C	-	-	0.9	V
t <sub>d</sub>	delay time	V <sub>CC</sub> = 12.5 V; I <sub>C</sub> = 1 A; I <sub>Bon</sub> = 50 mA; I <sub>Boff</sub> = -50 mA; T <sub>amb</sub> = 25 °C	-	10	-	ns
t <sub>r</sub>	rise time		-	50	-	ns
t <sub>on</sub>	turn-on time		-	60	-	ns
t <sub>s</sub>	storage time		-	310	-	ns
t <sub>f</sub>	fall time		-	60	-	ns
t <sub>off</sub>	turn-off time		-	370	-	ns
f <sub>T</sub>	transition frequency		V <sub>CE</sub> = 10 V; I <sub>C</sub> = 50 mA; f = 100 MHz; T <sub>amb</sub> = 25 °C	60	120	-
C <sub>c</sub>	collector capacitance	V <sub>CB</sub> = 10 V; I <sub>E</sub> = 0 A; i <sub>e</sub> = 0 A; f = 1 MHz; T <sub>amb</sub> = 25 °C	-	13.5	18	pF
<b>TR2 (PNP)</b>						
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = -24 V; I <sub>E</sub> = 0 A	-	-	-100	nA
		V <sub>CB</sub> = -24 V; I <sub>E</sub> = 0 A; T <sub>j</sub> = 150 °C	-	-	-50	μA
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = -5 V; I <sub>C</sub> = 0 A	-	-	-100	nA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = -2 V; I <sub>C</sub> = -100 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02 ; T <sub>amb</sub> = 25 °C	260	370	-	
		V <sub>CE</sub> = -2 V; I <sub>C</sub> = -500 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02 ; T <sub>amb</sub> = 25 °C	210	290	-	
		V <sub>CE</sub> = -2 V; I <sub>C</sub> = -1 A; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02 ; T <sub>amb</sub> = 25 °C	160	230	-	
		V <sub>CE</sub> = -2 V; I <sub>C</sub> = -2 A; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02 ; T <sub>amb</sub> = 25 °C	100	145	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = -500 mA; I <sub>B</sub> = -50 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02 ; T <sub>amb</sub> = 25 °C	-	-75	-110	mV
		I <sub>C</sub> = -1 A; I <sub>B</sub> = -50 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02 ; T <sub>amb</sub> = 25 °C	-	-155	-220	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$I_C = -2\text{ A}; I_B = -100\text{ mA};$ pulsed; $t_p \leq 300\ \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25\text{ }^\circ\text{C}$	-	-295	-420	mV
		$I_C = -2\text{ A}; I_B = -200\text{ mA};$ pulsed; $t_p \leq 300\ \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25\text{ }^\circ\text{C}$	-	-275	-390	mV
$R_{\text{CEsat}}$	collector-emitter saturation resistance	$I_C = -1\text{ A}; I_B = -100\text{ mA};$ pulsed; $t_p \leq 300\ \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25\text{ }^\circ\text{C}$	-	-	195	m $\Omega$
$V_{\text{BEsat}}$	base-emitter saturation voltage	$I_C = -500\text{ mA}; I_B = -50\text{ mA};$ pulsed; $t_p \leq 300\ \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25\text{ }^\circ\text{C}$	-	-	-1	V
		$I_C = -1\text{ A}; I_B = -50\text{ mA};$ pulsed; $t_p \leq 300\ \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25\text{ }^\circ\text{C}$	-	-	-1	V
		$I_C = -2\text{ A}; I_B = -100\text{ mA};$ pulsed; $t_p \leq 300\ \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25\text{ }^\circ\text{C}$	-	-	-1.1	V
		$I_C = -2\text{ A}; I_B = -200\text{ mA};$ pulsed; $t_p \leq 300\ \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25\text{ }^\circ\text{C}$	-	-	-1.2	V
$V_{\text{BEon}}$	base-emitter turn-on voltage	$V_{\text{CE}} = -2\text{ V}; I_C = -0.5\text{ A};$ pulsed; $t_p \leq 300\ \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25\text{ }^\circ\text{C}$	-	-	-0.9	V
$t_d$	delay time	$V_{\text{CC}} = -12.5\text{ V}; I_C = -1\text{ A}; I_{\text{Bon}} = -0.05\text{ A};$ $I_{\text{Boff}} = 0.05\text{ A}; T_{\text{amb}} = 25\text{ }^\circ\text{C}$	-	10	-	ns
$t_r$	rise time		-	50	-	ns
$t_{\text{on}}$	turn-on time		-	60	-	ns
$t_s$	storage time		-	200	-	ns
$t_f$	fall time		-	45	-	ns
$t_{\text{off}}$	turn-off time		-	245	-	ns
$f_T$	transition frequency		$V_{\text{CE}} = -10\text{ V}; I_C = -50\text{ mA}; f = 100\text{ MHz};$ $T_{\text{amb}} = 25\text{ }^\circ\text{C}$	50	95	-
$C_c$	collector capacitance	$V_{\text{CB}} = -10\text{ V}; I_E = 0\text{ A}; i_e = 0\text{ A};$ $f = 1\text{ MHz}; T_{\text{amb}} = 25\text{ }^\circ\text{C}$	-	22	29	pF

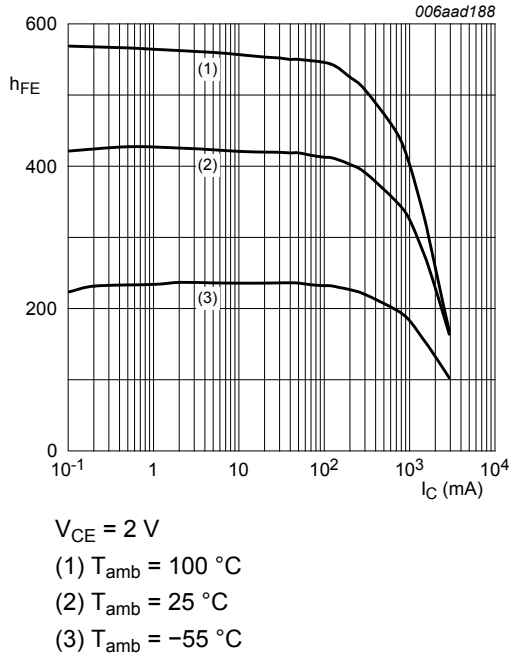


Fig. 10. TR1 (NPN): DC current gain as a function of collector current; typical values

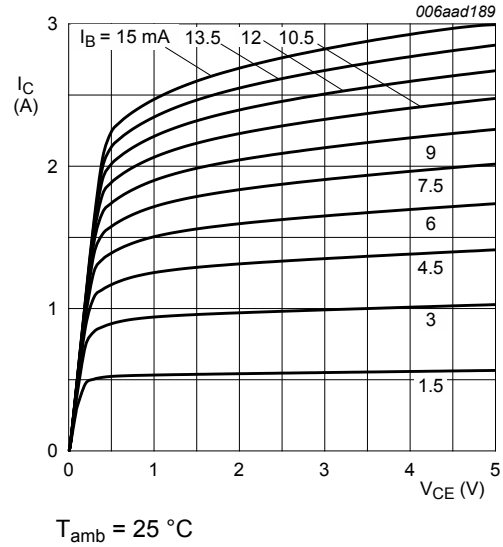


Fig. 11. TR1 (NPN): Collector current as a function of collector-emitter voltage; typical values

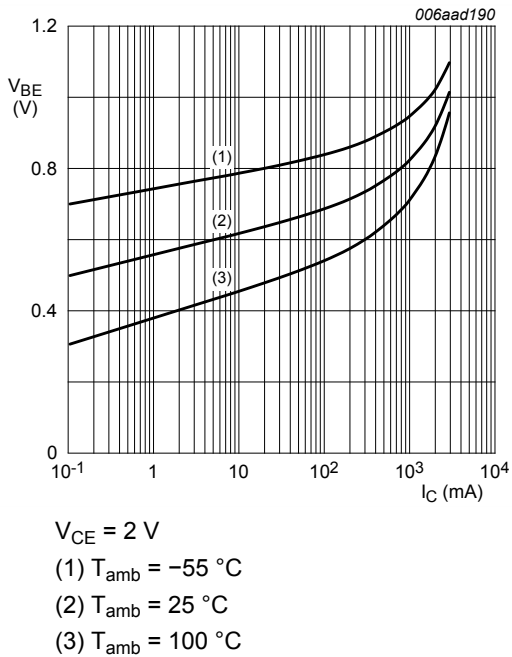


Fig. 12. TR1 (NPN): Base-emitter voltage as a function of collector current; typical values

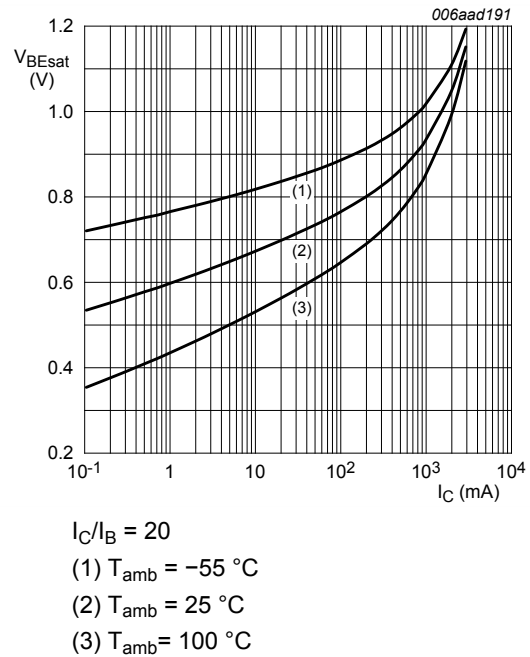
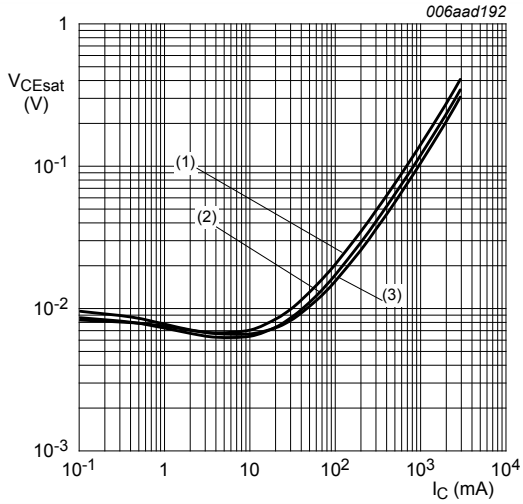
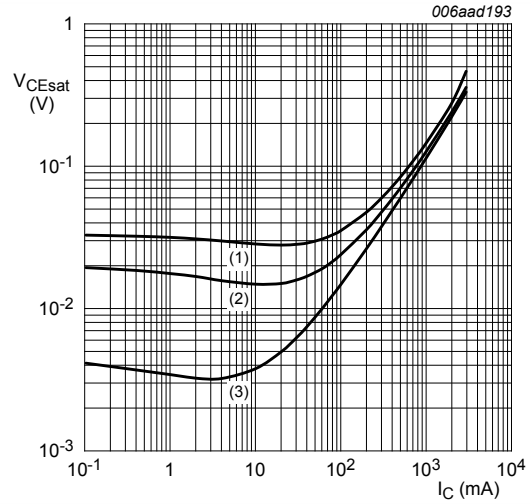


Fig. 13. TR1 (NPN): Base-emitter saturation voltage as a function of collector current; typical values



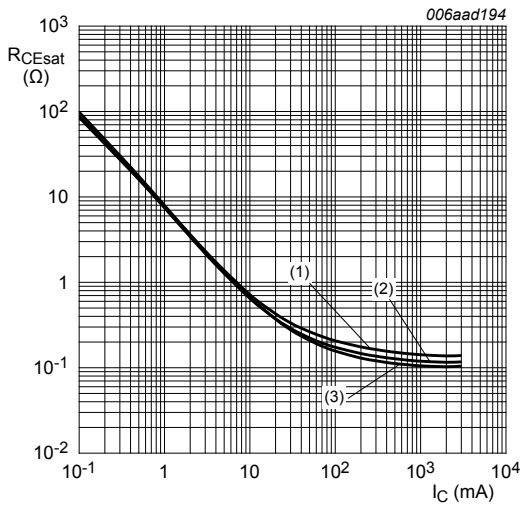
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -55\text{ °C}$

**Fig. 14. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values**



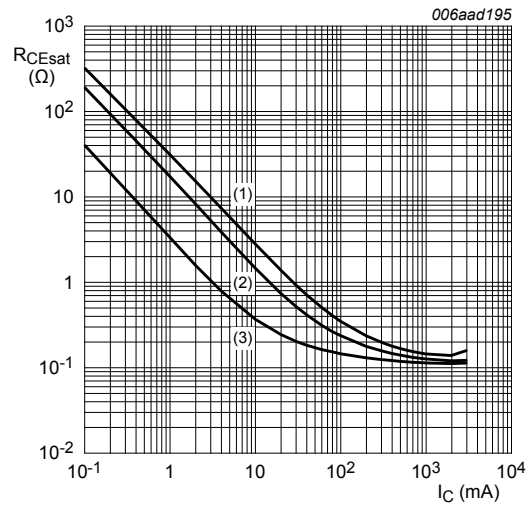
$T_{amb} = 25\text{ °C}$   
 (1)  $I_C/I_B = 100$   
 (2)  $I_C/I_B = 50$   
 (3)  $I_C/I_B = 10$

**Fig. 15. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values**



$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -55\text{ °C}$

**Fig. 16. TR1 (NPN): Collector-emitter saturation resistance as a function of collector current; typical values**



$T_{amb} = 25\text{ °C}$   
 (1)  $I_C/I_B = 100$   
 (2)  $I_C/I_B = 50$   
 (3)  $I_C/I_B = 10$

**Fig. 17. TR1 (NPN): Collector-emitter saturation resistance as a function of collector current; typical values**

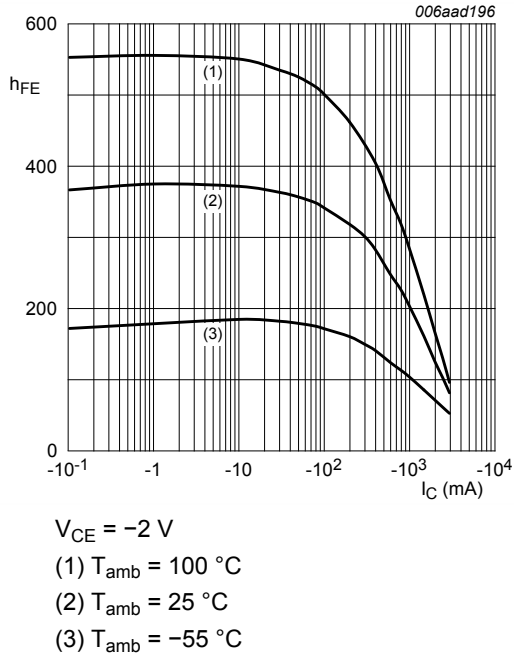


Fig. 18. TR2 (PNP): DC current gain as a function of collector current; typical values

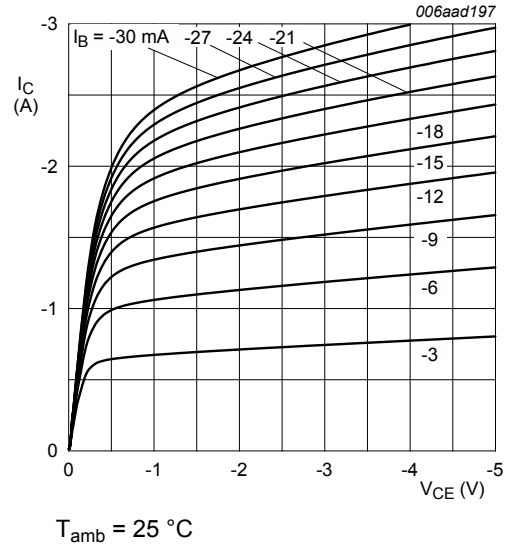


Fig. 19. TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values

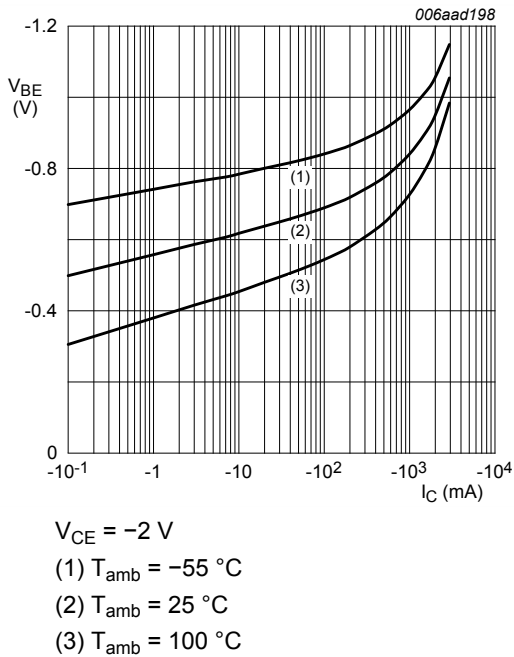


Fig. 20. TR2 (PNP): Base-emitter voltage as a function of collector current; typical values

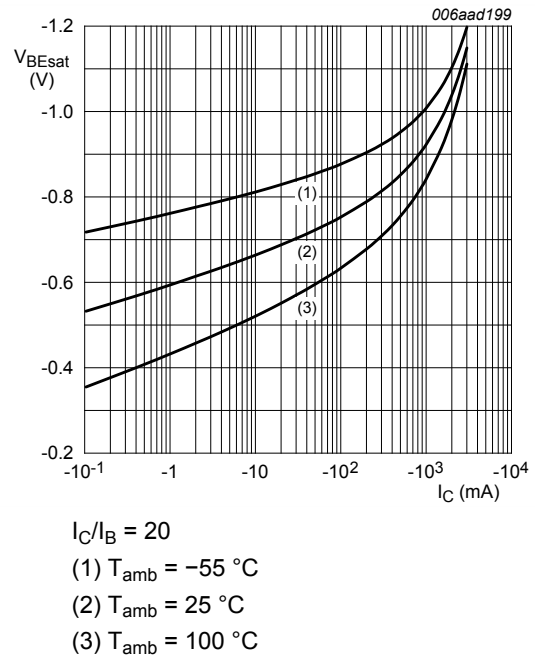
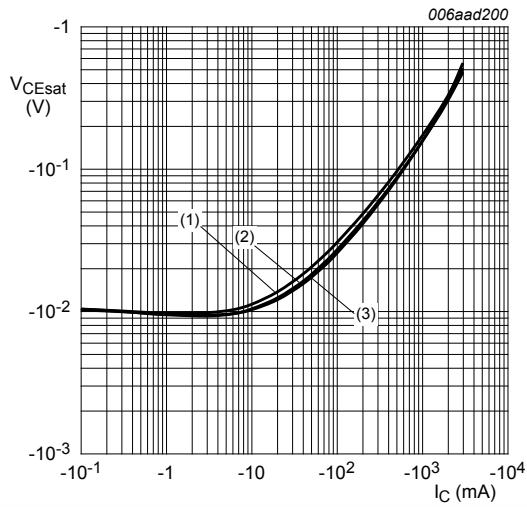
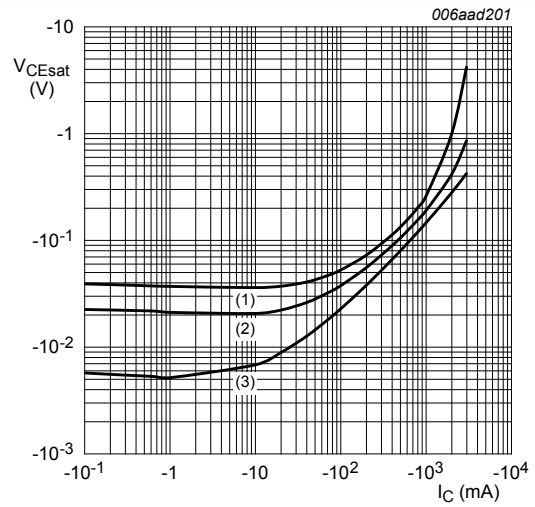


Fig. 21. TR2 (PNP): Base-emitter saturation voltage as a function of collector current; typical values



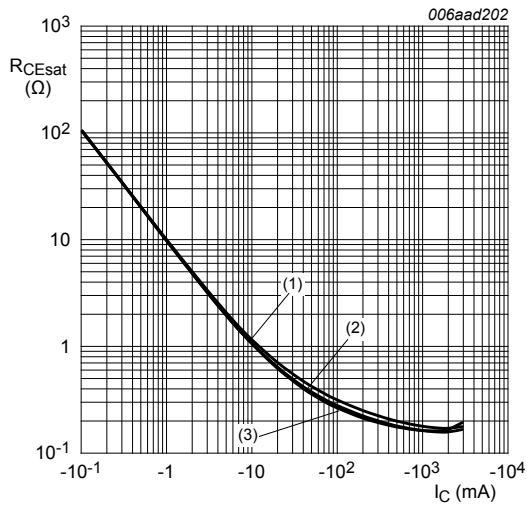
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = -55\text{ }^\circ\text{C}$

**Fig. 22. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values**



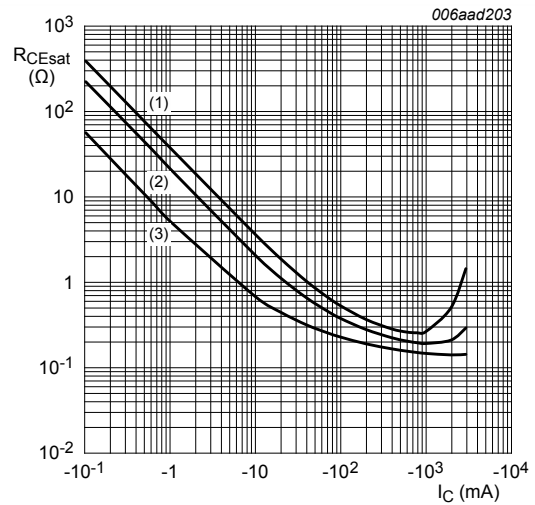
$T_{amb} = 25\text{ }^\circ\text{C}$   
 (1)  $I_C/I_B = 100$   
 (2)  $I_C/I_B = 50$   
 (3)  $I_C/I_B = 10$

**Fig. 23. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values**



$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = -55\text{ }^\circ\text{C}$

**Fig. 24. TR2 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values**



$T_{amb} = 25\text{ }^\circ\text{C}$   
 (1)  $I_C/I_B = 100$   
 (2)  $I_C/I_B = 50$   
 (3)  $I_C/I_B = 10$

**Fig. 25. TR2 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values**

11. Test information

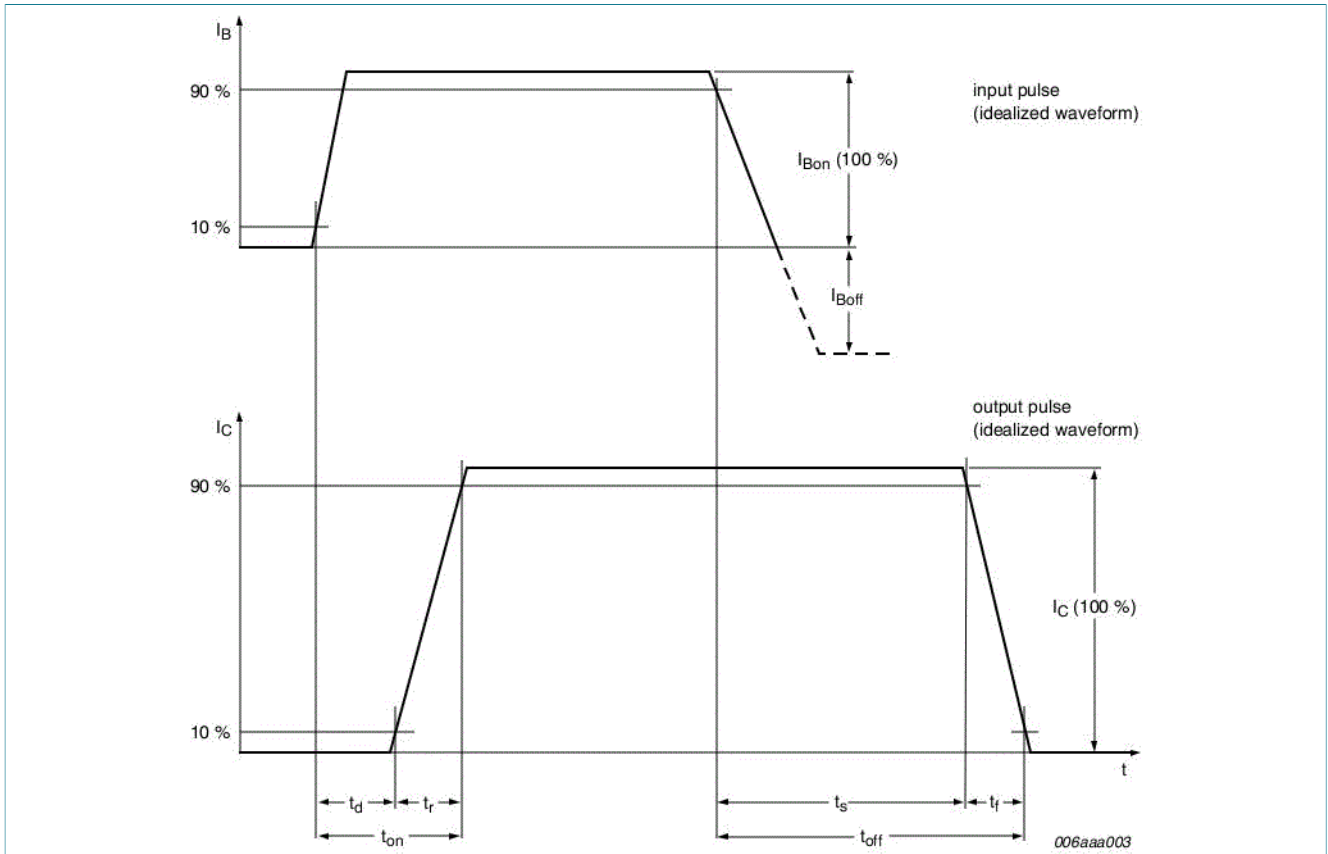


Fig. 26. TR1 (NPN): BISS transistor switching time definition

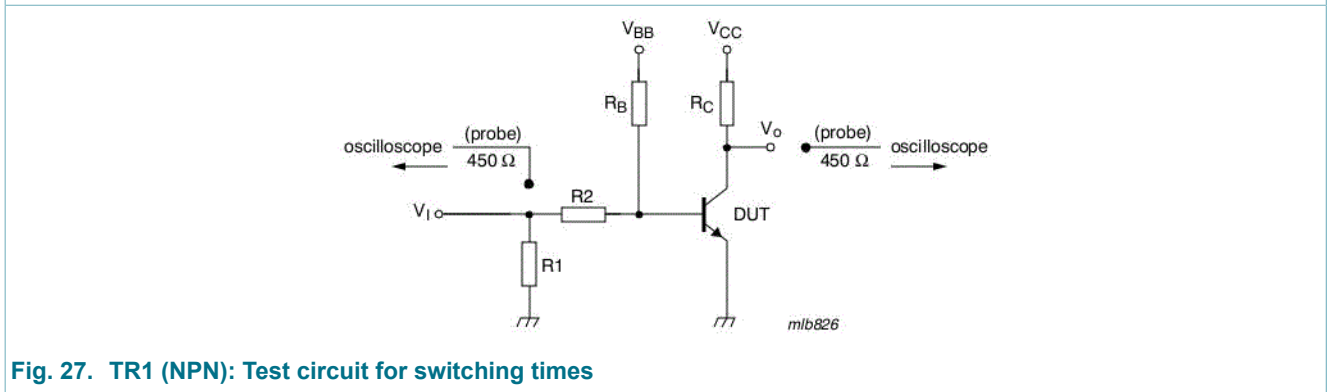


Fig. 27. TR1 (NPN): Test circuit for switching times



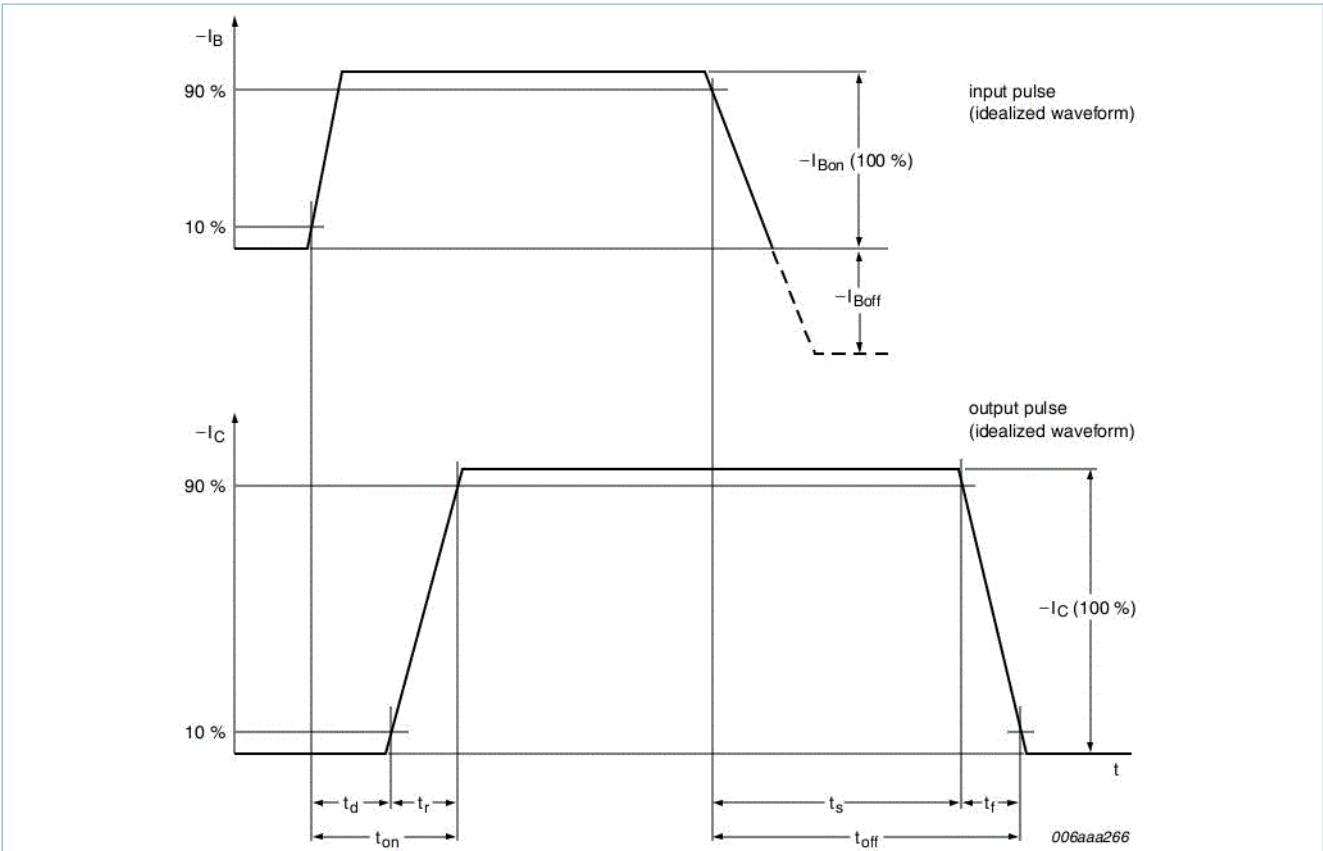


Fig. 28. TR2 (PNP): BISS transistor switching time definition

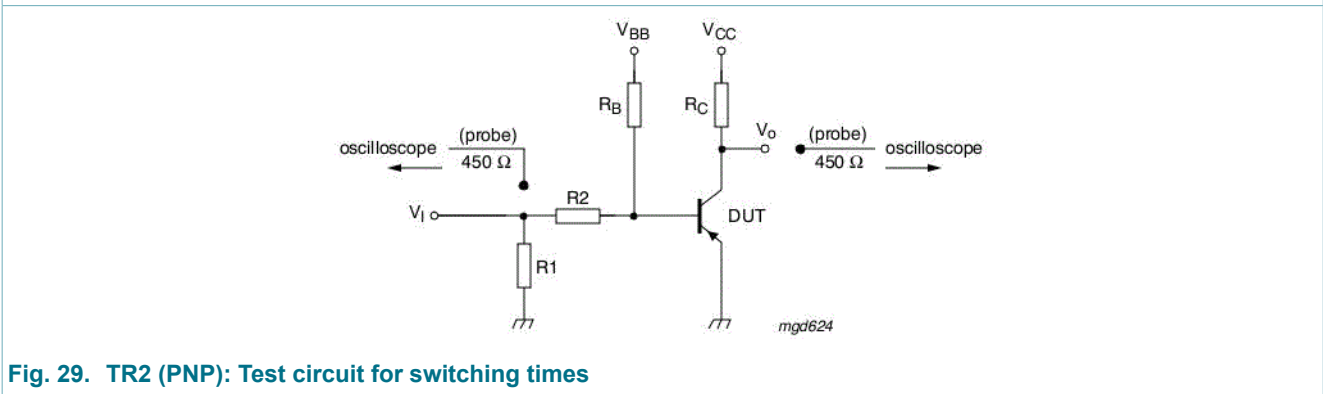


Fig. 29. TR2 (PNP): Test circuit for switching times

### 11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

### 12. Package outline

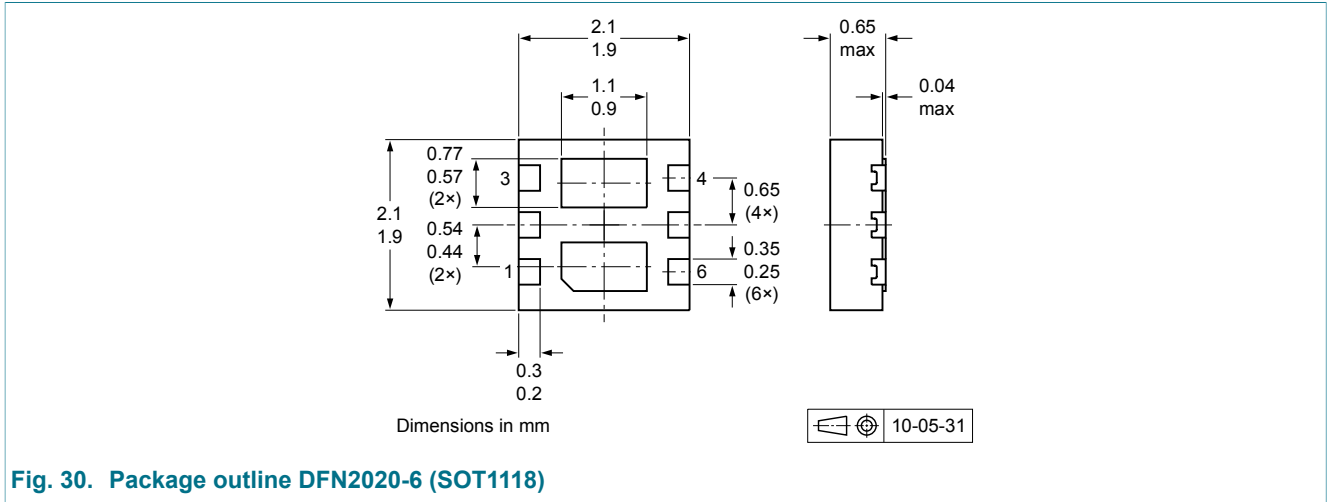


Fig. 30. Package outline DFN2020-6 (SOT1118)

### 13. Soldering

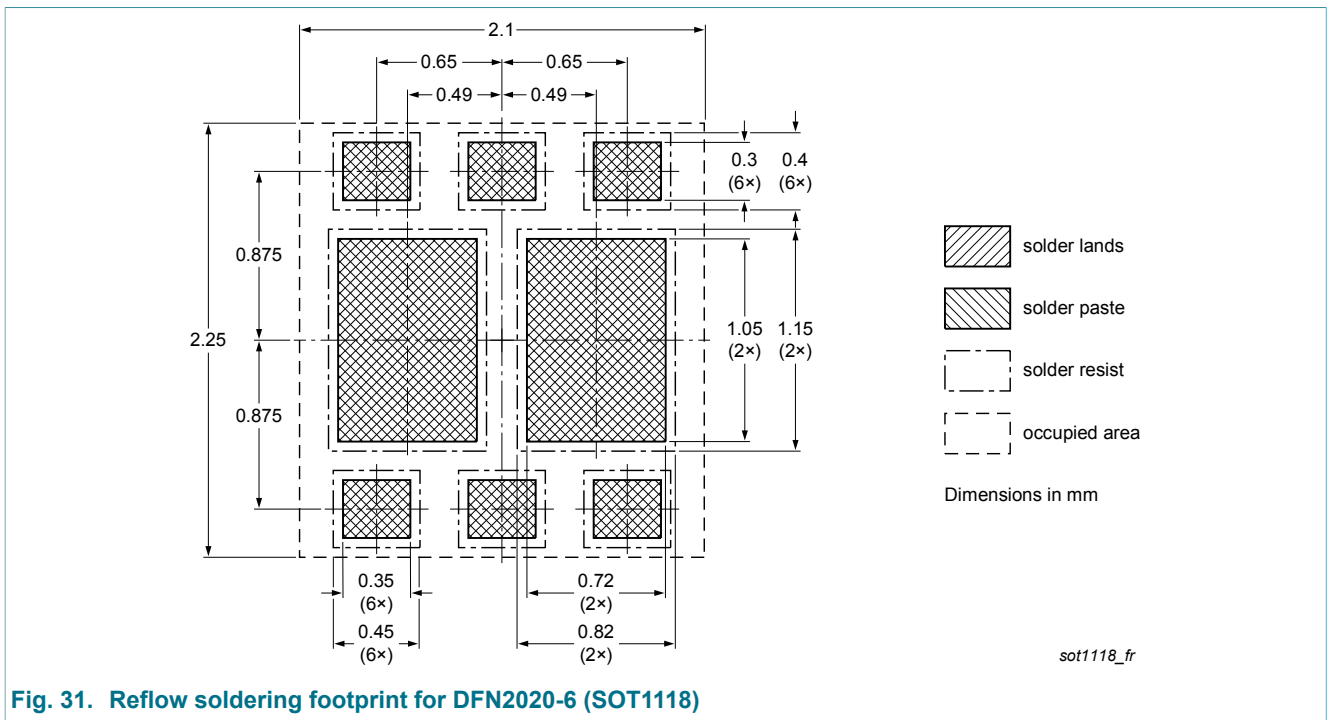


Fig. 31. Reflow soldering footprint for DFN2020-6 (SOT1118)

### 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBSS4230PANP v.1	20121214	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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## 16. Contents

<b>1</b>	<b>General description .....</b>	<b>1</b>
<b>2</b>	<b>Features and benefits .....</b>	<b>1</b>
<b>3</b>	<b>Applications .....</b>	<b>1</b>
<b>4</b>	<b>Quick reference data .....</b>	<b>1</b>
<b>5</b>	<b>Pinning information .....</b>	<b>2</b>
<b>6</b>	<b>Ordering information .....</b>	<b>2</b>
<b>7</b>	<b>Marking .....</b>	<b>2</b>
<b>8</b>	<b>Limiting values .....</b>	<b>2</b>
<b>9</b>	<b>Thermal characteristics .....</b>	<b>4</b>
<b>10</b>	<b>Characteristics .....</b>	<b>9</b>
<b>11</b>	<b>Test information .....</b>	<b>16</b>
11.1	Quality information .....	
<b>12</b>	<b>Package outline .....</b>	<b>18</b>
<b>13</b>	<b>Soldering .....</b>	<b>18</b>
<b>14</b>	<b>Revision history .....</b>	<b>18</b>
<b>15</b>	<b>Legal information .....</b>	<b>19</b>
15.1	Data sheet status .....	19
15.2	Definitions .....	19
15.3	Disclaimers .....	19
15.4	Trademarks .....	20

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