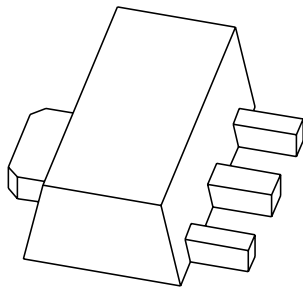


DATA SHEET



PBSS4520X

20 V, 5 A

NPN low V_{CEsat} (BISS) transistor

Product specification
Supersedes data of 2004 Jun 11

2004 Nov 08

20 V, 5 A NPN low V_{CEsat} (BISS) transistor

PBSS4520X

FEATURES

- High h_{FE} and low V_{CEsat} at high current operation
- High collector current capability: I_C maximum 5 A
- Higher efficiency leading to less heat generation.

APPLICATIONS

- Medium power peripheral drivers, e.g. fans and motors
- Strobe flash units for DSC and mobile phones
- Inverter applications, e.g. TFT displays
- Power switch for LAN and ADSL systems
- Medium power DC-to-DC conversion
- Battery chargers.

DESCRIPTION

NPN low V_{CEsat} BISS transistor in a SOT89 (SC-62) plastic package.

PNP complement: PBSS5520X.

MARKING

TYPE NUMBER	MARKING CODE ⁽¹⁾
PBSS4520X	*1F

Note

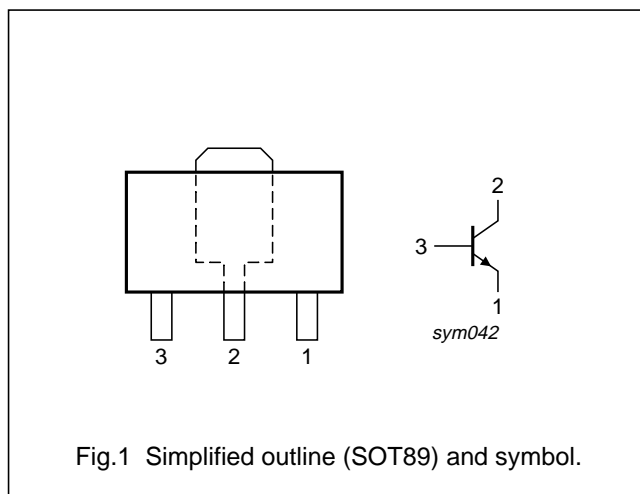
- * = p: made in Hong Kong
* = t: made in Malaysia
* = W: made in China.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CEO}	collector-emitter voltage	20	V
I_C	collector current (DC)	5	A
I_{CM}	peak collector current	10	A
R_{CEsat}	equivalent on-resistance	44	m Ω

PINNING

PIN	DESCRIPTION
1	emitter
2	collector
3	base



ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PBSS4520X	SC-62	plastic surface mounted package; collector pad for good heat transfer; 3 leads	SOT89

20 V, 5 A NPN low V_{CEsat} (BISS) transistor

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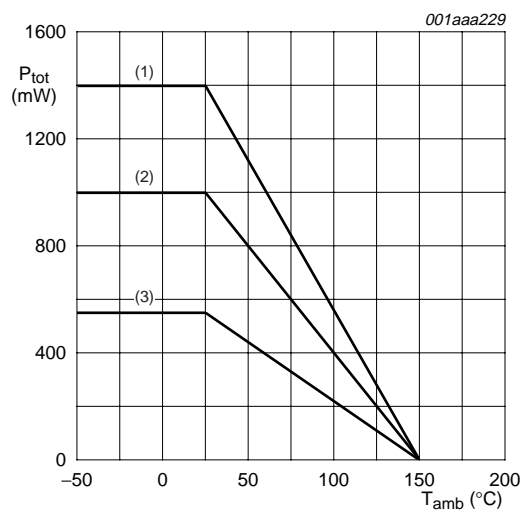
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	20	V
V_{CEO}	collector-emitter voltage	open base	–	20	V
V_{EBO}	emitter-base voltage	open collector	–	5	V
I_C	collector current (DC)		–	5	A
I_{CRM}	repetitive peak collector current	notes 1 and 2	–	7	A
I_{CM}	peak collector current	$t_p \leq 1$ ms	–	10	A
I_B	base current (DC)		–	1	A
I_{BM}	peak base current	$t_p \leq 1$ ms	–	2	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C			
		notes 1 and 2	–	2.5	W
		note 2	–	0.55	W
		note 3	–	1	W
		note 4	–	1.4	W
		note 5	–	1.6	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	ambient temperature		–65	+150	°C

Notes

1. Operated under pulsed conditions: pulse width $t_p \leq 10$ ms; duty cycle $\delta \leq 0.2$.
2. Device mounted on a printed-circuit board, single-sided copper, tin-plated and standard footprint.
3. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 1 cm².
4. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 6 cm².
5. Device mounted on a 7 cm² ceramic printed-circuit board, 1 cm² single-sided copper and tin-plated. For other mounting conditions, see "Thermal considerations for SOT89 in the General Part of associated Handbook".

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- (1) FR4 PCB; 6 cm² mounting pad for collector.
(2) FR4 PCB; 1 cm² mounting pad for collector.
(3) FR4 PCB; standard footprint.

Fig.2 Power derating curves.

20 V, 5 A
NPN low V_{CEsat} (BISS) transistor

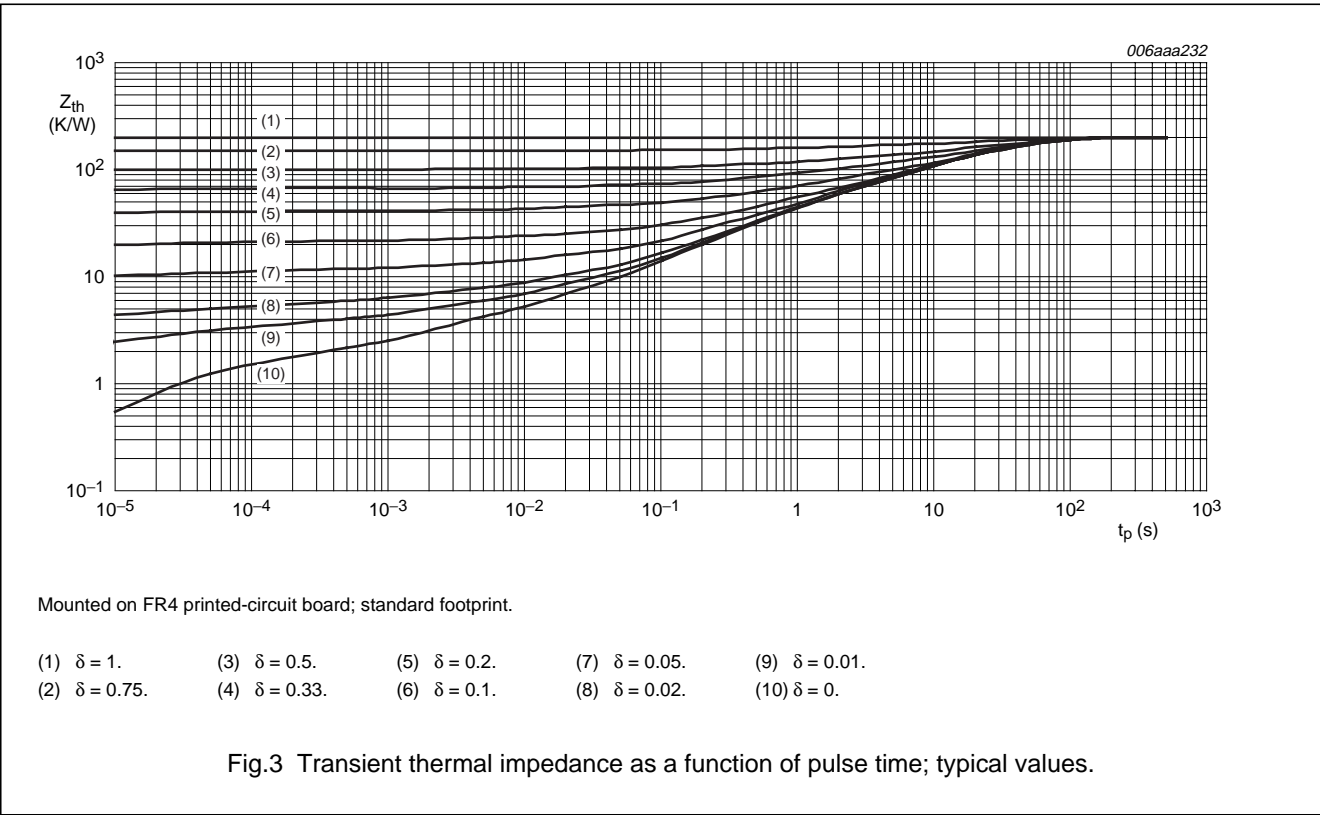
PBSS4520X

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
		notes 1 and 2	50	K/W
		note 2	225	K/W
		note 3	125	K/W
		note 4	90	K/W
		note 5	80	K/W
$R_{th(j-s)}$	thermal resistance from junction to soldering point		16	K/W

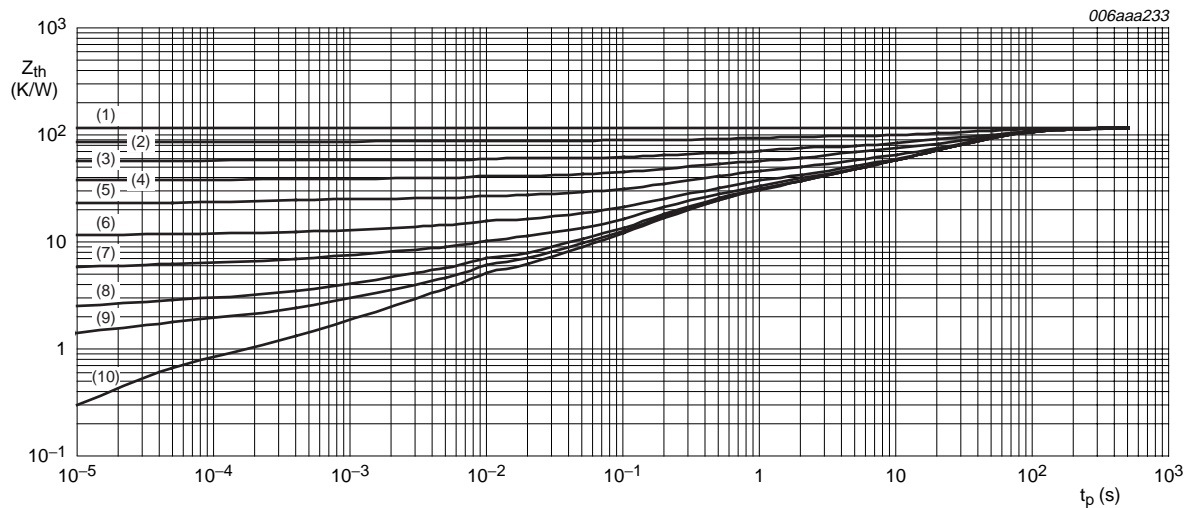
Notes

- 1. Operated under pulsed conditions: pulse width $t_p \leq 10$ ms; duty cycle $\delta \leq 0.2$.
- 2. Device mounted on a printed-circuit board, single-sided copper, tin-plated and standard footprint.
- 3. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 1 cm².
- 4. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 6 cm².
- 5. Device mounted on a 7 cm² ceramic printed-circuit board, 1 cm² single-sided copper and tin-plated. For other mounting conditions, see “Thermal considerations for SOT89 in the General Part of associated Handbook”.



20 V, 5 A
NPN low V_{CEsat} (BISS) transistor

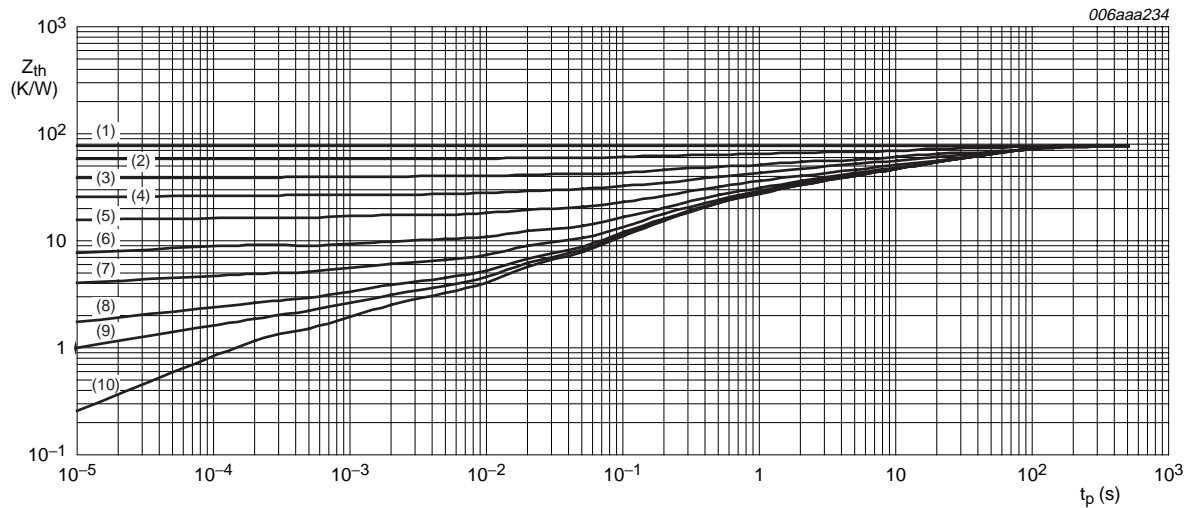
PBSS4520X



Mounted on FR4 printed-circuit board; mounting pad for collector 1 cm².

- | | | | | |
|----------------------|----------------------|---------------------|----------------------|----------------------|
| (1) $\delta = 1.$ | (3) $\delta = 0.5.$ | (5) $\delta = 0.2.$ | (7) $\delta = 0.05.$ | (9) $\delta = 0.01.$ |
| (2) $\delta = 0.75.$ | (4) $\delta = 0.33.$ | (6) $\delta = 0.1.$ | (8) $\delta = 0.02.$ | (10) $\delta = 0.$ |

Fig.4 Transient thermal impedance as a function of pulse time; typical values.



Mounted on FR4 printed-circuit board; mounting pad for collector 6 cm².

- | | | | | |
|----------------------|----------------------|---------------------|----------------------|----------------------|
| (1) $\delta = 1.$ | (3) $\delta = 0.5.$ | (5) $\delta = 0.2.$ | (7) $\delta = 0.05.$ | (9) $\delta = 0.01.$ |
| (2) $\delta = 0.75.$ | (4) $\delta = 0.33.$ | (6) $\delta = 0.1.$ | (8) $\delta = 0.02.$ | (10) $\delta = 0.$ |

Fig.5 Transient thermal impedance as a function of pulse time; typical values.

20 V, 5 A NPN low V_{CEsat} (BISS) transistor

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CHARACTERISTICS $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

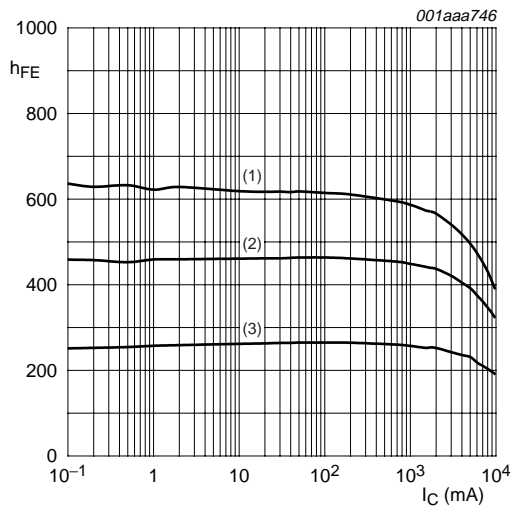
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$V_{CB} = 20\text{ V}; I_E = 0\text{ A}$	–	–	100	nA
		$V_{CB} = 20\text{ V}; I_E = 0\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$	–	–	50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}$	–	–	100	nA
I_{CES}	collector-emitter cut-off current	$V_{CE} = 20\text{ V}; V_{BE} = 0\text{ V}$	–	–	100	nA
h_{FE}	DC current gain	$V_{CE} = 2\text{ V}$ $I_C = 0.5\text{ A}$	300	450	–	
		$I_C = 1\text{ A}; \text{note 1}$	300	440	–	
		$I_C = 2\text{ A}; \text{note 1}$	250	420	–	
		$I_C = 5\text{ A}; \text{note 1}$	200	380	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 0.5\text{ A}; I_B = 5\text{ mA}$	–	35	50	mV
		$I_C = 1\text{ A}; I_B = 10\text{ mA}$	–	50	70	mV
		$I_C = 2.5\text{ A}; I_B = 125\text{ mA}; \text{note 1}$	–	85	120	mV
		$I_C = 4\text{ A}; I_B = 200\text{ mA}; \text{note 1}$	–	130	180	mV
		$I_C = 5\text{ A}; I_B = 500\text{ mA}; \text{note 1}$	–	160	220	mV
R_{CEsat}	equivalent on-resistance	$I_C = 5\text{ A}; I_B = 500\text{ mA}; \text{note 1}$	–	32	44	$\text{m}\Omega$
V_{BEsat}	base-emitter saturation voltage	$I_C = 4\text{ A}; I_B = 200\text{ mA}; \text{note 1}$	–	0.9	1.05	V
		$I_C = 5\text{ A}; I_B = 500\text{ mA}; \text{note 1}$	–	0.96	1.1	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = 2\text{ V}; I_C = 2\text{ A}$	–	0.74	0.85	V
f_T	transition frequency	$I_C = 100\text{ mA}; V_{CE} = 10\text{ V};$ $f = 100\text{ MHz}$	100	125	–	MHz
C_c	collector capacitance	$V_{CB} = 10\text{ V}; I_E = i_e = 0\text{ A}; f = 1\text{ MHz}$	–	90	110	pF

Note

1. Pulse test: $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02$.

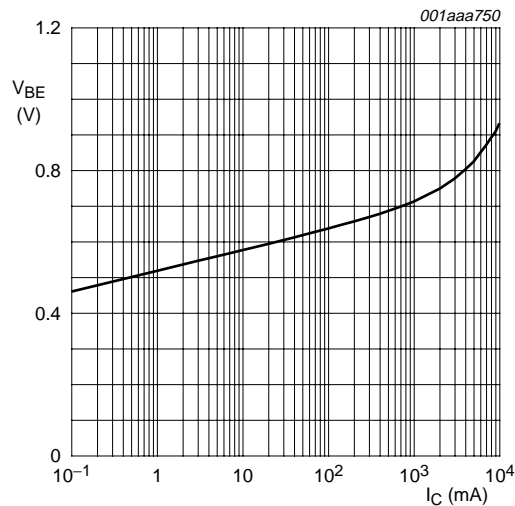
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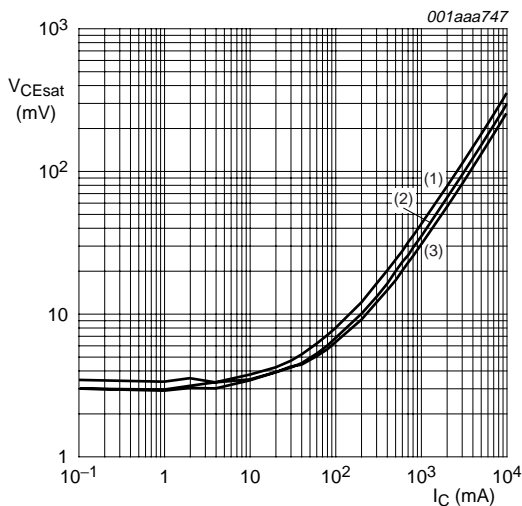
$V_{CE} = 2\text{ V}$.
(1) $T_{amb} = 100^\circ\text{C}$.
(2) $T_{amb} = 25^\circ\text{C}$.
(3) $T_{amb} = -55^\circ\text{C}$.

Fig.6 DC current gain as a function of collector current; typical values.



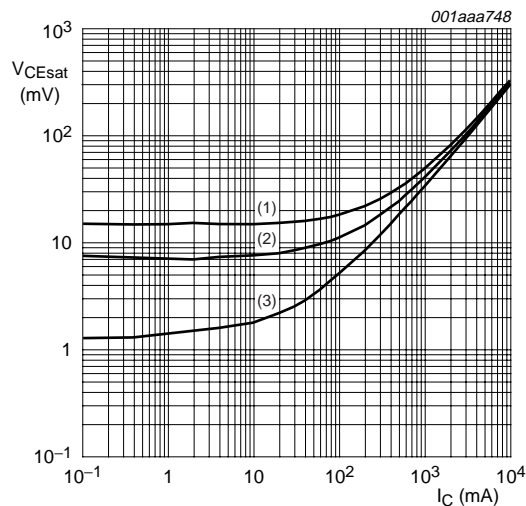
$V_{CE} = 2\text{ V}$.
 $T_{amb} = 25^\circ\text{C}$.

Fig.7 Base-emitter voltage as a function of collector current; typical values.



$I_C/I_B = 20$.
(1) $T_{amb} = 100^\circ\text{C}$.
(2) $T_{amb} = -55^\circ\text{C}$.
(3) $T_{amb} = 25^\circ\text{C}$.

Fig.8 Collector-emitter saturation voltage as a function of collector current; typical values.

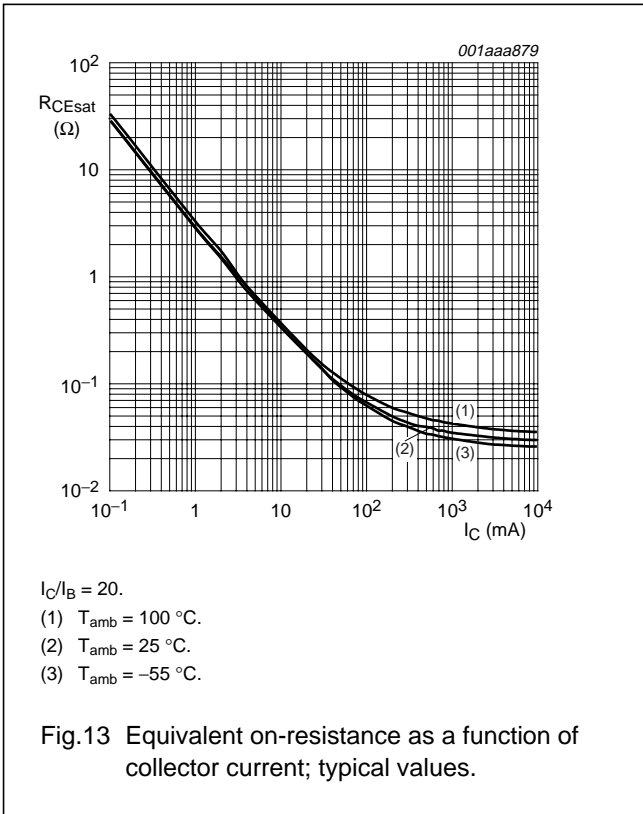
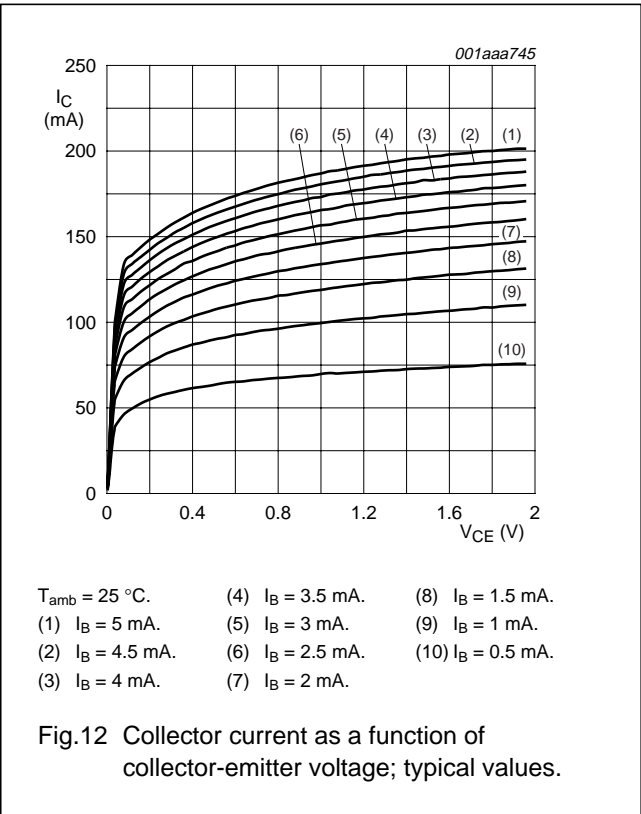
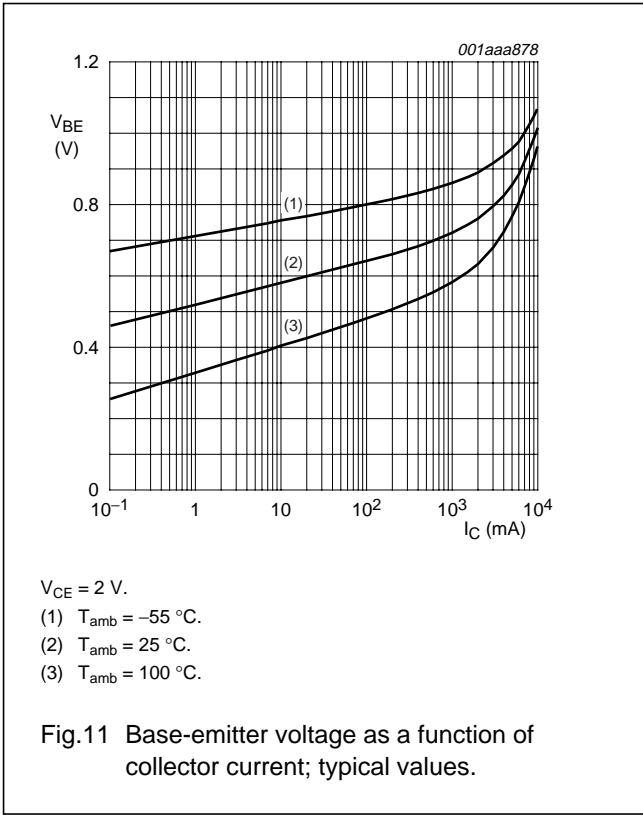
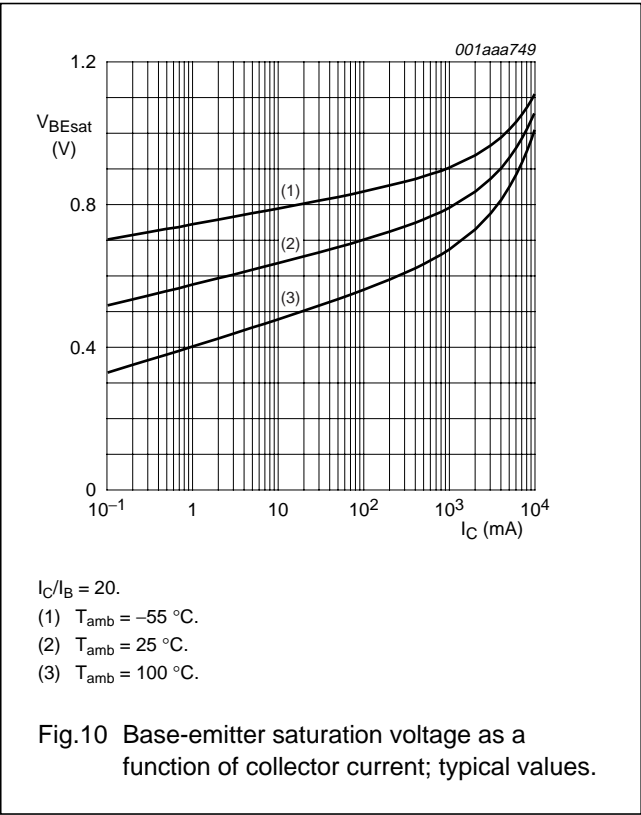


$T_{amb} = 25^\circ\text{C}$.
(1) $I_C/I_B = 100$.
(2) $I_C/I_B = 50$.
(3) $I_C/I_B = 10$.

Fig.9 Collector-emitter saturation voltage as a function of collector current; typical values.

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[illegible]

Technical drawing of the MLE322 component. The overall dimensions are 32 mm in width and 40 mm in height. The component features a central rectangular body with a width of 10 mm and a height of 10 mm. Below this body, there are three vertical structures. The leftmost structure has a width of 3.96 mm and a height of 2.5 mm. The middle structure has a width of 1.6 mm and a height of 0.5 mm. The rightmost structure has a width of 1.6 mm and a height of 0.5 mm. The distance between the left and middle structures is 1 mm, and the distance between the middle and right structures is 1 mm. The total height of the component is 40 mm, and the total width is 32 mm.

Technical drawing of a rectangular block with a central cavity and three vertical channels. The block has a total width of 32 mm and a total height of 40 mm. The top surface is 32 mm wide. The central cavity is 30 mm wide and 20 mm high. The three vertical channels are 2.5 mm wide and 0.5 mm deep. The distance between the centers of the channels is 3.96 mm. The distance from the center of the central cavity to the center of the rightmost channel is 1.6 mm. The drawing is labeled 001aaa235.

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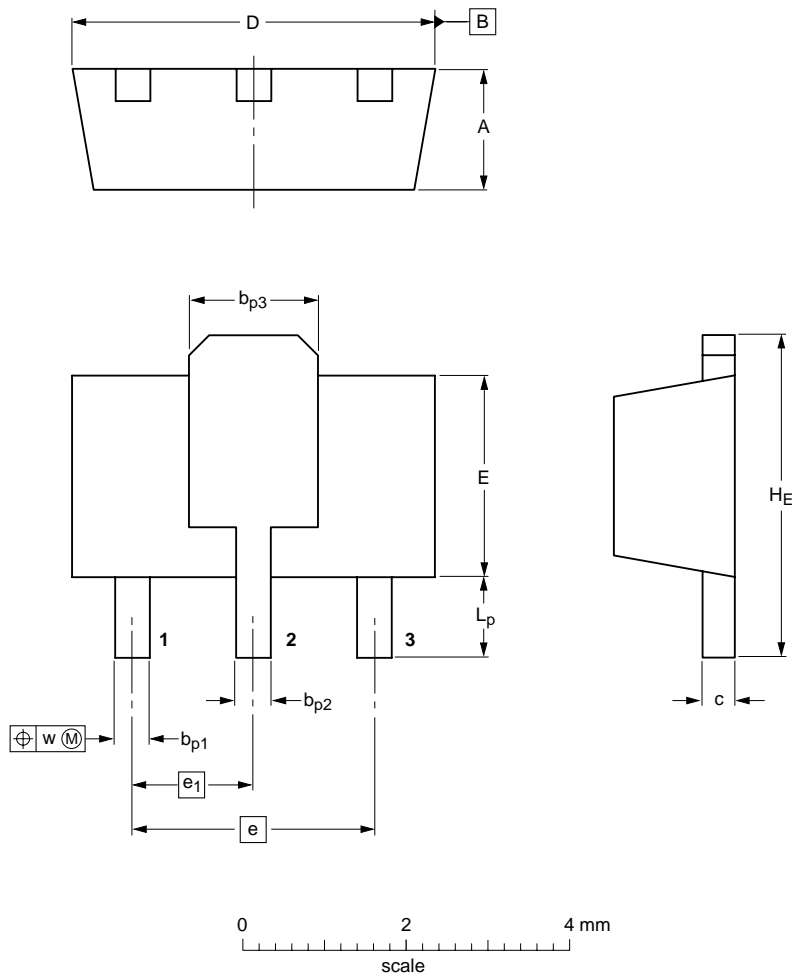
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PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 3 leads

SOT89



DIMENSIONS (mm are the original dimensions)

UNIT	A	b _{p1}	b _{p2}	b _{p3}	c	D	E	e	e ₁	H _E	L _p	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.23	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	1.2 0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT89		TO-243	SC-62			99-09-13 04-08-03

20 V, 5 A NPN low V_{CEsat} (BISS) transistor

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DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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