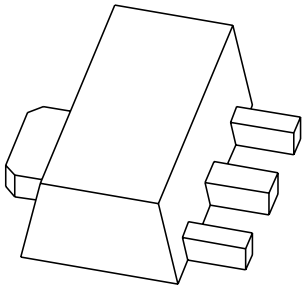
DATA SHEET



PBSS5540X
40 V, 5 A
PNP low V_{CEsat} (BISS) transistor

Product specification
Supersedes data of 2004 Jan 15

2004 Nov 04

Philips
Semiconductors

PHILIPS

40 V, 5 A PNP low V_{CEsat} (BISS) transistor

PBSS5540X

FEATURES

- Low collector-emitter saturation voltage V_{CEsat}
- High collector current capability: I_C and I_{CM}
- High efficiency leading to less heat generation.

APPLICATIONS

- Supply line switching circuits
- Battery management applications
- DC/DC converter applications
- Strobe flash units
- Medium power driver (e.g. relays, buzzers and motors).

DESCRIPTION

PNP low V_{CEsat} transistor in a medium power SOT89 (SC-62) package.

NPN complement: PBSS4540X.

MARKING

TYPE NUMBER	MARKING CODE(1)
PBSS5540X	*1G

Note

1. * = p: Made in Hong Kong.
   * = t: Made in Malaysia.
   * = W: Made in China.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CEO}	collector-emitter voltage	–40	V
I_C	collector current (DC)	–4	A
I_{CRP}	repetitive peak collector current	–5	A
R_{CEsat}	equivalent on-resistance	75	mΩ

PINNING

PIN	DESCRIPTION
1	emitter
2	collector
3	base

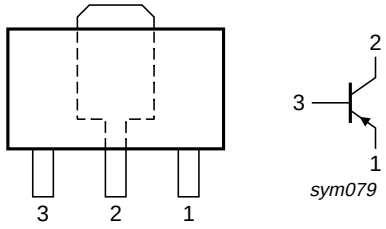


Fig.1 Simplified outline (SOT89) and symbol.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PBSS5540X	SC-62	plastic surface mounted package; collector pad for good heat transfer; 3 leads	SOT89

40 V, 5 A PNP low V_{CEsat} (BISS) transistor

PBSS5540X

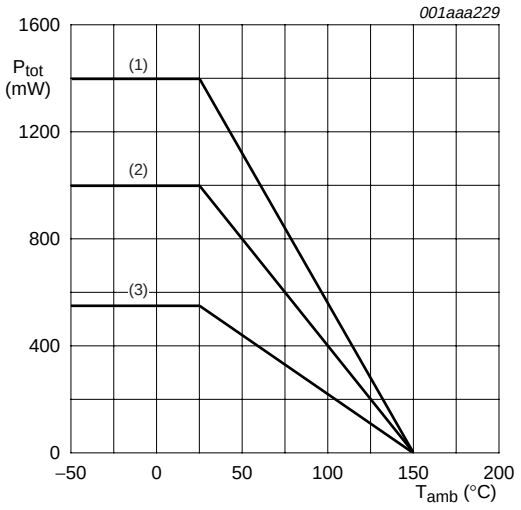
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–40	V
V_{CEO}	collector-emitter voltage	open base	–	–40	V
V_{EBO}	emitter-base voltage	open collector	–	–6	V
I_{CM}	peak collector current	$t_p \leq 1$ ms	–	–10	A
I_{CRP}	repetitive peak collector current	$t_p \leq 10$ ms; $\delta \leq 0.2$	–	–5	A
I_C	collector current (DC)		–	–4	A
I_{BM}	peak base current	$t_p \leq 1$ ms	–	–2	A
I_B	base current (DC)		–	–1	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C			
		$t_p \leq 10$ ms; $\delta \leq 0.2$; note 1	–	2.5	W
		note 1	–	0.55	W
		note 2	–	1	W
		note 3	–	1.4	W
		note 4	–	1.6	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	ambient temperature		–65	+150	°C

Notes

1. Device mounted on a printed-circuit board, single-sided copper, tin-plated and standard footprint.
2. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 1 cm^2.
3. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 6 cm^2.
4. Device mounted on a 7 cm^2 ceramic printed-circuit board, 1 cm^2 single-sided copper and tin-plated.



(1) FR4 PCB; 6 cm^2 mounting pad for collector.
(2) FR4 PCB; 1 cm^2 mounting pad for collector.
(3) FR4 PCB; standard footprint.

Fig.2 Power derating curves.

40 V, 5 A PNP low V_{CEsat} (BISS) transistor

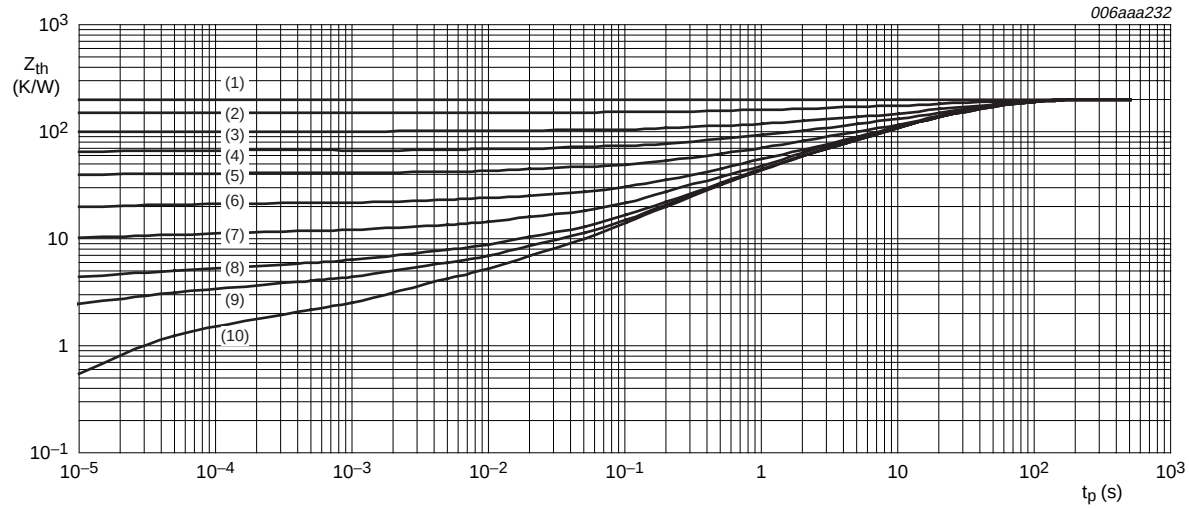
PBSS5540X

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
		notes 1 and 2	50	K/W
		note 2	225	K/W
		note 3	125	K/W
		note 4	90	K/W
		note 5	80	K/W
$R_{th(j-s)}$	thermal resistance from junction to soldering point		16	K/W

Notes

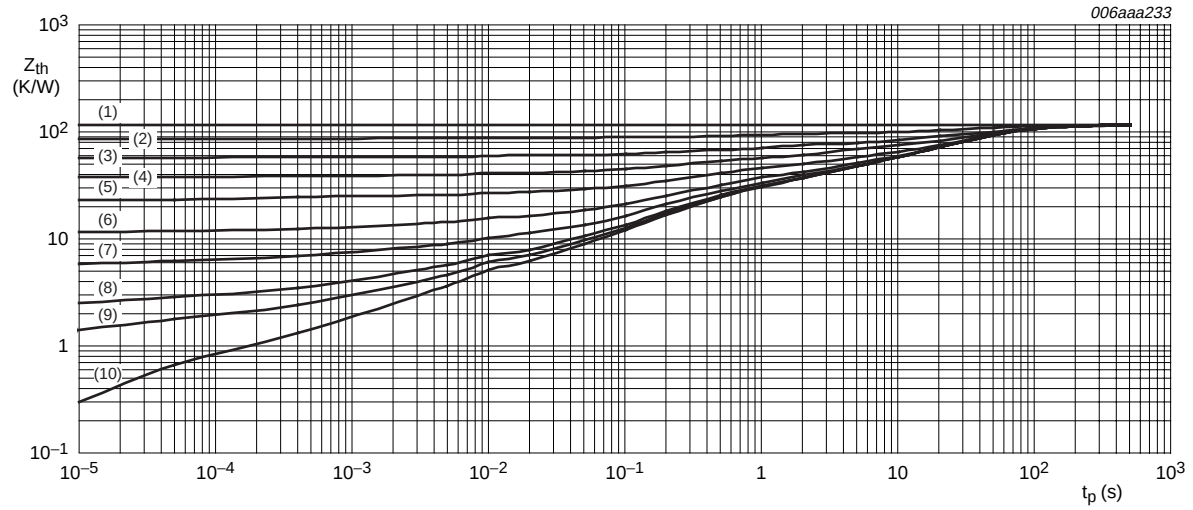
1. Pulse test: $t_p \leq 10$ ms; $\delta \leq 0.2$.
2. Device mounted on a printed-circuit board, single-sided copper, tin-plated and standard footprint.
3. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 1 cm^2.
4. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 6 cm^2.
5. Device mounted on a 7 cm^2 ceramic printed-circuit board, 1 cm^2 single-sided copper and tin-plated.



Mounted on FR4 printed-circuit board; standard footprint.

(1) δ = 1. (3) δ = 0.5. (5) δ = 0.2. (7) δ = 0.05. (9) δ = 0.01.
(2) δ = 0.75. (4) δ = 0.33. (6) δ = 0.1. (8) δ = 0.02. (10) δ = 0.

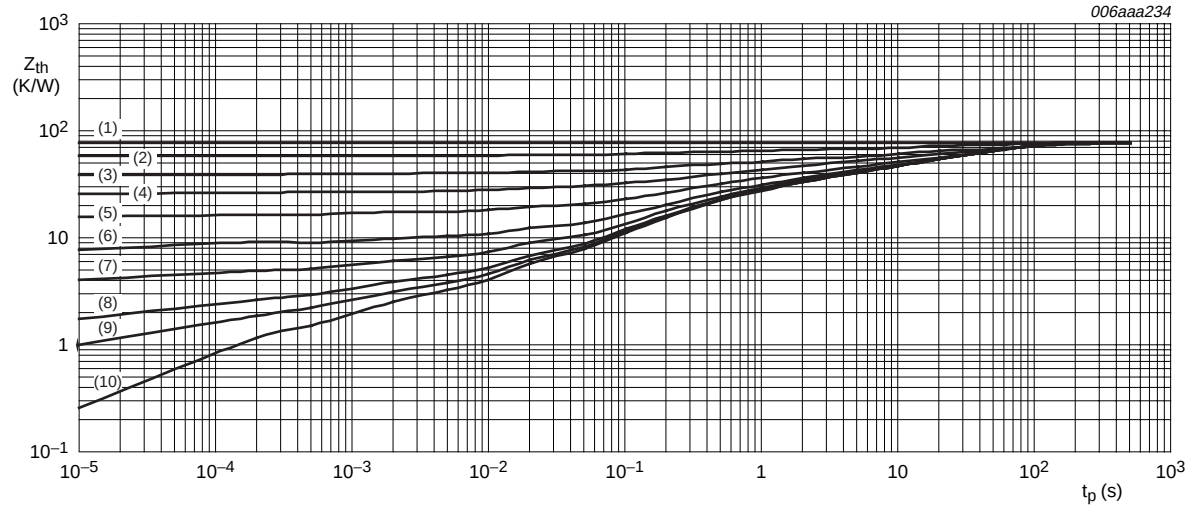
Fig.3 Transient thermal impedance as a function of pulse time; typical values.



Mounted on FR4 printed-circuit board; mounting pad for collector 1 cm^2.

(1) δ = 1. (3) δ = 0.5. (5) δ = 0.2. (7) δ = 0.05. (9) δ = 0.01.
(2) δ = 0.75. (4) δ = 0.33. (6) δ = 0.1. (8) δ = 0.02. (10) δ = 0.

Fig.4 Transient thermal impedance as a function of pulse time; typical values.



Mounted on FR4 printed-circuit board; mounting pad for collector 6 cm^2.

(1) δ = 1. (3) δ = 0.5. (5) δ = 0.2. (7) δ = 0.05. (9) δ = 0.01.
(2) δ = 0.75. (4) δ = 0.33. (6) δ = 0.1. (8) δ = 0.02. (10) δ = 0.

Fig.5 Transient thermal impedance as a function of pulse time; typical values.

40 V, 5 A PNP low V_{CEsat} (BISS) transistor

PBSS5540X

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

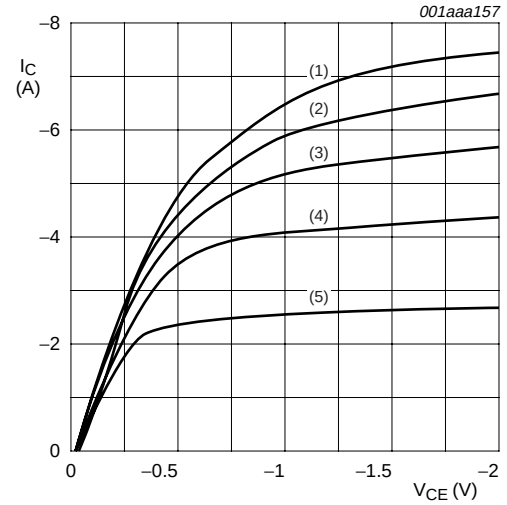
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	V_{CB} = –30 V; I_E = 0 A	–	–	–100	nA
		V_{CB} = –30 V; I_E = 0 A; T_j = 150 °C	–	–	–50	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = –5 V; I_C = 0 A	–	–	–100	nA
h_{FE}	DC current gain	V_{CE} = –2 V; I_C = –0.5 A	250	–	–	
		V_{CE} = –2 V; I_C = –1 A; note 1	200	–	–	
		V_{CE} = –2 V; I_C = –2 A; note 1	150	–	–	
		V_{CE} = –2 V; I_C = –5 A; note 1	50	–	–	
V_{CEsat}	collector-emitter saturation voltage	I_C = –0.5 A; I_B = –5 mA	–	–	120	mV
		I_C = –1 A; I_B = –10 mA	–	–	170	mV
		I_C = –2 A; I_B = –200 mA	–	–	160	mV
		I_C = –4 A; I_B = –200 mA; note 1	–	–	340	mV
		I_C = –5 A; I_B = –500 mA; note 1	–	–	375	mV
R_{CEsat}	equivalent on-resistance	I_C = –5 A; I_B = –500 mA; note 1	–	45	75	mΩ
V_{BEsat}	base-emitter saturation voltage	I_C = –4 A; I_B = –200 mA; note 1	–	–	–1.1	V
		I_C = –5 A; I_B = –500 mA; note 1	–	–	–1.2	V
V_{BEon}	base-emitter turn-on voltage	V_{CE} = –2 V; I_C = –2 A	–	–	–1.0	V
f_T	transition frequency	V_{CE} = –10 V; I_C = –0.1 A; f = 100 MHz	60	–	–	MHz
C_c	collector capacitance	V_{CB} = –10 V; I_E = i_e = 0 A; f = 1 MHz	–	–	105	pF

Note

1. Pulse test: $t_p \leq 300$ µs; $\delta \leq 0.02$.

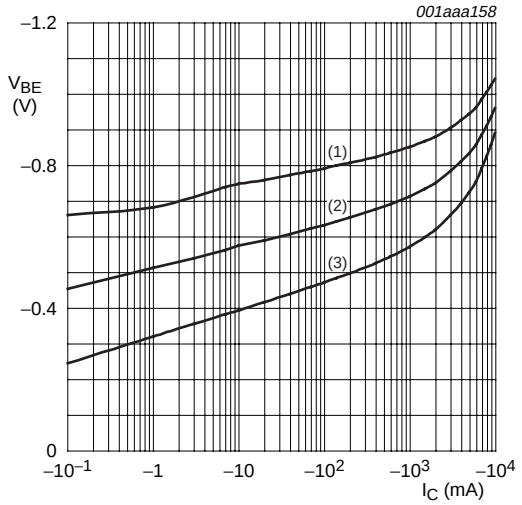
40 V, 5 A
PNP low V_{CEsat} (BISS) transistor

PBSS5540X



(1) I_{B1} = −11 mA.
(2) I_{B2} = −22 mA.
(3) I_{B3} = −33 mA.
(4) I_{B4} = −44 mA.
(5) I_{B5} = −55 mA.

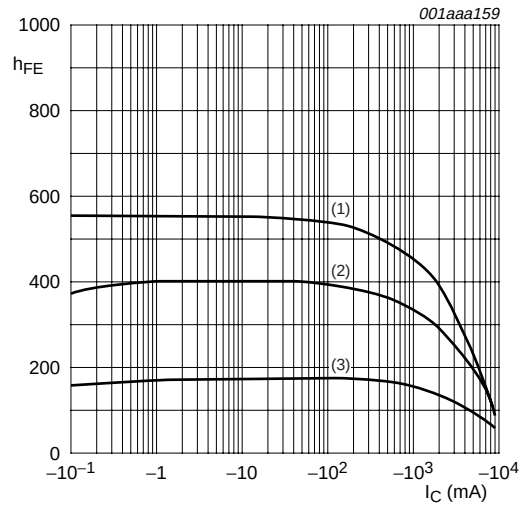
Fig.6 Collector current as a function of collector-emitter voltage; typical values.



V_{CE} = −2 V.

(1) T_{amb} = −55 °C. (2) T_{amb} = 25 °C. (3) T_{amb} = 100 °C.

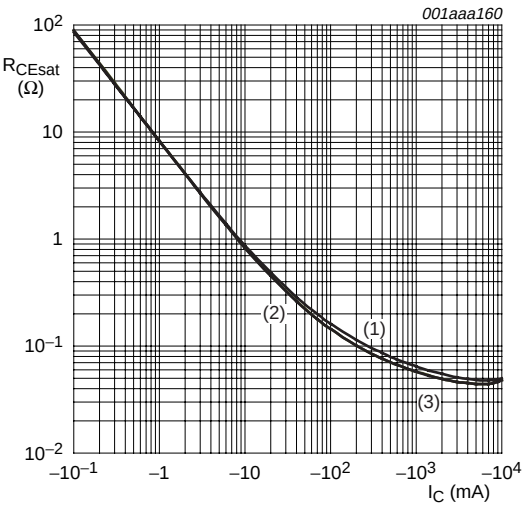
Fig.7 Base-emitter voltage as a function of collector current; typical values.



V_{CE} = −2 V.

(1) T_{amb} = 100 °C. (2) T_{amb} = 25 °C. (3) T_{amb} = −55 °C.

Fig.8 DC current gain as a function of collector current; typical values.



I_C/I_B = 20.

(1) T_{amb} = 100 °C. (2) T_{amb} = 25 °C. (3) T_{amb} = −55 °C.

Fig.9 Equivalent on-resistance as a function of collector current; typical values.

40 V, 5 A
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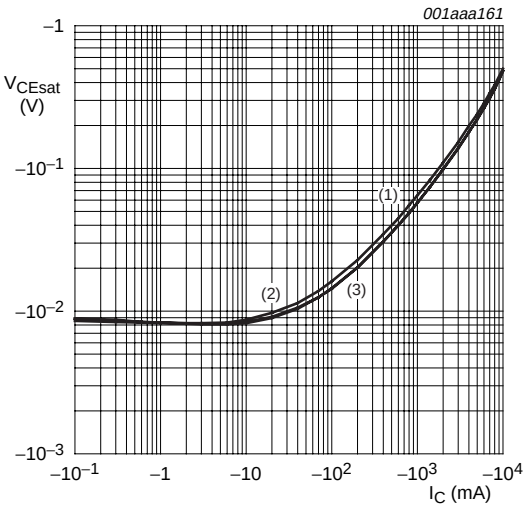
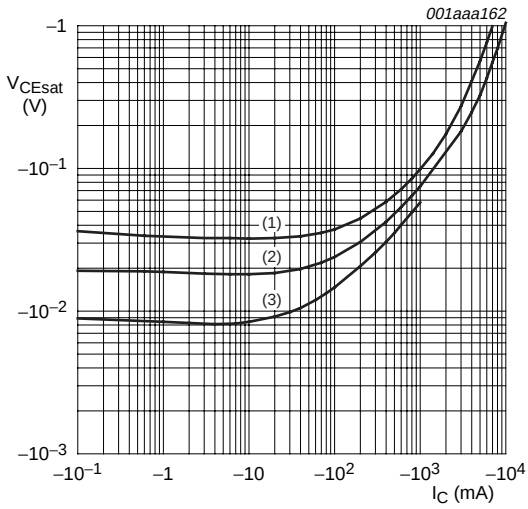
PBSS5540X



I_C/I_B = 20.

(1) T_{amb} = 100 °C. (2) T_{amb} = 25 °C. (3) T_{amb} = −55 °C.

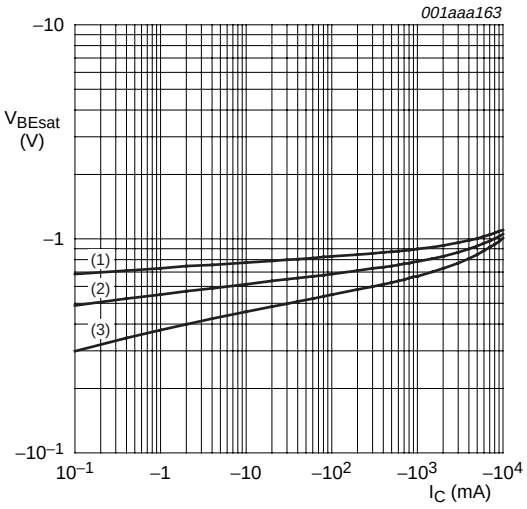
Fig.10 Collector-emitter saturation voltage as a function of collector current; typical values.



T_{amb} = 25 °C.

(1) I_C/I_B = 100. (2) I_C/I_B = 50. (3) I_C/I_B = 10.

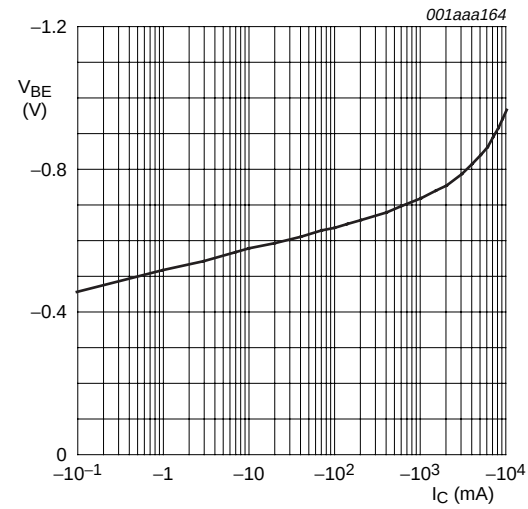
Fig.11 Collector-emitter saturation voltage as a function of collector current; typical values.



I_C/I_B = 20.

(1) T_{amb} = −55 °C. (2) T_{amb} = 25 °C. (3) T_{amb} = 100 °C.

Fig.12 Base-emitter saturation voltage as a function of collector current; typical values.



T_{amb} = 25 °C.

Fig.13 Base-emitter voltage as a function of collector current; typical values.

40 V, 5 A
PNP low V_{CEsat} (BISS) transistor

PBSS5540X

Reference mounting conditions

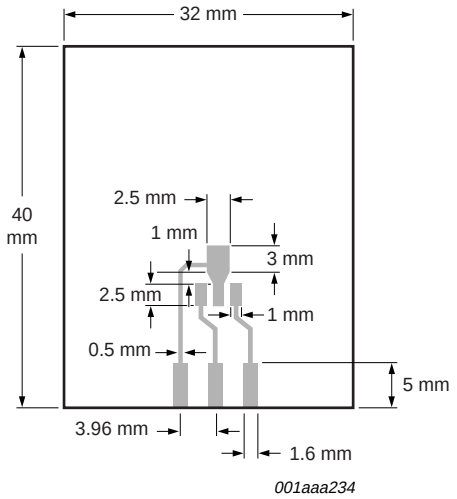


Fig.14 FR4, standard footprint.

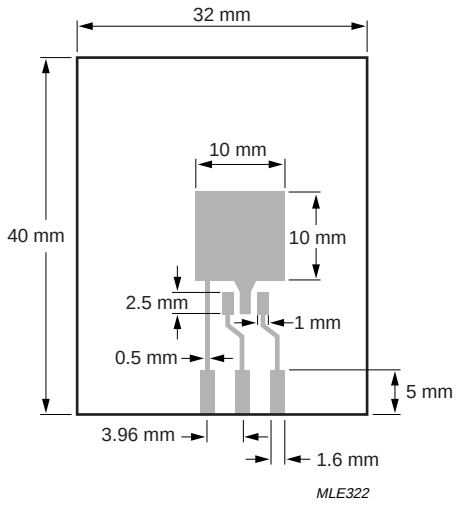


Fig.15 FR4, mounting pad for collector 1 cm^2.

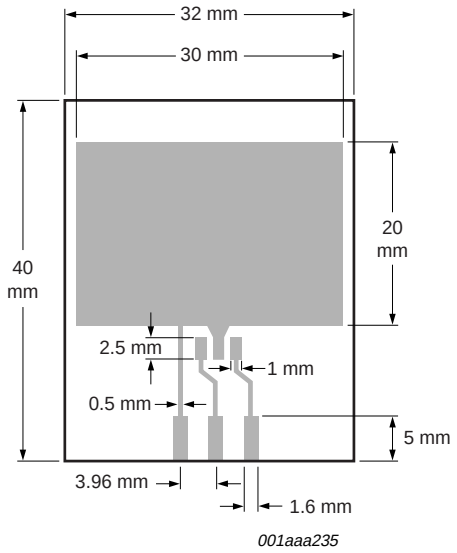
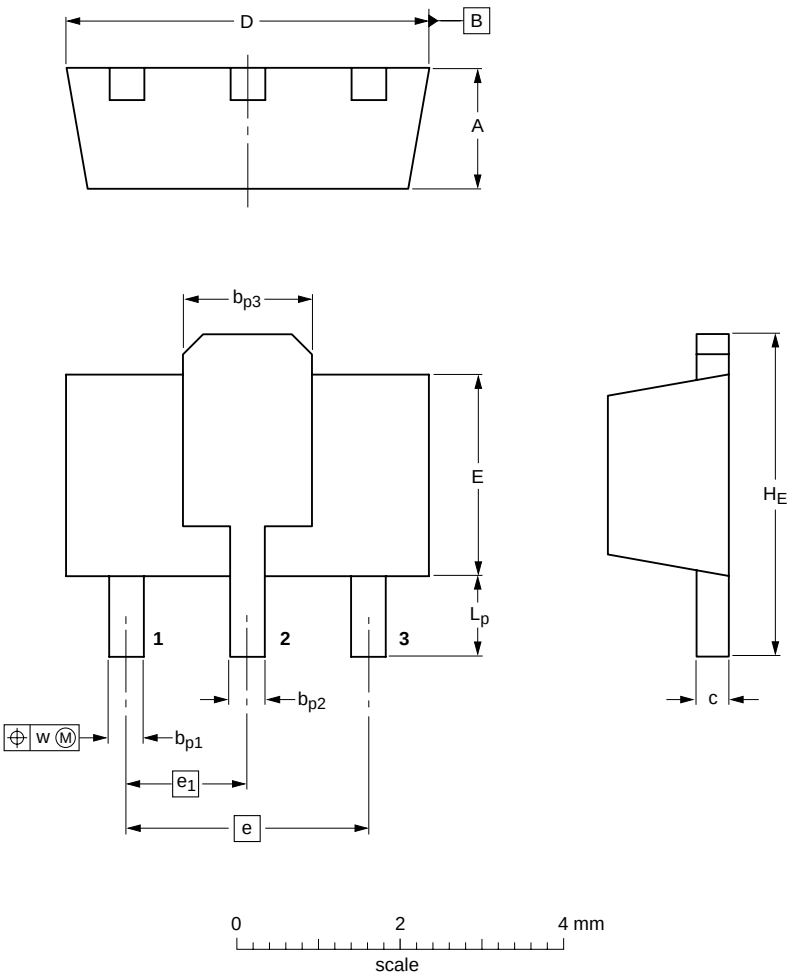


Fig.16 FR4, mounting pad for collector 6 cm^2.

PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 3 leads **SOT89**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_{p1}	b_{p2}	b_{p3}	c	D	E	e	e_1	H_E	L_p	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.23	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	1.2 0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT89		TO-243	SC-62			~~99-09-13~~ 04-08-03

40 V, 5 A PNP low V_{CEsat} (BISS) transistor

PBSS5540X

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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