PIXELPLUS CO., LTD.

Preliminary Customer Data sheet

1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

PC1089K

Rev 1.1

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1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

▶ *Revision History*

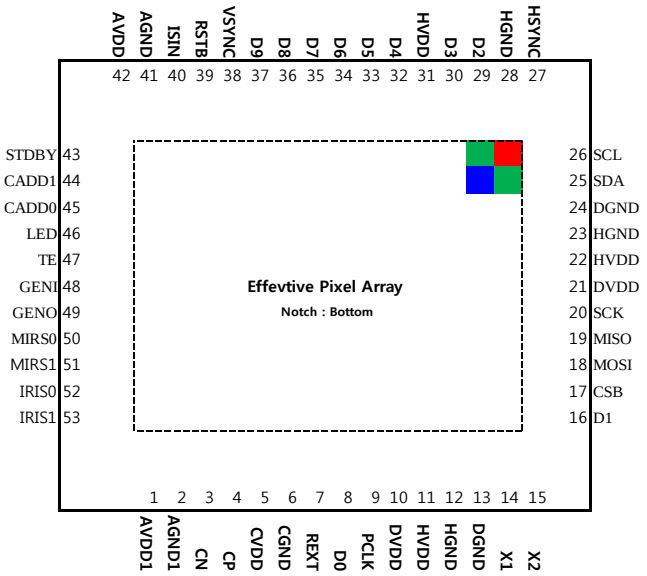
Version	Date [D/M/Y]	Notes	Writer
0.0	21/07/2010	*(Preliminary)*	DS Min
0.1	30/08/2010	Modified PIN description	HS Park
0.2	27/09/2010	Added strapping information	CH Ye
0.3	27/10/2010	Modified table2.Pin description. Added typical parameters on table1	DS Min
0.4	03/11/2010	Added to DC Characteristics Added to AC Characteristics Add Electro Optical Characteristics	SH Han
0.5	05/11/2010	[Table3] edited on page15,16(DO9~0 → D9~0)	BH Moon
0.6	16/11/2010	Added register table and detail information	CH Ye
0.7	29/11/2010	Edited on page 3~144 page	BH Moon
0.8	08/12/2010	Modified Sensitivity and Dark signal	HS Park
0.9	06/01/2011	Modified Operating Temperature (Page 3)	HS Park
1.0	25/03/2011	Modified Device ID page 25,26,32,42	SH Han
1.1	26/07/2011	Changed HVDD Power (page 3~5)	HS Park

Caution : This datasheet can be changed without prior notice !! If you want to get up-to-date version, please contact to localized agent.

1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

▶ Features

- ▷ 762 x 504 total pixel array with RGB bayer color filters and micro-lens.
- ▷ Power supply : AVDD : 2.8V, HVDD : 3.3V, CVDD : 2.8V
- ▷ Output formats :
  - ◆ Composite Output mode :
    - CVBS (NTSC/PAL),
  - ◆ Digital Output mode :
    - max. D1 (720x480) YCbCr422/RGB565/ RGB444. (progressive, 60 fps @ 54MHz)
    - max. D1 (720x480) Bayer (progressive, 60 fps @ 27MHz)
  - ◆ Analog/Digital Output mode :
    - ITU-R. BT656 (720x240/288) (interlaced, 60 fields @ 27MHz)
    - CVBS (30 fps @ 27MHz)
- ▷ Image processing on chip : lens shading, gamma / defect / color correction, low pass filter, color interpolation, saturation, edge enhancement, brightness, contrast, special effects, auto black level , auto white balance, auto exposure control and back light compensation.
- ▷ Frame size, window size and position can be programmed through a 2-wire serial interface bus.
- ▷ VGA / QVGA / QQVGA / CIF / QCIF Scaling.
- ▷ High Image Quality and Ultra low light performance.
- ▷ I2C master include.
- ▷ Motion detection support
- ▷ Alarm mode, Privacy mode support
- ▷ Artificial Intelligence power save mode.
- ▷ Chip Address Selection PADs
- ▷ Horizontal / Vertical mirroring.
- ▷ 50Hz, 60Hz flicker automatic cancellation.
- ▷ Software Reset.
- ▷ External Sync (Gen. Lock) support
- ▷ Off-chip IR-LED control.
- ▷ Crystal input support.
- ▷ On chip regulator for DVDD.
- ▷ CSP/CLCC/PLCC Package type supports



[Fig. 1] PIN Description

Total Pixel Array	762(H) x 504(V)
Effective Pixel Array	728(H) x 488(V)
Pixel Size	6.35 um x 7.4 um
Effective Image Area	4622.8 um x 3611.2 um
Optical Format	1/3 inch
Max. Clock frequency	54 MHz
Max. Frame Rate	- 60fps, 720x480 YCbCr @ 54MHz - 60fps, 720x480 Bayer @ 27MHz - 60field, 720x240(288) YCbCr @ 27MHz - CVBS 30 fps @ 27MHz
Dark Signal	12.0 [mV/sec] @60℃
Sensitivity	13.8 [V/Lux.sec]
Power Supply	Analog : 2.8V, HVDD : 3.3V, CVDD : 2.8V
Power Consumption	281.1 mW @Dynamic 616.6 uW @Standby
Operating Temp. (Fully Functional Temp)	-40 ~ 105 [℃]
Dynamic Range	63.7 [dB]
SNR	46.4 [dB]

[Table 1] Typical Parameters

1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

▶ PIN Descriptions

Num	NAME	I/O Type	PAD Description
1	AVDD1	P	Analog VDD1 :2.8V DC.
2	AGND1	P	Analog Ground1
3	CN	O	Composite Differential Negative signal (75 ohm single termination(LCD), 37.5 ohm double termination (CRT))
4	CP	O	Composite Differential Positive signal. (75 ohm single termination(LCD), 37.5 ohm double termination (CRT))
5	CVDD	P	DAC power supply : 2.8V DC
6	CGND	P	DAC power ground
7	REXT	I	External Resistor. The resistor value can be changed by user tuning. (Typically 30k ohm when CN/CP 37.5 ohm termination, 60k ohm when CN/CP 75 ohm termination)
8	D0	O	Bit 0 of data output
9	PCLK	O	Pixel clock. Data can be latched by external devices at the rising or falling edge of PCLK. The polarity can be controlled anyway.
10	DVDD	P	Digital Power supply : In case of using on-chip digital regulator, DVDD must be tied to DGND by total 1uF bypass capacitor. Otherwise, 1.5V DC must be supplied with 100nF to DGND.
11	HVDD	P	Digital VDD for I/O : 3.3V. Voltage range for all output signals is (0V or HVDD)
12	HGND	P	Digital GND for I/O
13	DGND	P	Digital GND for core
14	X1	I	Crystal input pad or **Master clock input pad**
15	X2	O	Crystal output pad *(1)
16	D1	O	Bit 1 of data output
17	CSB	O	Chip Select Signal for Serial Peripheral Interface(SPI)
18	MOSI	O	Data Output for Serial Peripheral Interface(SPI)
19	MISO	I	Data Input Signal for Serial Peripheral Interface(SPI)
20	SCK	O	Clock Signal for Serial Peripheral Interface(SPI)

(1) In case of using External clock, crystal output pad(X2) must be floated and clock input PAD is X1.

[Table 2] Pin Descriptions (continue)

21	DVDD	P	Digital Power supply : In case of using on-chip digital regulator, DVDD must be tied to DGND by total 1uF bypass capacitor. Otherwise, 1.5V DC must be supplied with 100nF to DGND.
22	HVDD	P	Digital VDD for I/O : 3.3V. Voltage range for all output signals is (0V~HVDD)
33	HGND	P	Digital GND for I/O
24	DGND	P	Digital GND for core
25	SDA	I/O	2-wire serial interface data.
26	SCL	I/O	2-wire serial interface clock.
27	HSYNC	O	Horizontal synchronization pulse. HSYNC is high (or low) for the horizontal window of interest. It can be programmed to appear or not outside the vertical window of interest.
28	HGND	P	Digital GND for I/O
29	D2	O	Bit 2 of data output
30	D3	O	Bit 3 of data output
31	HVDD	P	Digital vdd: 3.3V for I/O. Voltage range for all output signals is (0V~HVDD)
32	D4	O	Bit 4 of data output
33	D5	O	Bit 5 of data output
34	D6	O	Bit 6 of data output
35	D7	O	Bit 7 of data output
36	D8	O	Bit 8 of data output
37	D9	O	Bit 9 of data output
38	VSYNC	O	Vertical sync : Indicates the start of a new frame
39	RSTB	I	System reset must remain low for at least 8 master clocks after power is stabilized. When the sensor is reset, all registers are set to their default values.
40	ISIN	I	Illumination sensor input (must be under 1.0V).
41	AGND	P	Analog Ground
42	AVDD	P	Analog VDD : 2.8V DC
43	STDBY	I	Power stdby mode. When Stdby ='1', there's no current flow in any analog circuit branch, neither any beat of digital clock.
44	CADD1	I	Chip Address selection bits [1:0], Default [11]
45	CADD0	I	
46	LED	O	LED provides the enable signal which can turn-on LED device when low light condition
47	TE	I	Chip Test mode enable.
48	GENI	I	External Frame sync input. Slave chip can receive the external frame sync signal from master chip
49	GENO	O	External Frame sync output. Master chip can output the external frame sync signal through this pad to synchronize all digital outputs of two or more chips
50	MIRS0	O	Moving IR/AR transition Switch control PADs
51	MIRS1	O	
52	IRIS0	O	IRIS control PADs
53	IRIS1	O	

[Table 2] Pin Descriptions

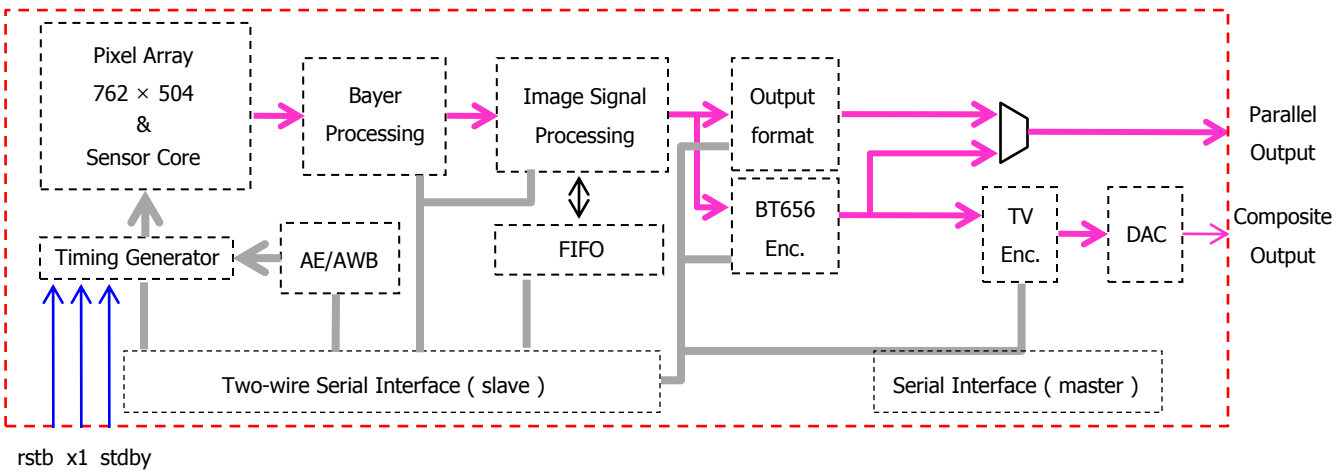
1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

▶ *Signal Environment*

PC1089K has 2.8V tolerant Input pads. Input signals must be higher than or equal to HVDD but cannot be higher than 2.8V. PC1089K input pad has built in reverse current protection circuit, which makes it possible to apply input voltage even if the HVDD is disconnected or floating. Voltage range for all output signals is 0V ~ HVDD.

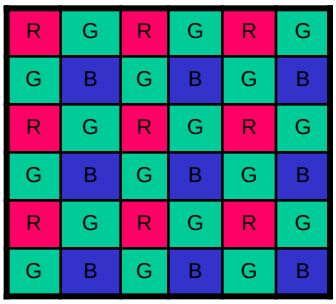
▶ *Chip Architecture*

PC1089K has 762 x 504 total pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing blocks to finally produce YCbCr 4:2:2 output data. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through 2-wire serial interface.



[Fig. 2] Block Diagram

▶ Data Formats



[Fig. 4] Bayer Color filter pattern

Pixel array is covered by Bayer color filters as can be seen in the [Fig. 4]. Since each pixel can have only one type of filter on it, only one color component can be produced by a pixel. PC1089K provides this Bayer pattern RGB data through an 10bit channel. It takes one PCLK to pass one pixel RGB data to output bus. But since it is necessary to know all 3 color components R, G, B to produce a color for a pixel, the other two components must be inferred from other pixel data. For example, G component for a B pixel is calculated as an average of its four nearest G neighbors, and its R component as an average of its four nearest R neighbors. This operation of inferring missing data from existing ones is called the color interpolation. Color interpolation produces an undesirable artifact in image. Sampling nature of color filter can leave an interference pattern around an area with repetitive fine lines. PC1089K adopts a low pass filter to prevent the interference patterns (called Moire pattern) from degrading the image quality too much. After color interpolation, every pixel has all three color components. These three color components R, G, B can be routed to 10 bits output pins in such a way RGB565. It takes two PCLK's to pass one pixel RGB data to output bus.

It is possible to extract monochrome luminance data from RGB color components and the conversion equation is : Y = 0.299R + 0.587G + 0.114B where R,G and B are gamma corrected color components. And the color information is separated from luminance information according to following equations.

$$U = 0.492 (B – Y), \quad V = 0.877 (R – Y)$$

Since human eyes are less sensitive to color variation than to luminance, color components can be sub-sampled to reduce the amount of data to be transmitted, but preserving almost the same image quality.

U1	Y1	V1	Y2	U3	Y3	V3	Y4	…

[Fig. 5] 4:2:2 YUV data sequence.

[Fig. 5] shows 4:2:2 YUV data sequence. PC1089K supports 4:2:2 YUV data format where U and V components are horizontally sub-sampled such that U and V for every other pixel are omitted. PC1089K also supports ITU-R BT.601 YC_BC_R format which is a scaled, offset version of YUV. Y is the same in both formats but the C_BC_R is formed as follows.

$$C_B = 0.564 (B – Y) + 128$$
$$C_R = 0.713 (R – Y) + 128$$

▶ Data and Synchronization Timing

1) VGA (640x480) or D1 (720x480)

[Fig. 6] shows the default data sequence of PC1089K. In [Fig. 6] VSYNC/HSYNC/PCLK polarity can have any combinations possible. Data can be latched at the rising or falling edge of PCLK. HSYNC can be set to be active high or active low. The sequence default YUV data is [U,Y, V, Y, …] for common even / odd rows.

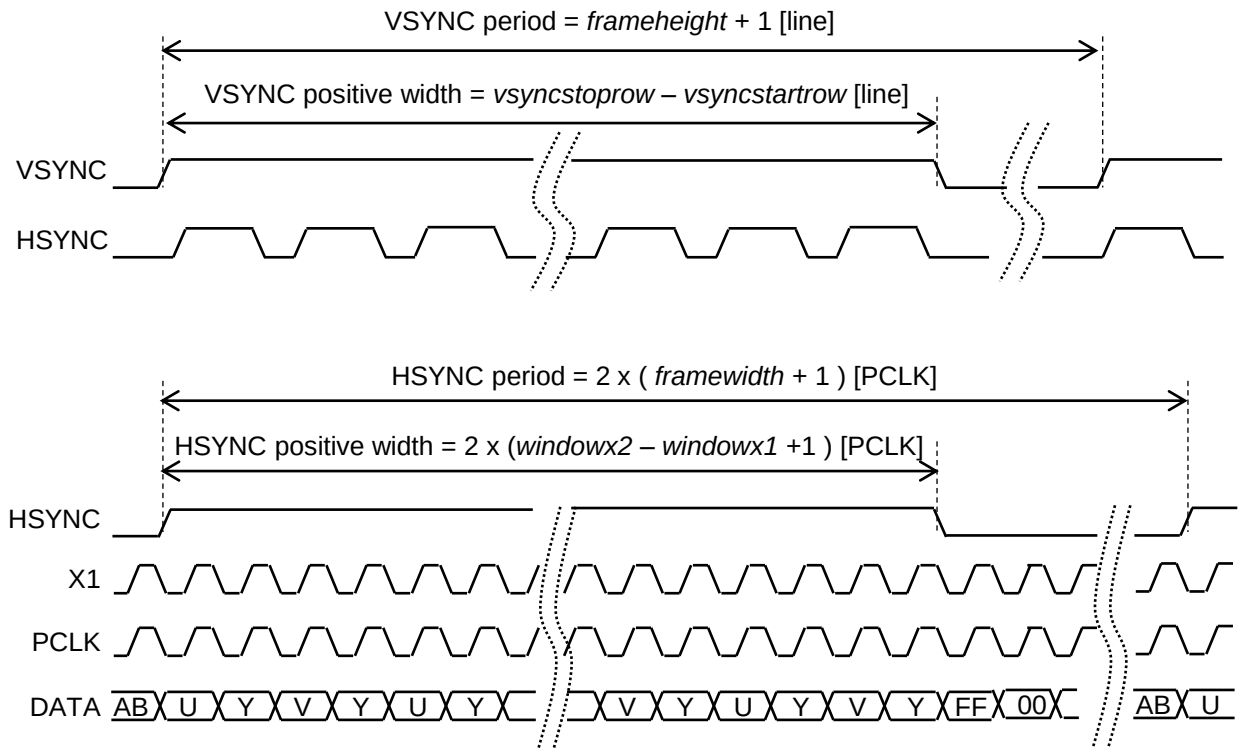
The positive width of VSYNC can be programmed by *vsyncstartrow* and *vsyncstoprow* (register value) and given by

VSYNC positive width = *vsyncstartrow* – *vsyncstoprow* [line]

The positive width of HSYNC can be programmed by *windowx1 / x2(Register Value)* and given by

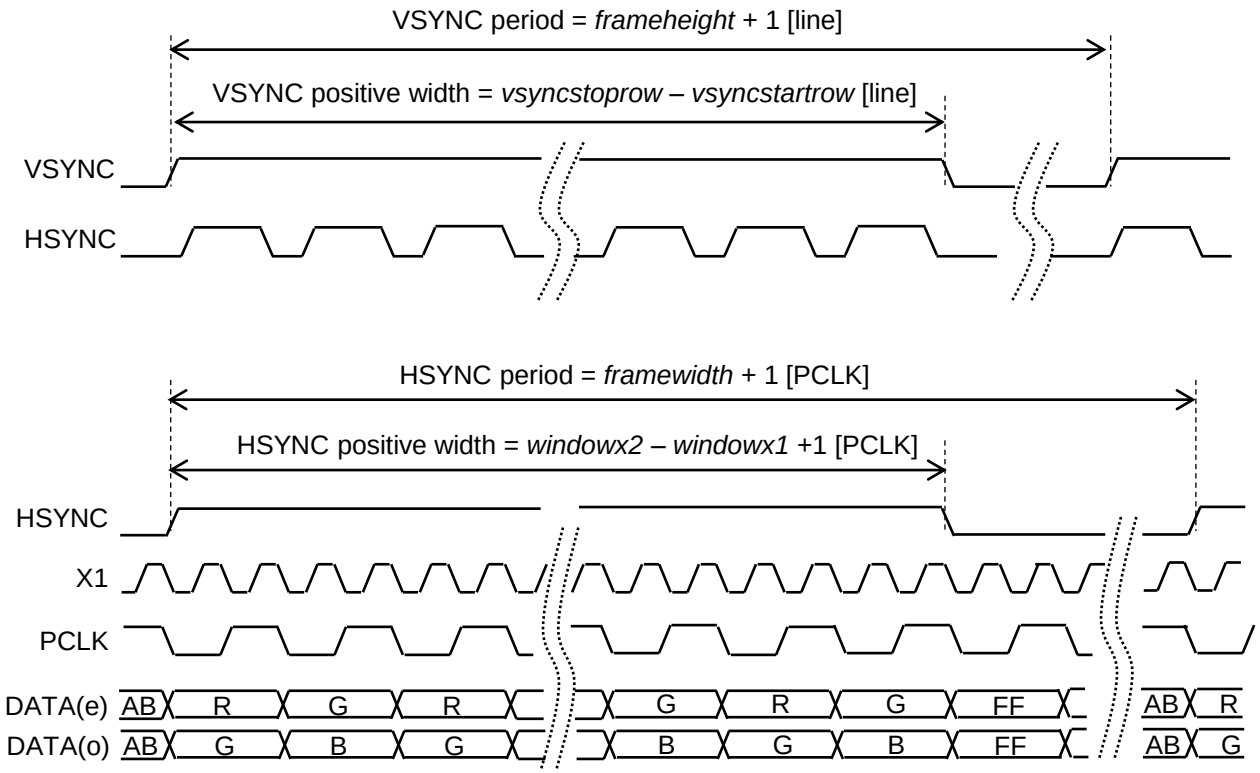
HSYNC positive width = 2 x (*windowx2* - *windowx1* + *1)* [PCLK]

Data sequence of YUV format can change to [U, Y, V, Y], [V, Y, U, Y], [Y, U, Y, V] and [Y, V, Y, U] by *format* (register value). Data value can be selected in Invalid or blanking region.



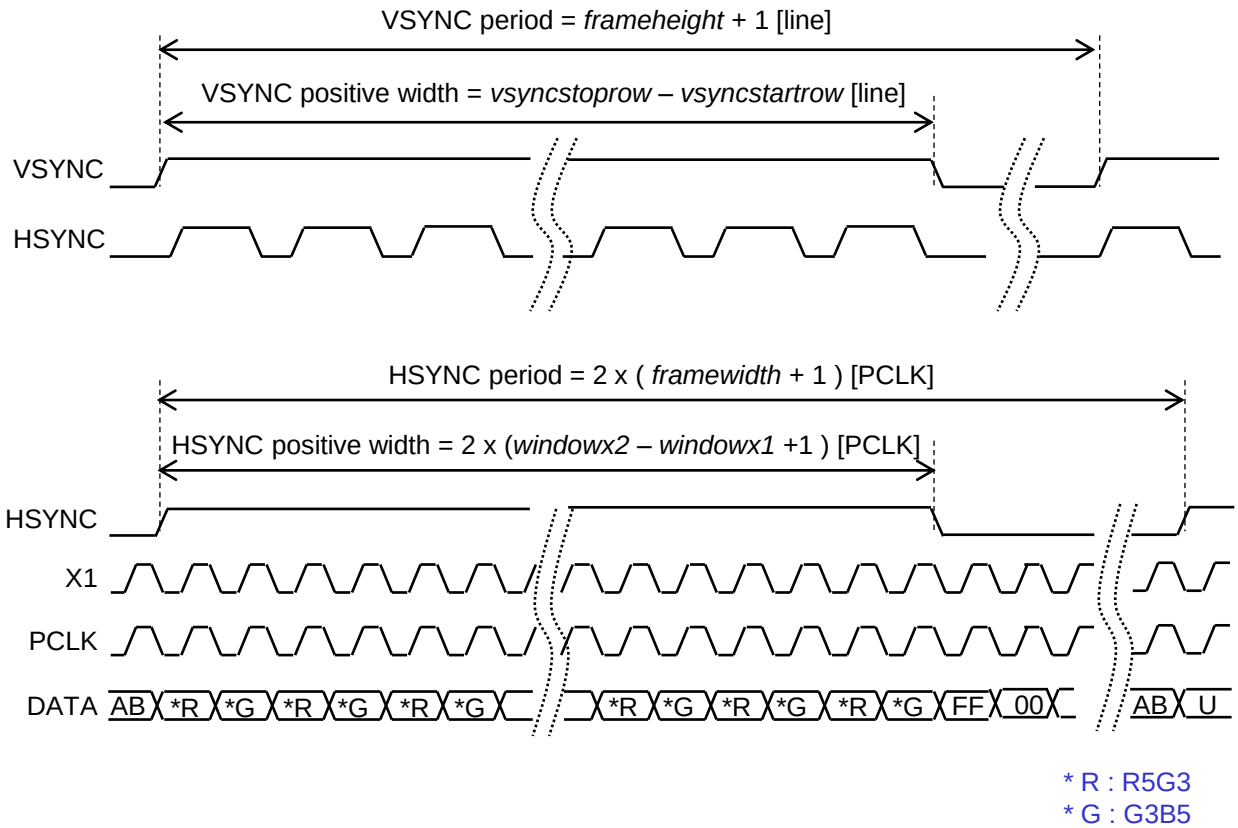
[Fig. 6] Timing diagram for VSYNC, HSYNC, X1, PCLK and Data (YUV mode : default)

[Fig. 7] shows the bayer data sequence of PC1089K. The default sequence Bayer data is [RGRG…] for even rows and [GBGB…] for odd rows.



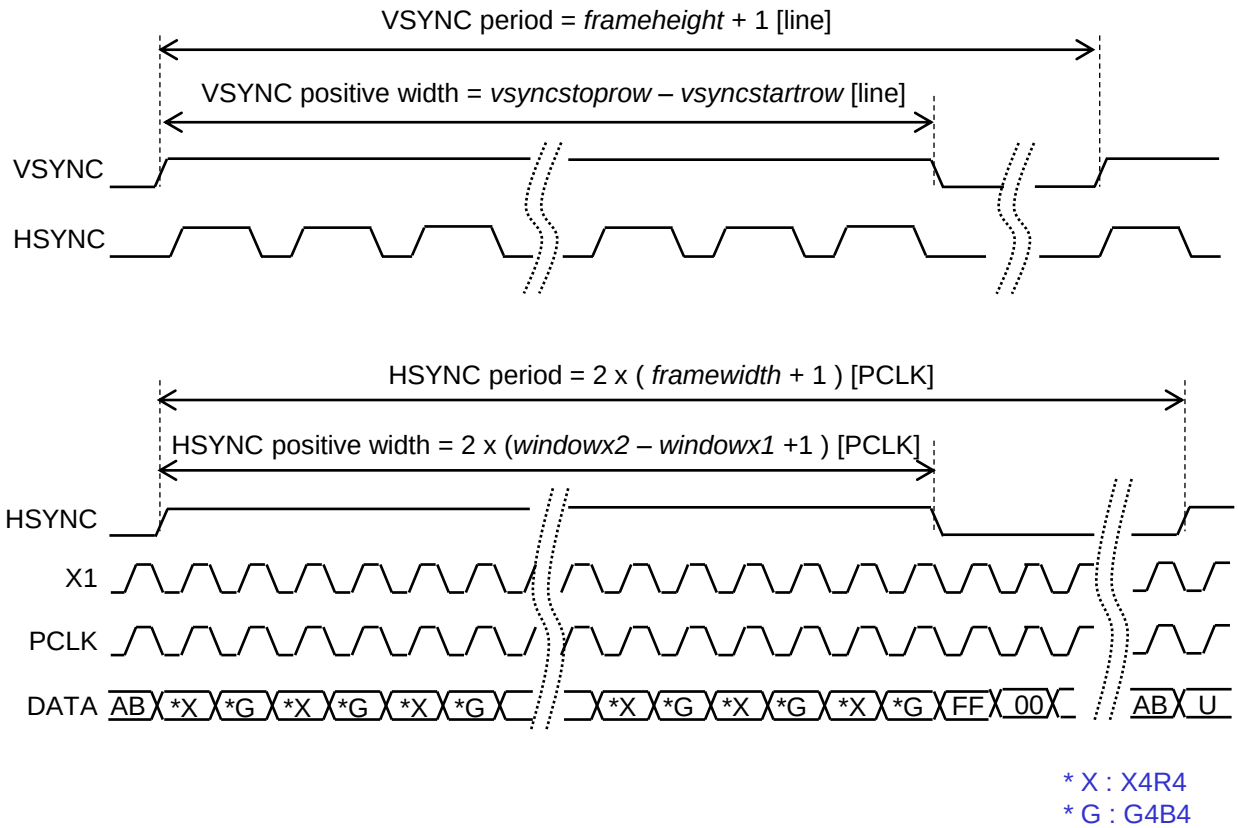
[Fig. 7] Timing diagram for VSYNC, HSYNC, X1, PCLK and Data (Bayer mode)

[Fig. 8] shows the RGB565 data sequence of PC1089K. The RGB565 data sequence can change to [R5G3, G3R5], [G3R5, R5G3], [B5G3, G3R5] and [G3R5, B5G3] by *format* (register value).



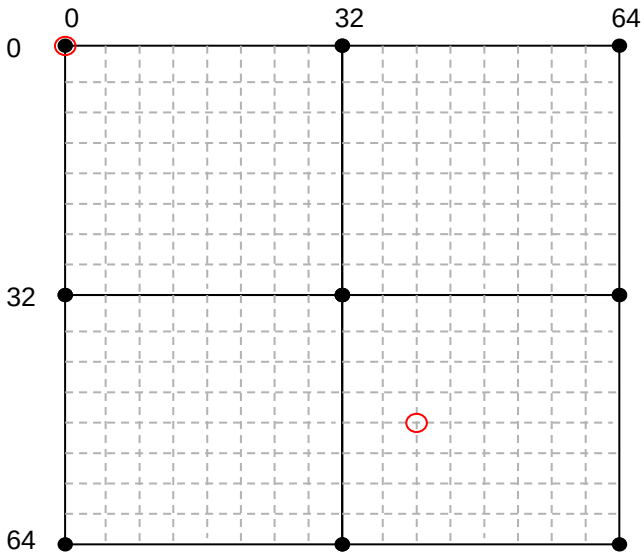
[Fig. 8] Timing diagram for VSYNC, HSYNC, X1, PCLK and Data (RGB565 mode)

[Fig. 9] shows the RGB444 data sequence of PC1089K. The RGB444 data sequence can change to [x4R4, G4B4] and [G4B4, X4R4] by *format* (register value).



[Fig. 9] Timing diagram for VSYNC, HSYNC, X1, PCLK and Data (RGB444 mode)

▶ Scaling



[Fig. 12] Free Scaling

● Full image pixel locations

X points = 32 * M

Y points = 32 * N

○ Scaled image sampling points

X Sampling points = reg_scale_x * P

Y Sampling points = reg_scale_y * Q

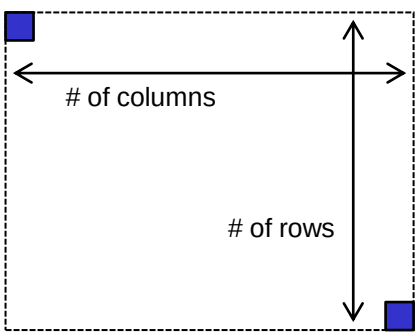
← Example

reg_scale_x = 40

reg_scale_y = 48

(reg_window_x1, reg_window_y1)

minimum = (1, 1)



[Fig. 13] Output Image Size

(reg_window_x2, reg_window_y2)

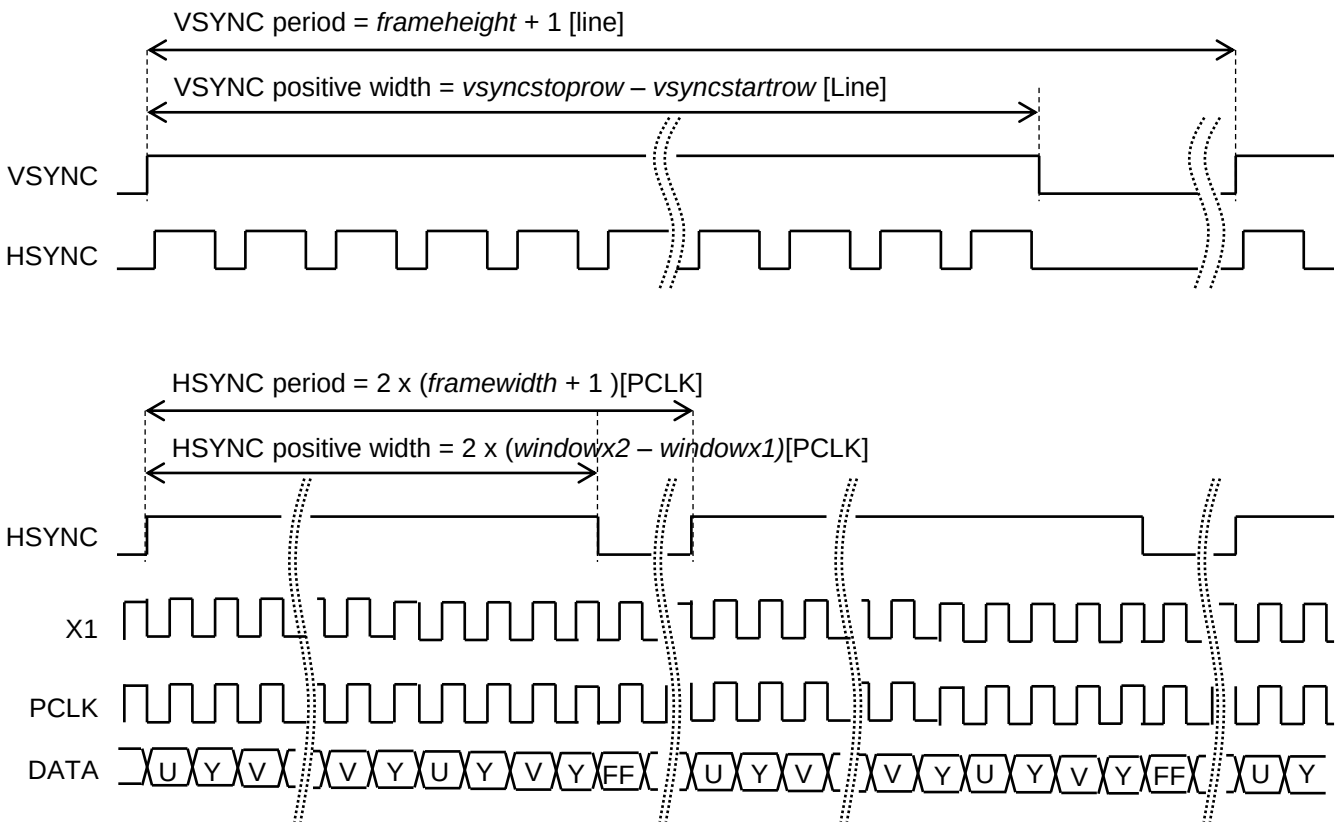
maximum = (720, 480)

Where,

Number of columns = reg_window_x2 - reg_window_x1 + 1

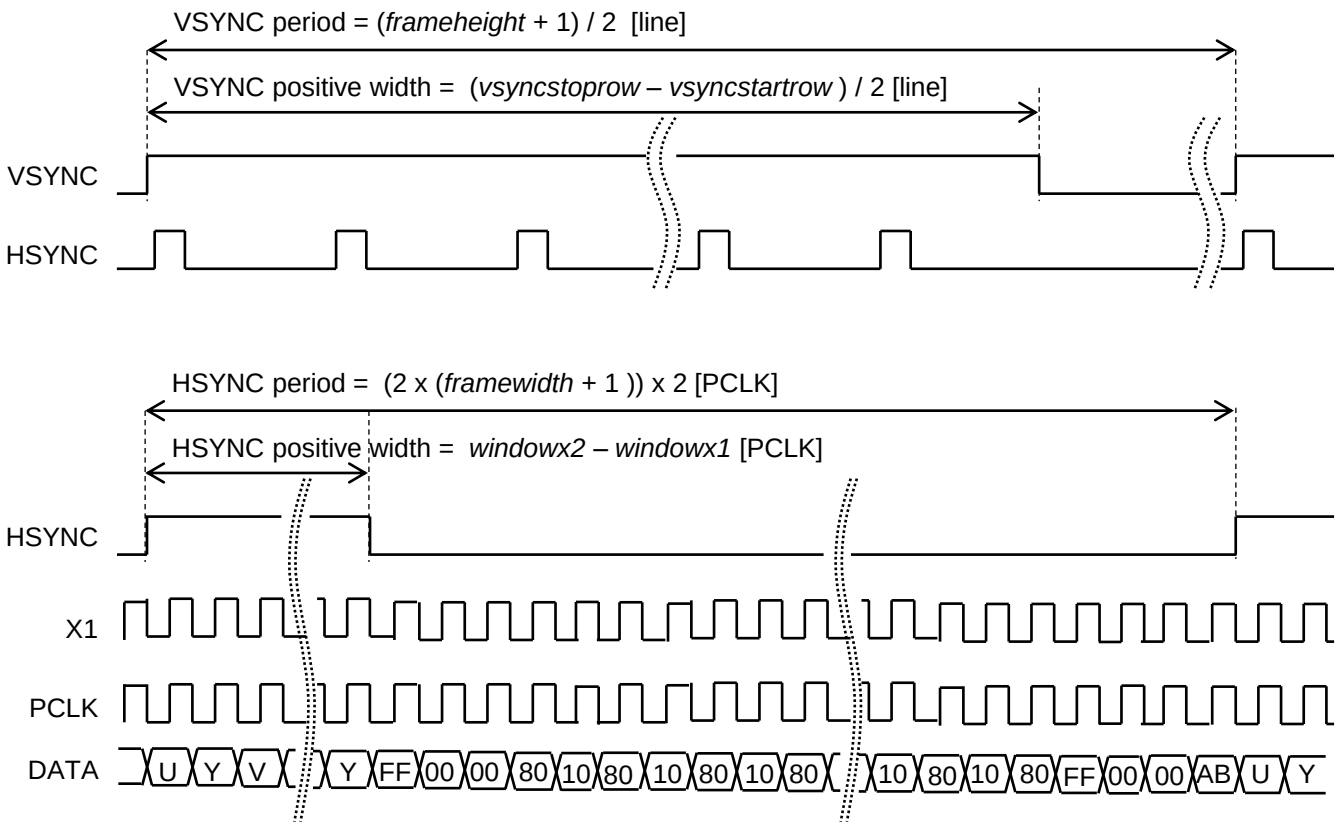
Number of rows = reg_window_y2 - reg_window_y2 + 1

(1) X Full Sampling Mode / Y Full Sampling Mode



[Fig. 14] Timing Diagram for Full Mode

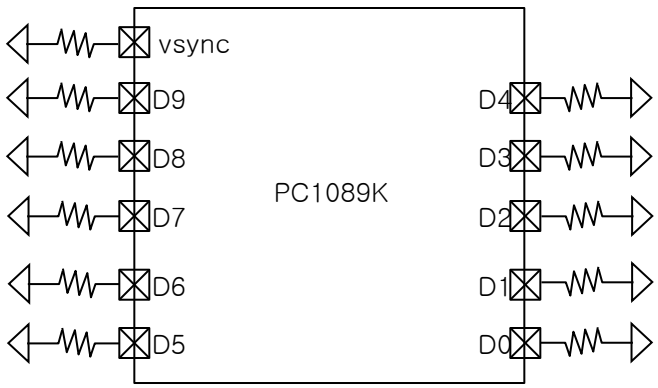
(2) X 1/2 Scale Mode / Y 1/2 Scale Mode



[Fig. 15] Timing Diagram for XY-Scaling Mode

▶ Wire-strapping

Wire-strapping is a function of chip mode selection. Chip mode is automatically selected according to D9~D0 pads wired with pull-up or pull-down. [Fig.16] shows one example of Wire-strapping configuration and [Table 3] shows chip mode selection by wire-strapping.



[Fig.16] Example of wire-strapping

		vsync	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TV_MODE	(M)NTSC	-	-	-	-	-	-	L	L	L	-	-
	NTSC-J	-	-	-	-	-	-	L	L	H	-	-
	(M)PAL	-	-	-	-	-	-	L	H	L	-	-
	(Nc)PAL	-	-	-	-	-	-	L	H	H	-	-
	(N)PAL	-	-	-	-	-	-	H	L	L	-	-
	(B,D,G,H,I)PAL	-	-	-	-	-	-	H	L	H	-	-
FLICKER	No Flicker cancel	-	-	-	-	L	L	-	-	-	-	-
	Manual-A	-	-	-	-	L	H	-	-	-	-	-
	Manual-B	-	-	-	-	H	L	-	-	-	-	-
MIRROR	NO MIRROR	-									H	L
	MIRROR-V	-	-	-	-	-	-	-	-	-	L	L
	MIRROR-H	-	-	-	-	-	-	-	-	-	H	H
	MIRROR-VH	-	-	-	-	-	-	-	-	-	L	H
BLC	ON	-	-	-	L	-	-	-	-	-	-	-
	OFF	-	-	-	H	-	-	-	-	-	-	-
Indoor/ Outdoor	Indoor mode	-	-	H	-	-	-	-	-	-	-	-
	Outdoor mode	-	-	L	-	-	-	-	-	-	-	-

[Table 3] Wire-strapping (continue)

▶ *Wire-strapping*

		vsync	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OSD	Enable	-	H	-	-	-	-	-	-	-	-	-
	Disable	-	L	-	-	-	-	-	-	-	-	-
MASTER MODE	ON	H	-	-	-	-	-	-	-	-	-	-
	OFF	L	-	-	-	-	-	-	-	-	-	-

[Table 3] Wire-strapping

[Table 4] shows TV_mode wire-strapping registers. These registers are changed by D4~D2.

	"000b"	"001b"	"010b"	"011b"	"100b"	"101b"
Register name	(M)NTSC	NTSC-J	(M)PAL	(Nc)PAL	(N)PAL	(OTHER)PALs
chip_mode	00	00	00	01	01	01
framewidth	0359	0359	0359	040D	040D	040D
frameheight	020C	020C	020C	0207	0207	0207
windowy2	00F0	00F0	00F0	0120	0120	0120
scale_y	40	40	40	35	35	35
fd_a_step	03E8	03E8	03E8	04BD	04BD	04BD
fd_b_step	0340	0340	0340	03F0	03F0	03F0
fd_period_a	01068B	01068B	01068B	00D8F8	00D8F8	00D8F8
fd_period_b	013B0D	013B0D	013B0D	01045D	01045D	01045D
fd_period_c	0627	0627	0627	0515	0515	0515
fd_fheight_a	020C	020C	020C	0207	0207	0207
fd_fheight_b	020C	020C	020C	0207	0207	0207
enc_scfreq	00	00	03	02	01	01
enc_blank	F0	F0	F0	FC	F0	FC
enc_pedestal	2A	00	2A	00	2A	00
enc_burst	70	70	75	75	75	75
enc_Ygain	82	8D	82	89	82	89
enc_Ugain	6F	78	6F	75	6F	75
enc_Vgain	9C	A9	9C	A6	9C	A6
enc_Crange_L	48	62	48	5B	48	5B
enc_chroma_max_L	CD	DF	CD	D7	CD	D7
enc_chroma_min_L	6D	35	6D	45	6D	45
expfrmH	0207	0207	0207	0202	0202	0202
midfrmheight	0207	0207	0207	0202	0202	0202
maxfrmheight	0207	0207	0207	0202	0202	0202
ae_win_fy2	00F0	00F0	00F0	0120	0120	0120
ae_win_cy1	0000	0000	0000	0000	0000	0000
ae_win_cy2	0000	0000	0000	0000	0000	0000
ae_yaxis	0079	0079	0079	0091	0091	0091
awb_win_fy2	00F0	00F0	00F0	0120	0120	0120
awb_win_cy1	0051	0051	0051	0061	0061	0061
awb_win_cy2	00A0	00A0	00A0	00C0	00C0	00C0

[Table 4] TV_mode registers

[Table 5~8] show registers and setting values related with Flicker mode, Mirror mode, BLC mode and Indoor/Outdoor mode.

	"00b"	"01b"	"10b"
Register name	Normal(off)	manual A	manual B
flicker_control_1	00	08	04

[Table 5] Flicker mode register

	"00b"	"01b"	"10b"	"11b"
Register name	V mirror	HV mirror	No mirror	H mirror
mirror	02	03	00	01

[Table 6] Mirror mode register

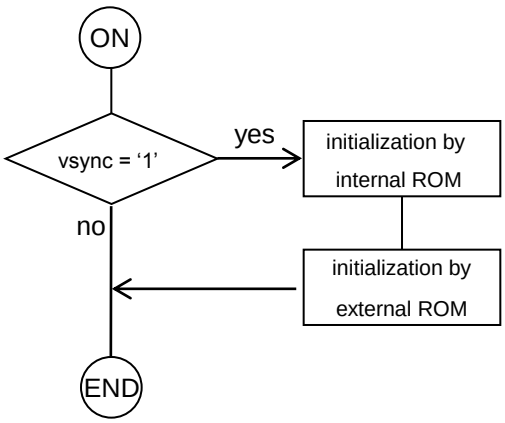
	"0b"	“1b"
Register name	BLC off	BLC on
ae_weight1	08	08
ae_weight2	08	08
ae_weight3	08	08
ae_weight4	08	08
ae_weightc	38	08
max_yt1	B0	B0
max_yt2	80	80
min_yt1	84	84
min_yt2	50	50

[Table 7] BLC mode register

	"0b"	“1b"
Register name	Outdoor	Indoor
awb_rgain_min1	40	2B
awb_rgain_min2	40	2B
awb_rgain_max1	50	6D
awb_rgain_max2	50	6D
awb_bgain_min1	60	57
awb_bgain_min2	60	57
awb_bgain_max1	A2	B2
awb_bgain_max2	A2	B2

[Table 8] Indoor/Outdoor mode register

[Table 9] show registers and setting values related with master mode.



[Fig. 17] shows initialization process of registers. When vsync is high, register default values are initialized by internal ROM and external ROM.

▶ If you want to see more processes, see [Fig. 20].

[Fig. 17] Initialization process of registers

	vsync = 0b	vsync = 1b
Registers	master mode off	master mode on
analog_control_4	42	4F
lens_gaing1	00	02
lens_gaing2	00	02
edge_gain	38	14
ec_pgain	30	80
ec_mgain	38	80
ccr_m11	33	2B
ccr_m12	8B	8A
ccr_m13	88	81
ccr_m21	86	8A
ccr_m22	31	32
ccr_m23	8A	88
ccr_m32	8F	9C
ccr_m33	32	3F
y_weight	40	00
awb_cwx1_l	F1	00
awb_cwx2_h	01	00
awb_cwx2_l	E0	00
awb_control_1	95	AD
minexp_l	0C	80

	vsync = 0b	vsync = 1b
Registers	master mode off	master mode on
midexp_h	85	81
midexp_m	40	80
maxexp_t	01	03
maxexp_h	85	03
maxexp_m	40	00
max_yt1	A0	B0
min_yt1	80	84
awb_p1Ax	29	00
awb_p1Ay	39	FF
awb_p2Ax	36	FF
awb_p2Ay	19	00
awb_osAx	09	FF
awb_osAy	10	FF
awb_slopeA	A0	00
awb_p1Bx	36	00
awb_p1By	21	FF
awb_p2Bx	69	FF
awb_p2By	14	00
awb_osBx	0C	FF
awb_osBy	04	FF

[Table 9] Internal ROM registers setting (continue)

	vsync = 0b	vsync = 1b
Registers	master mode off	master mode on
awb_slopeB	10	00
awb_maxc	FA	E0
awb_minc	08	0A
awb_weight_c	05	00
awb_weight_p	0B	01
rg_ratio_a	7A	80
bg_ratio_a	78	80
ratio_axis_a	2A	3A
ratio_axis_b	50	54
ratio_axis_c	57	59
lens_gainr_a	02	06
axis_a	2A	3A
axis_b	50	54
axis_c	57	59
user_cs	20	1C
dark_blf0	5F	7F
dark_blf1	3F	7F
dark_blf2	3F	7F
dark_nf0	40	00
dark_nf1	40	00
dark_nf2	40	00
dark_nf	01	00
dark_intp0	00	04
dark_intp1	08	04
dark_intp2	18	04
dark_intp	00	04
dark_hr_th0	04	00
dark_hr_th1	08	00

	vsync = 0b	vsync = 1b
Registers	master mode off	master mode on
dark_hr_th2	18	00
dark_hr_th	04	00
dark_ccr1	04	80
dark_ccr2	08	FF
dark_ec_pth1	18	04
dark_ec_pth2	20	04
dark_ec_mth1	18	04
dark_ec_mth2	20	04
dark_ec_pmax0	4F	80
dark_ec_pmax1	2F	80
dark_ec_pmax2	2F	80
dark_ec_pmax	4F	80
dark_ec_mmax0	4F	80
dark_ec_mmax1	2F	80
dark_ec_mmax2	2F	80
dark_ec_mmax	4F	80
resol_gain	00	08
enc_control	04	44

[Table 9] Internal ROM registers setting

▶ Access time of external i2c master

Because i2c master was designed as a single master and shares SDA/SCL with i2c slave, external i2c master must access to PC1089k after initialization routine as [Fig. 20]. Initialization time depends on the number of registers to be written by external i2c rom. If the number of setting register is 1024d (max.), it will take initialization time about 140ms to be finished after reset. After that, an external i2c master should access to PC1089K.

Access time as below.

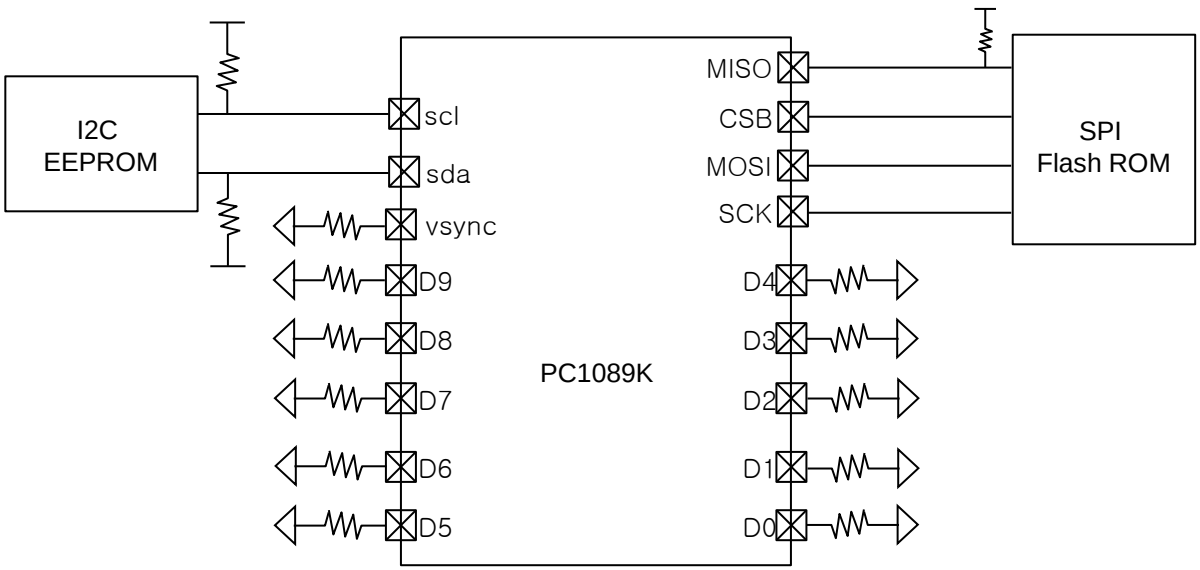
Case1 : master enable and with external i2c rom : variable (depend on register numbers, max. 140ms)

Case2 : master enable and without external i2c rom : after about 3ms(i2c rom detection time)

Case3 : master disable: always possible

▶ Registers Initializing

PC1089K supports user tuning registers can be set by I2C EEPROM or SPI Flash ROM initially. [Fig. 19] shows how to connect PC1089K with external ROM(I2C EEPROM/SPI Flash ROM). After reset, PC1089K reads initialization table stored in external ROM. [Fig. 20] shows Initialization routine.



[Fig. 19] Example of connection with external ROM

Initialization process is as below.

Case1 : Connect with I2C EEPROM & disconnect with SPI Flash ROM :
PC1089K is initialized by I2C EEPROM. SPI Flash ROM process is skipped.

Case2 : Connect with SPI Flash ROM & disconnect with I2C EEPROM :
PC1089K is initialized by SPI Flash ROM. I2C EEPROM process is skipped.

Case3 : Connect with I2C EEPROM & connect with SPI ROM :
PC1089K registers are overwritten by SPI Flash ROM.

* Caution : It covers up to 2K bytes I2C EEPROM. If the I2C EEPROM size is more than 2K bytes then register setting does not operate.

▶ 2-wire Serial Interface Description

The registers of PC1089K are written and read through the 2-wire Serial Interface. The PC1089K has 2-wire Serial Interface slave. The PC1089K is controlled by the Register Access Clock (SCL), which is driven by the 2-wire Serial Interface master. Data is transferred into and out of the PC1089K through the Register Access Data (SDA) line. The SCL and SDA lines are pulled up to VDD by a 2kΩ off-chip resistor. Either the slave or master device can pull the lines down. The 2-wire Serial Interface protocol determines which device is allowed to pull the two lines down at any given time.

Start bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a 2-wire Serial Interface device consists of 7-bit of address and 1-bit of direction. A '0' in the LSB of the address indicates write mode, and a '1' indicates read-mode.

Data bit transfer

One data bit is transferred during each clock pulse. The SCL pulse is provided by the master. The data must be stable during the HIGH period of the SCL. SDA can be only changed when the SCL is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge bit

The receiver generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

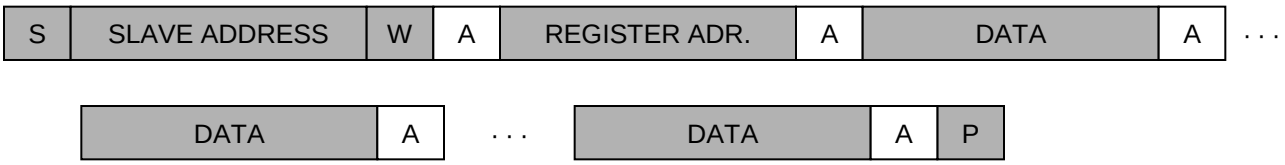
Sequence

A typical read or write sequence begins by the master sending a start bit. After start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a '0' indicates a write and a '1' indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master. If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The PC1089K uses 8 bit data for its internal registers, thus requiring one 8-bit transfer to write to one register. After 8 bits are transferred, the register address is automatically incremented, so that the next 8 bits are written to the next register address. The master stops writing by sending a start or stop bit. A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after each 8 bit is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

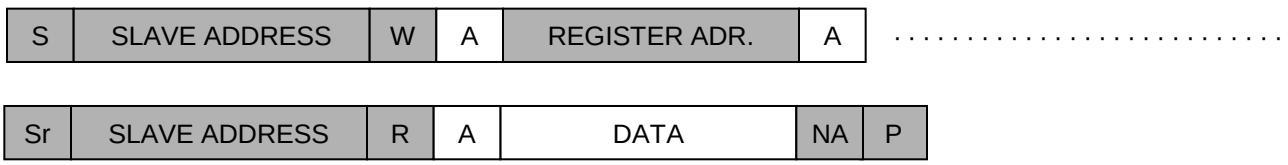
▶ 2-wire Serial Interface Functional Description

Single Write Mode operation

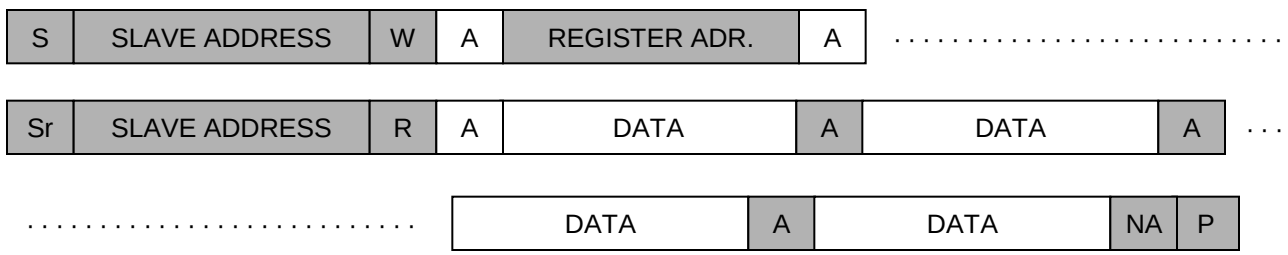
Multiple Write Mode (Register address is increased automatically)[1] operation



Single Read Mode operation



Multiple Read Mode (Register address is increased automatically)[1] operation



From master to slave From slave to master

S: Start condition. Sr : Repeated Start (Start without preceding stop.)

SLAVE ADDRESS: It can be extended 60h to 67h by CADDR0 and CADDR1 pad

write address	**60h**	**62h**	**64h**	**66h(default)**
read address	**61h**	**63h**	**65h**	**67h(default)**

R/W: Read/Write selection. High = read / LOW = write.

A: Acknowledge bit. NA : No Acknowledge. DATA: 8-bit data. P: Stop condition.

Note 1: Continuous writing or reading without any interrupt increases the register address automatically. If the address is increased above valid register address range, further writing does not affect the chip operation in write mode. Data from invalid registers are undefined in read mode.

1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

▶ Register Tables – Group A

GROUP A									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
0	00	DeviceID_H	16	10	00010000	RO	0	0	Device ID
1	01	DeviceID_L	137	89	10001001	RO	0	0	
2	02	RevNumber	0	00	00000000	RO	0	0	Revision number
3	03	bank	0	00	00000000	RW	5	0	Register group selector
4	04	chip_mode	u	u	uuuuuuuu	RW	7	aev	chip mode selection(NTSC, PAL, VGA)
5	05	mirror	u	u	uuuuuuuu	RW	7	aev	Mirror
6	06	framewidth_h	u	u	uuuuuuuu	RW	7	aev	Framewidth
7	07	framewidth_l	u	u	uuuuuuuu	RW	7	aev	
8	08	fd_fheight_a_h	2	02	00000010	RW	6	aev	Frameheight
9	09	fd_fheight_a_l	u	u	uuuuuuuu	RW	7	aev	
10	0A	fd_fheight_b_h	2	02	00000010	RW	6	aev	
11	0B	fd_fheight_b_l	u	u	uuuuuuuu	RW	7	aev	
12	0C	windowx1_h	0	00	00000000	RW	6	aev	Window
13	0D	windowx1_l	1	01	00000001	RW	6	aev	
14	0E	windowy1_h	0	00	00000000	RW	6	aev	
15	0F	windowy1_l	1	01	00000001	RW	6	aev	
16	10	windowx2_h	2	02	00000010	RW	6	aev	
17	11	windowx2_l	208	D0	11010000	RW	6	aev	
18	12	windowy2_h	u	u	uuuuuuuu	RW	7	aev	
19	13	windowy2_l	u	u	uuuuuuuu	RW	7	aev	
20	14	vsyncstartrow_f0_h	0	00	00000000	RW	6	aev	Vsync generation
21	15	vsyncstartrow_f0_l	23	17	00010111	RW	6	aev	
22	16	vsyncstoprow_f0_h	1	01	00000001	RW	6	aev	
23	17	vsyncstoprow_f0_l	u	u	uuuuuuuu	RW	7	aev	
24	18	vsyncstartrow_f1_h	1	01	00000001	RW	6	aev	
25	19	vsyncstartrow_f1_l	u	u	uuuuuuuu	RW	7	aev	
26	1A	vsyncstoprow_f1_h	2	02	00000010	RW	6	aev	
27	1B	vsyncstoprow_f1_l	u	u	uuuuuuuu	RW	7	aev	
28	1C	vsynccolumn_h	0	00	00000000	RW	5	0	
29	1D	vsynccolumn_l	2	02	00000010	RW	5	0	
31	1F	i2c_master_en	1	01	00000001	RW	5	0	I2c master enable
35	23	i2c_control_1	80	50	01010000	RW	5	0	I2c control register
36	24	softreset	0	00	00000000	RW	5	0	Soft reset
37	25	clkdiv	7	07	00000111	RW	6	aev	Colck divider
38	26	p_pp_equal	0	00	00000000	RW	5	0	PCLK& PPCLK control
39	27	pad_control1	102	66	01100110	RW	5	0	Pad control
40	28	pad_control2	0	00	00000000	RW	5	0	
41	29	pad_control3	0	00	00000000	RW	5	0	
42	2A	pad_control4	0	00	00000000	RW	5	0	
43	2B	pad_control5	192	C0	11000000	RW	5	0	
44	2C	pad_control6	0	00	00000000	RW	5	0	
45	2D	strap_control	255	FF	11111111	RW	5	0	Strap control
73	49	bayer_control_01	5	05	00000101	RW	5	0	bayer_control_01

(Group A – continued)

▶ Register Tables – Group B

GROUP B									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
256	00	DeviceID_H	16	10	00010000	RO	0	0	device ID
257	01	DeviceID_L	137	89	10001001	RO	0	0	
258	02	RevNumber	0	00	00000000	RO	0	0	revision number
259	03	bank	0	00	00000000	0	5	0	Register group selector
260	04	isp_func_0	247	F7	11110111	RW	6	aev	Isp function control
261	05	isp_func_1	255	FF	11111111	RW	6	aev	
262	06	isp_func_2	0	00	00000000	RW	6	aev	
263	07	isp_func_3	161	A1	10100001	RW	6	aev	
264	08	isp_func_4	0	00	00000000	RW	6	aev	
265	09	isp_func_5	0	00	00000000	RW	6	aev	
266	0A	tp_control_0	0	00	00000000	RW	5	0	Test pattern control
268	0C	lens_red_e	81	51	01010001	RW	5	0	Lens shading compensation scale control
269	0D	lens_red_w	81	51	01010001	RW	5	0	
270	0E	lens_red_n	81	51	01010001	RW	5	0	
271	0F	lens_red_s	81	51	01010001	RW	5	0	
272	10	lens_g1_e	81	51	01010001	RW	5	0	
273	11	lens_g1_w	81	51	01010001	RW	5	0	
274	12	lens_g1_n	81	51	01010001	RW	5	0	
275	13	lens_g1_s	81	51	01010001	RW	5	0	
276	14	lens_g2_e	81	51	01010001	RW	5	0	
277	15	lens_g2_w	81	51	01010001	RW	5	0	
278	16	lens_g2_n	81	51	01010001	RW	5	0	
279	17	lens_g2_s	81	51	01010001	RW	5	0	
280	18	lens_blu_e	81	51	01010001	RW	5	0	
281	19	lens_blu_w	81	51	01010001	RW	5	0	
282	1A	lens_blu_n	81	51	01010001	RW	5	0	
283	1B	lens_blu_s	81	51	01010001	RW	5	0	
284	1C	lens_gainr	0	00	00000000	RW	6	aev	Lens shading compensation R gain
285	1D	lens_gaing1	0	00	00000000	RW	6	aev	Lens shading compensation G1 gain
286	1E	lens_gaing2	0	00	00000000	RW	6	aev	Lens shading compensation G2 gain
287	1F	lens_gainb	0	00	00000000	RW	6	aev	Lens shading compensation B gain
288	20	lens_rx	0	00	00000000	RW	5	0	Lens shading compensation center control
289	21	lens_ry	0	00	00000000	RW	5	0	
290	22	lens_g1x	0	00	00000000	RW	5	0	
291	23	lens_g1y	0	00	00000000	RW	5	0	
292	24	lens_g2x	0	00	00000000	RW	5	0	
293	25	lens_g2y	0	00	00000000	RW	5	0	
294	26	lens_bx	0	00	00000000	RW	5	0	
295	27	lens_by	0	00	00000000	RW	5	0	
297	29	format	0	00	00000000	RW	6	aev	Format control

(Group B – continued)

1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

▶ Register Tables – Group B

GROUP B									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
303	2F	edge_gain	56	38	00111000	RW	5	0	Edge gain
304	30	ec_pgain	48	30	00110000	RW	5	0	Positive max edge clamp gain
305	31	ec_mgain	56	38	00111000	RW	5	0	Negative max edge clamp gain
307	33	ccr_m11	51	33	00110011	RW	5	0	Color correction matrix value
308	34	ccr_m12	139	8B	10001011	RW	5	0	
309	35	ccr_m13	136	88	10001000	RW	5	0	
310	36	ccr_m21	134	86	10000110	RW	5	0	
311	37	ccr_m22	49	31	00110001	RW	5	0	
312	38	ccr_m23	138	8A	10001010	RW	5	0	
313	39	ccr_m31	131	83	10000011	RW	5	0	
314	3A	ccr_m32	143	8F	10001111	RW	5	0	
315	3B	ccr_m33	50	32	00110010	RW	5	0	
317	3D	ygm1_y0	0	00	00000000	RW	5	0	Y gamma1 coefficient
318	3E	ygm1_y1	3	03	00000011	RW	5	0	
319	3F	ygm1_y2	12	0C	00001100	RW	5	0	
320	40	ygm1_y3	25	19	00011001	RW	5	0	
321	41	ygm1_y4	38	26	00100110	RW	5	0	
322	42	ygm1_y5	63	3F	00111111	RW	5	0	
323	43	ygm1_y6	82	52	01010010	RW	5	0	
324	44	ygm1_y7	110	6E	01101110	RW	5	0	
325	45	ygm1_y8	130	82	10000010	RW	5	0	
326	46	ygm1_y9	161	A1	10100001	RW	5	0	
327	47	ygm1_y10	185	B9	10111001	RW	5	0	
328	48	ygm1_y11	206	CE	11001110	RW	5	0	
329	49	ygm1_y12	224	E0	11100000	RW	5	0	
330	4A	ygm1_y13	240	F0	11110000	RW	5	0	
331	4B	ygm1_y14	255	FF	11111111	RW	5	0	
332	4C	ygm2_y0	0	00	00000000	RW	5	0	Y gamma2 coefficient
333	4D	ygm2_y1	11	0B	00001011	RW	5	0	
334	4E	ygm2_y2	23	17	00010111	RW	5	0	
335	4F	ygm2_y3	34	22	00100010	RW	5	0	
336	50	ygm2_y4	46	2E	00101110	RW	5	0	
337	51	ygm2_y5	64	40	01000000	RW	5	0	
338	52	ygm2_y6	80	50	01010000	RW	5	0	
339	53	ygm2_y7	110	6E	01101110	RW	5	0	
340	54	ygm2_y8	136	88	10001000	RW	5	0	
341	55	ygm2_y9	174	AE	10101110	RW	5	0	
342	56	ygm2_y10	202	CA	11001010	RW	5	0	
343	57	ygm2_y11	220	DC	11011100	RW	5	0	
344	58	ygm2_y12	236	EC	11101100	RW	5	0	
345	59	ygm2_y13	246	F6	11110110	RW	5	0	
346	5A	ygm2_y14	255	FF	11111111	RW	5	0	

(Group B – continued)

1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

▶ Register Tables – Group B

GROUP B									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
347	5B	cgm1_y0	0	00	00000000	RW	5	0	RGB gamma1 coefficient
348	5C	cgm1_y1	11	0B	00001011	RW	5	0	
349	5D	cgm1_y2	23	17	00010111	RW	5	0	
350	5E	cgm1_y3	34	22	00100010	RW	5	0	
351	5F	cgm1_y4	46	2E	00101110	RW	5	0	
352	60	cgm1_y5	64	40	01000000	RW	5	0	
353	61	cgm1_y6	80	50	01010000	RW	5	0	
354	62	cgm1_y7	110	6E	01101110	RW	5	0	
355	63	cgm1_y8	136	88	10001000	RW	5	0	
356	64	cgm1_y9	174	AE	10101110	RW	5	0	
357	65	cgm1_y10	202	CA	11001010	RW	5	0	
358	66	cgm1_y11	220	DC	11011100	RW	5	0	
359	67	cgm1_y12	236	EC	11101100	RW	5	0	
360	68	cgm1_y13	246	F6	11110110	RW	5	0	
361	69	cgm1_y14	255	FF	11111111	RW	5	0	
362	6A	cgm2_y0	0	00	00000000	RW	5	0	RGB gamma2 coefficient
363	6B	cgm2_y1	11	0B	00001011	RW	5	0	
364	6C	cgm2_y2	23	17	00010111	RW	5	0	
365	6D	cgm2_y3	34	22	00100010	RW	5	0	
366	6E	cgm2_y4	46	2E	00101110	RW	5	0	
367	6F	cgm2_y5	64	40	01000000	RW	5	0	
368	70	cgm2_y6	80	50	01010000	RW	5	0	
369	71	cgm2_y7	110	6E	01101110	RW	5	0	
370	72	cgm2_y8	136	88	10001000	RW	5	0	
371	73	cgm2_y9	174	AE	10101110	RW	5	0	
372	74	cgm2_y10	202	CA	11001010	RW	5	0	
373	75	cgm2_y11	220	DC	11011100	RW	5	0	
374	76	cgm2_y12	236	EC	11101100	RW	5	0	
375	77	cgm2_y13	246	F6	11110110	RW	5	0	
376	78	cgm2_y14	255	FF	11111111	RW	5	0	
378	7A	sketch_offset	140	8C	10001100	RW	6	aev	Sketch offset
379	7B	scale_x	32	20	00100000	RW	6	aev	Horizontal scale factor
380	7C	scale_y	u	u	uuuuuuuu	RW	7	aev	Vertical scale factor
381	7D	scale_th_h	0	00	00000000	RW	6	aev	Scale buffer TH
382	7E	scale_th_l	10	0A	00001010	RW	6	aev	
383	7F	bw_th	128	80	10000000	RW	5	0	Black&white TH
384	80	cs11	37	25	00100101	RW	6	aev	Color saturation matrix value
385	81	cs12	0	00	00000000	RW	6	aev	
386	82	cs21	0	00	00000000	RW	6	aev	
387	83	cs22	37	25	00100101	RW	6	aev	

(Group B – continued)

▶ Register Tables – Group B

GROUP B									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
392	88	cb_offset	128	80	10000000	RW	6	aev	Cb offset
393	89	cr_offset	128	80	10000000	RW	6	aev	Cr offset
394	8A	c_max	127	7F	01111111	RW	6	aev	Cb/Cr max
396	8C	auto_data_control	0	00	00000000	RW	5	0	Auto data control
397	8D	auto_off	0	00	00000000	RW	5	0	Auto off (MCU off)
399	8F	y_weight	64	40	01000000	RW	6	aev	Y weight
400	90	y_max	254	FE	11111110	RW	6	aev	Y max
401	91	ycontrast_ref0	64	40	01000000	RW	5	0	Dark Y contrast fitting control
402	92	ycontrast_ref1	64	40	01000000	RW	5	0	
403	93	ycontrast_ref2	64	40	01000000	RW	5	0	
404	94	ycontrast	64	40	01000000	RW	6	aev	
405	95	ybrightness_ref0	0	00	00000000	RW	5	0	Dark Y brightness fitting control
406	96	ybrightness_ref1	0	00	00000000	RW	5	0	
407	97	ybrightness_ref2	0	00	00000000	RW	5	0	
408	98	ybrightness	0	00	00000000	RW	6	aev	
410	9A	sync_control_0	128	80	10000000	RW	6	aev	Sync control
411	9B	sync_control_1	0	00	00000000	RW	6	aev	
412	9C	sync_control_2	128	80	10000000	RW	6	aev	
413	9D	blankvalue	0	00	00000000	RW	5	aev	Data of black period
416	A0	prvc_wx1_h	0	00	00000000	RW	5	0	Privacy window size control
417	A1	prvc_wx1_l	1	01	00000001	RW	5	0	
418	A2	prvc_wx2_h	2	02	00000010	RW	5	0	
419	A3	prvc_wx2_l	208	D0	11010000	RW	5	0	
420	A4	prvc_wy1_h	0	00	00000000	RW	5	0	
421	A5	prvc_wy1_l	1	01	00000001	RW	5	0	
422	A6	prvc_wy2_h	0	00	00000000	RW	5	0	
423	A7	prvc_wy2_l	240	F0	11110000	RW	5	0	
424	A8	prvc_y	0	00	00000000	RW	5	0	YCbCr of privacy window
425	A9	prvc_cb	128	80	10000000	RW	5	0	
426	AA	prvc_cr	128	80	10000000	RW	5	0	
435	B3	ae_fwx1_h	0	00	00000000	RW	5	0	AE full window X start position
436	B4	ae_fwx1_l	1	01	00000001	RW	5	0	
437	B5	ae_fwx2_h	2	02	00000010	RW	5	0	AE full window X stop position
438	B6	ae_fwx2_l	208	D0	11010000	RW	5	0	

(Group B – continued)

▶ Register Tables – Group B

GROUP B									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
439	B7	ae_fwy1_h	0	00	00000000	RW	5	0	AE full window Y start position
440	B8	ae_fwy1_l	1	01	00000001	RW	5	0	
441	B9	ae_fwy2_h	u	u	uuuuuuuu	RW	5	0	AE full window Y stop position
442	BA	ae_fwy2_l	u	u	uuuuuuuu	RW	5	0	
443	BB	ae_cwx1_h	0	00	00000000	RW	5	0	AE center window X start position
444	BC	ae_cwx1_l	241	F1	11110001	RW	5	0	
445	BD	ae_cwx2_h	1	01	00000001	RW	5	0	AE center window X stop position
446	BE	ae_cwx2_l	224	E0	11100000	RW	5	0	
447	BF	ae_cwy1_h	0	00	00000000	RW	5	0	AE center window Y start position
448	C0	ae_cwy1_l	u	u	uuuuuuuu	RW	5	0	
449	C1	ae_cwy2_h	0	00	00000000	RW	5	0	AE center window Y stop position
450	C2	ae_cwy2_l	u	u	uuuuuuuu	RW	5	0	
451	C3	ae_xaxis_h	1	01	00000001	RW	5	0	AE window X axis
452	C4	ae_xaxis_l	105	69	01101001	RW	5	0	
453	C5	ae_yaxis_h	0	00	00000000	RW	5	0	AE window Y axis
454	C6	ae_yaxis_l	u	u	uuuuuuuu	RW	5	0	
455	C7	awb_fwx1_h	0	00	00000000	RW	5	0	AWB full window X start position
456	C8	awb_fwx1_l	1	01	00000001	RW	5	0	
457	C9	awb_fwx2_h	2	02	00000010	RW	5	0	AWB full window X stop position
458	CA	awb_fwx2_l	208	D0	11010000	RW	5	0	
459	CB	awb_fwy1_h	0	00	00000000	RW	5	0	AWB full window Y start position
460	CC	awb_fwy1_l	1	01	00000001	RW	5	0	
461	CD	awb_fwy2_h	u	u	uuuuuuuu	RW	5	0	AWB full window Y stop position
462	CE	awb_fwy2_l	u	u	uuuuuuuu	RW	5	0	
463	CF	awb_cwx1_h	0	00	00000000	RW	5	0	AWB center window X start position
464	D0	awb_cwx1_l	241	F1	11110001	RW	5	0	
465	D1	awb_cwx2_h	1	01	00000001	RW	5	0	AWB center window X stop position
466	D2	awb_cwx2_l	224	E0	11100000	RW	5	0	
467	D3	awb_cwy1_h	0	00	00000000	RW	5	0	AWB center window Y start position
468	D4	awb_cwy1_l	u	u	uuuuuuuu	RW	5	0	
469	D5	awb_cwy2_h	0	00	00000000	RW	5	0	AWB center window Y stop position
470	D6	awb_cwy2_l	u	u	uuuuuuuu	RW	5	0	
472	D8	af_cwx1_h	0	00	00000000	RW	5	0	AF center window X start position
473	D9	af_cwx1_l	241	F1	11110001	RW	5	0	
474	DA	af_cwx2_h	1	01	00000001	RW	5	0	AF center window X stop position
475	DB	af_cwx2_l	224	E0	11100000	RW	5	0	
476	DC	af_cwy1_h	0	00	00000000	RW	5	0	AF center window Y start position
477	DD	af_cwy1_l	u	u	uuuuuuuu	RW	5	0	
478	DE	af_cwy2_h	0	00	00000000	RW	5	0	AF center window Y stop position
479	DF	af_cwy2_l	u	u	uuuuuuuu	RW	5	0	
480	E0	af_cweight	8	08	00001000	RW	5	0	AF weight center
481	E1	af_edge_th	0	00	00000000	RW	5	0	AF edge TH
483	E3	md_yth1	64	40	01000000	RW	5	0	Y threshold1 for motion detection
484	E4	md_yth2	64	40	01000000	RW	5	0	Y threshold2 for motion detection
485	E5	md_yth3	64	40	01000000	RW	5	0	Y threshold3 for motion detection

(Group B – continued)

▶ Register Tables – Group B

GROUP B									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
486	E6	md_yth4	64	40	01000000	RW	5	0	Y threshold4 for motion detection
487	E7	md_diff1	64	40	01000000	RW	5	0	Difference1 for motion detection
488	E8	md_diff2	64	40	01000000	RW	5	0	Difference2 for motion detection
489	E9	md_diff3	64	40	01000000	RW	5	0	Difference3 for motion detection
490	EA	md_diff4	64	40	01000000	RW	5	0	Difference4 for motion detection
491	EB	md_interval	8	08	00001000	RW	5	0	Intervals of frames used for motion detection
492	EC	md_alarm_y	0	00	00000000	RW	5	0	YCbCr for Motion detection alarm
493	ED	md_alarm_cb	128	80	10000000	RW	5	0	
494	EE	md_alarm_cr	128	80	10000000	RW	5	0	
495	EF	md_alarmnumb	4	04	00000100	RW	5	0	Number of Motion detection alarm
496	F0	md_alarm_xlw	4	04	00000100	RW	5	0	X width of motion detection alarm
497	F1	md_alarm_ylw	4	04	00000100	RW	5	0	Y width of motion detection alarm
498	F2	md_alarmdur_h	0	00	00000000	RW	5	0	Period of motion detection alarm
499	F3	md_alarmdur_l	60	3C	00111100	RW	5	0	
500	F4	md_sleepdur_h	2	02	00000010	RW	5	0	Motion detection sleep
501	F5	md_sleepdur_l	58	3A	00111010	RW	5	0	
502	F6	md_section7	0	00	00000000	RW	5	0	Image section 7 for motion detection
503	F7	md_section6	0	00	00000000	RW	5	0	Image section 6 for motion detection
504	F8	md_section5	0	00	00000000	RW	5	0	Image section 5 for motion detection
505	F9	md_section4	0	00	00000000	RW	5	0	Image section 4 for motion detection
506	FA	md_section3	0	00	00000000	RW	5	0	Image section 3 for motion detection
507	FB	md_section2	0	00	00000000	RW	5	0	Image section 2 for motion detection
508	FC	md_section1	0	00	00000000	RW	5	0	Image section 1 for motion detection
509	FD	md_section0	0	00	00000000	RW	5	0	Image section 0 for motion detection

▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
512	00	DeviceID_H	16	10	00010000	RO	0	0	device ID
513	01	DeviceID_L	137	89	10001001	RO	0	0	
514	02	RevNumber	0	00	00000000	RO	0	0	revision number
515	03	bank	0	00	00000000	0	5	0	
516	04	auto_control_1	152	98	10011000	RW	6	autov	Auto control
517	05	auto_control_2	101	65	01100101	RW	6	autov	
518	06	auto_control_3	128	80	10000000	RW	6	autov	
519	07	auto_control_4	128	80	10000000	RW	6	autov	
520	08	auto_control_5	0	00	00000000	RW	6	autov	
521	09	auto_control_6	1	01	00000001	RW	6	autov	
522	0A	awb_control_1	149	95	10010101	RW	6	autov	AWB control
523	0B	awb_control_2	119	77	01110111	RW	6	autov	
524	0C	awb_control_3	36	24	00100100	RW	6	autov	
525	0D	awb_control_4	128	80	10000000	RW	6	autov	
526	0E	event_control	238	EE	11101110	RW	5	0	Event control
528	10	expfrmh_h	2	02	00000010	RW	5	0	AE reference
529	11	expfrmh_l	u	u	uuuuuuuu	RW	5	0	
530	12	midfrmheight_h	2	02	00000010	RW	5	0	
531	13	midfrmheight_l	u	u	uuuuuuuu	RW	5	0	
532	14	maxfrmheight_h	2	02	00000010	RW	5	0	
533	15	maxfrmheight_l	u	u	uuuuuuuu	RW	5	0	
534	16	minexp_h	0	00	00000000	RW	5	0	
535	17	minexp_m	0	00	00000000	RW	5	0	
536	18	minexp_l	12	0C	00001100	RW	5	0	
537	19	midexp_t	1	01	00000001	RW	5	0	
538	1A	midexp_h	133	85	10000101	RW	5	0	
539	1B	midexp_m	64	40	01000000	RW	5	0	
540	1C	maxexp_t	1	01	00000001	RW	5	0	
541	1D	maxexp_h	133	85	10000101	RW	5	0	
542	1E	maxexp_m	64	40	01000000	RW	5	0	
544	20	ext_inttime_h	0	00	00000000	RW	6	autov	Manual integration time @ external AE mode
545	21	ext_inttime_m	128	80	10000000	RW	6	autov	
546	22	ext_inttime_l	0	00	00000000	RW	6	autov	
547	23	ext_glbg_h	1	01	00000001	RW	6	autov	Manual analog gain @ external AE mode
548	24	ext_glbg_l	0	00	00000000	RW	6	autov	
549	25	exposure_t	0	00	00000000	RW	6	autov	Exposure
550	26	exposure_h	1	01	00000001	RW	6	autov	
551	27	exposure_m	64	40	01000000	RW	6	autov	
552	28	exposure_l	0	00	00000000	RW	6	autov	
554	2A	ae_ysat	68	44	01000100	RW	6	autov	Saturation decision TH
556	2C	sratio_weight	8	08	00001000	RW	5	0	Saturation ratio weight
557	2D	sratio	0	00	00000000	RW	5	0	Saturation ratio

(Group C – continued)

1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
558	2E	ae_weight1	8	08	00001000	RW	5	0	AE weight peripheral
559	2F	ae_weight2	8	08	00001000	RW	5	0	
560	30	ae_weight3	8	08	00001000	RW	5	0	
561	31	ae_weight4	8	08	00001000	RW	5	0	
562	32	ae_weightc	8	08	00001000	RW	5	0	AE weight center
563	33	ymean_ref0	16	10	00010000	RW	5	0	Y mean extension reference
564	34	ymean_ref1	64	40	01000000	RW	5	0	
565	35	ymean_ref2	128	80	10000000	RW	5	0	
566	36	ymean_ref3	255	FF	11111111	RW	5	0	
567	37	ymean_h	0	00	00000000	RW	5	0	Y mean
568	38	ymean_l	128	80	10000000	RW	5	0	
569	39	max_yt1	160	A0	10100000	RW	6	autov	Dynamic Y target control
570	3A	max_yt2	128	80	10000000	RW	6	autov	
571	3B	min_yt1	128	80	10000000	RW	6	autov	
572	3C	min_yt2	80	50	01010000	RW	6	autov	
573	3D	gg_ref0	36	24	00100100	RW	6	autov	
574	3E	gg_ref1	75	4B	01001011	RW	6	autov	
575	3F	sratio_ref0	4	04	00000100	RW	6	autov	
576	40	sratio_ref1	16	10	00010000	RW	6	autov	
577	41	sratio_ref2	26	1A	00011010	RW	6	autov	
578	42	sratio_ref3	50	32	00110010	RW	6	autov	
579	43	yt_step	4	04	00000100	RW	5	0	
580	44	ytarget	112	70	01110000	R	5	0	Y target
581	45	user_wyt	128	80	10000000	RW	6	autov	User weight Y target
582	46	ae_up_speed	8	08	00001000	RW	6	autov	AE upside speed
583	47	ae_down_speed	8	08	00001000	RW	6	autov	AE downside speed
584	48	ae_lock	16	10	00010000	RW	6	autov	AE lock range
585	49	auto_flag	0	00	00000000	RW	5	0	Auto flag
588	4C	awb_full_th_t	1	01	00000001	RW	5	0	AWB full Control
589	4D	awb_full_th_h	133	85	10000101	RW	5	0	
590	4E	awb_full_th_m	64	40	01000000	RW	5	0	
591	4F	awb_full	0	00	00000000	RW	5	0	
593	51	awb_p1Ax	41	29	00101001	RW	5	0	AWB sampling range selection
594	52	awb_p1Ay	57	39	00111001	RW	5	0	
595	53	awb_p2Ax	54	36	00110110	RW	5	0	
596	54	awb_p2Ay	25	19	00011001	RW	5	0	
597	55	awb_osAx	9	09	00001001	RW	5	0	
598	56	awb_osAy	16	10	00010000	RW	5	0	
599	57	awb_slopeA	160	A0	10100000	RW	5	0	
600	58	awb_p1Bx	54	36	00110110	RW	5	0	
601	59	awb_p1By	33	21	00100001	RW	5	0	
602	5A	awb_p2Bx	105	69	01101001	RW	5	0	
603	5B	awb_p2By	20	14	00010100	RW	5	0	
604	5C	awb_osBx	12	0C	00001100	RW	5	0	

(Group C – continued)

▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
605	5D	awb_osBy	4	04	00000100	RW	5	0	AWB sampling range selection
606	5E	awb_slopeB	16	10	00010000	RW	5	0	
607	5F	awb_maxc	250	FA	11111010	RW	5	0	
608	60	awb_minc	8	08	00001000	RW	5	0	
609	61	awb_weight_c	5	05	00000101	RW	5	0	AWB weight for center
610	62	awb_weight_p	11	0B	00001011	RW	5	0	AWB weight for peripheral
611	63	awb_wspeed	4	04	00000100	RW	5	0	AWB weight speed
614	66	rg_ratio_a	122	7A	01111010	RW	5	0	Target awb ratio fitting reference
615	67	bg_ratio_a	120	78	01111000	RW	5	0	
616	68	rg_ratio_b	128	80	10000000	RW	5	0	
617	69	bg_ratio_b	128	80	10000000	RW	5	0	
618	6A	rg_ratio_c	128	80	10000000	RW	5	0	
619	6B	bg_ratio_c	128	80	10000000	RW	5	0	
620	6C	ratio_axis_a	42	2A	00101010	RW	5	0	
621	6D	ratio_axis_b	80	50	01010000	RW	5	0	
622	6E	ratio_axis_c	87	57	01010111	RW	5	0	
623	6F	awb_rgratio	128	80	10000000	RW	5	0	AWB RG ratio control
624	70	awb_bgratio	128	80	10000000	RW	5	0	AWB BG ratio control
625	71	awb_lock	16	10	00010000	RW	5	0	AWB lock range
626	72	awb_speed	4	04	00000100	RW	5	0	AWB speed
627	73	awb_rgain_min1	42	2A	00101010	RW	5	0	AWB gain clamping fitting control
628	74	awb_rgain_min2	40	28	00101000	RW	5	0	
629	75	awb_rgain_max1	90	5A	01011010	RW	5	0	
630	76	awb_rgain_max2	93	5D	01011101	RW	5	0	
631	77	awb_bgain_min1	80	50	01010000	RW	5	0	
632	78	awb_bgain_min2	77	4D	01001101	RW	5	0	
633	79	awb_bgain_max1	183	B7	10110111	RW	5	0	
634	7A	awb_bgain_max2	186	BA	10111010	RW	5	0	
635	7B	awb_cmp_th1_h	1	01	00000001	RW	5	0	
636	7C	awb_cmp_th1_m	0	00	00000000	RW	5	0	
637	7D	awb_cmp_th2_h	2	02	00000010	RW	5	0	
638	7E	awb_cmp_th2_m	7	07	00000111	RW	5	0	
639	7F	cs11_a	40	28	00101000	RW	5	0	Color saturation matrix fitting reference
640	80	cs12_a	0	00	00000000	RW	5	0	
641	81	cs21_a	0	00	00000000	RW	5	0	
642	82	cs22_a	40	28	00101000	RW	5	0	
643	83	cs11_b	36	24	00100100	RW	5	0	
644	84	cs12_b	0	00	00000000	RW	5	0	
645	85	cs21_b	0	00	00000000	RW	5	0	
646	86	cs22_b	40	28	00101000	RW	5	0	
647	87	cs11_c	32	20	00100000	RW	5	0	
648	88	cs12_c	0	00	00000000	RW	5	0	
649	89	cs21_c	0	00	00000000	RW	5	0	
650	8A	cs22_c	32	20	00100000	RW	5	0	

(Group C – continued)

1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
651	8B	lens_gainr_a	2	02	00000010	RW	5	0	Lens gain fitting reference
652	8C	lens_gainb_a	0	00	00000000	RW	5	0	
653	8D	lens_gainr_b	2	02	00000010	RW	5	0	
654	8E	lens_gainb_b	0	00	00000000	RW	5	0	
655	8F	lens_gainr_c	2	02	00000010	RW	5	0	
656	90	lens_gainb_c	0	00	00000000	RW	5	0	
657	91	axis_a	42	2A	00101010	RW	5	0	CS matrix / lens gain fitting reference
658	92	axis_b	80	50	01010000	RW	5	0	
659	93	axis_c	87	57	01010111	RW	5	0	
660	94	user_cs	32	20	00100000	RW	5	0	User CS gain
662	96	iris_exp_th_t	0	00	00000000	RW	5	0	Iris control
663	97	iris_exp_th_h	0	00	00000000	RW	5	0	
664	98	iris_exp_th_m	0	00	00000000	RW	5	0	
665	99	iris_led_th	0	00	00000000	RW	5	0	
666	9A	iris_close	0	00	00000000	RW	5	0	
670	9E	dark_xref1_g0	12	0C	00001100	RW	5	0	Dark filter x-axis reference
671	9F	dark_xref2_g0	32	20	00100000	RW	5	0	
672	A0	dark_xref3_g0	64	40	01000000	RW	5	0	
673	A1	dark_xref1_g1	12	0C	00001100	RW	5	0	
674	A2	dark_xref2_g1	24	18	00011000	RW	5	0	
675	A3	dark_xref3_g1	32	20	00100000	RW	5	0	
676	A4	totalgain	2	02	00000010	RW	6	autov	Total gain
678	A6	dark_lens0	0	00	00000000	RW	5	0	Dark lens fitting control
679	A7	dark_lens1	0	00	00000000	RW	5	0	
680	A8	dark_lens2	0	00	00000000	RW	5	0	
681	A9	dark_lens	0	00	00000000	RW	6	aev	
690	B2	dark_blf0	95	5F	01011111	RW	5	0	Dark bilateral filter fitting control
691	B3	dark_blf1	63	3F	00111111	RW	5	0	
692	B4	dark_blf2	63	3F	00111111	RW	5	0	
693	B5	dark_blf	127	7F	01111111	RW	6	aev	
694	B6	dark_nf0	64	40	01000000	RW	5	0	Dark noise floor fitting control
695	B7	dark_nf1	64	40	01000000	RW	5	0	
696	B8	dark_nf2	64	40	01000000	RW	5	0	
697	B9	dark_nf	1	01	00000001	RW	6	aev	

(Group C – continued)

▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
711	C7	y_cont_th_ref0	255	FF	11111111	RW	5	0	Dark y contrast th fitting control
712	C8	y_cont_th_ref1	255	FF	11111111	RW	5	0	
713	C9	y_cont_th_ref2	255	FF	11111111	RW	5	0	
714	CA	y_cont_th	255	FF	11111111	RW	6	aev	
715	CB	y_cont_slope_ref0	80	50	01010000	RW	5	0	Dark y contrast slope fitting control
716	CC	y_cont_slope_ref1	80	50	01010000	RW	5	0	
717	CD	y_cont_slope_ref2	80	50	01010000	RW	5	0	
718	CE	y_cont_slope	80	50	01010000	RW	6	aev	
722	D2	dark_y_gm0	0	00	00000000	RW	5	0	Dark Y gamma fitting control
723	D3	dark_y_gm1	16	10	00010000	RW	5	0	
724	D4	dark_y_gm2	63	3F	00111111	RW	5	0	
725	D5	dark_y_gm	0	00	00000000	RW	6	aev	
726	D6	dark_rgb_gm0	0	00	00000000	RW	5	0	Dark RGB gamma fitting control
727	D7	dark_rgb_gm1	0	00	00000000	RW	5	0	
728	D8	dark_rgb_gm2	0	00	00000000	RW	5	0	
729	D9	dark_rgb_gm	0	00	00000000	RW	6	aev	
730	DA	dark_ccr0	0	00	00000000	RW	5	0	Dark color correction fitting control
731	DB	dark_ccr1	4	04	00000100	RW	5	0	
732	DC	dark_ccr2	8	08	00001000	RW	5	0	
733	DD	dark_ccr	0	00	00000000	RW	6	aev	
735	DF	inttime_h	1	01	00000001	RW	6	aev	Integration time (line)
736	E0	inttime_m	64	40	01000000	RW	6	aev	
737	E1	inttime_l	0	00	00000000	RW	6	aev	Integration time (column)
738	E2	globalgain	0	00	00000000	RW	6	aev	Analog gain
739	E3	digitalgain	64	40	01000000	RW	6	aev	Digital gain
741	E5	refgain_min	0	00	00000000	RW	5	0	Reference gain for analog gain fitting

(Group C – continued)

▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
748	EC	wb_rgain	93	5D	01011101	RW	6	aev	White balance R gain
749	ED	wb_ggain	64	40	01000000	RW	6	aev	White balance G gain
750	EE	wb_bgain	94	5E	01011110	RW	6	aev	White balance B gain
758	F6	wb_gratio	128	80	10000000	RW	5	0	Gr/Gb ratio of white balance gain

1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

▶ Register Tables – Group D

GROUP D									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
867	63	sync_blankEAV_f0	182	B6	10110110	RW	5	0	Blank EAV for field0 of CCIR656 data or blank EAV for frame data
868	64	sync_blankSAV_f0	171	AB	10101011	RW	5	0	Blank SAV for field0 of CCIR656 data or blank SAV for frame data
869	65	sync_activeEAV_f0	157	9D	10011101	RW	5	0	Active EAV for field0 of CCIR656 data or active EAV for frame data
870	66	sync_activeSAV_f0	128	80	10000000	RW	5	0	Active SAV for field0 of CCIR656 data or active SAV for frame data
871	67	sync_blankEAV_f1	241	F1	11110001	RW	5	0	blank EAV for field1 of CCIR656 data
872	68	sync_blankSAV_f1	236	EC	11101100	RW	5	0	blank SAV for field1 of CCIR656 data
873	69	sync_activeEAV_f1	218	DA	11011010	RW	5	0	active EAV for field1 of CCIR656 data
874	6A	sync_activeSAV_f1	199	C7	11000111	RW	5	0	active SAV for field1 of CCIR656 data
875	6B	sync_CCIR_FF	255	FF	11111111	RW	5	0	CCIR data format
876	6C	sync_CCIR_00	0	00	00000000	RW	5	0	
877	6D	sync_CCIR_80	128	80	10000000	RW	5	0	
878	6E	sync_CCIR_10	16	10	00010000	RW	5	0	
879	6F	ccir656enc_ctrl1	128	80	10000000	RW	5	0	Ccir656 control for encoder
880	70	xscale_th_h	2	02	00000010	RW	5	0	Xscale horizontal scaling TH for encoder
881	71	xscale_th_l	208	D0	11010000	RW	5	0	
883	73	flicker_control1	u	u	uuuuuuuu	RW	5	0	Flicker control
884	74	auto_fd	0	00	00000000	RW	5	0	Auto flicker detection enable monitoring
885	75	fd_a_step_h	u	u	uuuuuuuu	RW	5	0	Flicker detection step for A state
886	76	fd_a_step_l	u	u	uuuuuuuu	RW	5	0	
887	77	fd_b_step_h	3	03	00000011	RW	5	0	Flicker detection step for B state
888	78	fd_b_step_l	u	u	uuuuuuuu	RW	5	0	
889	79	fd_winheight	64	40	01000000	RW	5	0	Flicker detection window height
890	7A	fd_a_delay	0	00	00000000	RW	5	0	Flicker detection delay for A state
891	7B	fd_b_delay	0	00	00000000	RW	5	0	Flicker detection delay for A state
892	7C	fd_th	16	10	00010000	RW	5	0	Flicker detection TH.
893	7D	fd_period_a_h	u	u	uuuuuuuu	RW	5	0	Flicker period for A state
894	7E	fd_period_a_m	u	u	uuuuuuuu	RW	5	0	
895	7F	fd_period_a_l	u	u	uuuuuuuu	RW	5	0	
896	80	fd_period_b_h	1	01	00000001	RW	5	0	Flicker period for B state
897	81	fd_period_b_m	u	u	uuuuuuuu	RW	5	0	
898	82	fd_period_b_l	u	u	uuuuuuuu	RW	5	0	
899	83	fd_period_c_h	u	u	uuuuuuuu	RW	5	0	Flicker period for 1/20 second
900	84	fd_period_c_m	u	u	uuuuuuuu	RW	5	0	

(Group D – continued)

1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

▶ Register Tables – Group D

GROUP D									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
901	85	fd_minfr	4	04	00000100	RW	5	0	Flicker TH. for 1/20 second
902	86	led_control1	0	00	00000000	RW	5	0	Led control
903	87	led_control2	0	00	00000000	RW	5	0	
904	88	led_lvth1	0	00	00000000	RW	5	0	Led control level th.1
905	89	led_lvth2	0	00	00000000	RW	5	0	Led control level th.2
906	8A	led_frame	128	80	10000000	RW	5	0	led frame control
907	8B	mirs_pw	100	64	01100100	RW	5	0	Mirs pulse width
908	8C	iris_pw	100	64	01100100	RW	5	0	Iris pulse width
909	8D	periedge_gain	0	00	00000000	RW	5	0	Peripheral edge gain
910	8E	periedge_x	0	00	00000000	RW	5	0	Peripheral edge center control
911	8F	periedge_y	0	00	00000000	RW	5	0	
912	90	periedge_scalex	81	51	01010001	RW	5	0	Peripheral edge scale control
913	91	periedge_scaley	81	51	01010001	RW	5	0	
914	92	spi_addr_update	0	00	00000000	RW	5	0	Spi address update control
916	94	y_min	0	00	00000000	RW	5	0	Control register for Output Y min
934	A6	spi_baud_rate	13	0D	00001101	RW	5	0	Spi baud rate
935	A7	osd_opac	16	10	00010000	RW	5	0	OSD opacity control
936	A8	spi_osd_control	u	u	uuuuuuuu	RW	5	0	[1]: osd boundary, [0]: osd enable
937	A9	spi_saddr_h	0	00	00000000	RW	5	0	osd rom data read start address (SPI Flash ROM)
938	AA	spi_saddr_m	0	00	00000000	RW	5	0	
939	AB	spi_saddr_l	0	00	00000000	RW	5	0	
940	AC	spi_paddr_h	0	00	00000000	RW	5	0	osd rom data read stop address (SPI Flash ROM)
941	AD	spi_paddr_m	0	00	00000000	RW	5	0	
942	AE	spi_paddr_l	0	00	00000000	RW	5	0	

(Group D – continued)

▶ Register Tables – Group D

GROUP D									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
967	C7	resol_gain	0	00	00000000	RW	5	0	
968	C8	enc_fcnt_genlock	1	01	00000001	RW	5	0	
969	C9	enc_rcnt_genlock_h	0	00	00000000	RW	5	0	
970	CA	enc_rcnt_genlock_l	1	01	00000001	RW	5	0	
971	CB	enc_ccnt_genlock_h	0	00	00000000	RW	5	0	
972	CC	enc_ccnt_genlock_l	3	03	00000011	RW	5	0	
973	CD	enc_control	4	04	00000100	RW	5	0	Encoder control
974	CE	enc_scfreq	u	u	uuuuuuuu	RW	5	0	Subcarrier frequency selection for which TV mode
975	CF	enc_sync	16	10	00010000	RW	5	0	Encoder sync level
976	D0	enc_blankH	0	00	00000000	RW	5	0	Encoder blank level
977	D1	enc_blankL	u	u	uuuuuuuu	RW	5	0	
978	D2	enc_pedestal	u	u	uuuuuuuu	RW	5	0	Encoder pedestal
979	D3	enc_burst	u	u	uuuuuuuu	RW	5	0	Burst amplitude
980	D4	enc_Ygain	u	u	uuuuuuuu	RW	5	0	Y convergence gain from YCbCr to YUV
981	D5	enc_Ugain	u	u	uuuuuuuu	RW	5	0	U convergence gain from YCbCr to YUV
982	D6	enc_Vgain	u	u	uuuuuuuu	RW	5	0	V convergence gain from YCbCr to YUV
983	D7	enc_Yrange_H	3	03	00000011	RW	5	0	max. luminance
984	D8	enc_Yrange_L	32	20	00100000	RW	5	0	
985	D9	enc_Crange_H	1	01	00000001	RW	5	0	max. amplitudes of chrominance
986	DA	enc_Crange_L	u	u	uuuuuuuu	RW	5	0	
987	DB	enc_chroma_max_H	3	03	00000011	RW	5	0	maximum chrominance of composite output
988	DC	enc_chroma_max_L	u	u	uuuuuuuu	RW	5	0	
989	DD	enc_chroma_min_H	0	00	00000000	RW	5	0	minmum chrominance of composite output
990	DE	enc_chroma_min_L	u	u	uuuuuuuu	RW	5	0	
1016	F8	enc_SCH_offset_T	0	00	00000000	RW	5	0	SCH(subcarrier to horizontal) phase offset
1017	F9	enc_SCH_offset_H	0	00	00000000	RW	5	0	
1018	FA	enc_SCH_offset_M	0	00	00000000	RW	5	0	
1019	FB	enc_SCH_offset_L	0	00	00000000	RW	5	0	
1020	FC	DAC_tp_period	0	00	00000000	RW	5	0	DAC test pattern period
1021	FD	burst_toffset	0	00	00000000	RW	5	0	Burst time +/- offset
1023	FF	resol_th	0	00	00000000	RW	5	0	resolution enhance threshold

(Group D – continued)

1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

▶ Register Tables : Group A

Register names are written in *slanted* characters. To differentiate between decimal, binary, and hexa numbers, (d, b, and h) are appended. The sensor should be reset by RSTB pin set low, after power is up, for at least 16 master clock periods. And then all read-write registers are initialized by internal ROM for about 3 ms. So we recommend you to write data to registers after initialization. This will initialize all of the registers to their default values. Default values of 'U' are wire-strapping registers.

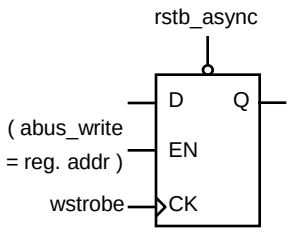
There are two register type.

1. Available Read Only (indicator is RO).
2. Available Read and Write (indicator is RW).

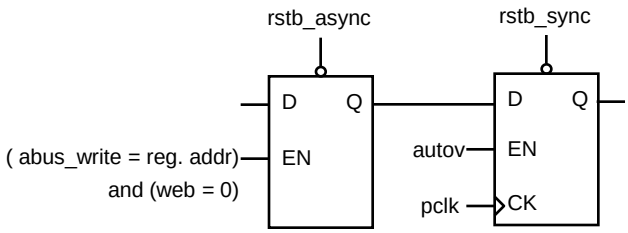
In addition, RW type register can be grouped by stage. There are 3 register stage.

1. 1 stage register (indicator is [5, 0]).
2. 2 stage register which is updated at auto vsync falling edge (indicator is [6, autov]).
3. 2 stage register which is updated at ae vsync falling edge (indicator is [6, aev]).
4. 2 stage register which is updated at ae vsync falling edge (indicator is [7, aev]) → this is 2 flip-flop structure.

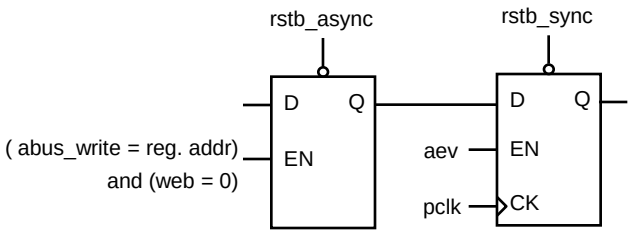
Below figure shows block diagram by register stage.



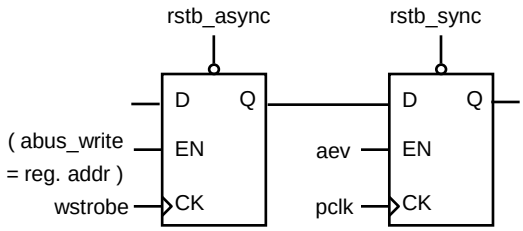
1. [1 stage register]



2. [2 stage register @ autov]



3. [2 stage register @ aev]



4. [2 stage register @ aev]

Where, abus_write means user input address by 2-wire serial interface. wstrobe and web is generated by SSCL pin. pclk means pixel clock for core. aev means ae vsync falling edge. autov means auto vsync falling edge. For more information of ae vsync and auto vsync, please refer to Reg. B-ACh~B1h.

(0~3) DeviceID, RevNumber, Register Selector

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
0	00	DeviceID_H	16	10	00010000	RO	0	0	Device ID
1	01	DeviceID_L	137	89	10001001	RO	0	0	
2	02	RevNumber	0	00	00000000	RO	0	0	Revision number
3	03	bank	0	00	xxxxxx00	RW	5	0	Register group selector

▷ DeviceID, RevNumber, Register Selector

Indicate PC1089K device ID, reversion number, Register Select.

Common registers of Group A(00h) / B(01h) / C(02h) / D(03h).

(4) Chip mode

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
4	04	chip_mode	U	UU	xxxxxxuu	RW	7	aev	chip mode selection(NTSC, PAL, VGA)

register name : chip_mdoe								
register #	bit#	name	default	**U**	default(h)	**UU**	default(b)	**xxxxxxuu**
04d (04h)	7	x	0	Reserved				
	6	x	0	Reserved				
	5	x	0	Reserved				
	4	x	0	Reserved				
	3	x	0	Reserved				
	2	x	0	Reserved				
	1	chip_mode	U	Chip mode selection 00b - NTSC, (M)PAL 01b - PAL else – VGA				
	0		U					

▷ chip_mode

default value : U ➔ wire-strapping register

Chip mode selection

The default value of this register is changed by wire-strapping.

After changed wire-strapping, the register can be set with other values through SCL and SDA.

< Group A >

(5) Mirror

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
5	05	mirror	U	UU	xxxxxxuu	RW	7	aev	Mirror

register name : mirror								
register #	bit#	name	default	**U**	default(h)	**UU**	default(b)	**xxxxxxuu**
05d (05h)	7	x	0	Reserved				
	6	x	0	Reserved				
	5	x	0	Reserved				
	4	x	0	Reserved				
	3	x	0	Reserved				
	2	x	0	Reserved				
	1	vm	U	vertical mirror ON/OFF				
	0	hm	U	horizontal mirror ON/OFF				

▷ ***vm/hm***

default value : U ➔ wire-strapping register

The default value of this register is changed by wire-strapping.

After changed wire-strapping, the register can be set with other values through SCL and SDA.

< Group A >

(6~11) FrameWidth, FrameHeight

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
6	06	framewidth_h	U	UU	uuuuuuuu	RW	7	aev	Framewidth
7	07	framewidth_l	U	UU	uuuuuuuu	RW	7	aev	
8	08	fd_fheight_a_h	2	02	00000010	RW	6	aev	Frameheight
9	09	fd_fheight_a_l	U	UU	uuuuuuuu	RW	7	aev	
10	0A	fd_fheight_b_h	2	02	00000010	RW	6	aev	
11	0B	fd_fheight_b_l	U	UU	uuuuuuuu	RW	7	aev	

▷ **FrameWidth, FrameHeight**

default value : U ➔ wire-strapping register

FrameWidth is the number of columns to be counted during one line time. FrameHeight is the number of rows. Column(Row) counter value is incremented 1 by 1 until it reaches FrameWidth(FrameHeight), then it is reset to 0. FrameHeight and FrameWidth determines the frame rate. Frame rate is given as follows.

Frame Rate = freq (PCLK) / ((FrameHeight +1) X (FrameWidth+1))

For example, If Pixel clock (PCLK) = 13.5MHz, FrameHeight = 857d and FrameWidth = 524d. then, the frame rate is 30 fps for 720x480 Mode. If you double the Frame Height , you cut the frame rate by half.

▶ fd_fheight_a : flicker A state frameheight
▶ fd_fheight_b : flicker B state frameheight

< Group A >

(12~19) Window

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
12	0C	windowx1_h	2	02	xxxxxx10	RW	6	aev	Window
13	0D	windowx1_l	128	80	10000000	RW	6	aev	
14	0E	windowy1_h	1	01	xxxxxx01	RW	6	aev	
15	0F	windowy1_l	1	E0	00000001	RW	6	aev	
16	10	windowx2_h	2	00	xxxxxx10	RW	6	aev	
17	11	windowx2_l	208	0A	11010000	RW	6	aev	
18	12	windowy2_h	U	UU	uuuuuuuu	RW	7	aev	
19	13	windowy2_l	U	UU	uuuuuuuu	RW	7	aev	

▷ Window

default value : U ➔ wire-strapping register

Window can be defined by 4 parameters : WindowX1, WindowY1, WindowX2, and WindowY2. Serial image data stream out pixel by pixel. Window specifies the area of pixels that we are interested in. Hsync signal indicates if the image data output is from a pixel that lies within the window area or not. Output data stream does not stop for pixels lying outside the window : just the Hsync signal is de-asserted.

The actual window position in the frame is given as

upper right corner = (Window X1 + 1, Window Y1)
lower left corner = (Window X2, Window Y2 - 1)

All the coordinates are with respect to the maximum window origin (0, 0) of <Fig. 3>. Window position and size are with respect to the full sampling mode. It is not necessary to change the window parameters when sampling mode is switched between one and another.

< Group A >

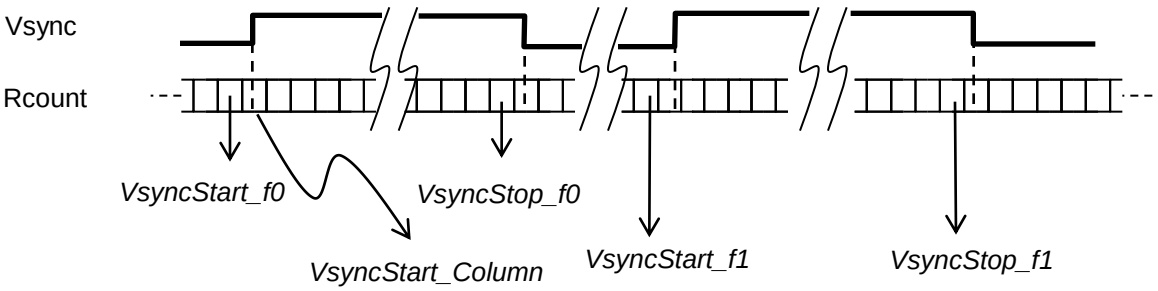
(20~29) Vsync Row Start/Stop, Vsync Column Start

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
20	14	vsyncstartrow_f0_h	0	00	00000000	RW	6	aev	Vsync generation
21	15	vsyncstartrow_f0_l	23	17	00010111	RW	6	aev	
22	16	vsyncstoprow_f0_h	1	01	00000001	RW	6	aev	
23	17	vsyncstoprow_f0_l	U	UU	uuuuuuuu	RW	7	aev	
24	18	vsyncstartrow_f1_h	1	01	00000001	RW	6	aev	
25	19	vsyncstartrow_f1_l	U	UU	uuuuuuuu	RW	7	aev	
26	1A	vsyncstoprow_f1_h	2	02	00000010	RW	6	aev	
27	1B	vsyncstoprow_f1_l	U	UU	uuuuuuuu	RW	7	aev	
28	1C	vsynccolumn_h	0	00	00000000	RW	5	0	
29	1D	vsynccolumn_l	2	02	00000010	RW	5	0	

▷ Output Vsync Generation

default value : U ➔ wire-strapping register

Output Vsync Row Start/Stop points and Column Start point



< Group A >

(31) i2c master enable

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
31	1F	i2c_master_en	1	01	xxxxxxx1	RW	5	0	I2c master enable

register name : i2c_master_en								
register #	bit#	name	default	**1**	default(h)	**01**	default(b)	**xxxxxxx1**
31d (1Fh)	7	x	0	Reserved				
	6	x	0	Reserved				
	5	x	0	Reserved				
	4	x	0	Reserved				
	3	x	0	Reserved				
	2	x	0	Reserved				
	1	x	0	Reserved				
	0	i2c_master_en	1	I2c master enable 0b : disable 1b : enable				

▷ ***i2c_master_en***

I2c_master initialize i2c-registers with internal or external ROM

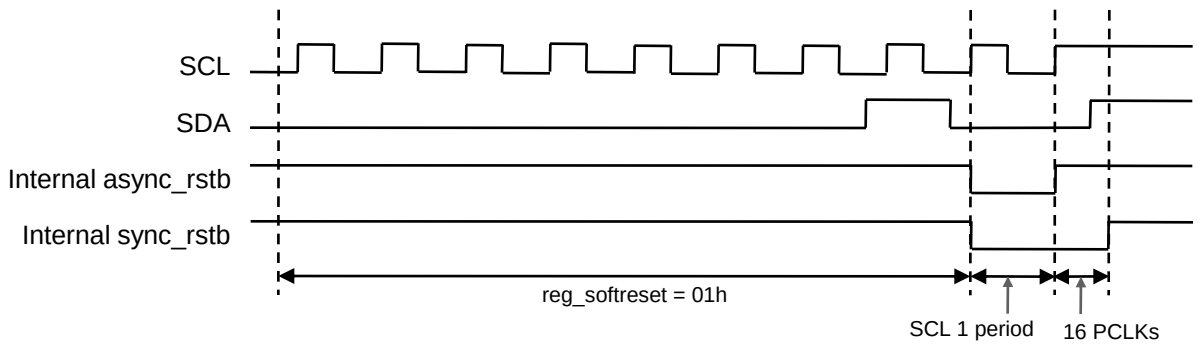
< Group A >

(36) Soft reset

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
36	24	softreset	0	00	xxxxxxx0	RW	5	0	Soft reset

▷ **softreset**

Soft reset bit is reg_softreset[0].



< Group A >

(37) Clock divider

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
37	25	clkdiv	7	07	xxxxx111	RW	6	aev	Clock divider

▷ **clock divider**

reg_clkdiv	PPCLK	PCLK
00h	MCLK	PPCLK x 1/2
01h	MCLK x 2/3	PPCLK x 1/2
02h	MCLK x 1/2	PPCLK x 1/2
03h	MCLK x 1/3	PPCLK x 1/2
04h	MCLK x 1/4	PPCLK x 1/2
05h	MCLK x 1/8	PPCLK x 1/2
else	MCLK	MCLK

(38) pclk/ppclk frequency equal mode selector

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
38	26	p_pp_equal	0	00	xxxxxxx0	RW	5	0	PCLK& PPCLK control

▷ **pclk/ppclk frequency equal mode**

< Group A >

(39) Pad_control1

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
39	27	pad_control1	102	66	01100110	RW	5	0	Pad control

register name : pad_control1								
register #	bit#	name	default	**102**	default(h)	**66**	default(b)	**01100110**
39d (27h)	7	stdby	0	Register stdby on/off 0b : normal mode, 1b : stdby mode,				
	6	x	1	Reserved				
	5	stdby_level	1	stdby data output pad level selector 1xb : hiz, 01b : high, 00b : low				
	4		0					
	3	clkoff	0	Clock kill control register 0b : not kill ,1b : clock Kill				
	2	osc_pad_en	1	osc(x1) pad enable				
	1	osc_pad_drv	1	osc(x1) pad drivability				
	0		0					

(40) Pad_control2

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
40	28	pad_control2	0	00	00000000	RW	5	0	Pad control

register name : pad_control2								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
40d (28h)	7	pad_drv	0	Left_TOP & Bottom pad drivability control register				
	6		0					
	5	pclk_drv	0	pclk drivability control				
	4		0					
	3	pclk_delay	0	pclk delay control				
	2		0					
	1		0					
	0	x	0	Reserved				

< Group A >

(41) Pad_control3

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
41	29	pad_control3	0	00	00000000	RW	5	0	Pad control

register name : pad_control3								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
41d (29h)	7	vsync_pad_en	0	Vsync pad enable 0b : disable ,1b : enable				
	6	hsync_drv	0	Hsync drivability control				
	5		0					
	4	hsync_pad_en	0	Hsync pad enable 0b : disable ,1b : enable				
	3	data_pad_en	0	Data pad enable 0b : disable ,1b : enable				
	2	motion_pad_en	0	Data0 pad enable bit 0b : disable, 1b : enable				
	1	d0 pad select	0	Data0 pad selection bit 0b : DO0, 1b : motion detection				
	0	x	0	reserved				

(42) Pad_control4

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
42	2A	pad_control4	0	00	00000000	RW	5	0	Pad control

register name : pad_control4								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
42d (2Ah)	7	ledctrl_en	0	IR LED control PAD enable 0b : disable ,1b : enable				
	6	ledctrl_pad_drv	0	IR LED control PAD drivability				
	5		0					
	4	x	0	Reserved				
	3	dac_test_mode	0	DAC test mode selection bits 0xxxb : DAC test mode disable 1000b : sign wave 1001b : sweep + 1010b : sweep - 1011b : triangle wave 11xxb : DAC DC Test				
	2		0					
	1		0					
	0		0					

< Group A >

(43) Pad_control5

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
43	2B	pad_control5	192	C0	11000000	RW	5	0	Pad control

register name : pad_control5								
register #	bit#	name	default	**192**	default(h)	**C0**	default(b)	**11000000**
43d (2Bh)	7	spi_pad_en	1	SPI output pad enable				
	6	spi_pad_ie	1	SPI input pad enable				
	5	spi_pad_drv	0	SPI PAD drivability control				
	4		0					
	3	geno_pad_en	0	genlock output pad enable				
	2	geno_pad_drv	0	genlock output pad drivability control				
	1		0					
	0	geni_en	0	genlock input pad enable				

(44) Pad_control6

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
44	2C	pad_control6	0	00	00000000	RW	5	0	Pad control

register name : pad_control6								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
44d (2Ch)	7	mirsctrl_en	0	MIRS output pad enable				
	6	mirsctrl_pad_drv	0	MIRS output pad drivability control				
	5		0					
	4	irisctrl_en	0	IRIS output pad enable				
	3	irisctrl_pad_drv	0	IRIS output pad drivability control				
	2		0					
	1	x	0	reserved				
	0	x	0	reserved				

< Group A >

(45) Strap_control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
45	2D	strap_control	255	FF	11111111	RW	5	0	Strap control

register name : strap_control								
register #	bit#	name	default	**255**	default(h)	**FF**	default(b)	**11111111**
45d (2Dh)	7	x	1	Reserved				
	6	Strap master	1	I2C master enable('1')/disable('0')				
	5	x	1	Reserved				
	4	Strap in/out door	1	Indoor / Outdoor select				
	3	Strap BLC	1	Back Light Compensation ON('1')/OFF('0')				
	2	Strap flicker	1	Flicker cancellation strap ON('1')/OFF('0')				
	1	Strap TV mode	1	TV mode strap enable ('1')/disable('0')				
	0	Strap Mirror	1	Horizontal & Vertical Mirror strap enable('1')/disable('0')				

< Group A >

(73) Bayer control 01

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
73	49	bayer_control_01	5	05	00000101	RW	5	0	Bayer control

register name : bayer_control_01								
register #	bit#	name	default	**5**	default(h)	**05**	default(b)	**00000101**
73d (49h)	7	mode_evenframe	0	Even frame indicator reverse on('1')/off('0')				
	6	frmvar_en	0	Variable Frame rate mode 0b : disable 1b : enable				
	5	genlock_en	0	External Frame Sync enable '0' : disable (default) '1' : enable				
	4	genlock_master	0	External Frame Sync master/slave selection 0b : slave (default) 1b : master				
	3	genlock_mode	0	Genlock syncin rising/falling edge detection bit				
	2		1					
	1	led_dsel	0	LED data selection (for 8bit)				
	0		1					

< Group A >

▶ Register Tables (Detailed) : Group B

(260) ISP function control 0

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
260	04	isp_func_0	247	F7	11110111	RW	6	aev	Isp function control

register name : isp_func_0								
register #	bit#	name	default	**247**	default(h)	**F7**	default(b)	**11110111**
260d (04h)	7	lens_en	1	lens shading compensation 0b : disable, 1b : enable				
	6	awb_en	1	white balance 0 b: disable, 1b : enable				
	5	Reserved	1	Should be fixed '1'				
	4	Reserved	1	Should be fixed '1'				
	3	Reserved	0	Should be fixed '0'				
	2	moire	1	moire suppression 0b : disable, 1b : enable				
	1	ccr_en	1	color correction 0b : disable, 1b : enable				
	0	Reserved	1	Should be fixed '1'				

(261) ISP function control 1

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
261	05	isp_func_1	255	FF	11111111	RW	6	aev	Isp function control

register name : isp_func_1								
register #	bit#	name	default	**251**	default(h)	**FB**	default(b)	**11111011**
261d (05h)	7	RGBgm_en	1	RGB gamma correction 0b : disable, 1b : enable				
	6	Ygm_en	1	Y gamma correction 0b : disable, 1b : enable				
	5	blf_en	1	noise reduction filter 0b : disable, 1b : enable				
	4	blf_mode	1	noise reduction filter mode 0b : noise reduction filter off 1b : noise reduction filter on				
	3	edge_en	1	edge enhancement 0b : disable, 1b : enable				
	2	edge_flat	1	flat edge selection 0b : disable, 1b : enable				
	1	Reserved	1	Should be fixed ‘11’				
	0		1					

< Group B >

(262) ISP function control 2

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
262	06	isp_func_2	0	00	00000000	RW	6	aev	Isp function control

register name : isp_func_2								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
262d (06h)	7	reverse	0	image reverse 0b : disable, 1b : enable				
	6	emboss_en	0	embossing effect enable 0b : disable, 1b: enable				
	5	emboss_mode	0	embossing effect mode selection 0b : disable, 1b : enable				
	4	sketch_en	0	sketch effect enable 0b : disable, 1b : enable				
	3	black&white	0	black&white effect enable 0b : disable, 1b : enable				
	2	md_sleep	0	motion detection sleep 0b : disable, 1b : enable				
	1	md_alarm	0	motion detection alarm on screen 0b : disable, 1b : enable				
	0	md_alarm_mode	0	motion detection alarm mode selection 0b : disable, 1b : enable				

< Group B >

(264) ISP function control 4

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
264	08	isp_func_4	0	00	00000000	RW	6	aev	Isp function control

register name : isp_func_4								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
264d (08h)	7	win_show	0	AE window show enable 0b : disable, 1b : enable				
	6		0	AWB window show enable 0b : disable, 1b : enable				
	5	sample_show	0	AWB good sample show enable 0b : disable, 1b : enable				
	4	Reserved	0	Should be fixed '0'				
	3	prvc_en	0	privacy window enable 0b : disable, 1b : enable				
	2	af_win_show	0	AF window show enable 0b : disable, 1b : enable				
	1	x	0	Reserved				
	0	Reserved	0	Should be fixed '0'				

< Group B >

(265) ISP function control 5

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
265	09	isp_func_5	0	00	00000000	RW	6	aev	Isp function control

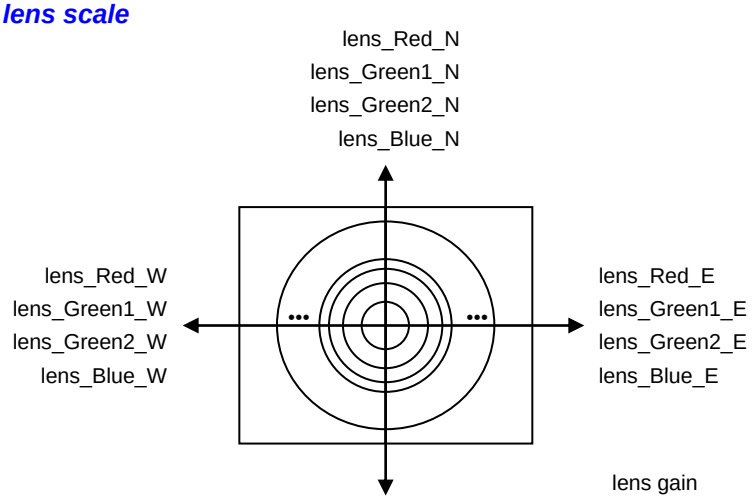
register name : isp_func_4								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
265d (09h)	7	Peri. edge_en	0	peripheral edge enhance enable 0b: disable, 1b : enable				
	6	yrange	0	yrange selection 0 b: 0~255 (reference 8bit output) 1b : 16~235 (reference 8bit output)				
	5	reserved	0	Should be fixed '0'				
	4	reserved	0	Should be fixed '0'				
	3	reserved	0	Should be fixed '0'				
	2	x	0	reserved				
	1	x	0	reserved				
	0	x	0	reserved				

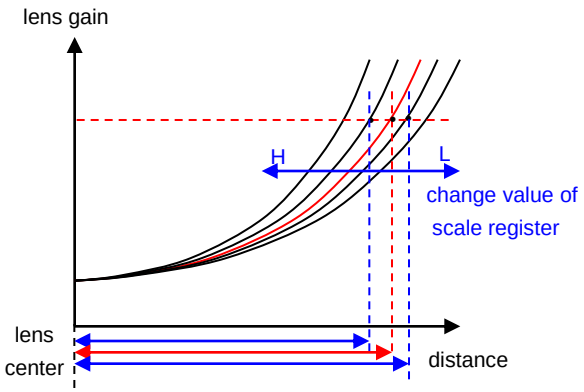
< Group B >

(268~283) Scale of lens shading compensation

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
268	0C	lens_red_e	81	51	01010001	RW	5	0	Lens shading compensation scale control
269	0D	lens_red_w	81	51	01010001	RW	5	0	
270	0E	lens_red_n	81	51	01010001	RW	5	0	
271	0F	lens_red_s	81	51	01010001	RW	5	0	
272	10	lens_g1_e	81	51	01010001	RW	5	0	
273	11	lens_g1_w	81	51	01010001	RW	5	0	
274	12	lens_g1_n	81	51	01010001	RW	5	0	
275	13	lens_g1_s	81	51	01010001	RW	5	0	
276	14	lens_g2_e	81	51	01010001	RW	5	0	
277	15	lens_g2_w	81	51	01010001	RW	5	0	
278	16	lens_g2_n	81	51	01010001	RW	5	0	
279	17	lens_g2_s	81	51	01010001	RW	5	0	
280	18	lens_blu_e	81	51	01010001	RW	5	0	
281	19	lens_blu_w	81	51	01010001	RW	5	0	
282	1A	lens_blu_n	81	51	01010001	RW	5	0	
283	1B	lens_blu_s	81	51	01010001	RW	5	0	

▷ **lens scale**





< Group B >

(284~287) Lens gain

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
284	1C	lens_gainr	0	00	00000000	RW	6	aev	Lens shading compensation R gain
285	1D	lens_gaing1	0	00	00000000	RW	6	aev	Lens shading compensation G1 gain
286	1E	lens_gaing2	0	00	00000000	RW	6	aev	Lens shading compensation G2 gain
287	1F	lens_gainb	0	00	00000000	RW	6	aev	Lens shading compensation B gain

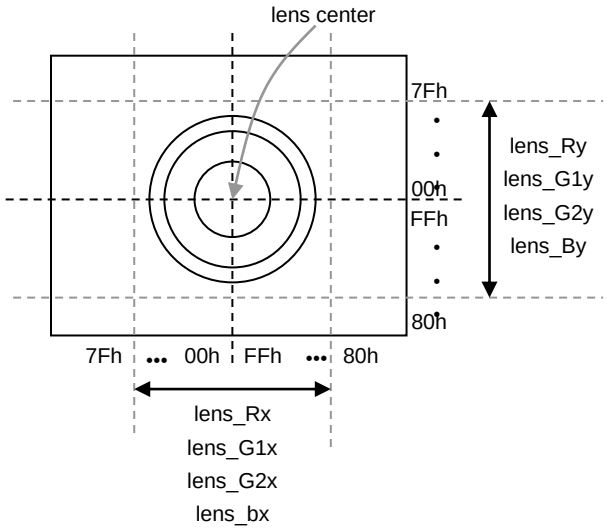
▷ **lens gain**

Lens Shading Gain : 0x20 = x 1 gain.

(288~295) Center control of lens shading compensation

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
288	20	lens_rx	0	00	00000000	RW	5	0	Lens shading compensation center control
289	21	lens_ry	0	00	00000000	RW	5	0	
290	22	lens_g1x	0	00	00000000	RW	5	0	
291	23	lens_g1y	0	00	00000000	RW	5	0	
292	24	lens_g2x	0	00	00000000	RW	5	0	
293	25	lens_g2y	0	00	00000000	RW	5	0	
294	26	lens_bx	0	00	00000000	RW	5	0	
295	27	lens_by	0	00	00000000	RW	5	0	

▷ **lens shading center control**



< Group B >

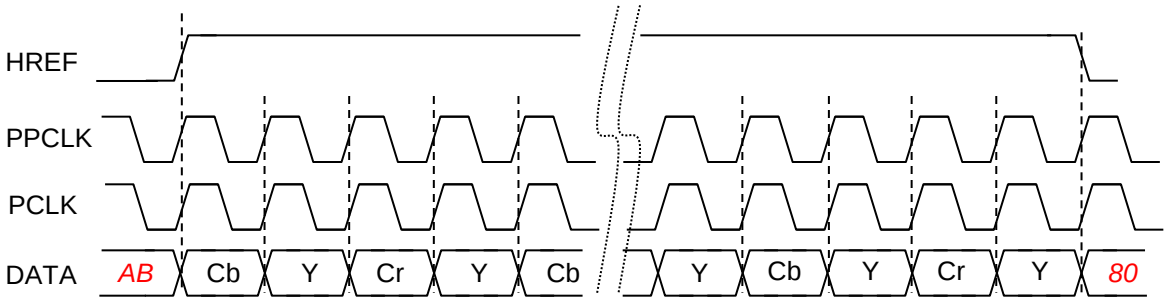
(297) Format

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
297	29	format	0	00	00000000	RW	6	aev	Format control

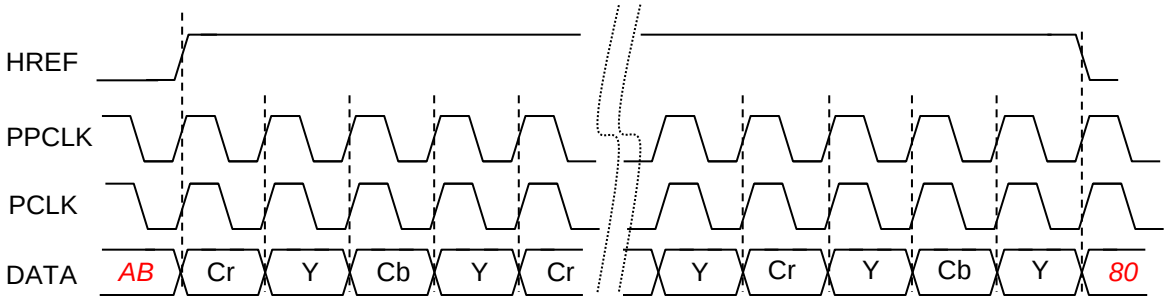
register name : format								
register #	bit#	name	default	**13**	default(h)	**0D**	default(b)	**00001101**
297d (29h)	7	format_control	0	00h : cbycry 01h : crycby 02h : ycbycr 03h : ycrycb 10h : rggb 11h : gbrg 12h : grbg 13h : bggr 30h : rgb565 31h : rgb565 (byte swap) 32h : bgr565 33h : bgr565 (byte swap) 36h : rgb444 37h : rgb444 (byte swap) 41h : bayer 43h : mono sensor only. (no interpolation) 44h : yyyy				
	6		0					
	5		0					
	4		0					
	3		0					
	2		0					
	1		0					
	0		0					

▷ Output timing diagrams for format register (1/4)

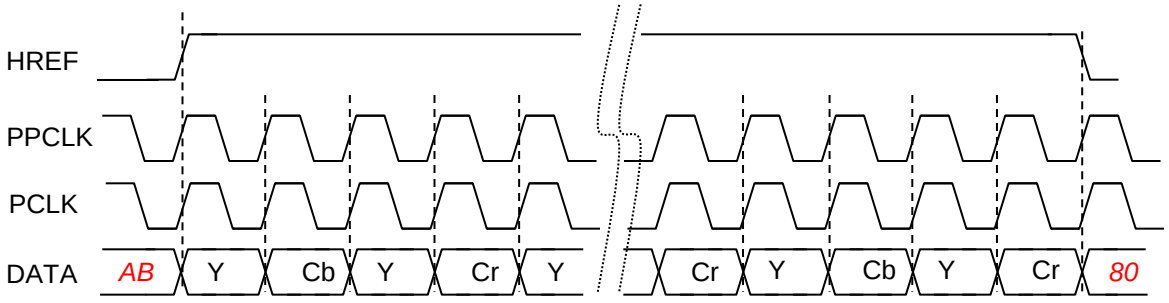
When format is 00h (Cb, Y, Cr, Y …),



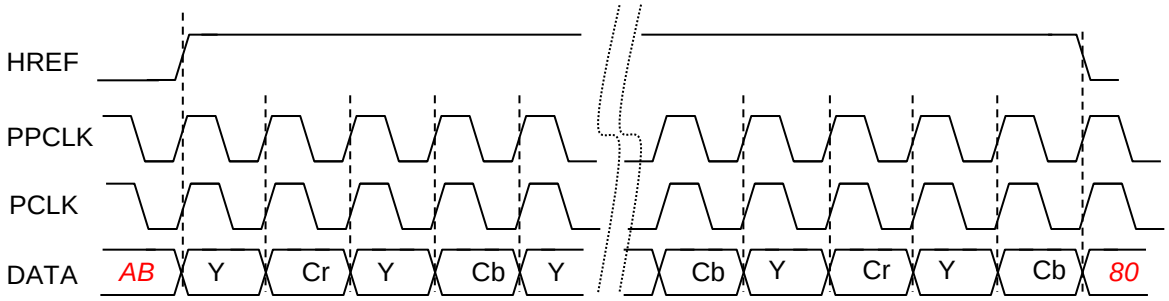
When format is 01h (Cr, Y, Cb, Y, …),



When format is 02h (Y, Cb, Y, Cr, …),



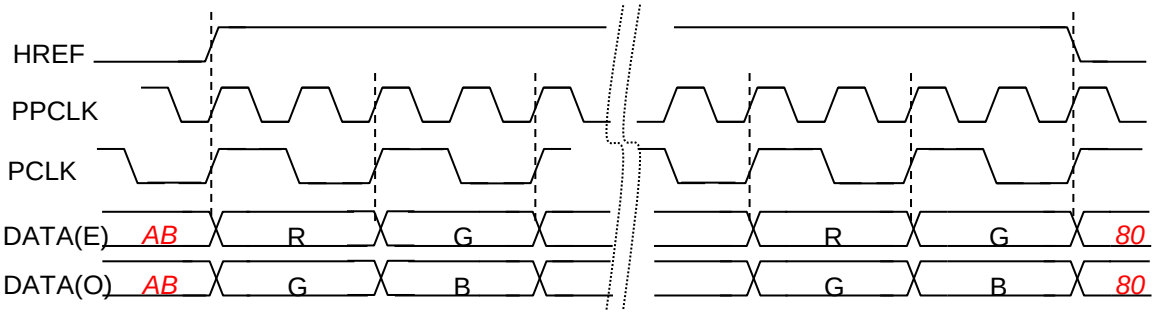
When format is 03h (Y, Cr, Y, Cb, …),



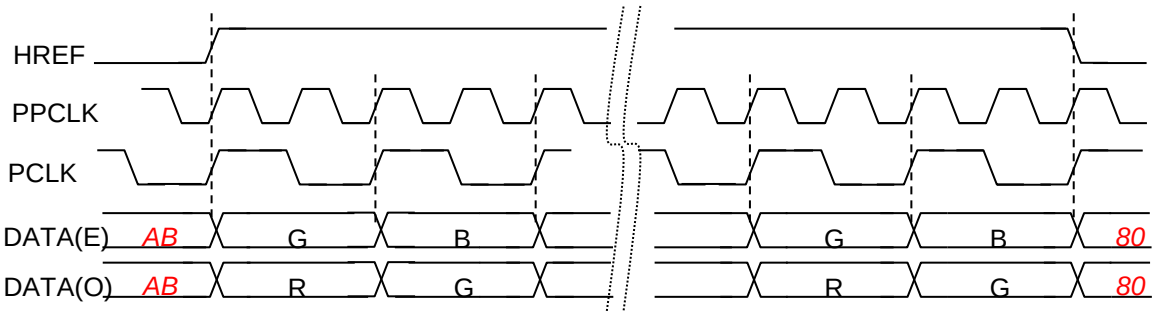
< Group B >

▷ Output timing diagrams for format register (2/4)

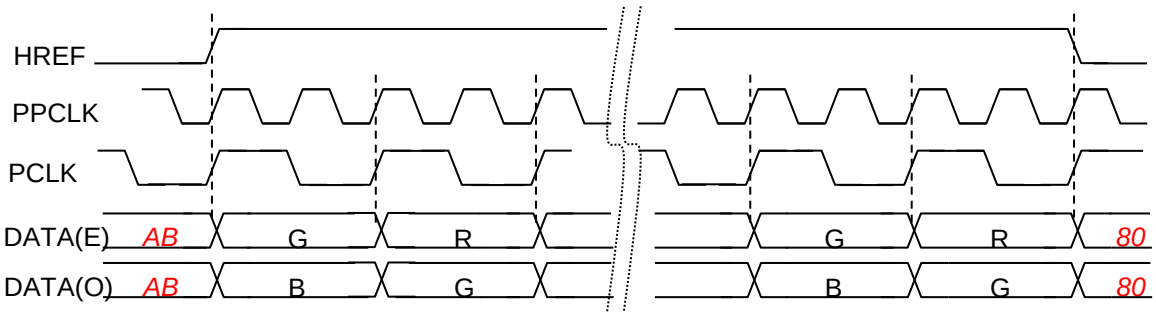
When format is 10h (ISP bayer, RGRG, GBGB, …),



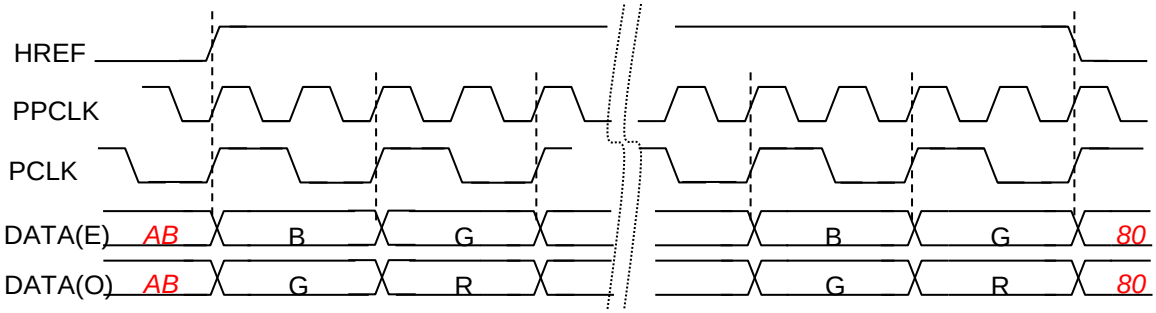
When format is 11h (ISP bayer, GBGB, RGRG, …),



When format is 12h (ISP bayer, GRGR, BGBG, …),



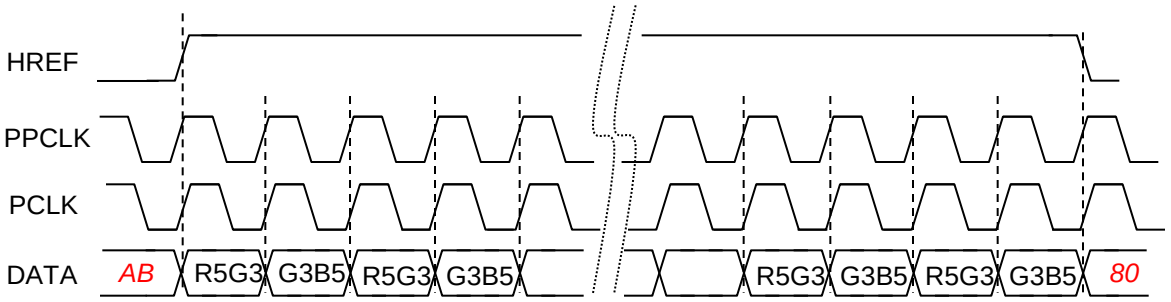
When format is 13h (ISP bayer, BGBG, GRGR, …),



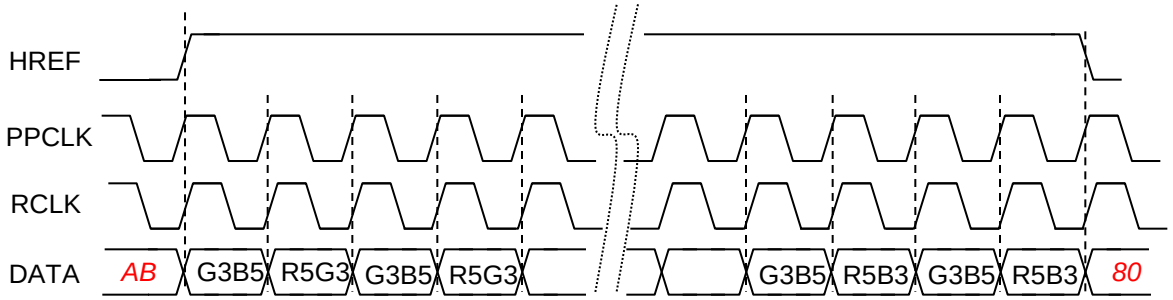
< Group B >

▷ Output timing diagrams for format register (3/4)

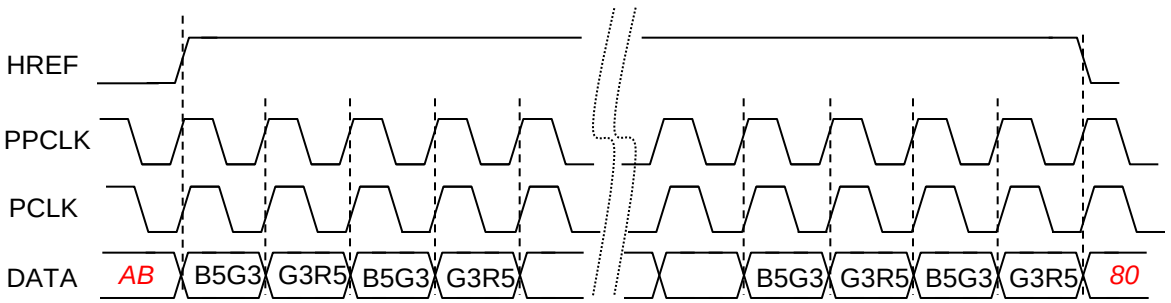
When format is 30h(R5G3, G3B5, …),



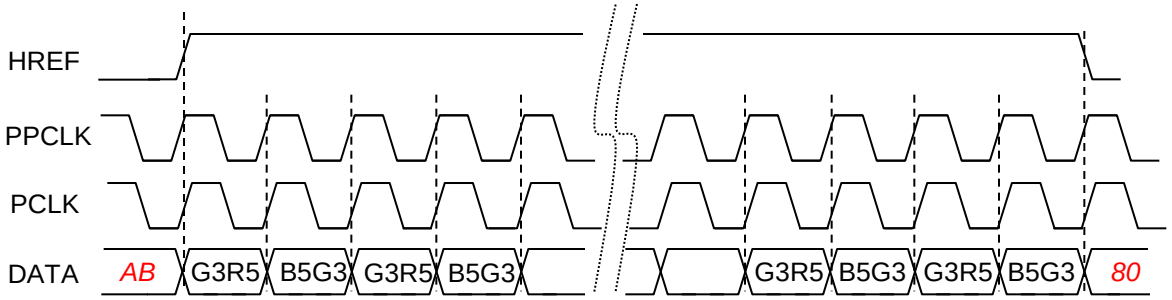
When format is 31h(G3B5, R5B3, …),



When format is 32h(B5G3, G3R5, …),



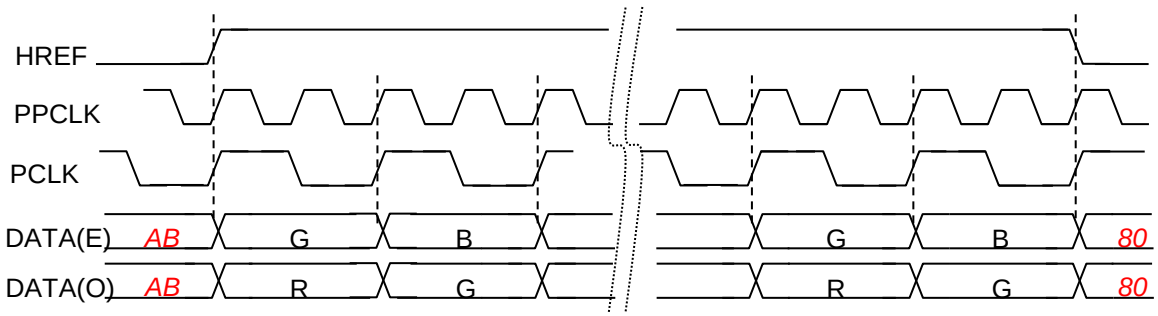
When format is 33h(G3R5, B5G3, …),



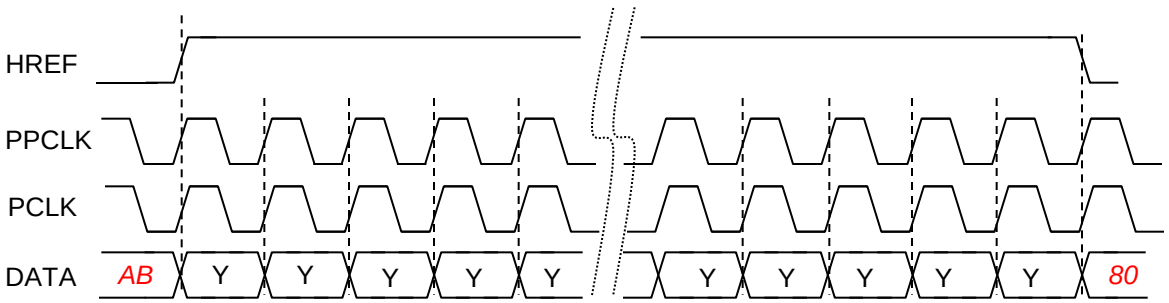
< Group B >

▷ Output timing diagrams for format register (4/4)

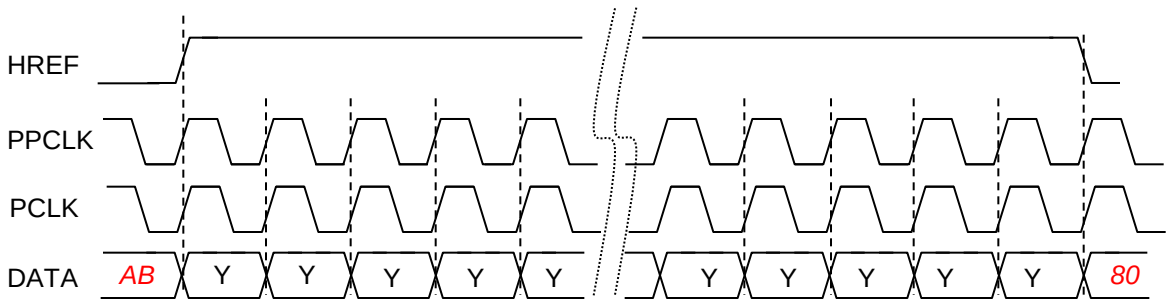
When format is 41h (Bayer),



When format is 43h(for mono sensor),



When format is 44h(only Y),



< Group B >

(303~305) Edge control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
303	2F	edge_gain	32	20	00100000	RW	5	0	Edge gain
304	30	ec_pgain	48	30	00110000	RW	5	0	Positive max edge clamp gain
305	31	ec_mgain	56	38	00111000	RW	5	0	Negative max edge clamp gain

▷ **edge gain**

Edge gain factor

▷ **ec_pgain/ec_mgain**

Edge max clamping gain factor

(307~315) Color correction matrix

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
307	33	ccr_m11	51	33	00110011	RW	5	0	Color correction matrix value
308	34	ccr_m12	139	8B	10001011	RW	5	0	
309	35	ccr_m13	136	88	10001000	RW	5	0	
310	36	ccr_m21	134	86	10000110	RW	5	0	
311	37	ccr_m22	49	31	00110001	RW	5	0	
312	38	ccr_m23	138	8A	10001010	RW	5	0	
313	39	ccr_m31	131	83	10000011	RW	5	0	
314	3A	ccr_m32	143	8F	10001111	RW	5	0	
315	3B	ccr_m33	50	32	00110010	RW	5	0	

▷ **color correction matrix**

The color specifications of the image sensor differ from the fabrication process like color filter. Due to the spectral characteristics of the optics, the native RGB data may not provide a faithful color rendition.

$$\begin{pmatrix} R' \\ G' \\ B' \end{pmatrix} = \begin{pmatrix} ccr\_m11 & ccr\_m12 & ccr\_m13 \\ ccr\_m21 & ccr\_m22 & ccr\_m23 \\ ccr\_m31 & ccr\_m32 & ccr\_m33 \end{pmatrix} \begin{pmatrix} R \\ G \\ B \end{pmatrix}$$

< Group B >

(317~331) Y Gamma1

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
317	3D	ygm1_y0	0	00	00000000	RW	5	0	Y gamma1 coefficient
318	3E	ygm1_y1	3	03	00000011	RW	5	0	
319	3F	ygm1_y2	12	0C	00001100	RW	5	0	
320	40	ygm1_y3	25	19	00011001	RW	5	0	
321	41	ygm1_y4	38	26	00100110	RW	5	0	
322	42	ygm1_y5	63	3F	00111111	RW	5	0	
323	43	ygm1_y6	82	52	01010010	RW	5	0	
324	44	ygm1_y7	110	6E	01101110	RW	5	0	
325	45	ygm1_y8	130	82	10000010	RW	5	0	
326	46	ygm1_y9	161	A1	10100001	RW	5	0	
327	47	ygm1_y10	185	B9	10111001	RW	5	0	
328	48	ygm1_y11	206	CE	11001110	RW	5	0	
329	49	ygm1_y12	224	E0	11100000	RW	5	0	
330	4A	ygm1_y13	240	F0	11110000	RW	5	0	
331	4B	ygm1_y14	255	FF	11111111	RW	5	0	

▷ Y gamma1 coefficient

Y Gamma1 Correction is applied to luminance signal which ranges from 0 to 255 to compensate non-linear characteristics of display brightness vs input brightness. In many cases, power function of 0.45 is used as gamma function for CRT display.

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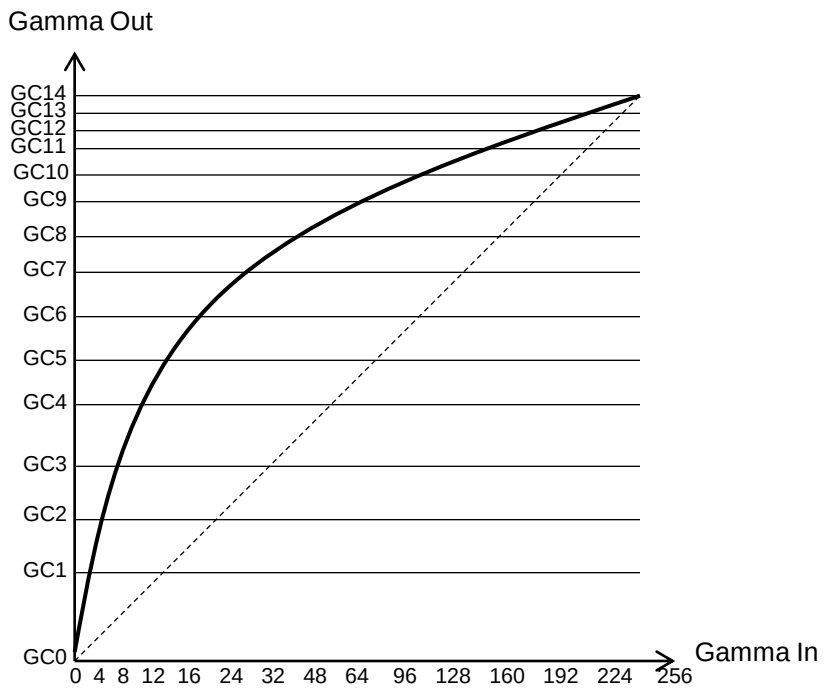


GC : Gamma coefficient

< Group B >

(332~346) Y Gamma2

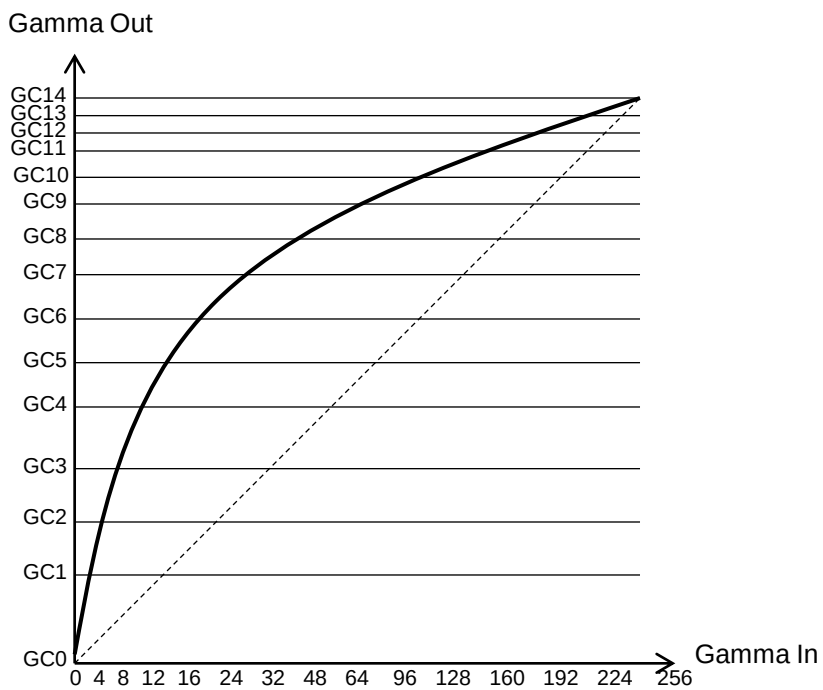
address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
332	4C	ygm2_y0	0	00	00000000	RW	5	0	Y gamma2 coefficient
333	4D	ygm2_y1	11	0B	00001011	RW	5	0	
334	4E	ygm2_y2	23	17	00010111	RW	5	0	
335	4F	ygm2_y3	34	22	00100010	RW	5	0	
336	50	ygm2_y4	46	2E	00101110	RW	5	0	
337	51	ygm2_y5	64	40	01000000	RW	5	0	
338	52	ygm2_y6	80	50	01010000	RW	5	0	
339	53	ygm2_y7	110	6E	01101110	RW	5	0	
340	54	ygm2_y8	136	88	10001000	RW	5	0	
341	55	ygm2_y9	174	AE	10101110	RW	5	0	
342	56	ygm2_y10	202	CA	11001010	RW	5	0	
343	57	ygm2_y11	220	DC	11011100	RW	5	0	
344	58	ygm2_y12	236	EC	11101100	RW	5	0	
345	59	ygm2_y13	246	F6	11110110	RW	5	0	
346	5A	ygm2_y14	255	FF	11111111	RW	5	0	

▷ Y gamma2 coefficient

Y Gamma2 Correction is applied to luminance signal which ranges from 0 to 255 to compensate non-linear characteristics of display brightness vs input brightness. In many cases, power function of 0.45 is used as gamma function for CRT display.

→ Difference of Y Gamma1 and Y Gamma2 was selected by exposure. When exposure's value is increasingly high, Y Output data is affected by the Y Gamma2.

.



GC : Gamma coefficient

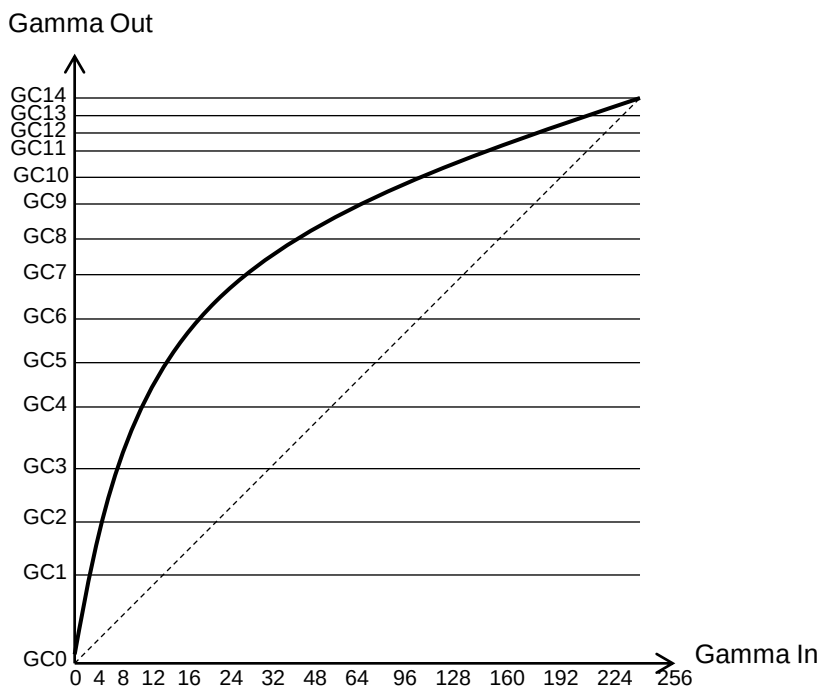
< Group B >

(347~361) RGB Gamma1

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
347	5B	cgm1_y0	0	00	00000000	RW	5	0	RGB gamma1 coefficient
348	5C	cgm1_y1	11	0B	00001011	RW	5	0	
349	5D	cgm1_y2	23	17	00010111	RW	5	0	
350	5E	cgm1_y3	34	22	00100010	RW	5	0	
351	5F	cgm1_y4	46	2E	00101110	RW	5	0	
352	60	cgm1_y5	64	40	01000000	RW	5	0	
353	61	cgm1_y6	80	50	01010000	RW	5	0	
354	62	cgm1_y7	110	6E	01101110	RW	5	0	
355	63	cgm1_y8	136	88	10001000	RW	5	0	
356	64	cgm1_y9	174	AE	10101110	RW	5	0	
357	65	cgm1_y10	202	CA	11001010	RW	5	0	
358	66	cgm1_y11	220	DC	11011100	RW	5	0	
359	67	cgm1_y12	236	EC	11101100	RW	5	0	
360	68	cgm1_y13	246	F6	11110110	RW	5	0	
361	69	cgm1_y14	255	FF	11111111	RW	5	0	

▷ RGB gamma1 coefficient

RGB Gamma1 Correction is applied to chrominance signal which ranges from 0 to 255 to compensate non-linear characteristics of display color vs input color.



GC : Gamma coefficient

< Group B >

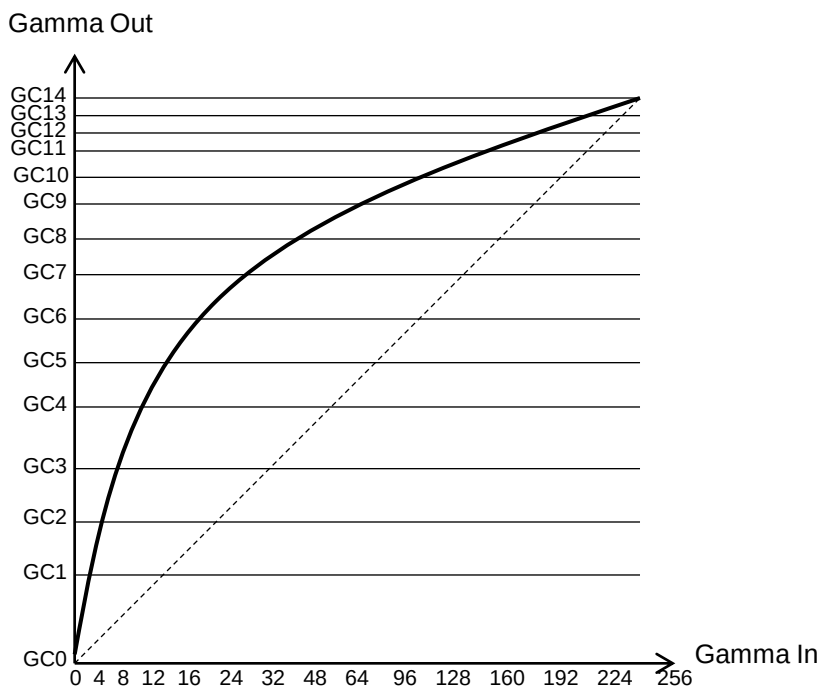
(362~376) RGB Gamma2

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
362	6A	cgm2_y0	0	00	00000000	RW	5	0	RGB gamma2 coefficient
363	6B	cgm2_y1	11	0B	00001011	RW	5	0	
364	6C	cgm2_y2	23	17	00010111	RW	5	0	
365	6D	cgm2_y3	34	22	00100010	RW	5	0	
366	6E	cgm2_y4	46	2E	00101110	RW	5	0	
367	6F	cgm2_y5	64	40	01000000	RW	5	0	
368	70	cgm2_y6	80	50	01010000	RW	5	0	
369	71	cgm2_y7	110	6E	01101110	RW	5	0	
370	72	cgm2_y8	136	88	10001000	RW	5	0	
371	73	cgm2_y9	174	AE	10101110	RW	5	0	
372	74	cgm2_y10	202	CA	11001010	RW	5	0	
373	75	cgm2_y11	220	DC	11011100	RW	5	0	
374	76	cgm2_y12	236	EC	11101100	RW	5	0	
375	77	cgm2_y13	246	F6	11110110	RW	5	0	
376	78	cgm2_y14	255	FF	11111111	RW	5	0	

▷ RGB gamma2 coefficient

RGB Gamma2 Correction is applied to chrominance signal which ranges from 0 to 255 to compensate non-linear characteristics of display color vs input color.

→ Difference of RGB Gamma1 and RGB Gamma2 was selected by exposure. When exposure's value is increasingly high, RGB Output data is affected by the Y Gamma2.



GC : Gamma coefficient

< Group B >

(378) Sketch offset

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
378	7A	sketch_offset	140	8C	10001100	RW	6	aev	Sketch offset

▷ **sketch offset**

Sketch offset is applied to chrominance signal which ranges from 0 to 255.

(379~382) Scale control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
379	7B	scale_x	32	20	00100000	RW	6	aev	Horizontal scale factor
380	7C	scale_y	U	UU	uuuuuuuu	RW	7	aev	Vertical scale factor
381	7D	scale_th_h	0	00	xxxxx000	RW	6	aev	Scale buffer TH
382	7E	scale_th_l	10	0A	00001010	RW	6	aev	

▷ **scale control**

scale_x : Horizontal scale factor, 20h = x1

scale_y : Vertical scale factor , 20h = x1

scale_th_h/l : Scale buffer size control register.

default value : U ➔ wire-strapping register

(383) Bw_th

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
383	7F	bw_th	128	80	10000000	RW	5	0	Black&white TH

▷ **bw_th**

Black & White output threshold control register. (Special Effect)

< Group B >

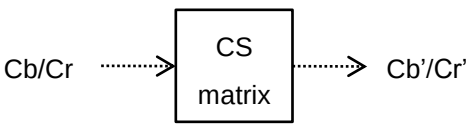
(384~387) Color saturation

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
384	80	cs11	37	25	00100101	RW	6	aev	Color saturation matrix value
385	81	cs12	0	00	00000000	RW	6	aev	
386	82	cs21	0	00	00000000	RW	6	aev	
387	83	cs22	37	25	00100101	RW	6	aev	

▷ **CS11/12/21/22**

Color Saturation matrix control register

$$\begin{bmatrix} Cb' \\ Cr' \end{bmatrix} = \begin{bmatrix} Cs11 & Cs12 \\ Cs21 & Cs22 \end{bmatrix} \begin{bmatrix} Cb \\ Cr \end{bmatrix}$$



(392~394) Cb/Cr_offset and C_max

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
392	88	cb_offset	128	80	10000000	RW	6	aev	Cb offset
393	89	cr_offset	128	80	10000000	RW	6	aev	Cr offset
394	8A	c_max	127	7F	01111111	RW	6	aev	Cb/Cr max

▷ Cb/Cr offset

Cb/Cr color offset control register.

- ▶ Cb` = Cb ± reg_cb_offset
- ▶ Cr` = Cr ± reg_cr_offset

▷ C_max

Max. color clamping control register.

(401~408) Dark_ycontrast and Dark_ybrightness

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
401	91	ycontrast_ref0	64	40	01000000	RW	5	0	Dark Y contrast fitting control
402	92	ycontrast_ref1	64	40	01000000	RW	5	0	
403	93	ycontrast_ref2	64	40	01000000	RW	5	0	
404	94	ycontrast	64	40	01000000	RW	6	aev	
405	95	ybrightness_ref0	0	00	00000000	RW	5	0	Dark Y brightness fitting control
406	96	ybrightness_ref1	0	00	00000000	RW	5	0	
407	97	ybrightness_ref2	0	00	00000000	RW	5	0	
408	98	ybrightness	0	00	00000000	RW	6	aev	

▷ ***dark_ycontrast & dark_ybrightness***

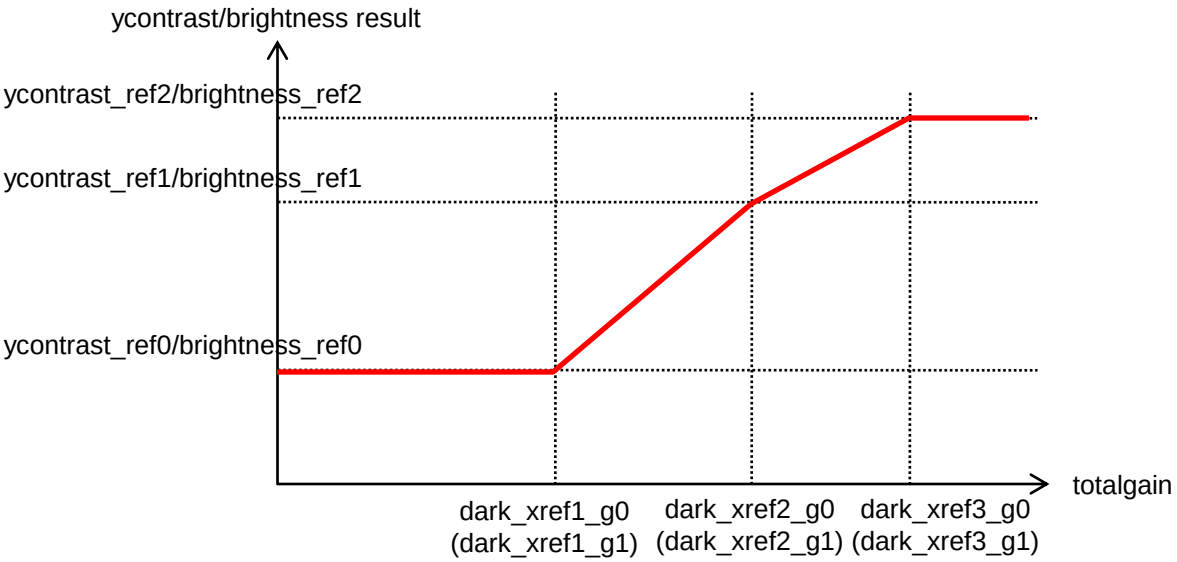
Ycontrast & Ybrightness darkness control registers.

When auto_control3[3] = '0b', then user can program ycontrast/ybrightness manually.

Also, user can change ycontrast/ybrightness with auto_control6[7,6](ycontrast/ybrightness group selection).

★ ***ycontrast/ybrightness conditions*** are given as

00h ≤ ycontrast_ref0/brightness_ref0 ≤ ycontrast_ref1/brightness_ref1 ≤ ycontrast_ref2/brightness_ref2 ≤ FFh



< Group B >

(410) Sync control 0

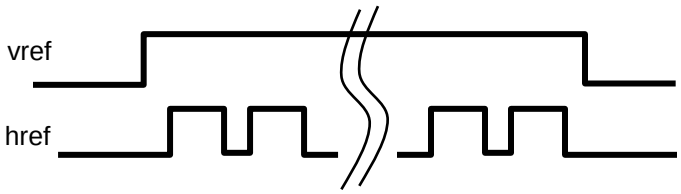
address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
410	9A	sync_control_0	128	80	10000000	RW	6	aev	Sync control

register name : sync_control_0								
register #	bit#	name	default	**128**	default(h)	**80**	default(b)	**10000000**
410d (9Ah)	7	x	1	Reserved				
	6	sync_drop	0	0 : disable 1 : hsync drop		2 : vsync drop 3 : hsync and vsync drop		
	5		0					
	4	sync_pclkrate	0	pclk rate				
	3		0					
	2		0					
	1		0					
	0		0					

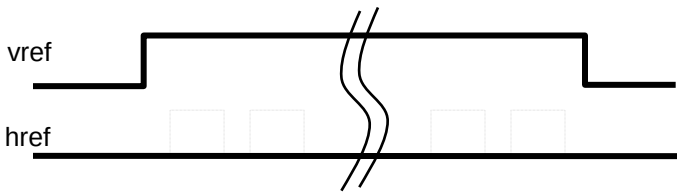
▷ ***Sync_drop***

Output H/V sync drop enable/disable control register.

▶ case 1 : sync_drop = “00” (normal)

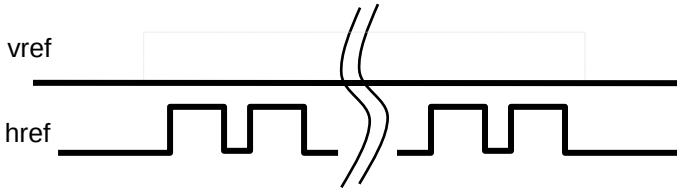


▶ case 2 : sync_drop = “01” (hsync drop)

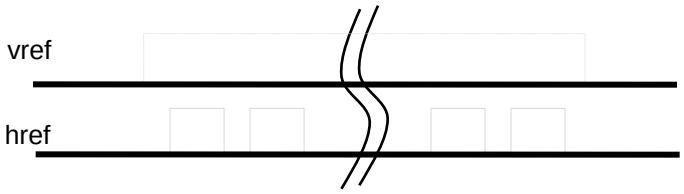


< Group B >

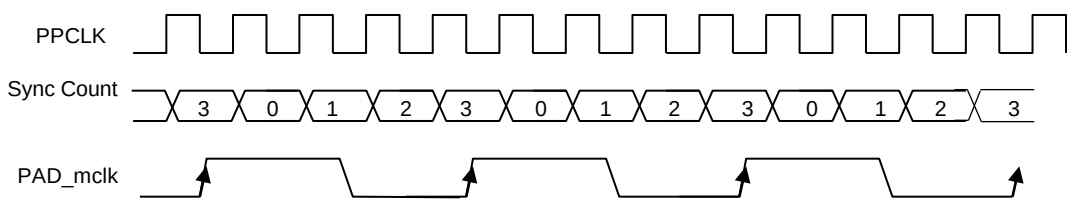
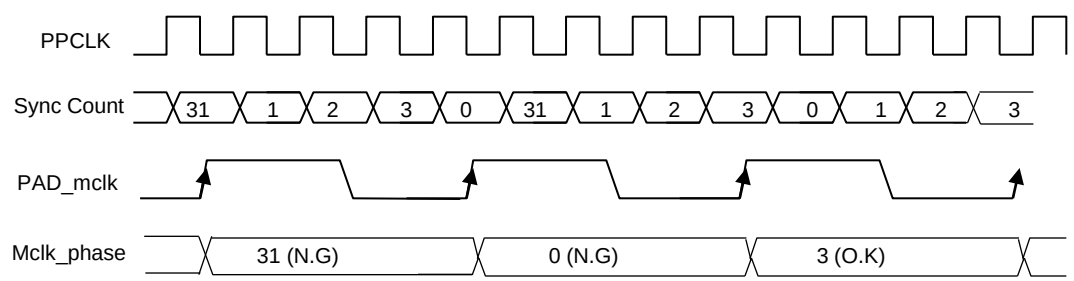
▶ case 3 : sync_drop = “10” (vsync drop)



▶ case 4 : sync_drop = “11” (hsync & vsync drop)



▷ PCLK rate

pclkrate	output pclk
0	ppclk
else	❖ mclkpahse_en= ‘0’ @ pclkrate = 3  ❖ mclkpahse_en = ‘1’ @ pclkrate = 3 

< Group B >

(411) Sync control 1

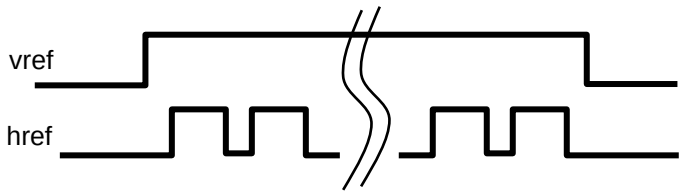
address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
411	9B	sync_control_1	0	00	00000000	RW	6	aev	Sync control

register name : sync_control_1								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
411d (9Bh)	7	x	0	Reserved				
	6	sync_vsyncPolarity	0	vsync polarity change				
	5	sync_hsyncAllLines	0	hsync output all lines enable(black and active)				
	4	sync_hsyncPolarity	0	hsync polarity change				
	3	sync_pclkwindow	0	pclk window				
	2	sync_pclkPolarity	0	pclk polarity change				
	1	bt601	0	output data 00h/FFh output enable				
	0	blkmask	0	blank period data masking enable				

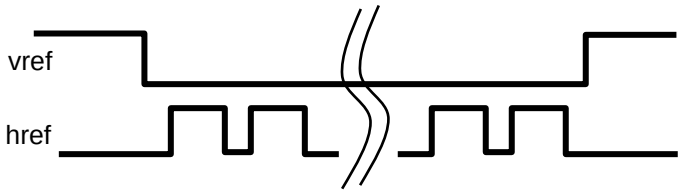
▷ ***Sync_vsyncpolarity***

Output vsync polarity control register.

▶ vsyncPolarity = '0'



▶ vsyncPolarity = '1'

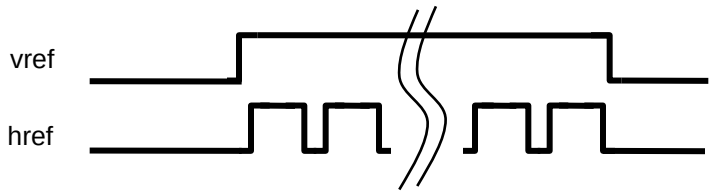


< Group B >

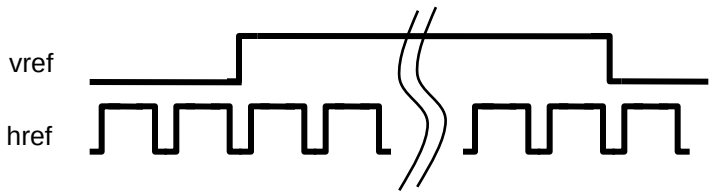
▷ Sync_hsyncAllLines

Output hsync control register.

▶ hsyncAllLines = '0'



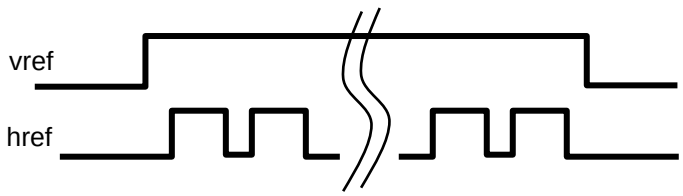
▶ hsyncAllLines = '1'



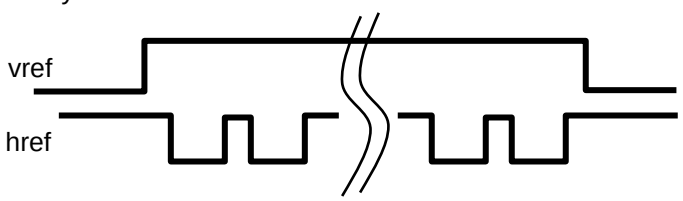
▷ Sync_hsyncpolarity

Output hsync polarity control register.

▶ hsyncPolarity = '0'



▶ hsyncPolarity = '1'

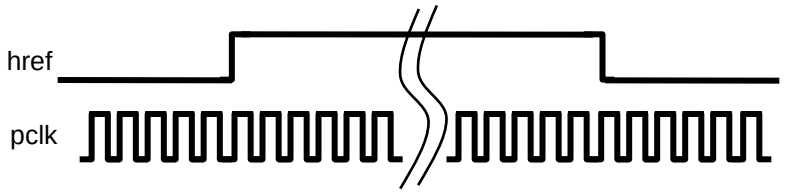


< Group B >

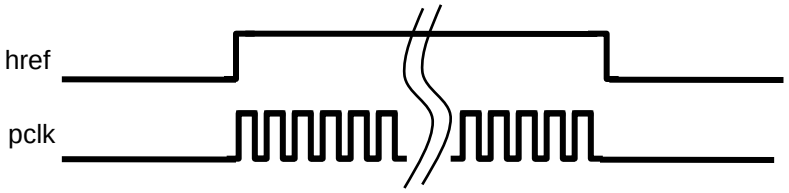
▷ Sync_pclkwindow

Output pclk control register.

▶ pclkwindow = '0'



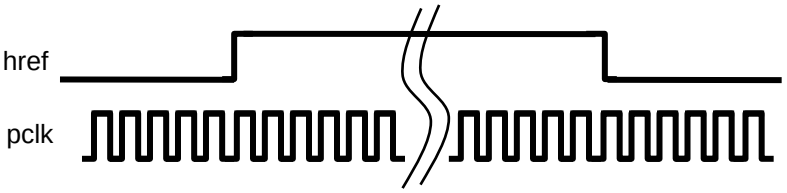
▶ pclkwindow = '1'



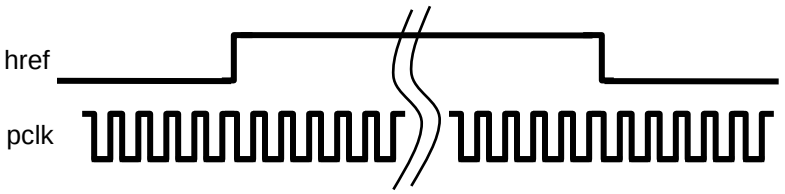
▷ Sync_pclkpolarity

Output pclk polarity control register.

▶ pclkpolarity = '0'



▶ pclkpolarity = '1'

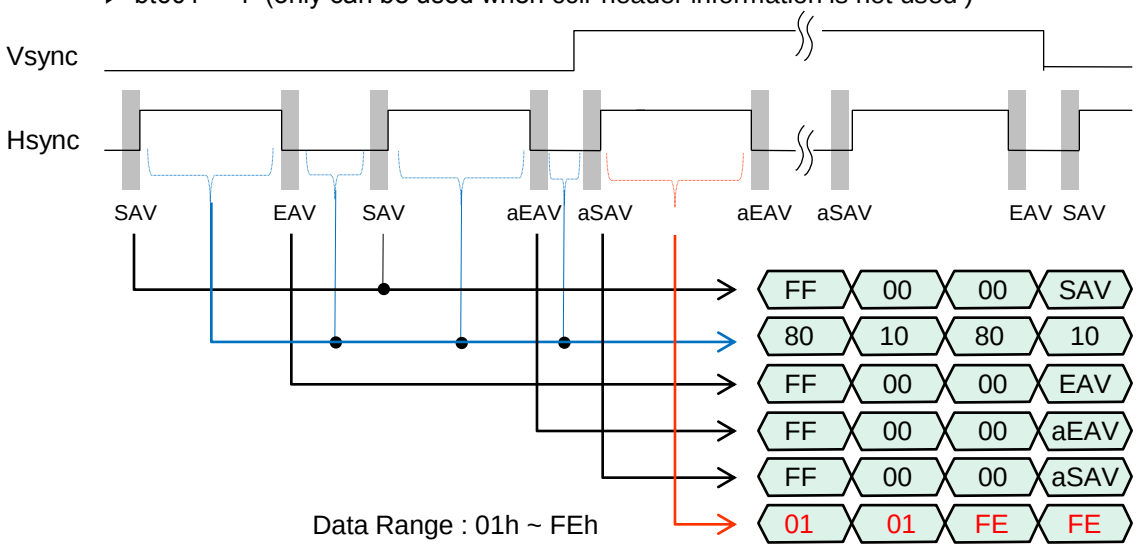


< Group B >

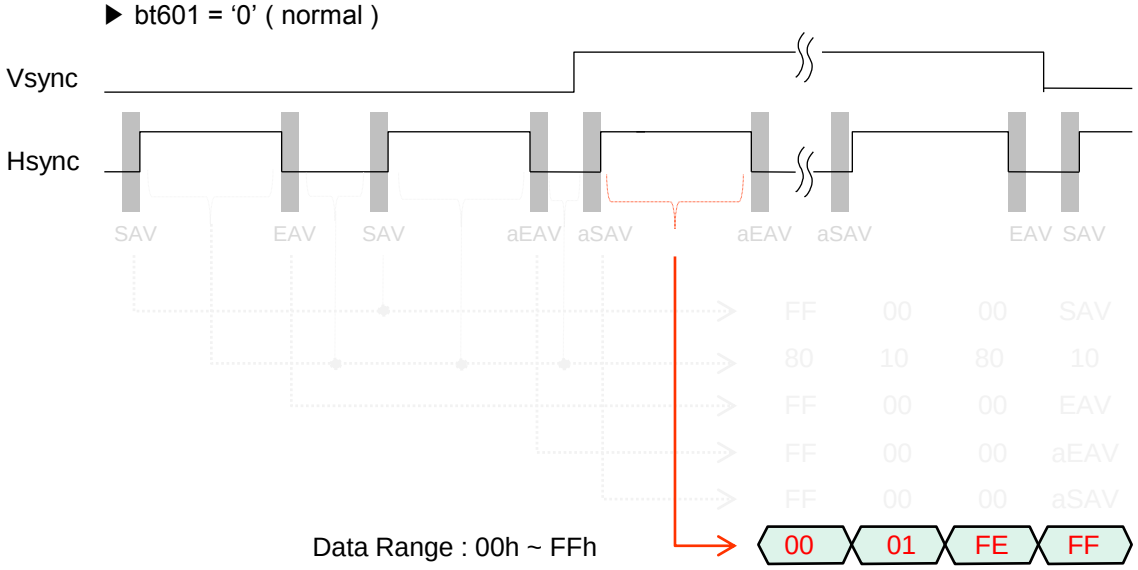
▷ bt601

Output data 00h / FFh output control register.

▶ bt601 = '1' (only can be used when ccir header information is not used)



▶ bt601 = '0' (normal)

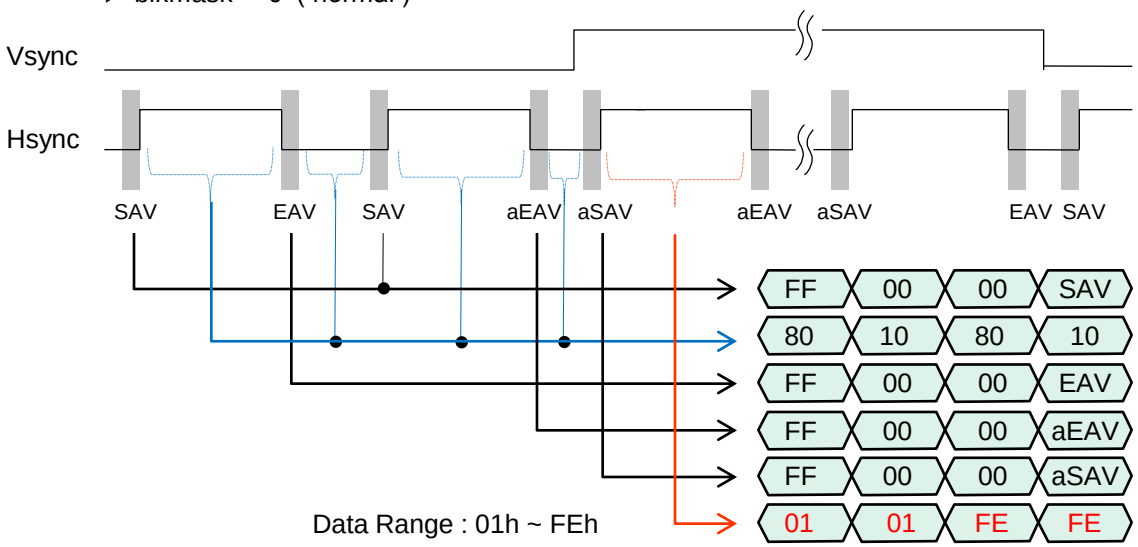


< Group B >

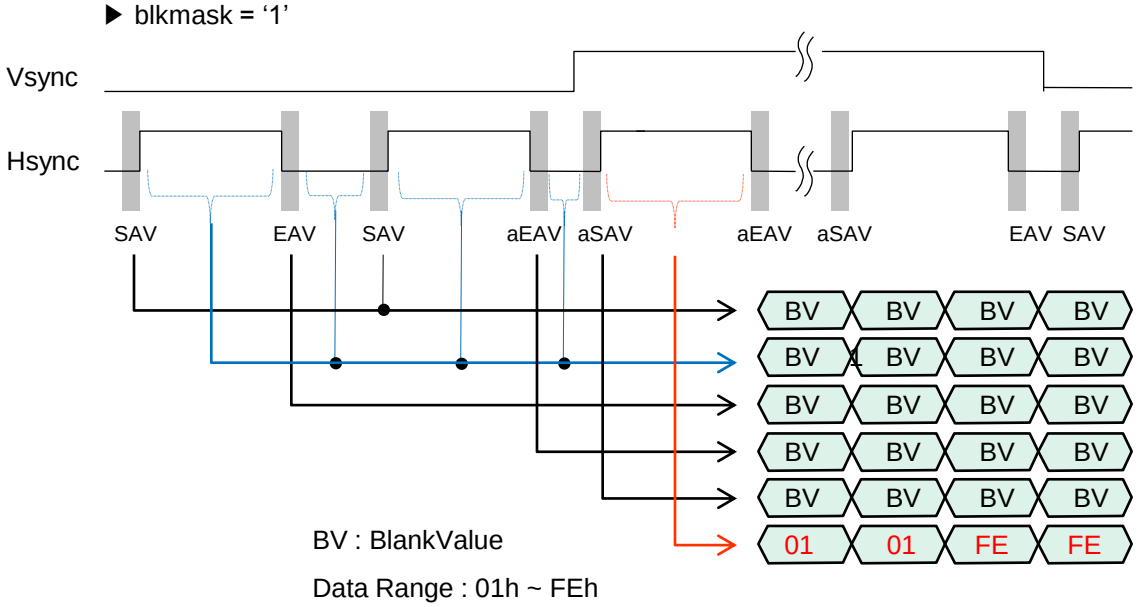
▷ blkmask

Blank period data masking control register.

▶ blkmask = '0' (normal)



▶ blkmask = '1'



< Group B >

(416~426) Privacy

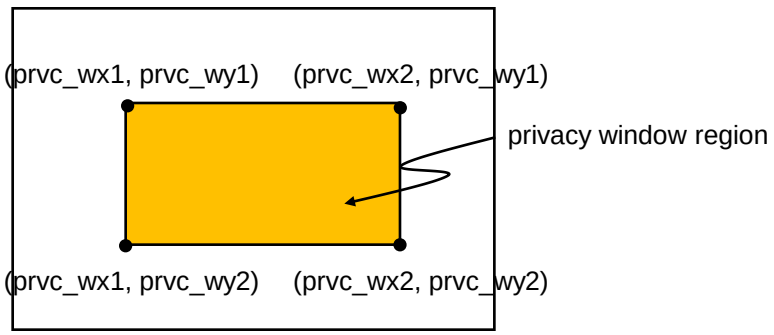
address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
416	A0	prvc_wx1_h	0	00	xxxxxx00	RW	5	0	Privacy window size control
417	A1	prvc_wx1_l	1	01	00000001	RW	5	0	
418	A2	prvc_wx2_h	2	02	xxxxxx10	RW	5	0	
419	A3	prvc_wx2_l	208	D0	11010000	RW	5	0	
420	A4	prvc_wy1_h	0	00	xxxxxx00	RW	5	0	
421	A5	prvc_wy1_l	1	01	00000001	RW	5	0	
422	A6	prvc_wy2_h	0	00	xxxxxx00	RW	5	0	
423	A7	prvc_wy2_l	240	F0	11110000	RW	5	0	
424	A8	prvc_y	0	00	00000000	RW	5	0	YCbCr of privacy window
425	A9	prvc_cb	128	80	10000000	RW	5	0	
426	AA	prvc_cr	128	80	10000000	RW	5	0	

▷ ***prvc_wx1/wx2, prvc_wy1/wy2***

Privacy window control registers.

▷ ***prvc_y/cb/cr***

Region of privacy window change the color.



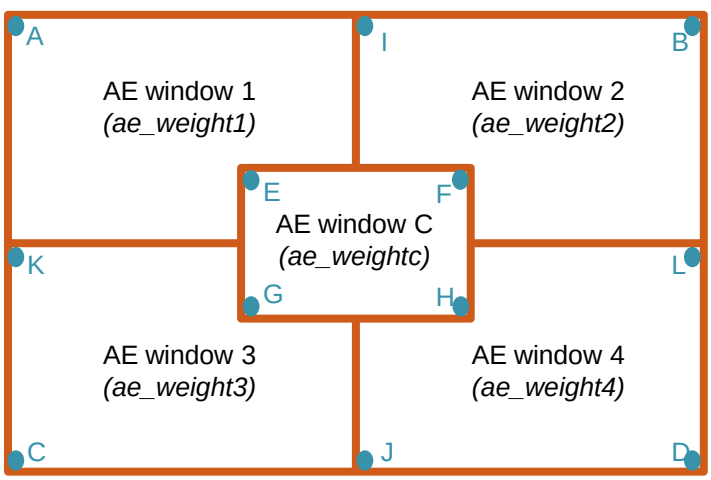
(435~454) Auto exposure window control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
435	B3	ae_fwx1_h	0	00	xxxxxx00	RW	5	0	AE full window X start position
436	B4	ae_fwx1_l	1	01	00000001	RW	5	0	
437	B5	ae_fwx2_h	2	02	xxxxxx10	RW	5	0	AE full window X stop position
438	B6	ae_fwx2_l	208	D0	11010000	RW	5	0	
439	B7	ae_fwy1_h	0	00	xxxxxx00	RW	5	0	AE full window Y start position
440	B8	ae_fwy1_l	1	01	00000001	RW	5	0	
441	B9	ae_fwy2_h	U	UU	uuuuuuuu	RW	5	0	AE full window Y stop position
442	BA	ae_fwy2_l	U	UU	uuuuuuuu	RW	5	0	
443	BB	ae_cwx1_h	0	00	xxxxxx00	RW	5	0	AE center window X start position
444	BC	ae_cwx1_l	241	F1	11110001	RW	5	0	
445	BD	ae_cwx2_h	1	01	xxxxxx01	RW	5	0	AE center window X stop position
446	BE	ae_cwx2_l	224	E0	11100000	RW	5	0	
447	BF	ae_cwy1_h	0	00	xxxxxx00	RW	5	0	AE center window Y start position
448	C0	ae_cwy1_l	U	UU	uuuuuuuu	RW	5	0	
449	C1	ae_cwy2_h	0	00	xxxxxx00	RW	5	0	AE center window Y stop position
450	C2	ae_cwy2_l	U	UU	uuuuuuuu	RW	5	0	
451	C3	ae_xaxis_h	1	01	xxxxxx01	RW	5	0	AE window X axis
452	C4	ae_xaxis_l	105	69	01101001	RW	5	0	
453	C5	ae_yaxis_h	0	00	xxxxxx00	RW	5	0	AE window Y axis
454	C6	ae_yaxis_l	U	UU	uuuuuuuu	RW	5	0	

▷ AE window control

AE window control registers.

default value : U ➔ wire-strapping register



A : *(ae_fwx1, ae_fwy1)*

B : *(ae_fwx2, ae_fwy1)*

C : *(ae_fwx1, ae_fwy2)*

D : *(ae_fwx2, ae_fwy2)*

E : *(ae_cwx1, ae_cwy1)*

F : *(ae_cwx2, ae_cwy1)*

G : *(ae_cwx1, ae_cwy2)*

H : *(ae_cwx2, ae_cwy2)*

I : *(ae_xaxis, ae_fwy1)*

J : *(ae_xaxis, ae_fwy2)*

K : *(ae_fwx1, ae_yaxis)*

L : *(ae_fwx2, ae_yaxis)*

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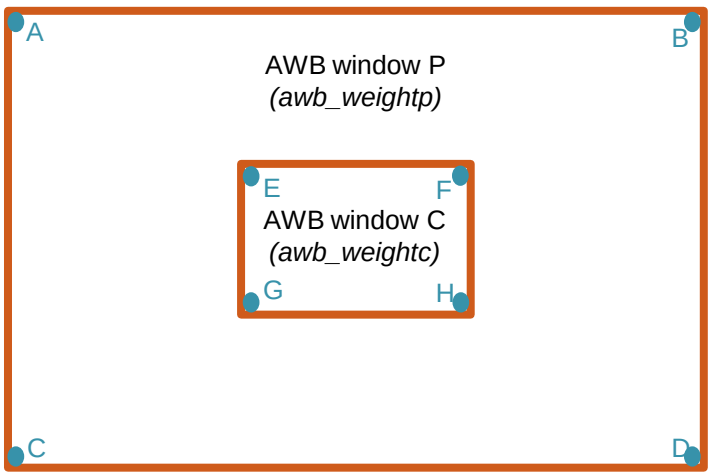
(455~470) AWB window control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
455	C7	awb_fwx1_h	0	00	00000000	RW	5	0	AWB full window X start position
456	C8	awb_fwx1_l	1	01	00000001	RW	5	0	
457	C9	awb_fwx2_h	2	02	00000010	RW	5	0	AWB full window X stop position
458	CA	awb_fwx2_l	208	D0	11010000	RW	5	0	
459	CB	awb_fwy1_h	0	00	00000000	RW	5	0	AWB full window Y start position
460	CC	awb_fwy1_l	1	01	00000001	RW	5	0	
461	CD	awb_fwy2_h	u	u	uuuuuuuu	RW	5	0	AWB full window Y stop position
462	CE	awb_fwy2_l	u	u	uuuuuuuu	RW	5	0	
463	CF	awb_cwx1_h	0	00	00000000	RW	5	0	AWB center window X start position
464	D0	awb_cwx1_l	241	F1	11110001	RW	5	0	
465	D1	awb_cwx2_h	1	01	00000001	RW	5	0	AWB center window X stop position
466	D2	awb_cwx2_l	224	E0	11100000	RW	5	0	
467	D3	awb_cwy1_h	0	00	00000000	RW	5	0	AWB center window Y start position
468	D4	awb_cwy1_l	u	u	uuuuuuuu	RW	5	0	
469	D5	awb_cwy2_h	0	00	00000000	RW	5	0	AWB center window Y stop position
470	D6	awb_cwy2_l	u	u	uuuuuuuu	RW	5	0	

▷ *AE window control*

AE window control registers.

default value : U ➔ wire-strapping register



A : *(awb_fwx1, awb_fwy1)*

B : *(awb_fwx2, awb_fwy1)*

C : *(awb_fwx1, awb_fwy2)*

D : *(awb_fwx2, awb_fwy2)*

E : *(awb_cwx1, awb_cwy1)*

F : *(awb_cwx2, awb_cwy1)*

G : *(awb_cwx1, awb_cwy2)*

H : *(awb_cwx2, awb_cwy2)*

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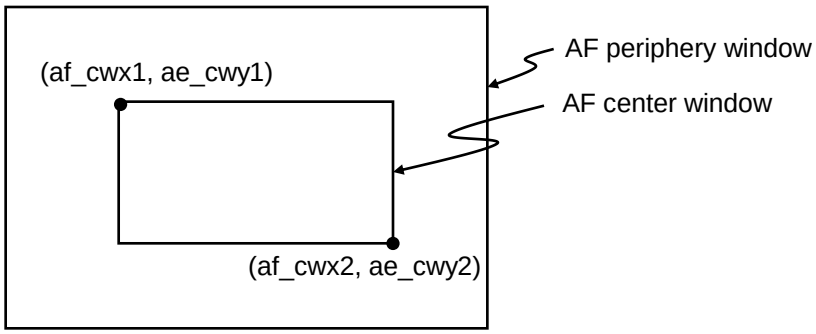
(472~481) Auto focus control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
472	D8	af_cwx1_h	0	00	xxxxxx00	RW	5	0	AF center window X start position
473	D9	af_cwx1_l	241	F1	11110001	RW	5	0	
474	DA	af_cwx2_h	1	01	xxxxxx01	RW	5	0	AF center window X stop position
475	DB	af_cwx2_l	224	E0	11100000	RW	5	0	
476	DC	af_cwy1_h	0	00	xxxxxx00	RW	5	0	AF center window Y start position
477	DD	af_cwy1_l	U	UU	uuuuuuuu	RW	5	0	
478	DE	af_cwy2_h	0	00	xxxxxx00	RW	5	0	AF center window Y stop position
479	DF	af_cwy2_l	U	UU	uuuuuuuu	RW	5	0	
480	E0	af_cweight	8	08	xxx01000	RW	5	0	AF weight center
481	E1	af_edge_th	0	00	0000000	RW	5	0	AF edge TH

▷ af_cwx1/x2/y1/y2

AF window control registers.

default value : U ➔ wire-strapping register



▶ AF window can't control AF periphery window.

▷ af_cweight

Control the weight of AF center.

▷ af_edge_th

Control the threshold of AF edge.

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(483~491) Motion detection threshold

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
483	E3	md_yth1	64	40	01000000	RW	5	0	Y threshold1 for motion detection
484	E4	md_yth2	64	40	01000000	RW	5	0	Y threshold2 for motion detection
485	E5	md_yth3	64	40	01000000	RW	5	0	Y threshold3 for motion detection
486	E6	md_yth4	64	40	01000000	RW	5	0	Y threshold4 for motion detection
487	E7	md_diff1	64	40	01000000	RW	5	0	Difference1 for motion detection
488	E8	md_diff2	64	40	01000000	RW	5	0	Difference2 for motion detection
489	E9	md_diff3	64	40	01000000	RW	5	0	Difference3 for motion detection
490	EA	md_diff4	64	40	01000000	RW	5	0	Difference4 for motion detection
491	EB	md_interval	8	08	00001000	RW	5	0	Intervals of frames used for motion detection

▷ md_yth1/2/3/4

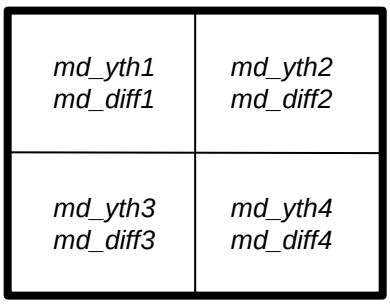
Threshold of Y (luminance) mean difference between current and previous frames at the same section.

▷ md_diff1/2/3/4

Difference between entire current and previous frame's brightness means.

▷ md_interval

Define frame interval for motion detection.



▶ PC1089K is assorted with forth area of motion detection and it can control motion's threshold

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(492~509) Motion detection

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
492	EC	md_alarm_y	0	00	00000000	RW	5	0	YCbCr for Motion detection alarm
493	ED	md_alarm_cb	128	80	10000000	RW	5	0	
494	EE	md_alarm_cr	128	80	10000000	RW	5	0	
495	EF	md_alarmnumb	4	04	00000100	RW	5	0	Number of Motion detection alarm
496	F0	md_alarm_xlw	4	04	00000100	RW	5	0	X width of motion detection alarm
497	F1	md_alarm_ylw	4	04	00000100	RW	5	0	Y width of motion detection alarm
498	F2	md_alarmdur_h	0	00	00000000	RW	5	0	Period of motion detection alarm
499	F3	md_alarmdur_l	60	3C	00111100	RW	5	0	
500	F4	md_sleepdur_h	2	02	00000010	RW	5	0	Motion detection sleep
501	F5	md_sleepdur_l	58	3A	00111010	RW	5	0	
502	F6	md_section7	0	00	00000000	RW	5	0	Image section 7 for motion detection
503	F7	md_section6	0	00	00000000	RW	5	0	Image section 6 for motion detection
504	F8	md_section5	0	00	00000000	RW	5	0	Image section 5 for motion detection
505	F9	md_section4	0	00	00000000	RW	5	0	Image section 4 for motion detection
506	FA	md_section3	0	00	00000000	RW	5	0	Image section 3 for motion detection
507	FB	md_section2	0	00	00000000	RW	5	0	Image section 2 for motion detection
508	FC	md_section1	0	00	00000000	RW	5	0	Image section 1 for motion detection
509	FD	md_section0	0	00	00000000	RW	5	0	Image section 0 for motion detection

▷ **md_alarm_y/cb/cr**

Alarm of motion detection change the color.

▷ **md_alarmnumb**

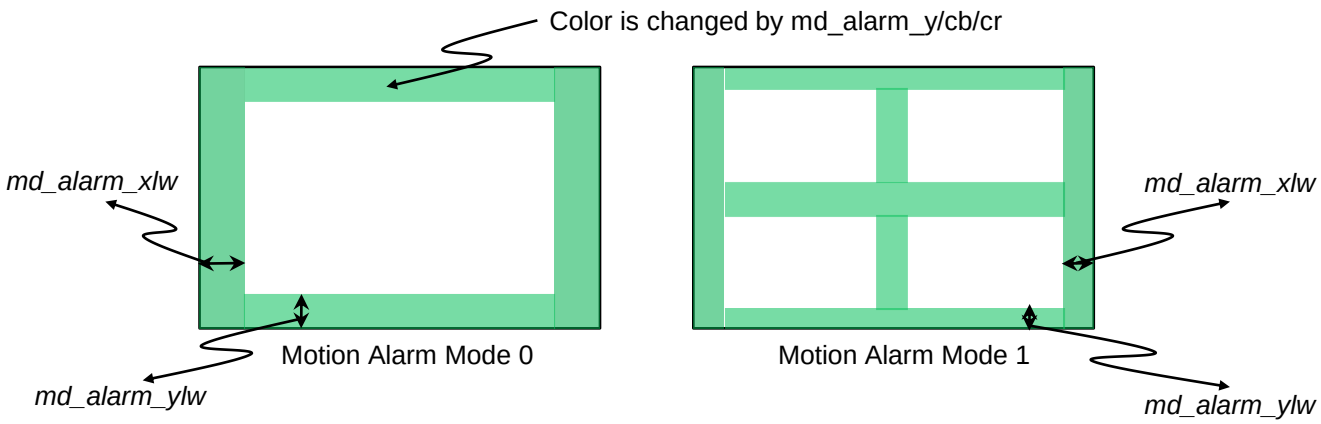
Control the number of motion detection alarm.

▷ **md_alarm_xlw**

Control the width of X's direction.

▷ **md_alarm_ylw**

Control the width of Y's direction.



▶ By the motion alarm mode showed with the upper 2 picture and according to fixed period, motion alarm blink.

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▷ md_alarmdur_h/l

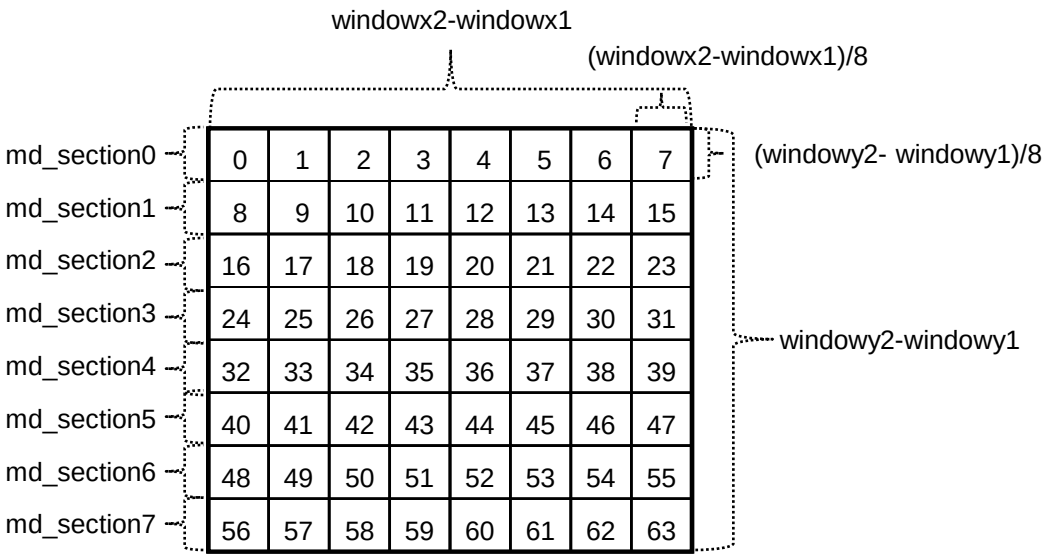
Control the flickering speed of motion alarm.

▷ md_sleepdur_h/l

When image don't have the motion during fixed time, control the power of DAC.

▷ md_section7/6/5/4/3/2/1/0

Masks of 64 sections on one frame.



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▶ Register Tables (Detailed) : Group C

(516) Auto_control_1

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
516	04	auto_control_1	152	98	10011000	RW	6	autov	Auto control

register name : auto_control_1								
register #	bit#	name	default	**152**	default(h)	**98**	default(b)	**10011000**
516d (04h)	7	reserved	1	should be fixed '1'				
	6	reserved	0	should be fixed '0'				
	5	reserved	0	should be fixed '0'				
	4	AE frame interval	1	AE frame interval selection 0b : 4 frame (speed down), 1b : 2frame (speed up)				
	3	AWB frame interval	1	AWB frame interval selection 0b : 4 frame (speed down), 1b : 2frame (speed up)				
	2	AWB mode	0	white blance mode selection 0b : auto mode, 1b : manual mode				
	1	exposure mode	0	exposure mode selection 00b : auto mode 01b : manual mode (exposure write) 10b : manual mode (ext_inttime, ext_glbgain write) 11b : manual mode (inttime, globalgain write)				
	0		0					

▷ AE interval & AWB interval

When auto_control_1[4] is '1', auto exposure block operate every 2 frame. When auto_control_1[4] is '0', auto exposure block is operate every 4 frame. When auto_control_1[3] is '1', auto white balance block operate every 2 frame. When auto_control_1[3] is '0', auto white balance block operate every 4 frame. This function is for internal test.

▷ AWB mode

When auto_control_1[2] is '1', auto white balance does not operation and you can write white balance gain (Reg. C-ECh~EEh). Please set disable, before writing white balance gain.

▷ AE mode

This product provides auto exposure mode and 3 types of manual exposure mode. User can select auto exposure mode by writing auto_control_1[1:0].

▶ **auto_control_1[1:0] = 00b (auto exposure mode)**

When auto_control_1[1:0] is 00b, integration time, globalgain and **digitalgain** are calculated by auto exposure block. Refer to auto exposure reference registers (Reg. C-10h~1Eh).

▶ **auto_control_1[1:0] = 01b (manual exposure mode1)**

When auto_control_1[1:0] is 01b, you can control integration time, globalgain and **digitalgain** by exposure registers (Reg. C-25h~28h). Refer to exposure registers (Reg. C-25h~28h) and auto exposure reference registers (Reg. C-10h~1Eh).

▶ **auto_control_1[1:0] = 10b (manual exposure mode2)**

When auto_control_1[1:0] is 10b, you can control integration time, globalgain and **digitalgain** by external integration time and external linear globalgain registers (Reg. C-20h~24h).

Refer to Reg. C-20h~24h.

▶ **auto_control_1[1:0] = 11b (manual exposure mode3)**

When auto_control_1[1:0] is 11b, you can write integration time, globalgain and **digitalgain** registers. Refer to Reg. C-DFh~E3h.

1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

(517) Auto_control_2

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
517	05	auto_control_2	101	65	01100101	RW	6	autov	Auto control

register name : auto_control_2								
register #	bit#	name	default	**101**	default(h)	**65**	default(b)	**01100101**
517d (05h)	7	LG/CS fitting x-aixs	0	lens gain, color saturation fitting x-axis selection 0b: LG & CS evaluation by redgain 1b: LG (Lens Gain) & CS (Color Saturation Matrix) evaluation by bluegain				
	6	LG/CS fitting	1	lens gain, color saturatin fitting enable 0b : disable 1b : LG & CS fitting enable				
	5	min/max YT fitting	1	mininum & maximum Y target fitting enable 0b : disable 1b : dynamic minimum/maximum clamping of Y target function enable				
	4	reserved	0	Should be fixed '0'				
	3	reserved	0	Should be fixed '0'				
	2	digitalgain mode	1	digitagain mode selectin 1b : auto digitalgain calculation mode 0b : manual digitalgain mode				
	1	iris_close_en	0	iris_close auto control enable '0' : disable '1' : enable				
	0	reserved	1	Should be fixed '1'				

▷ LG/CS fitting x-axis & LG/CS fitting

LG/CS fitting x-axis (bit7) is x-axis selection bit for lens gain and CS matrix fitting function. In addition, LG/CS fitting (bit6) is enable bit for lens gain and CS matrix fitting function. For more information, please refer to lens gain and CS matrix fitting reference registers (Reg. C-7Fh~93h).

▷ min/max YT fitting

Min/Max YT fitting (bit5) is enable bit for dynamic minimum & maximum clamping of Y target function. For more information, please refer to min/max ytarget reference registers (Reg. C-39h~3Eh).

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▷ ***iris_close_en***

iris_colose_en is iris_colose_control enable bit. when iris_close_en is '0', reg_iris_close (Reg. C-9Ah) is not changed by auto block. when iris_close_en is '1', reg_iris_close is changed by auto block. For more information, please refer to the iris_close_control (Reg. C-96h~9Ah).

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(522) AWB_control_1

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
522	0A	awb_control_1	149	95	10010101	RW	6	autov	Awb control

register name : awb_control_1									
register #	bit#	name	default	**149**	default(h)	**95**	default(b)	**10010101**	
522d (0Ah)	7	reserved	1	Should be fixed '1'					
	6	reserved	0	Should be fixed '0'					
	5	awb_acc_size_c	0	AWB accumulator size selection for center window 0 : 8K 4 : 128K 1 : 16K 5 : 256K 2 : 32K 6 : 512K 3 : 64K 7 : 1024K					
	4		1						
	3		0						
	2	awb_acc_size_p	1	AWB accumulator size selection for peripheral window 0 : 8K 4 : 128K 1 : 16K 5 : 256K 2 : 32K 6 : 512K 3 : 64K 7 : 1024K					
	1		0						
	0		1						

▷ AWB_acc_size_c & AWB_acc_size_p

awb_acc_size_c is selection register that number of accumulation data in AWB center window.

awb_acc_size_p is selection register that number of accumulation data in AWB peripheral window.

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(528~542) AE reference registers

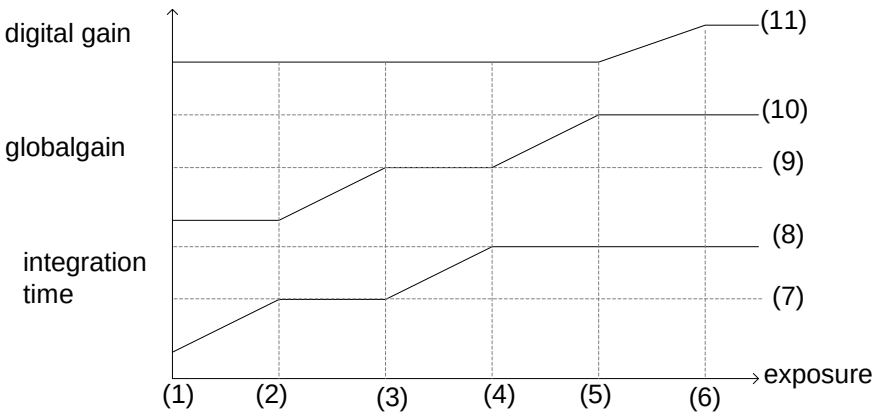
address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
528	10	expfrmh_h	2	02	00000010	RW	5	0	AE reference
529	11	expfrmh_l	u	u	uuuuuuuu	RW	5	0	
530	12	midfrmheight_h	2	02	00000010	RW	5	0	
531	13	midfrmheight_l	u	u	uuuuuuuu	RW	5	0	
532	14	maxfrmheight_h	2	02	00000010	RW	5	0	
533	15	maxfrmheight_l	u	u	uuuuuuuu	RW	5	0	
534	16	minexp_h	0	00	00000000	RW	5	0	
535	17	minexp_m	0	00	00000000	RW	5	0	
536	18	minexp_l	12	0C	00001100	RW	5	0	
537	19	midexp_t	1	01	00000001	RW	5	0	
538	1A	midexp_h	133	85	10000101	RW	5	0	
539	1B	midexp_m	64	40	01000000	RW	5	0	
540	1C	maxexp_t	1	01	00000001	RW	5	0	
541	1D	maxexp_h	133	85	10000101	RW	5	0	
542	1E	maxexp_m	64	40	01000000	RW	5	0	

▷ AE reference registers

Auto Exposure reference control registers.

When auto_control_1[1:0] is 00b or 01b, integration time, globalgain and **digitalgain** are calculated using AE reference registers .

default value : U ➔ wire-strapping register



(1) minimum exposure
(2) frame height for exposure
(3) mid frame height for exposure
(4) max frame height for exposure
(5) mid exposure
(6) max exposure
(7) mid integration time = (2)
(8) max integration time = (4)/(9)
(9) mid globalgain = (3)/(2)
(10) max globalgain =(5)/(8)
(11) max digital gain = (6)/{ (10)*(8) }

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(544~548) Manual integration time and linear globalgain for external AE mode

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
544	20	ext_inttime_h	0	00	00000000	RW	6	autov	Manual integration time @ external AE mode
545	21	ext_inttime_m	128	80	10000000	RW	6	autov	
546	22	ext_inttime_l	0	00	00000000	RW	6	autov	
547	23	ext_glbg_h	1	01	00000001	RW	6	autov	Manual analog gain @ external AE mode
548	24	ext_glbg_l	0	00	00000000	RW	6	autov	

▷ ext_inttime

When auto_control_1[1:0] is 10b, user can control integration time by writing external integration time registers. Ext_inttime_h and ext_inttime_m are line of external integration time. Ext_inttime_l is column of external integration time.

Set auto_control_1[1:0] to 10b, before writing external integration time.

▷ ext_globalgain

When auto_control_1[1:0] is 10b, user can control globalgain by writing external linear globalgain registers. Globalgain is calculated by external linear globalgain and reference gain in manual exposure mode 2. Set auto_control_1[1:0] to 10b, before writing external integration time.
For more information, refer to reference gain (Reg. A-E5h~EAh).

(549~552) Exposure

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
549	25	exposure_t	0	00	00000000	RW	6	autov	Exposure
550	26	exposure_h	0	00	00000000	RW	6	autov	
551	27	exposure_m	128	80	10000000	RW	6	autov	
552	28	exposure_l	0	00	00000000	RW	6	autov	

▷ exposure

When auto_control_1[1:0] is 00b, exposure registers are calculated by auto exposure block. Exposure registers are used in calculating integration time, globalgain and **digital gain**.
When auto_control_1[1:0] is 01b, user can write exposure registers.
Set auto_control_1[1:0] to 01b, before writing exposure registers.

(554~557) Saturation ratio control register

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
554	2A	ae_ysat	68	44	01000100	RW	6	autov	Saturation decision TH
556	2C	sratio_weight	8	08	00001000	RW	5	0	Saturation ratio weight
557	2D	sratio	0	00	00000000	RW	5	0	Saturation ratio

▷ **ae_ysat**

Saturation decision threshold for Y data

▷ **sratio_weight**

Saturation ratio weight factor.

▷ **sratio**

Saturation ratio value for monitoring

$$SR\_c/p = \frac{(\text{\# of saturation pixel in AE window})\_c/p}{(\text{\# of pixel in AE window})\_c/p}$$

$$sratio = \frac{(SR\_c \times sratio\_weight) + (SR\_p \times (16 - sratio\_weight))}{16}$$

(558~562) AE weight

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
558	2E	ae_weight1	8	08	xx001000	RW	5	0	AE weight peripheral
559	2F	ae_weight2	8	08	xx001000	RW	5	0	
560	30	ae_weight3	8	08	xx001000	RW	5	0	
561	31	ae_weight4	8	08	xx001000	RW	5	0	
562	32	ae_weightc	8	08	xx001000	RW	5	0	AE weight center

▷ **ae_weight1**

AE peripheral weight1 for back light compensation.

▷ **ae_weight2**

AE peripheral weight2 for back light compensation.

▷ **ae_weight3**

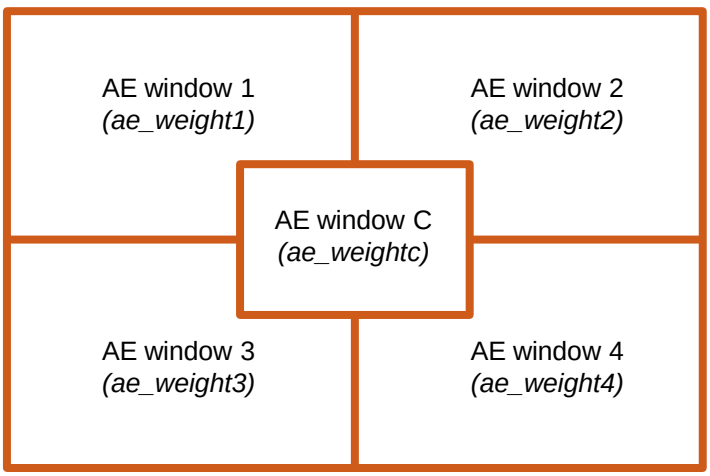
AE peripheral weight3 for back light compensation.

▷ **ae_weight4**

AE peripheral weight4 for back light compensation.

▷ **ae_weightc**

AE center weightc for back light compensation.



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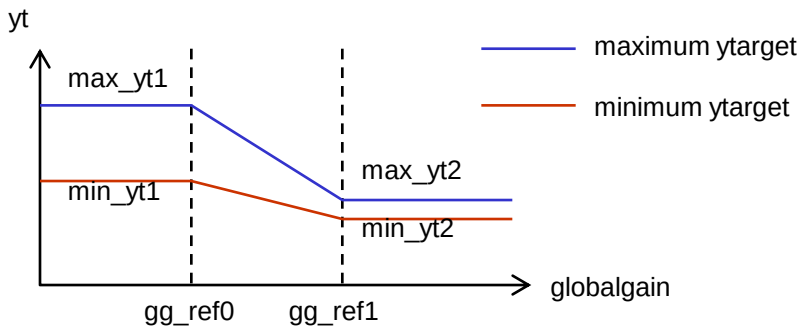
(569~574) Min/Max Y target reference

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
569	39	max_yt1	160	A0	10100000	RW	6	autov	min / max ytarget control reference
570	3A	max_yt2	128	80	10000000	RW	6	autov	
571	3B	min_yt1	128	80	10000000	RW	6	autov	
572	3C	min_yt2	80	50	01010000	RW	6	autov	
573	3D	gg_ref0	36	24	00100100	RW	6	autov	
574	3E	gg_ref1	75	4B	01001011	RW	6	autov	

▷ min/max_yt1/2

User can program dynamic y_target with these registers. Dynamic y_target means that y_target can be changed to match current brightness automatically.



When auto_control_2[5] is 1b, min./max. y_target is given like graph.

When auto_control_2[5] is 0b, min./max. y_target is given like min_yt1 / max_yt1.

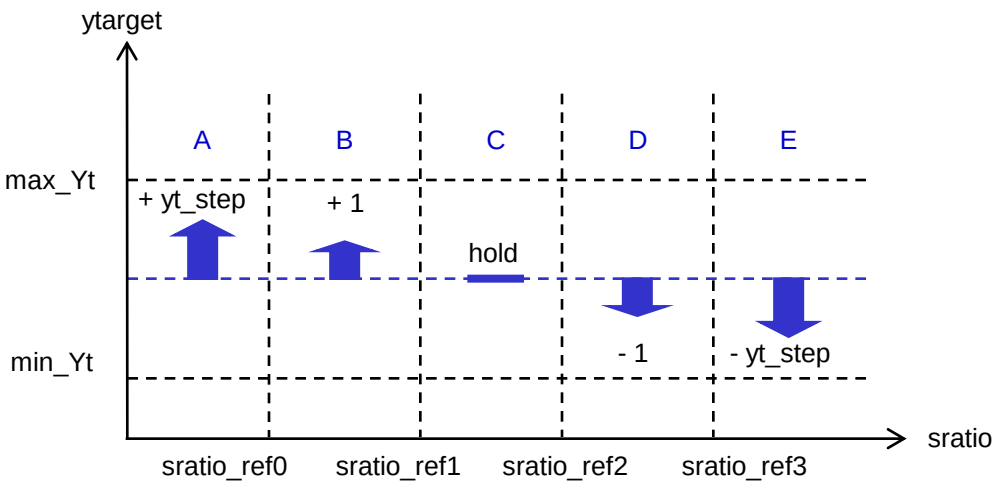
< Group C >

(575~581) Y target reference & Y target

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
575	3F	sratio_ref0	4	04	00000100	RW	6	autov	Ytarget control reference
576	40	sratio_ref1	16	10	00010000	RW	6	autov	
577	41	sratio_ref2	26	1A	00011010	RW	6	autov	
578	42	sratio_ref3	50	32	00110010	RW	6	autov	
579	43	yt_step	4	04	00000100	RW	5	0	
580	44	ytarget	112	70	01110000	RW	5	0	Y target
581	45	user_wyt	128	80	10000000	RW	6	autov	User weight Y target

▷ sratio_ref0/1/2/3

Saturation ratio reference fitting registers for y_target control.



▷ yt_step

Y target step control register.

▷ ytarget

Y target register.

▷ user_wyt

Weighted Y target control register.

Final Ytarget is given as

Ytarget = (ytarget x user_wyt) / 128d

< Group C >

(582~583) AE speed

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
582	46	ae_up_speed	8	08	00001000	RW	6	autov	AE upside speed
583	47	ae_down_speed	8	08	00001000	RW	6	autov	AE downside speed

▷ **ae_up_speed & ae_down_speed**

ae_up_speed : AE up speed control .

ae_down_speed : AE down speed control .

Setting range of both register is 01h to 10h. If ae_up_speed and ae_down_speed have high value, auto exposure speed will be faster. However, high ae_up_speed and ae_down_speed value may cause AE oscillation.

(584~585) AE lock range & auto flag

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
584	48	ae_lock	16	10	00010000	RW	6	autov	AE lock range
585	49	auto_flag	0	00	00000000	RW	5	0	Auto flag

▷ **ae_lock**

AE lock range control register.

Setting range of ae_lock is 00h to FFh. If ae_lock has low value, auto exposure lock range will be smaller. However, small value of ae_lock may cause AE oscillation.

▷ **auto_flag**

Current AE state indicator.

If auto_flag[0] = ‘0b’ , then AE state is “not hold”

If auto_flag[0] = ‘1b’ , then AE state is “hold”

(586~587) Auto flicker detection control register

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
586	4A	afd_th_h	2	02	00000010	RW	5	0	Auto flicker detection TH between high and low lux.
587	4B	afd_th_m	7	07	00000111	RW	5	0	

▷ **afd_th_h & afd_th_m**

Auto flicker detection OFF threshold control registers.
If current exposure > afd_th, then flicker detection mode will be OFF automatically even if auto flicker detection mode.

(588~591) AWB sampling range threshold

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
588	4C	awb_full_th_t	1	01	00000001	RW	5	0	AWB sampling range threshold
589	4D	awb_full_th_h	133	85	10000101	RW	5	0	
590	4E	awb_full_th_m	64	40	01000000	RW	5	0	
591	4F	awb_full	0	00	00000000	RW	5	0	

▷ **awb_full_th & awb_full**

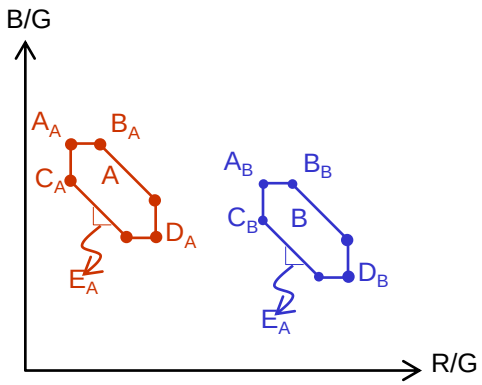
When exposure (Reg. C-25h~28h) is bigger than awb_full_th, awb_full is set 01h and all data in AWB window (both center & peripheral) is used AWB function irrespective of AWB data sampling control registers (Reg. C-51h~60h). In other case, some data is filtered by AWB data sampling control registers (Reg. C-51h~60h).

(593~608) AWB data sampling control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
593	51	awb_p1Ax	41	29	00101001	RW	5	0	AWB sampling range selection
594	52	awb_p1Ay	57	39	00111001	RW	5	0	
595	53	awb_p2Ax	54	36	00110110	RW	5	0	
596	54	awb_p2Ay	25	19	00011001	RW	5	0	
597	55	awb_osAx	9	09	00001001	RW	5	0	
598	56	awb_osAy	16	10	00010000	RW	5	0	
599	57	awb_slopeA	160	A0	10100000	RW	5	0	
600	58	awb_p1Bx	54	36	00110110	RW	5	0	
601	59	awb_p1By	33	21	00100001	RW	5	0	
602	5A	awb_p2Bx	105	69	01101001	RW	5	0	
603	5B	awb_p2By	20	14	00010100	RW	5	0	
604	5C	awb_osBx	12	0C	00001100	RW	5	0	
605	5D	awb_osBy	4	04	00000100	RW	5	0	AWB sampling range selection
606	5E	awb_slopeB	16	10	00010000	RW	5	0	
607	5F	awb_maxc	250	FA	11111010	RW	5	0	
608	60	awb_minc	8	08	00001000	RW	5	0	

▷ AWB data sample area control registers

These registers are used for more correct AWB operation.



A_A : (awb_p1Ax, awb_p1Ay)
B_A : (awb_p1Ax+awb_osAx, awb_p1Ay)
C_A : (awb_p1Ax, awb_p1Ay-awb_osAy)
D_A : (awb_p2Ax, awb_p2Ay)
E_A : awb_slopeA

A_B : (awb_p1Bx, awb_p1By)
B_B : (awb_p1Bx+awb_osBx, awb_p1By)
C_B : (awb_p1Bx, awb_p1By-awb_osBy)
D_B : (awb_p2Bx, awb_p2By)
E_B : awb_slopeB

If data are not included in region A or region B, then all of data are bad samples and not used AWB operations. In addition, if one of R, G, B is bigger than awb_maxc or lower than awb_minc, then data is bad sample and not used AWB operation.

< Group C >

(609~611) AWB weight & weight changing speed

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
609	61	awb_weight_c	5	05	00000101	RW	5	0	AWB weight for center
610	62	awb_weight_p	11	0B	00001011	RW	5	0	AWB weight for peripheral
611	63	awb_wspeed	4	04	00000100	RW	5	0	AWB weight speed

▷ **AWB_weight**

awb_weight_c : AWB center weight control register

awb_weight_p : AWB peripheral weight control register

caution) awb_weight_c & awb_weight_p should be, awb_weight_c + awb_weight_p = 64d

$$\text{R/G/Bmean\_c/p} = \frac{\text{(Sum. of R/G/B data in AWB window)\_c/p}}{\text{(\# of pixel in AWB window)\_c/p}}$$

$$\text{Weighted\_R/G/Bmean} = \frac{\text{(R/G/Bmean\_c x ae\_weight\_c) + (R/G/Bmean\_p x ae\_weight\_p)}}{\text{awb\_weight\_c + awb\_weight\_p}}$$

▷ **AWB_wspeed**

AWB weight change speed control register

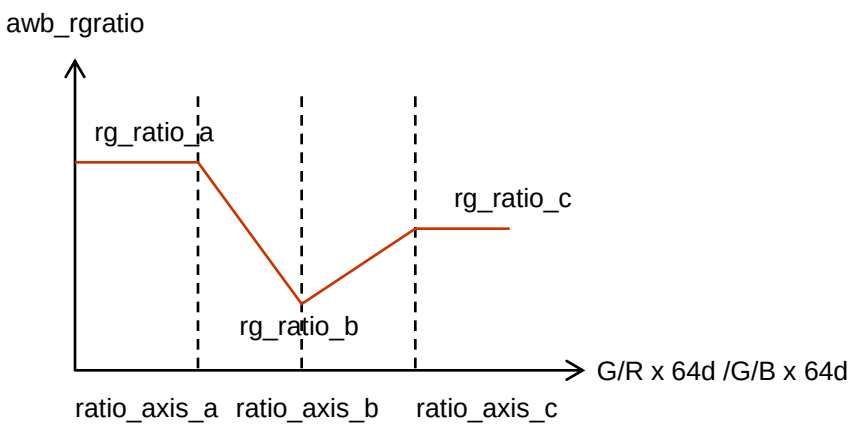
< Group C >

(614~624) rg/bg ratio reference & rg/bg ratio

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
614	66	rg_ratio_a	122	7A	01111010	RW	5	0	Target awb ratio fitting reference
615	67	bg_ratio_a	120	78	01111000	RW	5	0	
616	68	rg_ratio_b	128	80	10000000	RW	5	0	
617	69	bg_ratio_b	128	80	10000000	RW	5	0	
618	6A	rg_ratio_c	128	80	10000000	RW	5	0	
619	6B	bg_ratio_c	128	80	10000000	RW	5	0	
620	6C	ratio_axis_a	42	2A	00101010	RW	5	0	
621	6D	ratio_axis_b	80	50	01010000	RW	5	0	
622	6E	ratio_axis_c	87	57	01010111	RW	5	0	
623	6F	awb_rgratio	128	80	10000000	RW	5	0	AWB RG ratio control
624	70	awb_bgratio	128	80	10000000	RW	5	0	AWB BG ratio control

▷ RG/BG_ratio_a/b/c

These registers are used for changing AWB target with light source automatically.
If auto_control_3[7] is '1b', then automatic AWB target change function is enable.
If '0b', then function is disable.



User can select X-axis using auto_cotnrol_3[6]. (1b : G/B x 64 , 0b : G/R x 64).

Caution)

ratio_axis_a, ratio_axis_b and ratio_axis_c should be,

ratio_axis_a < ratio_axis_b < ratio_axis_c

▷ AWB_RG/BGratio

AWB target control registers

< Group C >

(625~626) AWB lock range & speed

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
625	71	awb_lock	16	10	00010000	RW	5	0	AWB lock range
626	72	awb_speed	4	04	00000100	RW	5	0	AWB speed

▷ AWB_lock

Used for AWB lock range control

(awb_lock range = | R/Bgain – R/Btarget | / R/Btarget)

▷ AWB_speed

Used for AWB speed control.

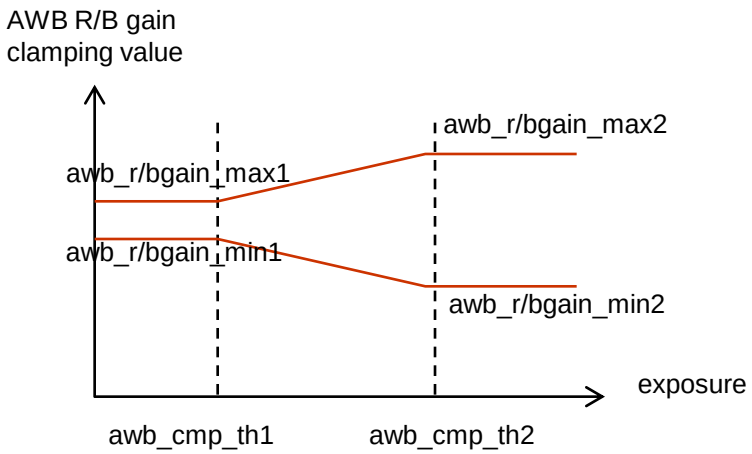
Setting range of awb_speed is 01h to 10h. If awb_speed has high value, auto white balance speed will be faster. However, high awb_speed value may cause AWB oscillation.

(627~638) AWB gain min/max clamping reference

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
627	73	awb_rgain_min1	42	2A	00101010	RW	5	0	AWB gain clamping fitting control
628	74	awb_rgain_min2	40	28	00101000	RW	5	0	
629	75	awb_rgain_max1	90	5A	01011010	RW	5	0	
630	76	awb_rgain_max2	93	5D	01011101	RW	5	0	
631	77	awb_bgain_min1	80	50	01010000	RW	5	0	
632	78	awb_bgain_min2	77	4D	01001101	RW	5	0	
633	79	awb_bgain_max1	183	B7	10110111	RW	5	0	
634	7A	awb_bgain_max2	186	BA	10111010	RW	5	0	
635	7B	awb_cmp_th1_h	1	01	00000001	RW	5	0	
636	7C	awb_cmp_th1_m	0	00	00000000	RW	5	0	
637	7D	awb_cmp_th2_h	2	02	00000010	RW	5	0	
638	7E	awb_cmp_th2_m	7	07	00000111	RW	5	0	

▷ AWB_r/bgain_min/max

These registers are used for AWB gain clamping control.



AWB R/B gain min/max clamping reference registers should be,

00h < awb_r/bgain_min1 < awb_r/bgain_max1 < FFh

00h < awb_r/bgain_min2 < awb_r/bgain_max2 < FFh

minexp < awb_cmp_th1 < awb_cmp_th2 < maxexp

Where, minexp/maxexp are register value.

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(639~660) Lens gain & CS matrix fitting reference

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
639	7F	cs11_a	40	28	00101000	RW	5	0	Color saturation matrix fitting reference
640	80	cs12_a	0	00	00000000	RW	5	0	
641	81	cs21_a	0	00	00000000	RW	5	0	
642	82	cs22_a	40	28	00101000	RW	5	0	
643	83	cs11_b	36	24	00100100	RW	5	0	
644	84	cs12_b	0	00	00000000	RW	5	0	
645	85	cs21_b	0	00	00000000	RW	5	0	
646	86	cs22_b	40	28	00101000	RW	5	0	
647	87	cs11_c	32	20	00100000	RW	5	0	
648	88	cs12_c	0	00	00000000	RW	5	0	
649	89	cs21_c	0	00	00000000	RW	5	0	
650	8A	cs22_c	32	20	00100000	RW	5	0	
651	8B	lens_gainr_a	2	02	00000010	RW	5	0	Lens gain fitting reference
652	8C	lens_gainb_a	0	00	00000000	RW	5	0	
653	8D	lens_gainr_b	2	02	00000010	RW	5	0	
654	8E	lens_gainb_b	0	00	00000000	RW	5	0	
655	8F	lens_gainr_c	2	02	00000010	RW	5	0	
656	90	lens_gainb_c	0	00	00000000	RW	5	0	
657	91	axis_a	42	2A	00101010	RW	5	0	CS matrix / lens gain fitting reference
658	92	axis_b	80	50	01010000	RW	5	0	
659	93	axis_c	87	57	01010111	RW	5	0	
660	94	user_cs	32	20	00100000	RW	5	0	User CS gain

▷ Color saturation matrix

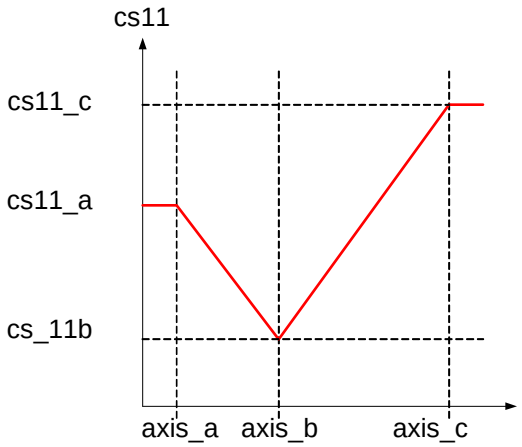
Color saturation matrix fitting registers.

▷ Lens_gainr/g/b

lens gain fitting registers.

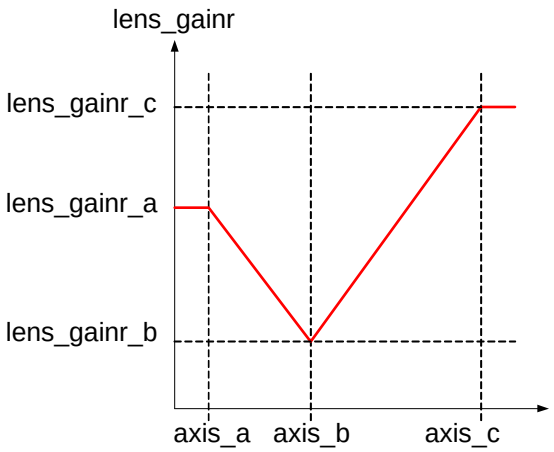
▷ *lens gain & CS matrix fitting reference*

PC1089K provides lens gain (R, B) and CS matrix fitting function by light source. When auto_control_2[6] is '1b', lens gain (R, B) and CS matrix fitting function is enabled. Below diagram shows that how to calculate lens gain (R, B) and CS matrix.



* calculation method of cs12, cs21 and cs22 are same as calculation method of cs11.

* bit define of cs11_a/b/c
  [7] : sign
  [6:5] : magnitude of integer
  [4:0] : magnitude of fraction



* calculation method of lens_gainb is same as calculation method of lens_gainr.

* bit define of lens_gainr_a/b/c
  [7:5] : magnitude of integer
  [4:0] : magnitude of fraction

User can select x axis using auto_control_2[7].
1b : wb_bgain
0b : wb_rgain

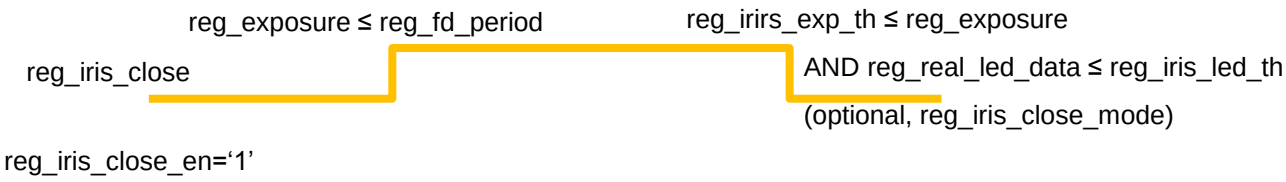
lens gain and CS matrix fitting reference should be,
axis_a < axis_b < axis_c

< Group C >

(662~666) iris close control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
662	96	iris_exp_th_t	0	00	00000000	RW	5	0	Iris close control
663	97	iris_exp_th_h	0	00	00000000	RW	5	0	
664	98	iris_exp_th_m	0	00	00000000	RW	5	0	
665	99	iris_led_th	0	00	00000000	RW	5	0	
666	9A	iris_close	0	00	00000000	RW	5	0	

▷ iris close control



reg_iris_close_en='1'

(670~675) Dark filter horizontal axis control register

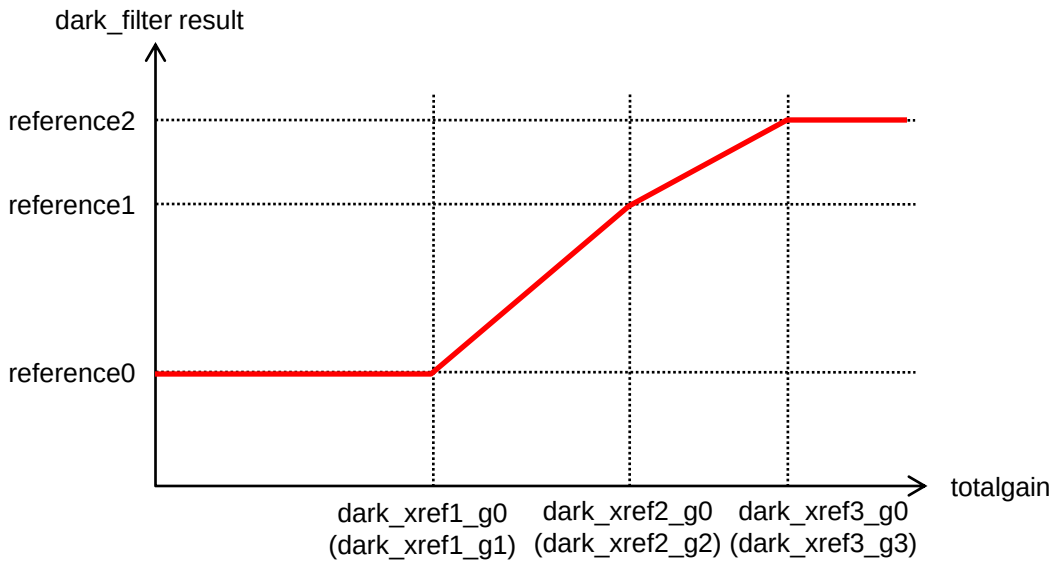
address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
670	9E	dark_xref1_g0	16	10	00010000	RW	5	0	Dark filter x-axis reference
671	9F	dark_xref2_g0	32	20	00100000	RW	5	0	
672	A0	dark_xref3_g0	48	30	00110000	RW	5	0	
673	A1	dark_xref1_g1	16	10	00010000	RW	5	0	
674	A2	dark_xref2_g1	32	20	00100000	RW	5	0	
675	A3	dark_xref3_g1	48	30	00110000	RW	5	0	

▷ **dark_xref1/2/3_g0, dark_xref1/2/3_g1**

dark_filter horizontal axis fitting registers.

User can program dark_filter with auto_control4[7] by automatically or manually.

Also, user can program dark_filter with group selection registers(Reg. C-07~09h).



< Group C >

(676) Total gain

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
676	A4	totalgain	2	02	00000010	RW	6	autov	Total gain

▷ **totalgain**

dark_filter reference control registers.

Totalgain is given as

totalgain = linear_gain x digitalgain

(678~681) dark_lens gain for lens shading compensation

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
678	A6	dark_lens0	0	00	00000000	RW	5	0	Dark lens fitting control
679	A7	dark_lens1	0	00	00000000	RW	5	0	
680	A8	dark_lens2	0	00	00000000	RW	5	0	
681	A9	dark_lens	0	00	00000000	RW	6	aev	

▷ **dark_lens**

dark_lens gain for lens shading compensation.

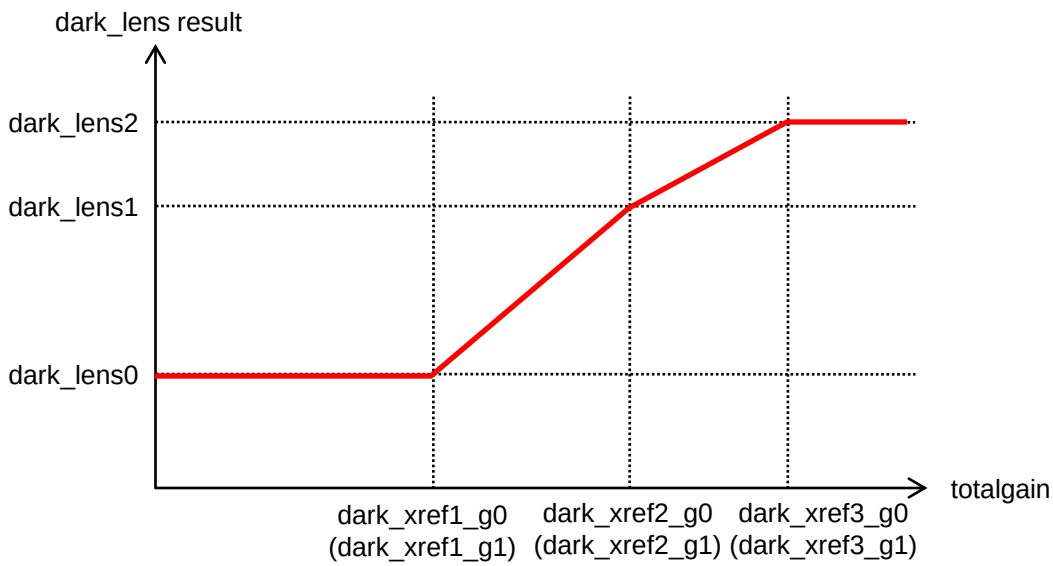
When auto_control4[7] = '0b', then user can program dark_lens manually.

Also, user can change dark_lens gain with auto_control4[6] (dark_lens group selection)

.

★ ***dark_lens0/1/2 conditions*** are given as

00h ≤ dark_lens0 ≤ dark_lens1 ≤ dark_lens2 ≤ FFh



< Group C >

(711~718) y_cont_th/y_cont_slope

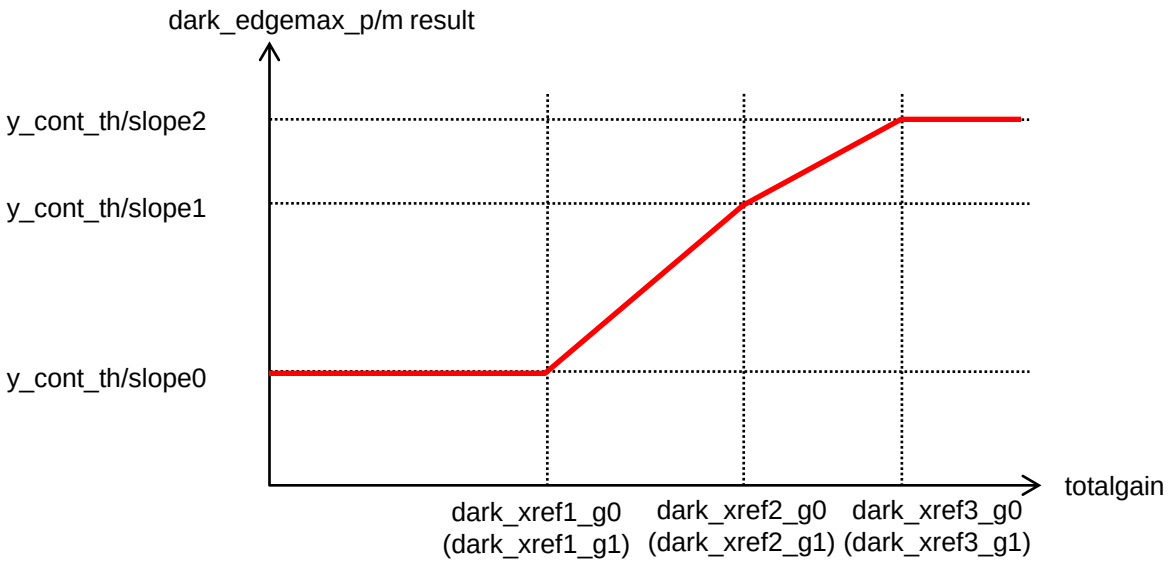
address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
711	C7	y_cont_th_ref0	255	FF	11111111	RW	5	0	Dark y contrast th fitting control
712	C8	y_cont_th_ref1	255	FF	11111111	RW	5	0	
713	C9	y_cont_th_ref2	255	FF	11111111	RW	5	0	
714	CA	y_cont_th	255	FF	11111111	RW	6	aev	
715	CB	y_cont_slope_ref0	80	50	01010000	RW	5	0	Dark y contrast slope fitting control
716	CC	y_cont_slope_ref1	80	50	01010000	RW	5	0	
717	CD	y_cont_slope_ref2	80	50	01010000	RW	5	0	
718	CE	y_cont_slope	80	50	01010000	RW	6	aev	

▷ **y_cont_th/y_cont_slope**

y contrast slope/th control registers.

When auto_control3[3] = '0b', then user can program y_cont_th/slope manually.

Also, user can change y_cont_th/slope with auto_control6[1]/auto_control6[0]. (y_cont_th/slope group selection).



< Group C >

(722~729) dark_Y / RGB_gamma for Gamma Correction

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
722	D2	dark_y_gm0	0	00	00000000	RW	5	0	Dark Y gamma fitting control
723	D3	dark_y_gm1	16	10	00010000	RW	5	0	
724	D4	dark_y_gm2	63	3F	00111111	RW	5	0	
725	D5	dark_y_gm	0	00	00000000	RW	6	aev	
726	D6	dark_rgb_gm0	0	00	00000000	RW	5	0	Dark RGB gamma fitting control
727	D7	dark_rgb_gm1	0	00	00000000	RW	5	0	
728	D8	dark_rgb_gm2	0	00	00000000	RW	5	0	
729	D9	dark_rgb_gm	0	00	00000000	RW	6	aev	

▷ **dark_y_gm/0/1/2 and dark_rgb_gm/0/1/2**

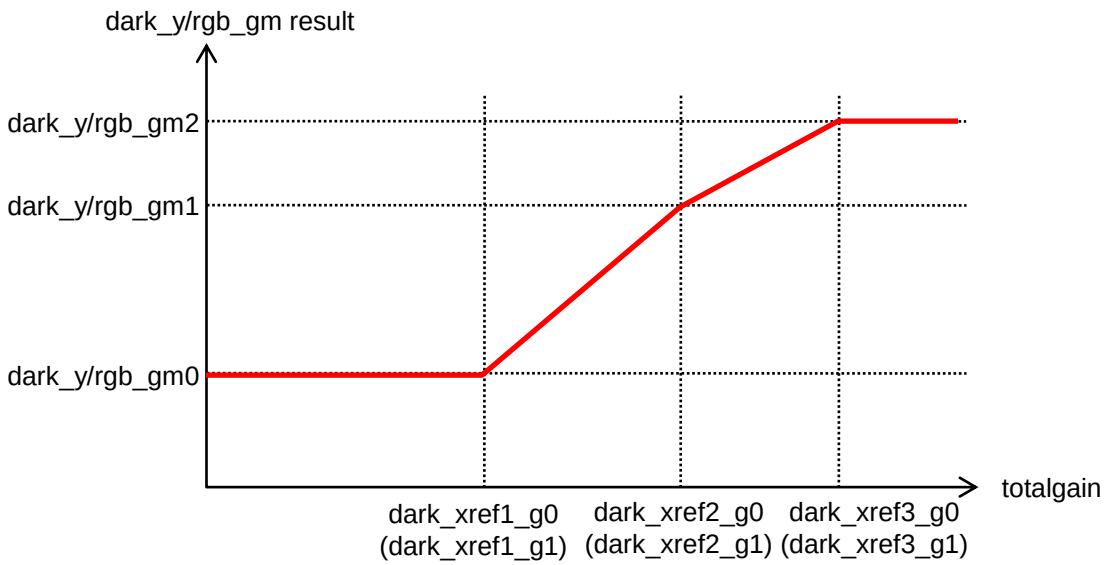
Y gamma & RGB gamma darkness control registers.

When auto_control4[7] = '0b', then user can program dark_y/rgb_gm manually.

Also, user can change dark_y/rgb_gm with auto_control5[2,1]. (dark_y/rgb_gm group selection)

★ ***dark_y/rgb_gm conditions*** are given as

00h ≤ dark_y/rgb_gm0 ≤ dark_y/rgb_gm1 ≤ dark_y/rgb_gm2 ≤ 20h



< Group C >

(730~733) dark CCR for color correction

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
730	DA	dark_ccr0	0	00	00000000	RW	5	0	Dark color correction fitting control
731	DB	dark_ccr1	4	04	00000100	RW	5	0	
732	DC	dark_ccr2	8	08	00001000	RW	5	0	
733	DD	dark_ccr	0	00	00000000	RW	6	aev	

▷ ***dark_ccr***

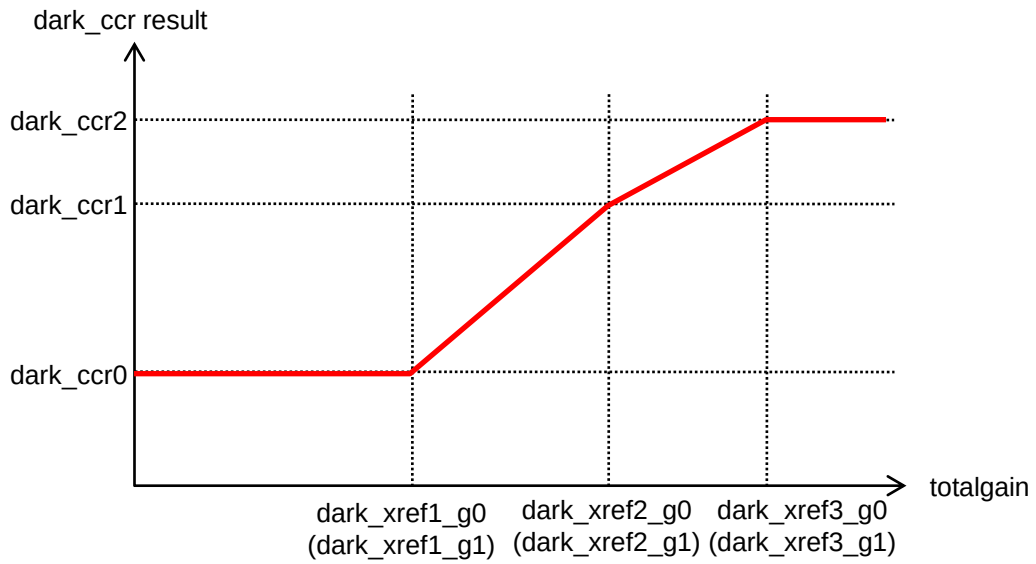
Color correction control registers.

When auto_control4[7] = '0b', then user can program dark_ccr manually.

Also, user can change dark_ccr with auto_control5[0] (dark_ccr group selection)

★ ***dark_ccr conditions*** are given as

00h ≤ dark_ccr0 ≤ dark_ccr1 ≤ dark_ccr2 ≤ FFh



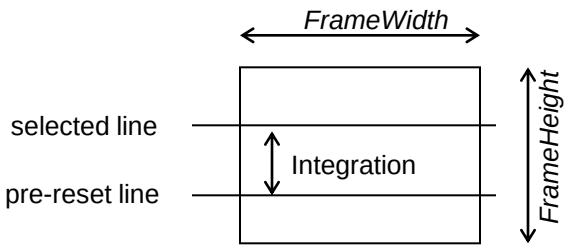
< Group C >

(735~737) Integration time.

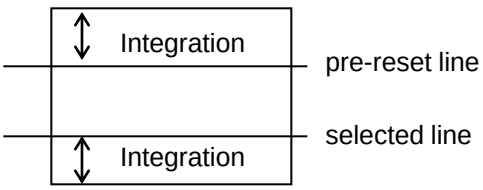
address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
735	DF	inttime_h	1	01	00000001	RW	6	aev	Integration time (line)
736	E0	inttime_m	64	40	01000000	RW	6	aev	
737	E1	inttime_l	0	00	00000000	RW	6	aev	Integration time (column)

▷ integration time

There are 3 bytes of registers to control the photo-charge accumulation interval for each pixel. DFh and E0h registers indicate how many line times the integration will continue until they are all reset. E1h register further sub-divides one line time into 256 smaller intervals. Total integration time is the sum of the integral multiple and fractional parts of one line time. As the row counter value is incremented from 0 to FrameHeight, each line relevant to the row count is selected and all pixel data of that line is read out all at once. The read- out operation involves pixel reset pulses, so all pixels that are selected and read out are reset to initial states. To control exposure time, there runs another counter to select and reset a line other than the one that is selected to be read out. The space between the two lines is equal to the number of integration lines. There are two possible situations concerning the position of selected line and reset line. The 1st case is where the pre-reset counter runs ahead of read-out counter. And the other case Is just the reverse of the 1st one. The number of integration lines is different for the two cases as is shown in the left figures. Since the basic unit of integration time for PC1089K is 1/ 256 line time, it is easy to implement Auto Exposure algorithms without worrying about strong light environment where the image may change abruptly in brightness or it may even blink.



Case 1. Reset line preceding select line



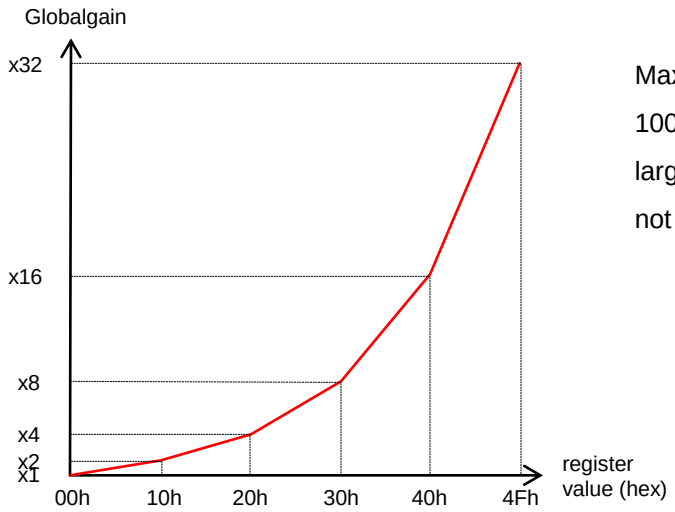
Case 2. Select line preceding reset line

(738) Global gain

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
738	E2	globalgain	0	00	00000000	RW	6	aev	Analog gain

▷ global gain

GlobalGain has effect on all of R, G, and B pixel outputs. Raw R, G, B data are amplified by a common factor of GlobalGain. The relation between GlobalGain and amplification factor is shown in the picture below.



Maximum value of *GlobalGain* is 1001111. Gain factors for *GlobalGain* larger than or equal to 1010000 are not defined.

(739) Digital gain

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
739	E3	digitalgain	64	40	01000000	RW	6	aev	Digital gain

▷ digital gain

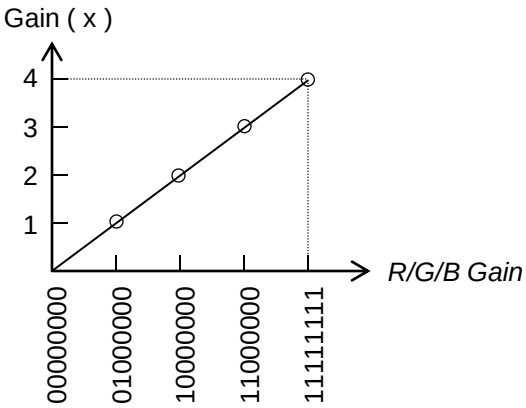
digitalgain[7:6] : Integer

digitalgain[5:0] : Fraction

(748~750) Normalized white balance gain

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
748	EC	wb_rgain	93	5D	01011101	RW	6	aev	White balance R gain
749	ED	wb_ggain	64	40	01000000	RW	6	0	White balance G gain
750	EE	wb_bgain	94	5E	01011110	RW	6	0	White balance B gain

▷ ***wb_rgain/ggain/bgain***



R / G / B gain can be used for white balance control. Bit7 of *R/G/B Gain* is weighted by 2, bit6 by 1 and the other consecutive bits are weighted by 1/2, 1/4, 1/8, … respectively. That is, *R/G/B gain* is a binary number with decimal point between bit6 and bit5.

< Group C >

▶ Register Tables (Detailed) : Group D

(772~816) Monitoring registers

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
779	0B	real_led_data	0	00	00000000	RO	0	0	Current LED data
780	0C	sif_state	0	00	00000000	RO	0	0	I2c master state monitor
781	0D	fd_state	0	00	00000000	RO	0	0	Current Flicker state
782	0E	fd_period_h	0	00	00000000	RO	0	0	Current Flicker period
783	0F	fd_period_m	0	00	00000000	RO	0	0	
784	10	fd_period_l	0	00	00000000	RO	0	0	
785	11	fd_fheight_h	0	00	00000000	RO	0	0	Current frameheight
786	12	fd_fheight_l	0	00	00000000	RO	0	0	
788	14	num_sample1_byte2	0	00	00000000	RO	0	0	Number of pixel in AE peripheral 1 window
789	15	num_sample1_byte1	0	00	00000000	RO	0	0	
790	16	num_sample1_byte0	0	00	00000000	RO	0	0	
791	17	num_sample2_byte2	0	00	00000000	RO	0	0	Number of pixel in AE peripheral 2 window
792	18	num_sample2_byte1	0	00	00000000	RO	0	0	
793	19	num_sample2_byte0	0	00	00000000	RO	0	0	
794	1A	num_sample3_byte2	0	00	00000000	RO	0	0	Number of pixel in AE peripheral 3 window
795	1B	num_sample3_byte1	0	00	00000000	RO	0	0	
796	1C	num_sample3_byte0	0	00	00000000	RO	0	0	
797	1D	num_sample4_byte2	0	00	00000000	RO	0	0	Number of pixel in AE peripheral 4 window
798	1E	num_sample4_byte1	0	00	00000000	RO	0	0	
799	1F	num_sample4_byte0	0	00	00000000	RO	0	0	
800	20	num_samplec_byte2	0	00	00000000	RO	0	0	Number of pixel in AE center window
801	21	num_samplec_byte1	0	00	00000000	RO	0	0	
802	22	num_samplec_byte0	0	00	00000000	RO	0	0	
803	23	num_sat_center_byte 2	0	00	00000000	RO	0	0	Number of saturation pixel in AE peripheral window
804	24	num_sat_center_byte 1	0	00	00000000	RO	0	0	
805	25	num_sat_center_byte 0	0	00	00000000	RO	0	0	
806	26	num_sat_peri_byte2	0	00	00000000	RO	0	0	Number of saturation pixel In AE peripheral 1 window
807	27	num_sat_peri_byte1	0	00	00000000	RO	0	0	
808	28	num_sat_peri_byte0	0	00	00000000	RO	0	0	
809	29	sum_sample1_byte3	0	00	00000000	RO	0	0	Summation of Y In AE peripheral 1 window
810	2A	sum_sample1_byte2	0	00	00000000	RO	0	0	
811	2B	sum_sample1_byte1	0	00	00000000	RO	0	0	
812	2C	sum_sample1_byte0	0	00	00000000	RO	0	0	
813	2D	sum_sample2_byte3	0	00	00000000	RO	0	0	Summation of Y n AE peripheral 2 window
814	2E	sum_sample2_byte2	0	00	00000000	RO	0	0	
815	2F	sum_sample2_byte1	0	00	00000000	RO	0	0	
816	30	sum_sample2_byte0	0	00	00000000	RO	0	0	

(817~861) Monitoring registers

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
817	31	sum_sample3_byte3	0	00	00000000	RO	0	0	Summation of Y In AE peripheral 3 window
818	32	sum_sample3_byte2	0	00	00000000	RO	0	0	
819	33	sum_sample3_byte1	0	00	00000000	RO	0	0	
820	34	sum_sample3_byte0	0	00	00000000	RO	0	0	
821	35	sum_sample4_byte3	0	00	00000000	RO	0	0	Summation of Y In AE peripheral 4 window
822	36	sum_sample4_byte2	0	00	00000000	RO	0	0	
823	37	sum_sample4_byte1	0	00	00000000	RO	0	0	
824	38	sum_sample4_byte0	0	00	00000000	RO	0	0	
825	39	sum_samplec_byte3	0	00	00000000	RO	0	0	Summation of Y In AE center window
826	3A	sum_samplec_byte2	0	00	00000000	RO	0	0	
827	3B	sum_samplec_byte1	0	00	00000000	RO	0	0	
828	3C	sum_samplec_byte0	0	00	00000000	RO	0	0	
829	3D	auto_fcnt	0	00	00000000	RO	0	0	Current auto frame counter
831	3F	awb_flag	0	00	00000000	RO	0	0	AWB flag
832	40	avg_r_c	0	00	00000000	RO	0	0	Current R mean in AWB center window
833	41	avg_g_c	0	00	00000000	RO	0	0	Current G mean in AWB center window
834	42	avg_b_c	0	00	00000000	RO	0	0	Current B mean in AWB center window
835	43	avg_r_p	0	00	00000000	RO	0	0	Current R mean in AWB peripheral window
836	44	avg_g_p	0	00	00000000	RO	0	0	Current G mean in AWB peripheral window
837	45	avg_b_p	0	00	00000000	RO	0	0	Current B mean in AWB peripheral window
838	46	monitor_awb_weight_c	0	00	00000000	RO	0	0	Current AWB weight for center
839	47	monitor_awb_weight_p	0	00	00000000	RO	0	0	Current AWB weight for peripheral
854	56	motion_monitor7	0	00	00000000	RO	0	0	Current motion detection indicator.
855	57	motion_monitor6	0	00	00000000	RO	0	0	
856	58	motion_monitor5	0	00	00000000	RO	0	0	
857	59	motion_monitor4	0	00	00000000	RO	0	0	
858	5A	motion_monitor3	0	00	00000000	RO	0	0	
859	5B	motion_monitor2	0	00	00000000	RO	0	0	
860	5C	motion_monitor1	0	00	00000000	RO	0	0	
861	5D	motion_monitor0	0	00	00000000	RO	0	0	

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(862~865) Monitoring registers

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
862	5E	af_edge_sum3	0	00	00000000	RO	0	0	Edge data for auto focus
863	5F	af_edge_sum2	0	00	00000000	RO	0	0	
864	60	af_edge_sum1	0	00	00000000	RO	0	0	
865	61	af_edge_sum0	0	00	00000000	RO	0	0	

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(867~878) CCIR656 control

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
867	63	sync_blankEAV_f0	182	B6	10110110	RW	5	0	Blank EAV for field0 of CCIR656 data or blank EAV for frame data
868	64	sync_blankSAV_f0	171	AB	10101011	RW	5	0	Blank SAV for field0 of CCIR656 data or blank SAV for frame data
869	65	sync_activeEAV_f0	157	9D	10011101	RW	5	0	Active EAV for field0 of CCIR656 data or active EAV for frame data
870	66	sync_activeSAV_f0	128	80	10000000	RW	5	0	Active SAV for field0 of CCIR656 data or active SAV for frame data
871	67	sync_blankEAV_f1	241	F1	11110001	RW	5	0	blank EAV for field1 of CCIR656 data
872	68	sync_blankSAV_f1	236	EC	11101100	RW	5	0	blank SAV for field1 of CCIR656 data
873	69	sync_activeEAV_f1	218	DA	11011010	RW	5	0	active EAV for field1 of CCIR656 data
874	6A	sync_activeSAV_f1	199	C7	11000111	RW	5	0	active SAV for field1 of CCIR656 data
875	6B	sync_CCIR_FF	255	FF	11111111	RW	5	0	CCIR data format
876	6C	sync_CCIR_00	0	00	00000000	RW	5	0	
877	6D	sync_CCIR_80	128	80	10000000	RW	5	0	
878	6E	sync_CCIR_10	16	10	00010000	RW	5	0	

▷ **ccir656 sync index value**

EAV and SAV data value for synchronization.

Address	Name	Description
64, 68h	*BlankSAV*	Blank Range Start of Video
63, 67h	*BlankEAV*	Blank Range End of Video
65, 69h	*ActiveEAV*	Active Range End of Video
66, 6Ah	*ActiveSAV*	Active Range Start of Video

▷ **sync_ccirFF**

CCIR data format FFh

▷ **sync_ccir00**

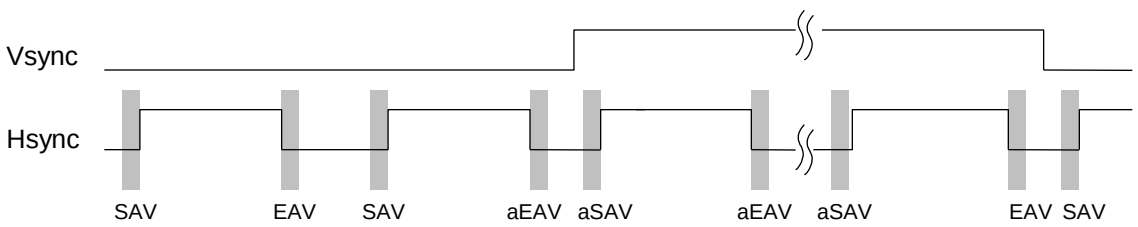
CCIR data format 00h

▷ **sync_ccir80**

CCIR data format 80h

▷ **sync_ccir10**

CCIR data format 10h



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(879) CCIR656 control 1

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
879	6F	ccir656enc_ctrl1	128	80	10000000	RW	5	0	Ccir656 control for encoder

register name : ccir656en_ctrl1								
register #	bit#	name	default	**128**	default(h)	**80**	default(b)	**10000000**
879d (6Fh)	7	bt656_sel	1	BT656 mode selection bits @ NTSC mode 00b : even field output(720x240), odd filed output (720x240) 10b : even field output(720x243), odd filed output (720x243) 11b : even field output(720x244), odd filed output (720x243)				
	6		0					
	5	hscale_sel	0	Input image horizontal width selection bits 00b : 720 01b : 640 10b : 768				
	4		0					
	3	winy_sel	0	Digital output vertical size selection bits@ NTSC mode 00b : even field digital output (720x240), odd field digital output (720x240) 01b : even field digital output (720x243), odd field digital output (720x243) 10b : even field digital output (720x244), odd field digital output (720x243) 11b : even field digital output (720x244), odd field digital output (720x244)				
	2		0					
	1	even_drop	0	Digital CCIR656 output even field drop enable 0b : disable 1b : enable (even field drop)				
	0	odd_drop	0	Digital CCIR656 output odd field drop enable 0b : disable 1b : enable (odd field drop)				

▷ bt656_sel

BT656 mode selection bits. Refer to fig.11 in page 15,16.

▷ hscale_sel

Select bits for input horizontal width. If the horizontal width is 640 pixel, hscale_sel selects 01b.

▷ winy_sel

Select bits for vertical size of digital output.

▷ even_drop

Drop even field of digital CCIR656.

▷ odd_drop

Drop odd field of digital CCIR656.

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(880~881) Xscale threshold

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
880	70	xscale_th_h	2	02	00000010	RW	5	0	Xscale horizontal scaling TH for encoder
881	71	xscale_th_l	208	D0	11010000	RW	5	0	

▷ **xscale_th**

Threshold for line data scaling in encoder

In case of window cropping as much as 640 size, these registers should set as '640d'.

Related register is D-6Fh.

(883) Flicker control 1

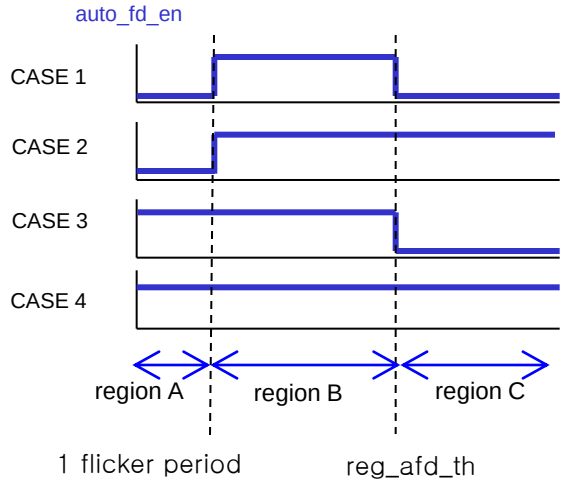
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
883	73	flicker_control1	u	u	uuuuuuuu	RW	5	0	Flicker control

register name : flicker_control1								
register #	bit#	name	default	**U**	default(h)	**UU**	default(b)	**uuuuuuuu**
883d (73h)	7	x	u	Reserved				
	6	fd_en	u	flicker enable 0b : disable 1b : enable				
	5	af_1pd_en	u	'1' : if (exposure< 1 flicker_period) then auto_fd_en='1'				
	4	af_fh_en	u	'1' : if (exposure > auto_fd_th) then auto_fd_en='1'				
	3	manual_A	u	manual_A				
	2	manual_B	u	manual_B				
	1	fd_comp	u	flicker comp : 00b : 2cycle detect, 01b : 3 cycle detect, else : 4 cycle detect				
	0		u					

▷ **fd_en**

Flicker detection enable/disable.

default value : U ➔ wire-strapping register



	flicker control1 [6:5]	auto_fd_en		
		inttime = region A	inttime = region B	inttime = region C
CASE 1	"00"	00h	01h	00h
CASE 2	"01"	00h	01h	01h
CASE 3	"10"	01h	01h	00h
CASE 4	"11"	01h	01h	01h

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(884~901) Flicker control

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
884	74	auto_fd	0	00	00000000	RW	5	0	Auto flicker detection enable monitoring
885	75	fd_a_step_h	u	u	uuuuuuuu	RW	5	0	Flicker detection step for A state
886	76	fd_a_step_l	u	u	uuuuuuuu	RW	5	0	
887	77	fd_b_step_h	3	03	00000011	RW	5	0	Flicker detection step for B state
888	78	fd_b_step_l	u	u	uuuuuuuu	RW	5	0	
889	79	fd_winheight	64	40	01000000	RW	5	0	Flicker detection window height
890	7A	fd_a_delay	0	00	00000000	RW	5	0	Flicker detection delay for A state
891	7B	fd_b_delay	0	00	00000000	RW	5	0	Flicker detection delay for A state
892	7C	fd_th	16	10	00010000	RW	5	0	Flicker detection TH.
893	7D	fd_period_a_h	u	u	uuuuuuuu	RW	5	0	Flicker period for A state
894	7E	fd_period_a_m	u	u	uuuuuuuu	RW	5	0	
895	7F	fd_period_a_l	u	u	uuuuuuuu	RW	5	0	
896	80	fd_period_b_h	1	01	00000001	RW	5	0	Flicker period for B state
897	81	fd_period_b_m	u	u	uuuuuuuu	RW	5	0	
898	82	fd_period_b_l	u	u	uuuuuuuu	RW	5	0	
899	83	fd_period_c_h	u	u	uuuuuuuu	RW	5	0	Flicker period for 1/20 second
900	84	fd_period_c_m	u	u	uuuuuuuu	RW	5	0	
901	85	fd_minfr	4	04	00000100	RW	5	0	Flicker TH. for 1/20 second

▷ Flicker detection step A & B

Before auto flicker detection mode enable, user must set fd_A_step and fd_B_step.

fd_A_step and fd_B_step are calculated by as below.

$$\text{fd\_A\_step} = \frac{256*256*4}{\text{fd\_period\_A\_h \& fd\_period\_A\_m}}$$

$$\text{fd\_B\_step} = \frac{256*256*4}{\text{fd\_period\_B\_h \& fd\_period\_B\_m}}$$

▷ Flicker period A & B

fd_period_A can be programmed by flicker period for 1/120 sec.

fd_period_B can be programmed by flicker period for 1/100 sec.

Flicker period for 1/120 sec and 1/100 sec are calculated by as below.

$$\text{fd\_period\_A} = \frac{256\ d*\ \text{PCLK FREQ.}}{120d\ *\ \text{framewidth}}$$

$$\text{fd\_period\_B} = \frac{256\ d*\ \text{PCLK FREQ.}}{100d\ *\ \text{framewidth}}$$

Where, framewidth is register value. PCLK FREQ. is frequency of pixel clock.

default value : U ➔ wire-strapping register

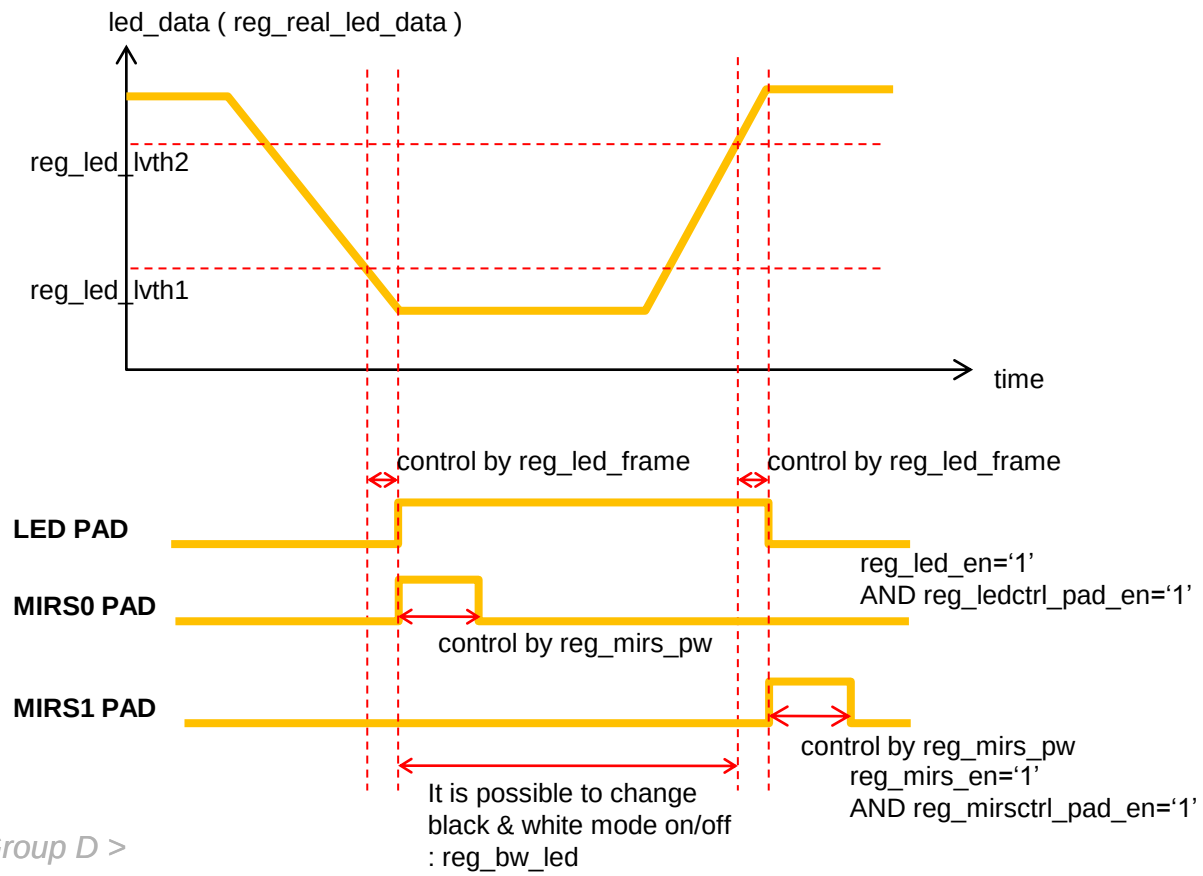
< Group D >

(902~908) LED control

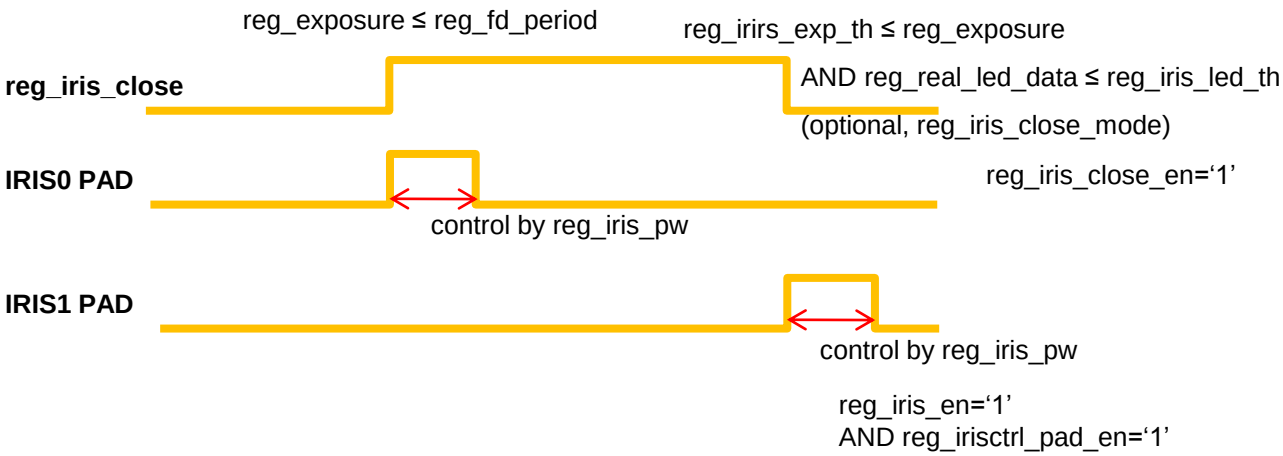
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
902	86	led_control1	0	00	00000000	RW	5	0	Led control
903	87	led_control2	0	00	00000000	RW	5	0	
904	88	led_lvth1	0	00	00000000	RW	5	0	Led control level th.1
905	89	led_lvth2	0	00	00000000	RW	5	0	Led control level th.2
906	8A	led_frame	128	80	10000000	RW	5	0	led frame control
907	8B	mirs_pw	100	64	01100100	RW	5	0	Mirs pulse width
908	8C	iris_pw	100	64	01100100	RW	5	0	Iris pulse width

register name : led_control1								
register #	bit#	name	default	**00**	default(h)	**00**	default(b)	**00000000**
902d (86h)	7	ledctl en	0	led control enable 0b : disable 1b : enable				
	6	ledctl manual	0	led output value @ led control disable				
	5	ledctl polarity	0	led output polarity change enable 0b : disable 1b : enable				
	4	bwled en	0	black & white mode @ led on enable 0b : disable 1b : enable				
	3	mirs en	0	moving IR/AR glass switch (MIRS) control enable 0b : disable 1b : enable				
	2	mirs manual	0	mirs output value @ mirs control disable				
	1		0					
	0	mirs polarity	0	mirs output polarity change enable 0b : disable 1b : enable				

register name : led_control2								
register #	bit#	name	default	00	default(h)	00	default(b)	00000000
903d (87h)	7	iris en	0	IRIS control enable 0b : disable 1b : enable				
	6	iris manual	0	mirs output value @ mirs control disable				
	5		0					
	4	iris polarity	0	mirs output polarity change enable 0b : disable 1b : enable				
	3	x	0	Reserved				
	2	x	0	Reserved				
	1	x	0	Reserved				
	0	x	0	Reserved				



< Group D >


reg_exposure ≤ reg_fd_period
reg_irirs_exp_th ≤ reg_exposure
reg_iris_close
AND reg_real_led_data ≤ reg_iris_led_th
(optional, reg_iris_close_mode)
IRIS0 PAD
reg_iris_close_en='1'
control by reg_iris_pw
IRIS1 PAD
control by reg_iris_pw
reg_iris_en='1'
AND reg_irisctrl_pad_en='1'

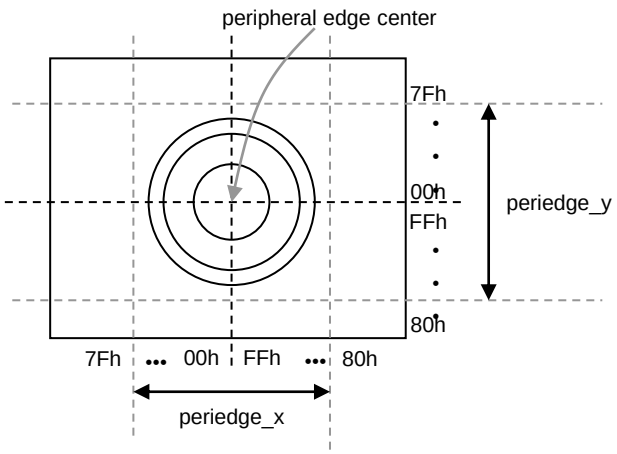
(909~913) Peripheral edge

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
909	8D	periedge_gain	0	00	00000000	RW	5	0	Peripheral edge gain
910	8E	periedge_x	0	00	00000000	RW	5	0	Peripheral edge center control
911	8F	periedge_y	0	00	00000000	RW	5	0	
912	90	periedge_scalex	81	51	01010001	RW	5	0	Peripheral edge scale control
913	91	periedge_scaley	81	51	01010001	RW	5	0	

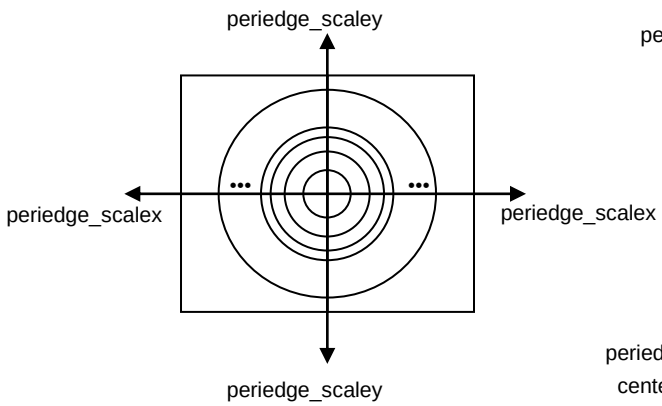
▷ periedge_gain

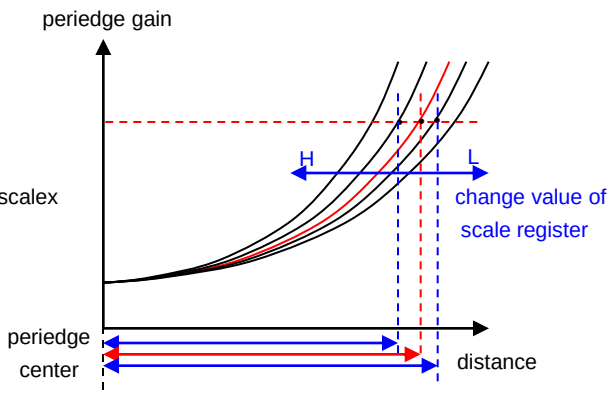
When we use a wide-angle lens , you know that peripheral edge become blurred. By using the periedge_gain, peripheral edges are enhanced.

▷ peripheral edge center control



▷ peripheral edge scale



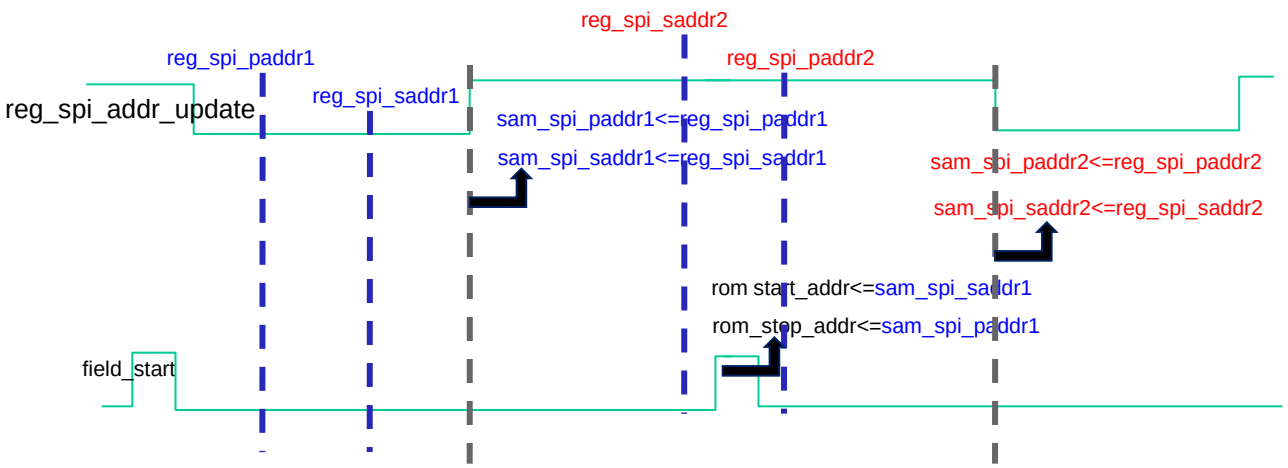


< Group D >

(914) Spi address update

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
914	92	spi_addr_update	0	00	00000000	RW	5	0	Updating read address of osd rom data

register name :spi_addr_update								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
914d (92h)	7	x	0	Reserved				
	6	x	0	Reserved				
	5	x	0	Reserved				
	4	x	0	Reserved				
	3	x	0	Reserved				
	2	x	0	Reserved				
	1	x	0	Reserved				
	0	Spi_addr_update	0	For sampling spi start address and spi stop address at same time Sampling time: rising(spi_addr_update) or falling(spi_addr_update)				



If you want to update spi_saddr and spi_paddr actually, you should reverse spi_addr_update[0] after writing spi_saddr and spi_paddr.

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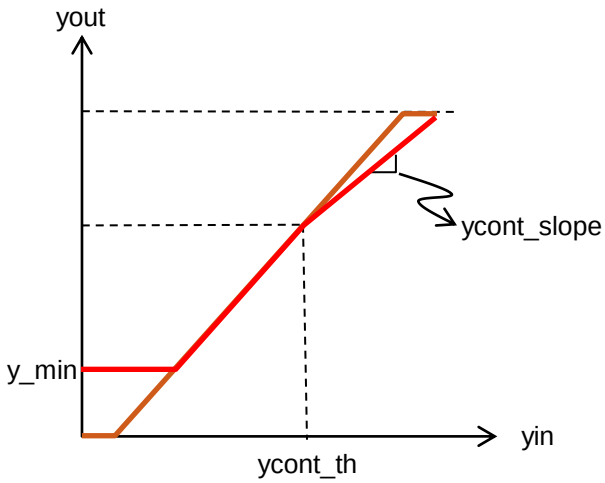
(916) Y min

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
916	94	y_min	0	00	00000000	RW	5	0	Control register for Output Y min

▷ ***y_min***

Y_min is minimum value of output data Y.



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(934) SPI baud rate

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
934	A6	spi_baud_rate	13	0D	00001101	RW	5	0	Spi baud rate

▷ spi_baud_rate

Default value of SPI_baud_rate is 0Dh which corresponds to SPI clock frequency of 1.13MHz. So, before up-loading large amount of data such as OSD data from SPI ROM, SPI_baud_rate must be adjusted to a reasonable value to maximize the data rate.

SPI_baud_rate = 0 : SCK= 27.00 MHz = 27/1
SPI_baud_rate = 1 : SCK= 13.50 MHz = 27/2
SPI_baud_rate = 2 : SCK= 09.50 MHz = 27/3
SPI_baud_rate = 3 : SCK= 06.75 MHz = 27/4
SPI_baud_rate = 4 : SCK= 05.40 MHz = 27/5
SPI_baud_rate = 5 : SCK= 04.50 MHz = 27/6
SPI_baud_rate = 6 : SCK= 03.86 MHz = 27/7
SPI_baud_rate = 7 : SCK= 03.38 MHz = 27/8
SPI_baud_rate = 8 : SCK= 03.00 MHz = 27/9
SPI_baud_rate = 9 : SCK= 02.70 MHz = 27/10
SPI_baud_rate = 10 : SCK= 02.25 MHz = 27/12
SPI_baud_rate = 11 : SCK= 01.69 MHz = 27/16
SPI_baud_rate = 12 : SCK= 01.35 MHz = 27/20
SPI_baud_rate = 13 : SCK= 01.13 MHz = 27/24
SPI_baud_rate = 14 : SCK= 00.96 MHz = 27/28
SPI_baud_rate = 15 : SCK= 00.84 MHz = 27/32

(935) osd opacity

#		register name	default value			type	stage	update	Description
Dec	hex		dec	hex	bin				
935	A7	osd_opac	16	10	00010000	RW	5	0	osd opacity

▷ osd opacity

OSD_opac<4:0> = osd_opacity

OSD image opacity can be controlled(0d ~ 16d).

CB = CB(OSD)

CR = CR(OSD)

(936) spi osd control

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
936	A8	spi_osd_control	u	uu	uuuuuuuu	RW	5	0	spi osd control

register name :spi_addr_update								
register #	bit#	name	default	**u**	default(h)	**uu**	default(b)	**uuuuuuuu**
936d (A8h)	7	Reserved	0	Reserved				
	6	Reserved	0	Reserved				
	5	Reserved	0	Reserved				
	4	Reserved	0	Reserved				
	3	Reserved	0	Reserved				
	2	Reserved	0	Reserved				
	1	osd boundary	0	osd_boundary = '0': Horizontal boundary is not generated. osd_boundary = '1': Horizontal boundary is generated at eac h osd line.				
	0	osd_enable	u	Initial value = '0' if DO9 pad='0' while RSTB='0' else '1' if DO9 pad='1' while RSTB='0'. osd_enable = '0' : osd disable osd_enable = '1' : osd enable				

(937~942) osd data start/stop address

#		register name	default value			type	stage	update	Description
Dec	hex		dec	hex	bin				
937	A9	spi_saddr_h	0	00	00000000	RW	5	0	osd data start address
938	AA	spi_saddr_m	0	00	00000000	RW	5	0	
939	AB	spi_saddr_l	0	00	00000000	RW	5	0	
940	AC	spi_paddr_h	0	00	00000000	RW	5	0	osd data stop address
941	AD	spi_paddr_m	0	00	00000000	RW	5	0	
942	AE	spi_paddr_l	0	00	00000000	RW	5	0	

▷ **spi_saddr/spi_paddr**

OSD data start/stop address. SPI master will read osd command stored in SPI-ROM from OSD data start address to OSD data stop address whenever a field start. Actually, user should reverse reg_spi_addr_update to apply osd data start/stop address after writing osd data start/stop address.

(967) resolution enhance gain

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
967	C7	resol_gain	0	00	00000000	RW	5	0	resolution enhance gain

▷ **resol_gain**

resolution enhance function gain.

(968~972) gen_lock control

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
968	C8	enc_fcnt_genlock	1	01	00000001	RW	5	0	gen_lock control for encoder block
969	C9	enc_rcnt_genlock_h	0	00	00000000	RW	5	0	
970	CA	enc_rcnt_genlock_l	1	01	00000001	RW	5	0	
971	CB	enc_ccnt_genlock_h	0	00	00000000	RW	5	0	
972	CC	enc_ccnt_genlock_l	3	03	00000011	RW	5	0	

▷ **gen_lock control**

gen_lock control for encoder block.

(973) Encoder control

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
973	CD	enc_control	4	04	00000100	RW	5	0	Encoder control

register name : enc_control								
register #	bit#	name	default	**4**	default(h)	**04**	default(b)	**00000100**
973d (CDh)	7	x	x	Reserved				
	6	enc_lpfY_off	0	0b : Luminance low pass filter on 1b : Luminance low pass filter off				
	5	enc_lpfC_off	0	0b : Chrominance low pass filter on 1b : Chrominance low pass filter off,				
	4	enc_colorbar_en	0	color bar on/off				
	3	enc_colorbar_mode	0	0b : 100% color bar, 1b : 75% color bar				
	2	bt656_standard	1	BT656 standard for 525 line system				
	1	enc_monitor_sw	0	monitor switch				
	0	yin_range	0	input Y range 0b : 1~254 1b : 16~235				

▷ ***enc_lpfY-off***

Luminance low-pass filter to transmit analog video data to channel.

Related registers : enc_lpyc0 ~ enc_lpyc4 , enc_lpys → low pass filter coefficients

▷ ***enc_lpfC_off***

Chrominance low-pass filter to transmit analog video data to channel. The bandwidth of chrominance signal is 1.3MHz.

Related registers : enc_lpcc0 ~ enc_lpcc15, enc_lpcsH, enc_lpcsL → low pass filter coefficients.

▷ ***enc_colorbar_en***

Encoder color bar output enable (For Test)

▷ ***enc_colorbar_mode***

100% color or 75% color selection (For Test)

▷ ***bt656_standard***

BT656 standard for 525 line system

▷ ***enc_monitor_sw***

Monitor swithch (For Test)

▷ ***yin_range***

Y input data range selection

(974) Encoder control

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
974	CE	enc_scfreq	u	u	uuuuuuuu	RW	5	0	Subcarrier frequency selection for which TV mode

▷ ***enc_scfreq***

sub-carrier frequency selection

"00" : 3.579545 MHz for (M) NTSC, NTSC-J

"01" : 4.43361875 MHz for (B, D, G, H, I, N) PAL

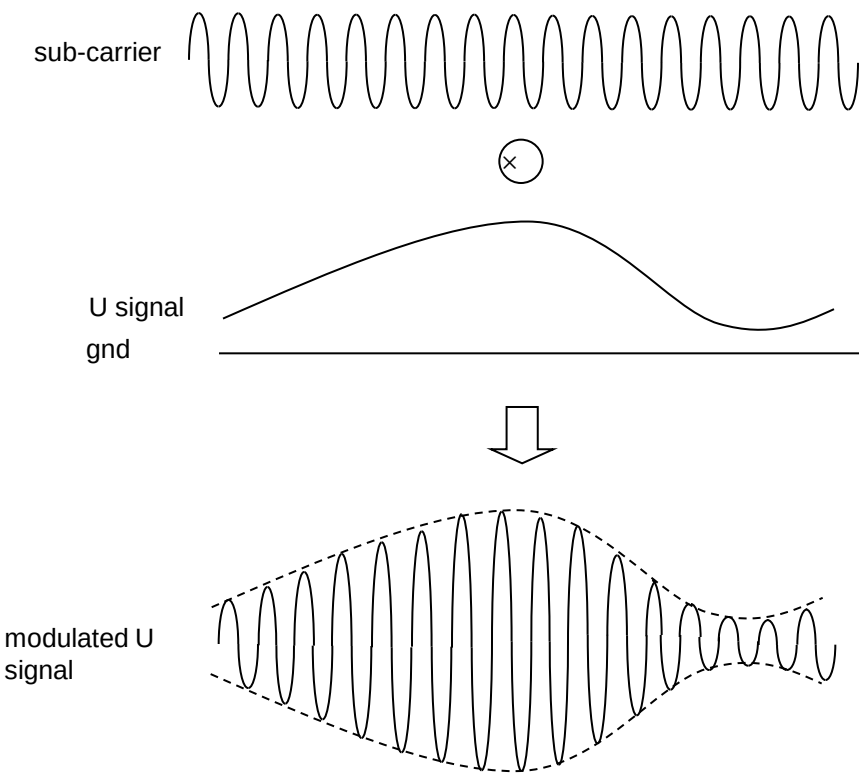
"10" : 3.58205625 MHz for (Nc) PAL

"11" : 3.57561149 MHz for (M) PAL

default value : U ➔ wire-strapping register

Sub-carrier signal is used for modulating chrominance data via QAM

C= U*sin(ωt) + V*cos(ωt)



(975~990) Composite level parameters

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
975	CF	enc_sync	16	10	00010000	RW	5	0	Encoder sync level
976	D0	enc_blankH	0	00	00000000	RW	5	0	Encoder blank level
977	D1	enc_blankL	u	u	uuuuuuuu	RW	5	0	
978	D2	enc_pedestal	u	u	uuuuuuuu	RW	5	0	Encoder pedestal
979	D3	enc_burst	u	u	uuuuuuuu	RW	5	0	Burst amplitude
980	D4	enc_Ygain	u	u	uuuuuuuu	RW	5	0	Y convergence gain from YCbCr to YUV
981	D5	enc_Ugain	u	u	uuuuuuuu	RW	5	0	U convergence gain from YCbCr to YUV
982	D6	enc_Vgain	u	u	uuuuuuuu	RW	5	0	V convergence gain from YCbCr to YUV
983	D7	enc_Yrange_H	3	03	00000011	RW	5	0	max. luminance
984	D8	enc_Yrange_L	32	20	00100000	RW	5	0	
985	D9	enc_Crange_H	1	01	00000001	RW	5	0	max. amplitudes of chrominance
986	DA	enc_Crange_L	u	u	uuuuuuuu	RW	5	0	
987	DB	enc_chroma_max_H	3	03	00000011	RW	5	0	maximum chrominance of composite output
988	DC	enc_chroma_max_L	u	u	uuuuuuuu	RW	5	0	
989	DD	enc_chroma_min_H	0	00	00000000	RW	5	0	minmum chrominance of composite output
990	DE	enc_chroma_min_L	u	u	uuuuuuuu	RW	5	0	

▷ ***enc_sync***

Encoder sync level

▷ ***enc_blank***

Encoder blank level

▷ ***enc_pedestal***

Encoder pedestal level

▷ ***enc_burst***

Burst amplitude

▷ ***enc_Y/U/Vgain***

Conversion gain of YCbCr to YUV

▷ ***enc_Yrange***

Separate Y range into positive and negative regions.

▷ ***enc_Crange***

Define maximum level of Chrominance.

▷ ***enc_chroma_max***

Define maximum level of Composite.

▷ ***enc_chroma_min***

Define minimum level of Composite.

default value : U ➔ wire-strapping register

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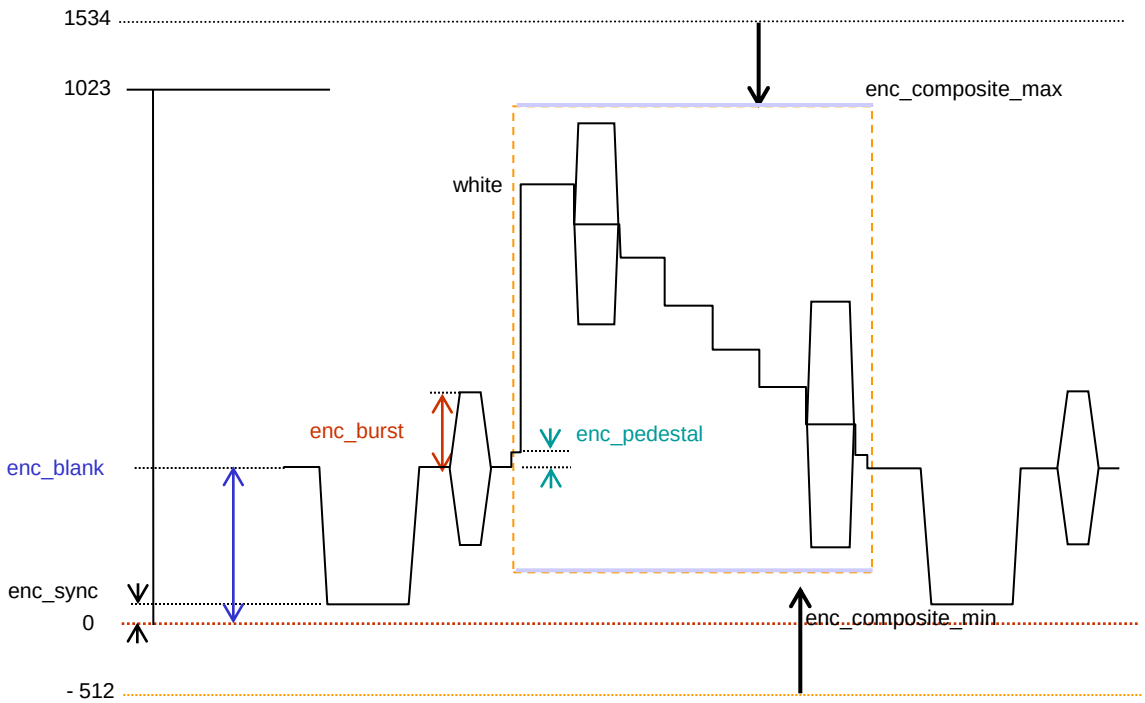
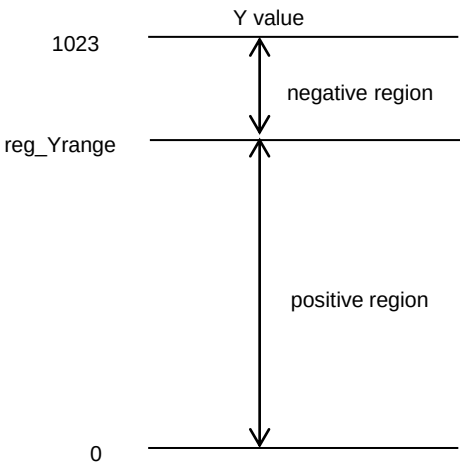
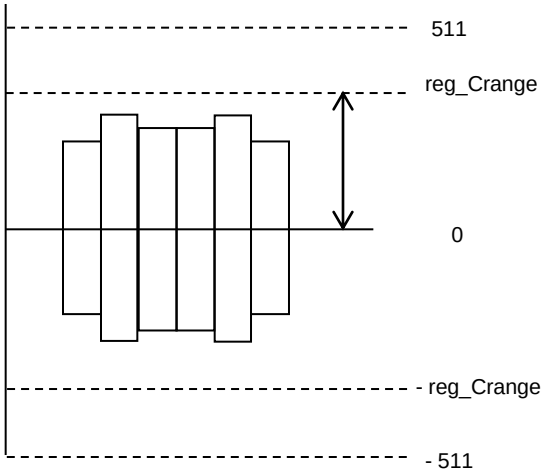


reg_enc_composite_max/min registers define the max. and min. of active data level.



reg_Yrange defines the boundary between positive or negative number of Y before composition.
In colorbar, Y might be negative values. It is the reason why the register exists.



reg_Crange designates the maximum amplitude of chroma.
It can be one of 0 to 511.

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(1016~1019) Subcarrier to horizontal phase offset

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1016	F8	enc_SCH_offset_T	0	00	00000000	RW	5	0	SCH(subcarrier to horizontal) phase offset
1017	F9	enc_SCH_offset_H	0	00	00000000	RW	5	0	
1018	FA	enc_SCH_offset_M	0	00	00000000	RW	5	0	
1019	FB	enc_SCH_offset_L	0	00	00000000	RW	5	0	

▷ **enc_SCH_offset**

Subcarrier to Horizontal phase.

0° = 00 00 00 00 h

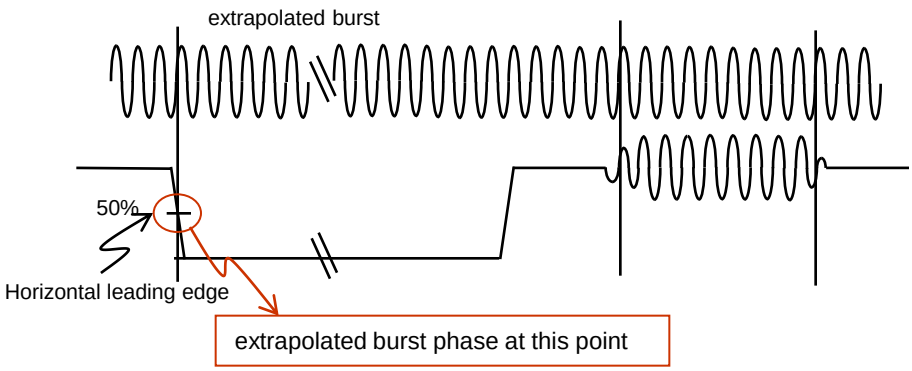
90° = 40 00 00 00 h

180° = 80 00 00 00 h

270° = C0 00 00 00 h

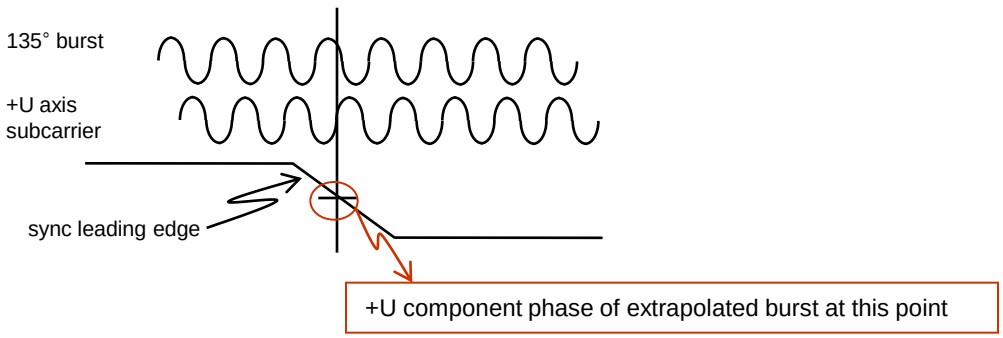
NTSC

Definition: The phase relationship between the leading edge of horizontal sync(at the 50% amplitude point) and the zero crossings of the color burst (by extrapolaing the color burst to the leading edge of sync)



PAL

Definition: The phase of the +U component of the color burst extrapolated to the half-amplitude point of the leading edge of the synchronizing pulse of line 1 of field 1. This means that the phase of the +U axis of the subcarrier is zero relative to the horizontal timing reference point(the mid-point of the leading edge of the line sync pulse)



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(1020) DAC test pattern period

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1020	FC	DAC_tp_period	0	00	00000000	RW	5	0	DAC test pattern period

▷ **DAC_tp_period**

It defines test pattern's change step of DAC test patterns respectively.

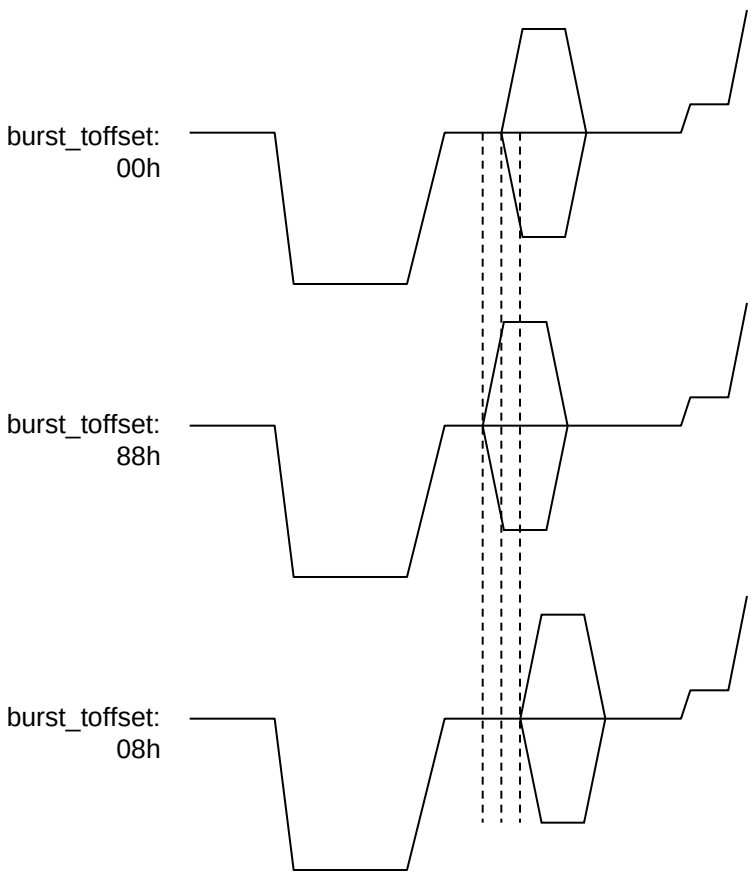
(1021) Burst time offset

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1021	FD	burst_toffset	0	00	00000000	RW	5	0	Burst time +/- offset

▷ **burst_toffset**

It changes burst position on Back Porch.

msb: sign, other bits : magnitude



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(1023) resolution enhance threshold

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1023	FF	resol_th	0	00	00000000	RW	5	0	resolution enhance threshold

▷ **resol_th**

resolution enhance function threshold

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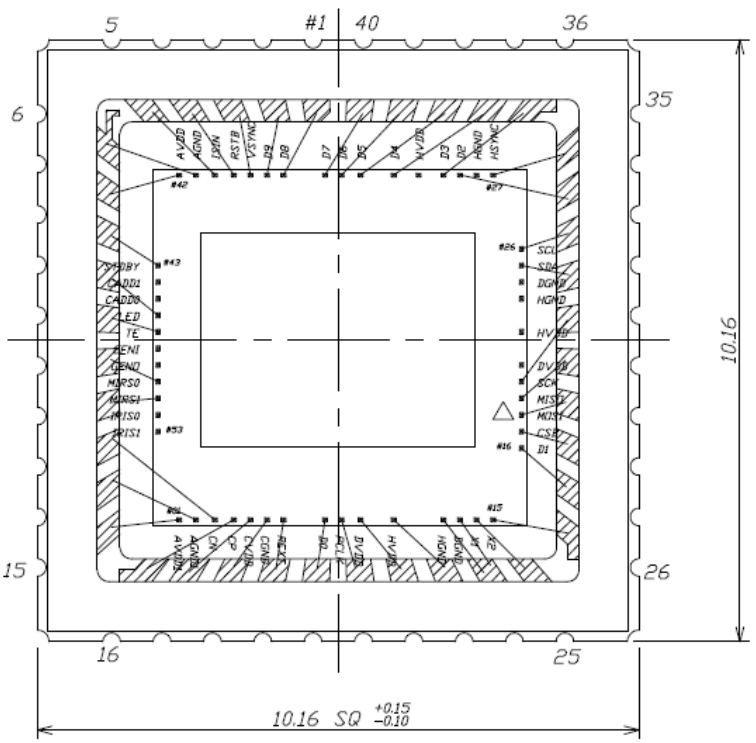
1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

▶ *package information*

IMAGE

TOP VIEW



PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	D8	11	MIRS0	21	PCLK	31	SCK
2	D9	12	MIRS1	22	DVDD	32	SDA
3	VSYNC	13	CN	23	HVDD	33	SCL
4	RSTB	14	AGND1	24	HGND, DGND	34	D2
5	ISIN	15	AVDD1	25	X1	35	HSYNC
6	AGND	16	CP	26	X2	36	D3
7	AVDD	17	CVDD	27	D1	37	D4
8	STDBY	18	CGND	28	CSB	38	D5
9	LED	19	REXT	29	MOSI	39	D6
10	TE	20	D0	30	MISO	40	D7