

POWERTIP TECH. CORP.

DISPLAY DEVICES FOR BETTER ELECTRONIC DESIGN

Specification For Approval

【產品規格書】

Customer : _____

Model Type : LCD Module

Sample Code : _____

Mass Production Code : PC1602ARS-ENH-A

Edition : 0

Customer Sign	Sales Sign	Approved By	Prepared By

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DISPLAY DEVICES FOR BETTER ELECTRONIC DESIGN

1. SPECIFICATIONS

1.1 Features

- 16-characters, two-lines liquid crystal display of 5*7 dot matrix + cursor
- 1/16 Duty, 1/4 bias
- STN LCD, positive, gray display
- Reflective LCD
- 6 o' clock viewing angle
- 4 bits or 8 bits parallel data input

1.2 Mechanical Specifications

- Outline dimension : 66.7mm(L)* 23.3mm(W)*4.7mm max.(H)
- Viewing area : 61.0mm * 15.9mm
- Active area : 56.2mm * 11.85mm
- Dot size : 0.55mm * 0.65mm
- Dot pitch : 0.6mm * 0.7mm
- Character Size : 2.95mm * 5.55mm

1.3 Absolute Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Power supply Voltage	V_{DD}	-	-0.3	7.0	V
LCD drive Supply voltage	$V_{DD}-V_O$	-	$V_{DD}-13.5$	$V_{DD}+0.3$	V
Input voltage	V_{IN}	-	-0.3	$V_{DD}+0.3$	V
Operating temperature	T_{OPR}	-	0	50	°C
Storage temperature	T_{STG}	-	-20	70	°C
Humidity	HD	-	-	90	%RH

1.4 DC Electrical Characteristics

$V_{DD}=+5V\pm 10\%$, $V_{SS}=0V$, $T_A=25^\circ C$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic Supply voltage	V_{DD}	-	4.5	5.0	5.5	V
“H” input voltage	V_{IH}	-	2.2	-	V_{DD}	V
“L” input voltage	V_{IL}	-	-0.3	-	0.8	V
“H” output voltage	V_{OH}	$I_{OH}=-0.25mA$	2.4	-	-	V
“L” output voltage	V_{OL}	$I_{OL}=1.2mA$	-	-	0.4	V
Supply current	I_{DD}	$V_{DD}=5V$	-	2.0	3.0	mA
LCD driving voltage	V_{OP}	$V_{DD}-V_O$	4.0	4.2	4.4	V



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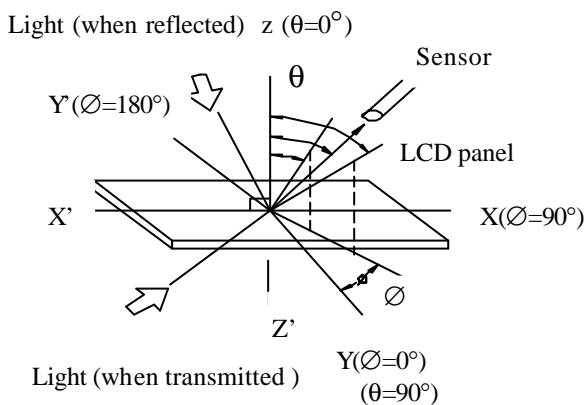
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1.5 Optical Characteristics

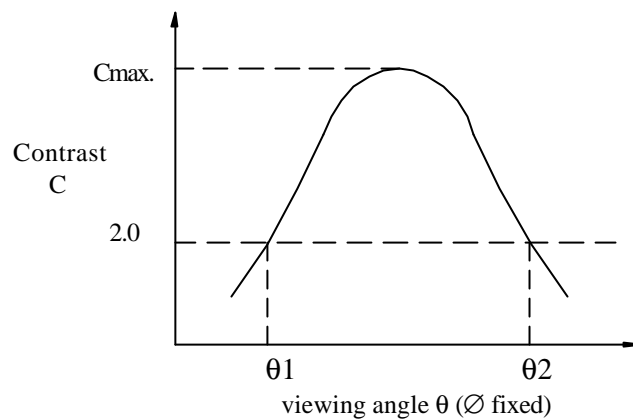
1/16 duty, 1/4 bias, $V_{OP}=4.2V$, $T_a=25^{\circ}C$

Item	Symbol	Conditions	Min.	Typ.	Max	Reference
Viewing angle	θ	$C \geq 2.0, \varnothing = 0^{\circ}$	45°	-	-	Notes 1 & 2
Contrast	C	$\theta = 25^{\circ}, \varnothing = 0^{\circ}$	5	7	-	Note 3
Response time(rise)	T_r	$\theta = 25^{\circ}, \varnothing = 0^{\circ}$	-	148ms	-	Note 4
Response time(fall)	T_f	$\theta = 25^{\circ}, \varnothing = 0^{\circ}$	-	302ms	-	Note 4

Note 1: Definition of angles θ and \varnothing



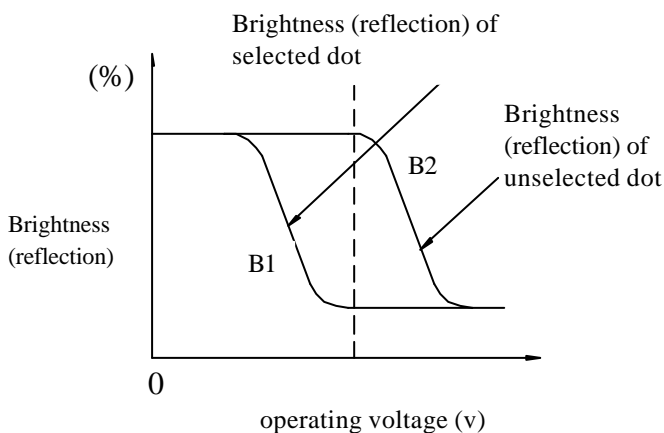
Note 2: Definition of viewing angles θ_1 and θ_2



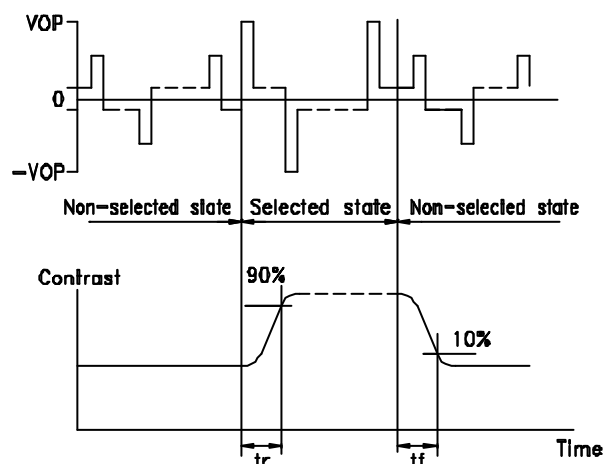
Note : Optimum viewing angle with the naked eye and viewing angle θ at C_{max} . Above are not always the same

Note 3: Definition of contrast C

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$



Note 4: Definition of response time



Note: Measured with a transmissive LCD panel which is displayed 1 cm^2

V_{OPR} : Operating voltage f_{FRM} : Frame frequency
 t_r : Response time (rise) t_f : Response time (fall)

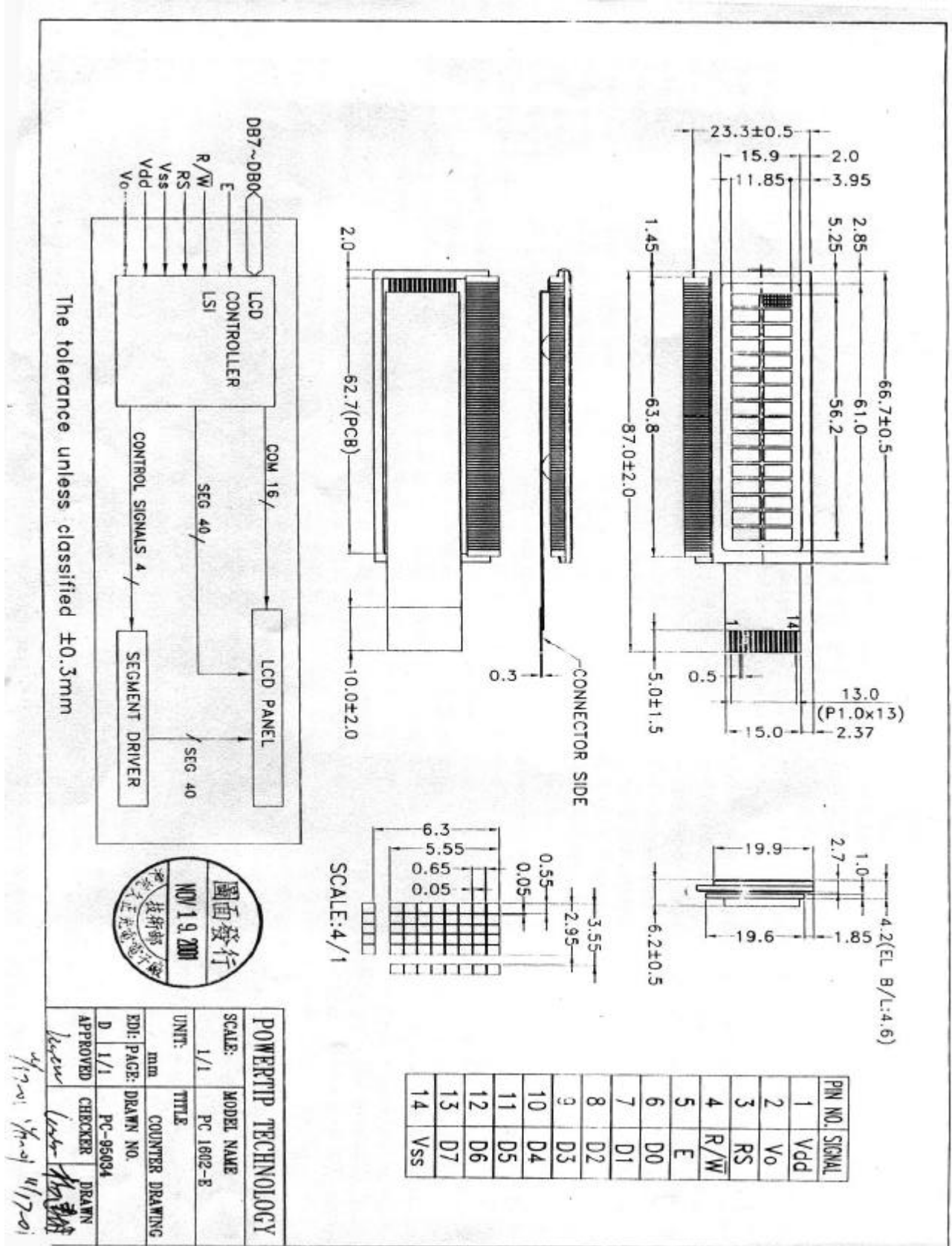


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2. MODULE STRUCTURE

2.1 Counter Drawing

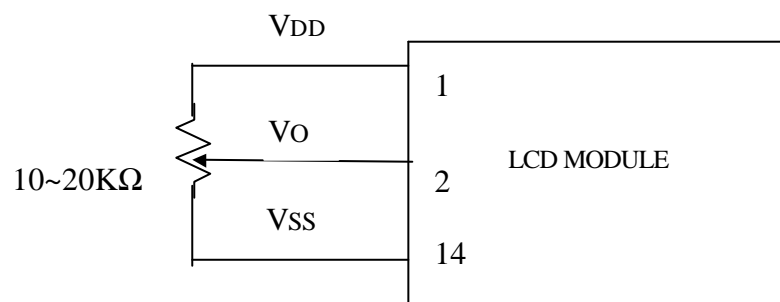


POWER TIP TECHNOLOGY	
SCALE: 1/1	MODEL NAME: PC 1602-B
UNIT: mm	TITLE: COUNTER DRAWING
EDI: PAGE: DRAWN NO.	
D 1/1	PC-95034
APPROVED	CHECKER
<i>Lee</i>	<i>Lee</i>
	DRAWN
	<i>Lee</i>

2.2 Interface Pin Description

Pin No.	Symbol	Function
1	VDD	Power Supply ($V_{DD} > V_{SS}$)
2	VO	Operating voltage (LCD Driver)
3	RS	Register Selection input High = Data register Low = Instruction register (for write) Busy flag address counter (for read)
4	$\overline{R/W}$	$\overline{R/W}$ signal input is used to select the read/write mode High = Read mode, Low = Write mode
5	E	Start enable signal to read or write the data
6~9	D0 ~ D3	Four low order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCD module. These four are not used during 4-bit operation.
10~13	D4~D7	Four high order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCD module. D7 can be used as a busy flag.
14	VSS	Power Supply ($V_{SS}=0$)

Contrast Adjust

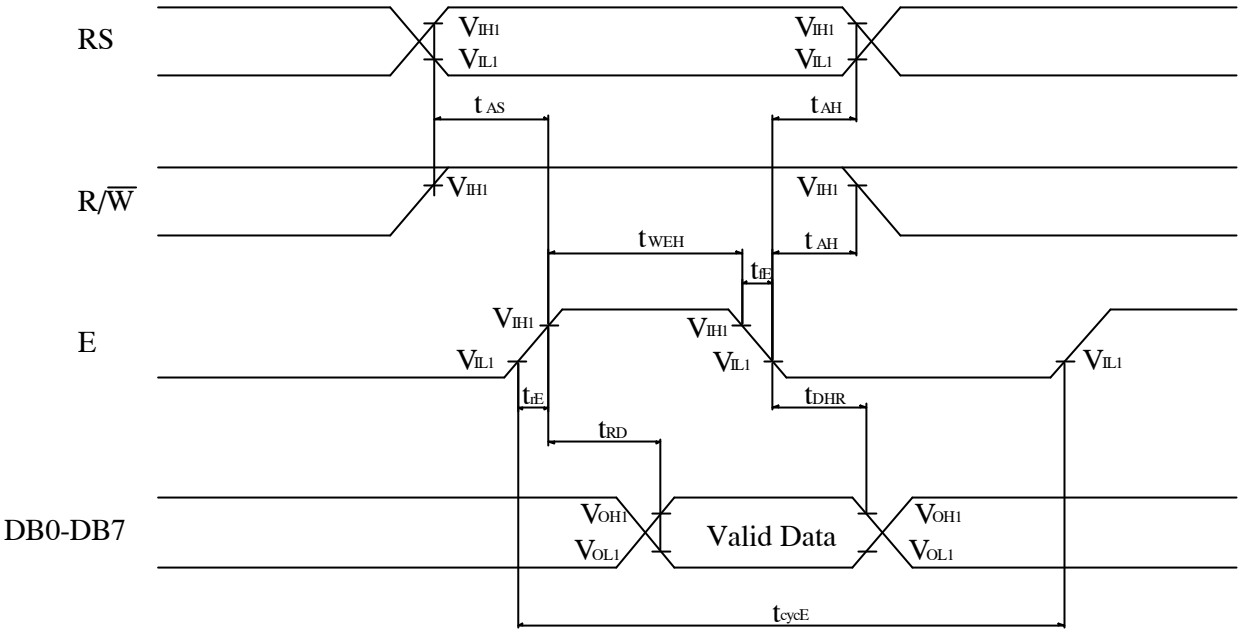


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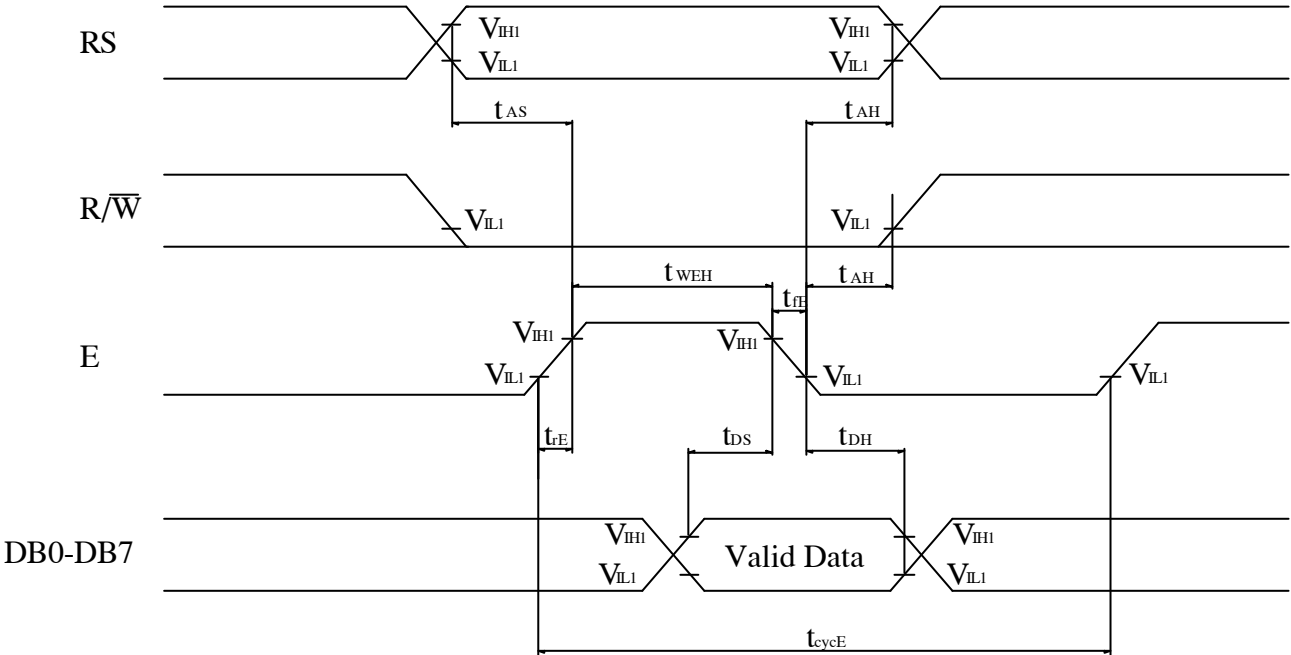
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2.3 Timing Characteristics

• Read cycle



• Write cycle



• Read cycle

VDD=5.0V ± 10%, VSS=0V, Ta=25

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{CYCE}	-	500	-	-	ns
Enable "H" level pulse width	t_{WEH}	-	300	-	-	ns
Enable rise/fall time	$t_{\text{rE}}, t_{\text{fE}}$	-	-	-	25	ns
RS,R/W setup time	t_{AS}	-	60 ¹	-	-	ns
			100 ²			
RS,R/W address hold time	t_{AH}	-	10	-	-	ns
Read data output delay	t_{RD}	$C_{\text{L}}=100\text{pF}$	-	-	190	ns
Read data hold time	t_{DHR}	-	20	-	-	ns

• Write cycle

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{CYCE}	-	500	-	-	ns
Enable "H" level pulse width	t_{WEH}	-	300	-	-	ns
Enable rise/fall time	$t_{\text{rE}}, t_{\text{fE}}$	-	-	-	25	ns
RS,R/W setup time	t_{AS}	-	60 ¹	-	-	ns
			100 ²			
RS,R/W address hold time	t_{AH}	-	10	-	-	ns
Data setup time	t_{DS}	-	100	-	-	ns
Write data hold time	t_{DH}	-	10	-	-	ns

Notes: 1: 8-bit operation mode

2: 4-bit operation mode

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2.4 Display Command

Instructions	Instruction Code										Description	Execution Time(max) ($t_{oc}=250\text{KHZ}$)	
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Clear Display	0	0	0	0	0	0	0	0	0	0	1	Clear entire display area, restore display from shift, and load address counter with DD RAM address 00H	1.64ms
Display/Cursor Home	0	0	0	0	0	0	0	0	0	1	×	Restore display from shift and load address counter with DD RAM address 00H	1.64ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S		Specify direction of cursor movement and display shift mode. This operation takes place after each data transfer (read/write)	40 μ s
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B		Specify activation of display (D) cursor (C) and blinking of character at cursor position (B).	40 μ s
Display/Cursor Shift	0	0	0	0	0	1	S/C	R/L	×	×		Shift display or move cursor.	40 μ s
Function Set	0	0	0	0	1	DL	N	F	×	×		Set interface data length (D), number of display line (N), and character font (F).	40 μ s
RAM Address Set	0	0	0	1	ACG							Load the address counter with a CG RAM address. Subsequent data access is for CG RAM data.	40 μ s
DD RAM Address Set	0	0	1	ADD							Load the address counter with a DD RAM address. Subsequent data access is for DD RAM data.	40 μ s	
Busy Flag/Address Counter Read	0	1	AC								Read Busy Flag (BF) and contents of Address Counter (AC).	40 μ s	
CG RAM/DD RAM Data Write	1	0	Write data								Write data to CG RAM or DD RAM.	40 μ s	
CG RAM/DD RAM Data Read	1	1	Read data								Read data from CG RAM or DD RAM	40 μ s	

Note 1: Symbol “ * ” signifies an insignificant bit (disregards).

Note 2: Correct input value for “ N ” is predetermined for each model.



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2.5 Character Pattern

CHARACTER PATTERN(SH/EH,NH)

Upper 4 Bits / Lower 4 Bits	LLLL	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL (1)	CG RAM		0	1	2	3	4			8	9	A	B	C	D
LLLH (2)	(2)	!	2	A	Q	a	9			7	8	W		U	V
LLHL (3)	(3)	"	2	B	R	b	r			E	6	t	u	W	X
LLHH (4)	(4)	#	3	C	S	c	s			H	6	W	!	Q	Y
LHLL (5)	(5)	\$	4	D	T	d	t			3	7	t	z	0	1
LHLH (6)	(6)	%	5	E	U	e	u			K	E	a	X	U	V
LHHL (7)	(7)	&	6	F	V	f	v			0	8	W	z	W	X
LHHH (8)	(8)	'	7	G	W	g	w			J	3	a	I	'	1
HLLL (1)	(1)	(8	H	X	h	x			0	K	o	U	"	2
HLLH (2)	(2))	9	I	Y	i	y			V	0	o	↑	'	3
HLHL (3)	(3)	*	:	J	Z	j	z			Φ	K	o	↓	0	4
HLHH (4)	(4)	+	;	K	[k]			4	7	"	W	0	5
HHLL (5)	(5)	,	<	L	o	l	o			W	M	0	W	U	6
HHLH (6)	(6)	-	=	M	J	m	5			6	H	o	W	*	7
HHHL (7)	(7)	.	>	N	^	n	4			W	0	0	z	o	8
HHHH (8)	(8)	/	?	O	_	o	3			3	T	e	.	o	9

Specification Revision History

Model No. :PC1602ARS-ENH-A				Total pages : 11	
No.	Version	Page	Description	Engineer	Date
1	0		Revised Contents	James	2002/05/13