

DUAL 4-BIT SERIAL-IN/PARALLEL-OUT SHIFT REGISTER

FEATURES

- Output capability: standard
- I^{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4015 are high-speed Si-gate CMOS devices and are pin compatible with the "4015" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4015 are dual edge-triggered 4-bit static shift registers (serial-to-parallel converters). Each shift register has a serial data input (1D and 2D), a clock input (1CP and 2CP), four fully buffered parallel outputs (1Q₀ to 1Q₃ and 2Q₀ to 2Q₃) and an overriding asynchronous master reset (1MR and 2MR). Information present on nD is shifted to the first register position, and all data in the register is shifted one position to the right on the LOW-to-HIGH transition of nCP. A HIGH on nMR clears the register and forces nQ₀ to nQ₃ to LOW, independent of nCP and nD.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay nCP to nQ _n	C _L = 15 pF V _{CC} = 5 V	16	18	ns
f _{max}	maximum clock frequency		110	74	MHz
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per register	notes 1 and 2	35	40	pF

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

Σ (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}

For HCT the condition is V_I = GND to V_{CC} - 1.5 V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).

16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
5, 4, 3, 10	1Q ₀ to 1Q ₃	flip-flop outputs
6, 14	1MR, 2MR	asynchronous master reset inputs (active HIGH)
7, 15	1D, 2D	serial data inputs
8	GND	ground (0 V)
9, 1	1CP, 2CP	clock inputs (LOW-to-HIGH, edge-triggered)
13, 12, 11, 2	2Q ₀ to 2Q ₃	flip-flop outputs
16	V _{CC}	positive supply voltage

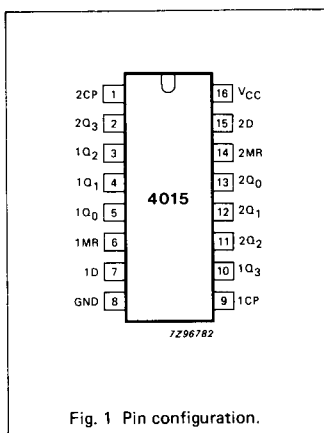


Fig. 1 Pin configuration.

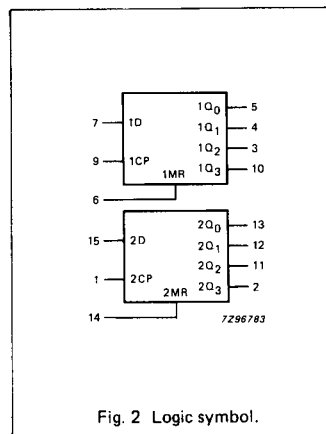


Fig. 2 Logic symbol.

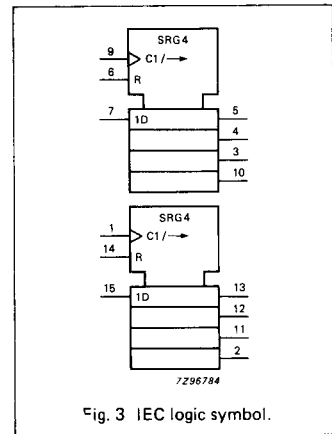


Fig. 3 IEC logic symbol.

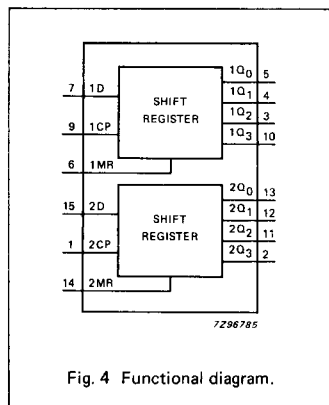


Fig. 4 Functional diagram.

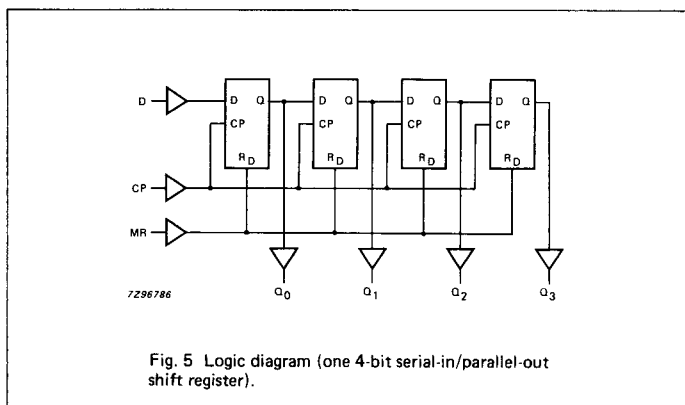


Fig. 5 Logic diagram (one 4-bit serial-in/parallel-out shift register).

FUNCTION TABLE

INPUTS				OUTPUTS			
n	nCP	nD	nMR	nQ ₀	nQ ₁	nQ ₂	nQ ₃
1	↑	D ₁	L	D ₁	X	X	X
2	↑	D ₂	L	D ₂	D ₁	X	X
3	↑	D ₃	L	D ₃	D ₂	D ₁	X
4	↑	D ₄	L	D ₄	D ₃	D ₂	D ₁
	↓	X	L	no change			
	X	X	H	L	L	L	L

H = HIGH voltage level

L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH clock transition

↓ = HIGH-to-LOW clock transition

n = number of clock pulse transitions

D_n = either HIGH or LOW

APPLICATIONS

- Serial-to-parallel converter
- Buffer stores
- General purpose register

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HC									V _{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay nCP to nQ _n		52 19 15	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL}	propagation delay nMR to nQ _n		44 16 13	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 7	
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6	
t _W	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6	
t _W	master reset pulse width HIGH	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	
t _{rem}	removal time nMR to nCP	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7	
t _{su}	set-up time nD to nCP	60 12 10	8 3 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8	
t _h	hold time nD to nCP	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8	
f _{max}	maximum clock pulse frequency	6.0 30 35	33 100 119		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nD	0.30
nMR	1.50
nCP	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay nCP to nQ _n		21	35		44		53	ns	4.5	Fig. 6
t _{PHL}	propagation delay nMR to nQ _n		18	35		44		53	ns	4.5	Fig. 7
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t _W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 6
t _W	master reset pulse width HIGH	16	5		20		24		ns	4.5	Fig. 7
t _{rem}	removal time nMR to nCP	20	10		25		30		ns	4.5	Fig. 7
t _{su}	set-up time nD to nCP	12	4		15		18		ns	4.5	Fig. 8
t _h	hold time nD to nCP	5	−2		5		5		ns	4.5	Fig. 8
f _{max}	maximum clock pulse frequency	30	67		24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

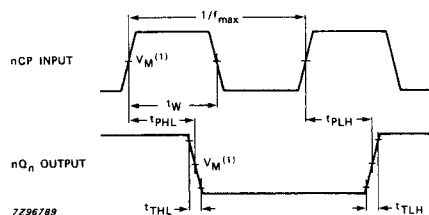


Fig. 6 Waveforms showing the clock (nCP) to output (nQ_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

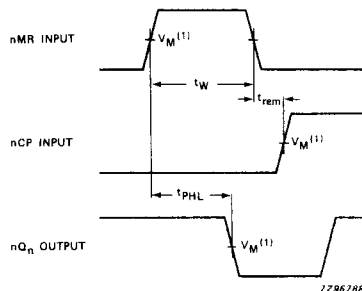


Fig. 7 Waveforms showing the master reset (nMR) pulse width, the master reset to output (nQ_n) propagation delay and the master reset to clock (nCP) removal time.

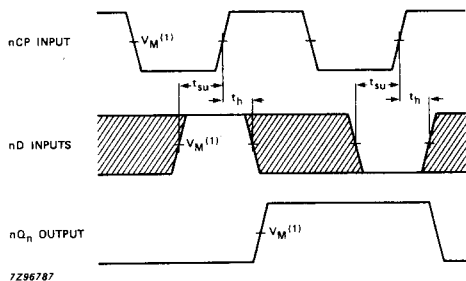


Fig. 8 Waveforms showing the data set-up and hold times for nD inputs.

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.