

## 7-STAGE BINARY RIPPLE COUNTER

### FEATURES

- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT4024 are high-speed Si-gate CMOS devices and are pin compatible with the "4024" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4024 are 7-stage binary ripple counters with a clock input (CP), an overriding asynchronous master reset input (MR) and seven fully buffered parallel outputs (Q<sub>0</sub> to Q<sub>6</sub>).

The counter advances on the HIGH-to-LOW transition of CP.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of CP.

Each counter stage is a static toggle flip-flop.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

### APPLICATIONS

- Frequency dividing circuits
- Time delay circuits

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>0</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	14	14	ns
f <sub>max</sub>	maximum clock frequency		90	70	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	25	27	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

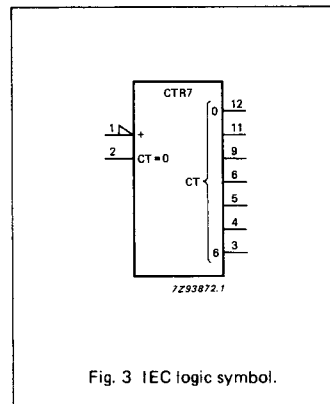
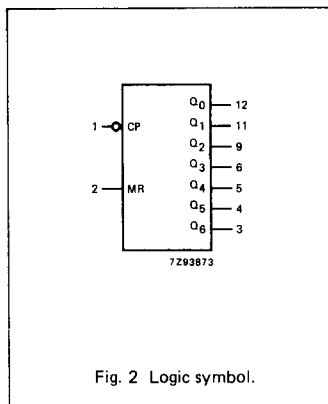
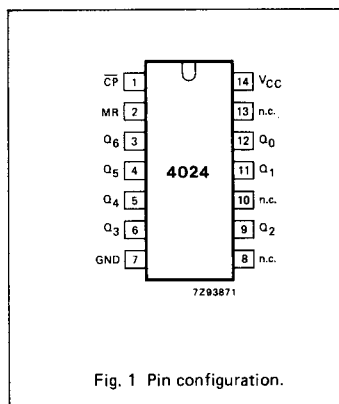
### PACKAGE OUTLINES

14-lead DIL; plastic (SOT27).

14-lead mini-pack; plastic (SO14; SOT108A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP	clock input (HIGH-to-LOW, edge-triggered)
2	MR	master reset input (active HIGH)
12, 11, 9, 6, 5, 4, 3	Q <sub>0</sub> to Q <sub>6</sub>	parallel outputs
7	GND	ground (0 V)
8, 10, 13	n.c.	not connected
14	V <sub>CC</sub>	positive supply voltage



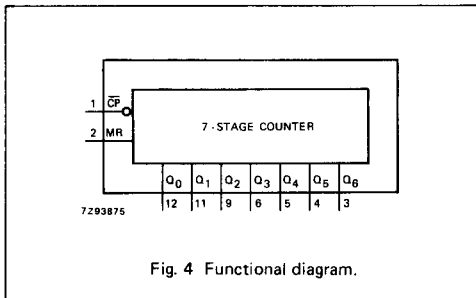


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{CP}$	MR	$Q_n$
↑	L	no change
↓	L	count
X	H	L

H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 ↑ = LOW-to-HIGH clock transition  
 ↓ = HIGH-to-LOW clock transition

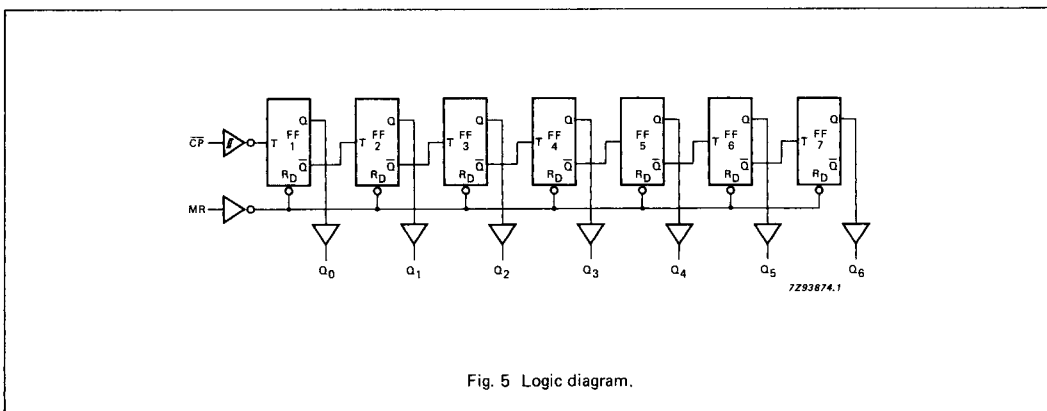


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>0</sub>		47 17 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub>	propagation delay MR to Q <sub>0</sub>		63 23 18	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay Q <sub>n</sub> to Q <sub>n+1</sub>		25 9 7	80 16 14		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	master reset pulse width HIGH	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>rem</sub>	removal time MR to CP	50 10 9	6 2 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 6
f <sub>max</sub>	maximum clock pulse frequency	6.0 30 35	27 82 98		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}$	0.75
MR	0.85

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{CP}$ to Q <sub>0</sub>		17	35		44		53	ns	4.5	Fig. 6
t <sub>PHL</sub>	propagation delay MR to Q <sub>0</sub>		21	40		50		60	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay Q <sub>n</sub> to Q <sub>n+1</sub>		9	16		20		24	ns	4.5	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	16	9		20		24		ns	4.5	Fig. 6
t <sub>W</sub>	master reset pulse width HIGH	16	6		20		24		ns	4.5	Fig. 6
t <sub>rem</sub>	removal time MR to $\overline{CP}$	10	0		13		15		ns	4.5	Fig. 6
f <sub>max</sub>	maximum clock pulse frequency	30	64		24		20		MHz	4.5	Fig. 6

## AC WAVEFORMS

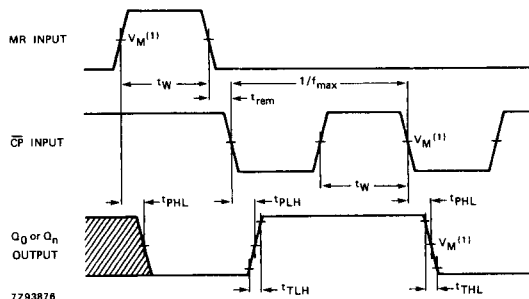


Fig. 6 Waveforms showing the clock ( $\overline{CP}$ ) to output ( $Q_n$ ) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

Also showing the master reset (MR) pulse width, the master reset to output ( $Q_n$ ) propagation delays and the master reset to clock ( $\overline{CP}$ ) removal time.

## Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .