National Semiconductor

PRODUCT BRIEF
August 2004
Revision 1.1

PC8374T
SafeKeeper™ Desktop TrustedI/O

General Description

The National Semiconductor PC8374T Advanced I/O product is a member of the PC837x SuperI/O family. All PC837x devices are highly integrated and are pin and software compatible, thus providing drop-in interchangeability and enabling a variety of assembly options using only a single motherboard and BIOS.

PC8374T integration allows for a reduced system board size and saves on total system cost.

The PC8374T includes legacy SuperI/O functions, Trusted Platform Module (TPM), system glue functions, health monitoring and control, commonly used functions such as GPIO, and ACPI-compliant Power Management support.

The Trusted Platform Module provides a solution for PC security, based on the TCG standard. The complete security solution includes hardware, software, and firmware.

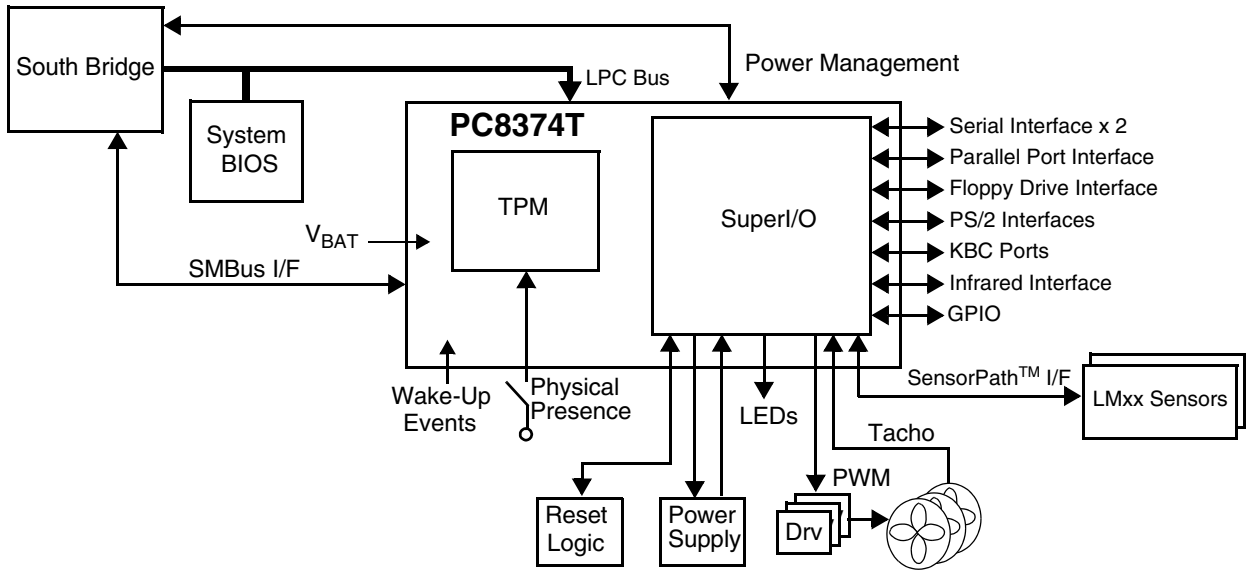
The PC8374T integrates miscellaneous analog and digital system glue functions to reduce the number of discrete components required. The host communicates with the functions integrated in the PC8374T through an LPC Bus Interface.

The PC8374T supports both I/O and memory mapping of module registers and enables building legacy-free systems.

Outstanding Features

- TCG 1.1b based Trusted Platform Module (TPM)
  - — Integrated non-volatile secure storage
  - — Hardware and software protection schemes
  - — Tamper resistance schemes
  - — Pin compatible to integrated TPM 1.2 device
- Legacy modules: Parallel Port, Floppy Disk Controller (FDC), two Serial Ports, Serial InfraRed Port and a Keyboard and Mouse Controller (KBC)
- Glue functions to complement the South Bridge functionality
- System health support, including SensorPath™ sensor interface, and fan monitor and control
- V_{SB3}-powered Power Management with 19 wake-up sources
- Controls three LED indicators
- 16 GPIO pins with a variety of wake-up options
- I/O-mapped and memory-mapped registers
- 128-pin PQFP package

PC8374T System Block Diagram



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Features

Trusted Platform Module (TPM)

- TCG 1.1b compliant
- Processing Unit
  - 16-bit embedded RISC processor core
- Internal Memory
  - On-chip Non-Volatile memory for secure storage
  - On-chip data RAM
- Host Interface
  - Using LPC Bus
  - Command/Data/Status standard interface
- Secured General-Purpose I/O (GPIO)
  - Internal processor controlled
  - Three GPIO pins, one used for Physical Presence
  - I/O pins individually configured as input or output
  - Configurable internal pull-up resistors
  - Owner authorization control
- Power Management Controller (PMC); power modes, switched by software or hardware
- TPM Firmware
  - V_{SB3} RAM-based storage for loadable keys
- Tamper Resistance
  - Clock Jitter protection
    - Protection on reference clock
    - Protection of security functions from LPC clock jitter
  - Power analysis resistance
  - Low and High Frequency monitor
  - Voltage attack detector
    - Low Voltage
    - Glitch and brownout detector
  - Secure storage contents protection
  - Permanent disable of all TPM test mechanisms when locked

System Health Support

- SensorPath interface to sensors optimizes digital/analog partitioning
  - Simplifies board design and routing
  - Supports distributed sensors and centralized control
  - Health monitoring is self-contained and requires minimal host attention
  - Faster boot time
  - Off loads SMBus, and enables ASF compliance
- Fan Monitor and Control
  - Three PWM-based fan controls
  - Four 16-bit resolution tachometer inputs
  - Software or local temperature feedback control
- Heceta6-compatible register set accessible via the LPC interface and SMBus
  - Supports the following combinations of LMxx devices:
    - LM96011
    - LM96011 and LM95010
    - LM96012
    - LM96010
  - Simultaneous read support via LPC interface and SMBus

General-Purpose Modules

- All 16 GPIO pins powered by V_{SB3}
- Each pin individually configured as input or output
- Programmable features for each output pin:
  - Drive type (open-drain, push-pull or TRI-STATE®)
  - TRI-STATE on detection of falling V_{DD3} for V_{SB3}-powered pins driving V_{DD}-supplied devices
- Programmable option for internal pull-up resistor on each input pin (some with internal pull-down resistor option)
- Lock option for the configuration and data of each output pin
- 15 GPIO pins generate IRQ/$\overline{\text{SIOPME}}$/$\overline{\text{SMI}}$ for wake-up events; each GPIO has separate:
  - Enable control of event status routing to IRQ
  - Enable control of event status routing to $\overline{\text{SIOPME}}$
  - Polarity and edge/level selection
    - Programmable debouncing

Glue Functions

- Generates the power-related signals:
  - Main Power good
  - Power distribution control (for switching between Main and Standby regulators)
  - Resume reset (Master Reset) according to the 5V standby supply status
  - Main power supply turn on ($\overline{\text{PS\_ON}}$)
- Voltage translation between 2.5V or 3.3V levels (DDC) and 5V levels (VGA) for the SMBus serial clock and data signals
- Isolation circuitry for the SMBus serial clock and data signals
- Buffers $\overline{\text{PCI\_RESET}}$ to generate three reset output signals
- Generates “highest active supply” reference voltage
  - Based on 3.3V and 5V Main supplies
  - Based on 3.3V and 5V Standby supplies
- High-current LED driver control for Hard Disk Drive activity indication
- Software selectable alternative functionality, through pin multiplexing

Features (Continued)

Bus Interface

- LPC Bus Interface
  - Based on Intel's *LPC Interface Specification Revision 1.1, August 2002*
  - I/O, Memory and 8-bit Firmware Memory read and write cycles, Firmware Memory writes may insert wait cycles
  - Up to four 8-bit DMA channels
  - Serial IRQ (SERIRQ)
  - Supports SuperI/O register memory and I/O mapping
- Configuration Control
  - PnP Configuration Register structure
  - Compliant with *PC01 Specification Revision 1.0, 1999-2000*
  - Base Address strap ($\overline{\text{BADDR}}$) to setup the address of the Index-Data register pair (defaults to 2Eh/2Fh)
    - TPM Index-Data register pair Base Address set by the TPM (defaults to 7Eh/7Fh) or via SuperI/O Configuration registers
  - Flexible resource allocation for all logical devices:
    - Relocatable base address
    - 15 IRQ routing options to serial IRQ
    - Up to four optional 8-bit DMA channels
  - Configurable feature sets:
    - V_{SB3}-powered pin multiplexing

Legacy Modules

- Serial Ports 1 and 2
  - Software compatible with the NS16550A and NS16450
  - Support shadow register for write-only bit monitoring
  - Data rates up to 1.5 Mbaud
- Serial Infrared Port (SIR)
  - Software compatible with the 16550A and the 16450
  - Shadow register support for write-only bit monitoring
  - HP-SIR
  - ASK-IR option of SHARP-IR
  - DASK-IR option of SHARP-IR
  - Consumer Remote Control supports RC-5, RC-6, NEC, RCA and RECS 80
- IEEE 1284-compliant Parallel Port
  - ECP, with Level 2 (14 mA sink and source output buffers)
  - Software or hardware control
  - Enhanced Parallel Port (EPP) compatible with EPP 1.7 and EPP 1.9
  - Supports EPP as mode 4 of the Extended Control Register (ECR)
  - Selection of internal pull-up or pull-down resistor for Paper End (PE) pin
  - Supports a demand DMA mode mechanism and a DMA fairness mechanism for improved bus utilization
  - Protection circuit that prevents damage to the parallel port when a printer connected to it is powered up or is operated at high voltages (in both cases, even if the PC8374T is in power-down state)
- Floppy Disk Controller (FDC)
  - Software compatible with the PC8477 (the PC8477 contains a superset of the FDC functions in the μDP8473, NEC μPD765A/B and N82077 devices)
  - Error-free handling of data overrun and underrun
  - Programmable write protect
  - Supports FM and MFM modes
  - Supports Enhanced mode command for three-mode Floppy Disk Drive (FDD)
  - Perpendicular recording drive support for 2.88 MBytes
  - Burst (16-byte FIFO) and Non-Burst modes
  - Full support for IBM Tape Drive Register (TDR) implementation of AT and PS/2 drive types
  - High-performance digital separator
  - Supports fast tape drives (2 Mbps) and standard tape drives (1 Mbps, 500 Kbps and 250 Kbps)
- Keyboard and Mouse Controller (KBC)
  - 8-bit microcontroller, software compatible with 8042AH and PC87911
  - Standard interface (60h, 64h, IRQ1 and IRQ12)
  - Supports two external swapable PS/2 interfaces for keyboard and mouse
  - Programmable, dedicated quasi-bidirectional I/O lines (GA20/P21, $\overline{\text{KBRST}}$/P20)

Power Management

- Supports *ACPI Specification Revision 2.0b, July 27, 2000*
- System Wake-Up Control (SWC)
  - Optional routing of events to generate SCI ($\overline{\text{SIOPME}}$) on detection of:
    - Keyboard or Mouse events
    - Ring Indication $\overline{\text{RI}}$ on each of the two serial ports
    - General-Purpose Input Events from 15 GPIO pins
    - IRQs of the Keyboard and Mouse Controller
    - IRQs of the other internal modules
  - Optional routing of the SCI ($\overline{\text{SIOPME}}$) to generate IRQ (SERIRQ)
  - Implements the GPE1_BLK of the ACPI General Purpose (Generic) Register blocks with "child" events
  - V_{SB3}-powered event detection and event-logic configuration
- Enhanced Power Management (PM), including:
  - Special configuration registers for power down
  - Low-leakage pins
  - Low-power CMOS technology
  - Ability to disable all modules
  - High-current LED drivers control (two LEDs) for power status indication with:
    - Standard blinking, controlled by software
    - Advanced blinking, controlled by power supply status, sleep state or software
    - Special blinking, controlled by power supply status, sleep state and software bit
  - V_{BAT}-powered indication of the Main power supply state before an AC power failure

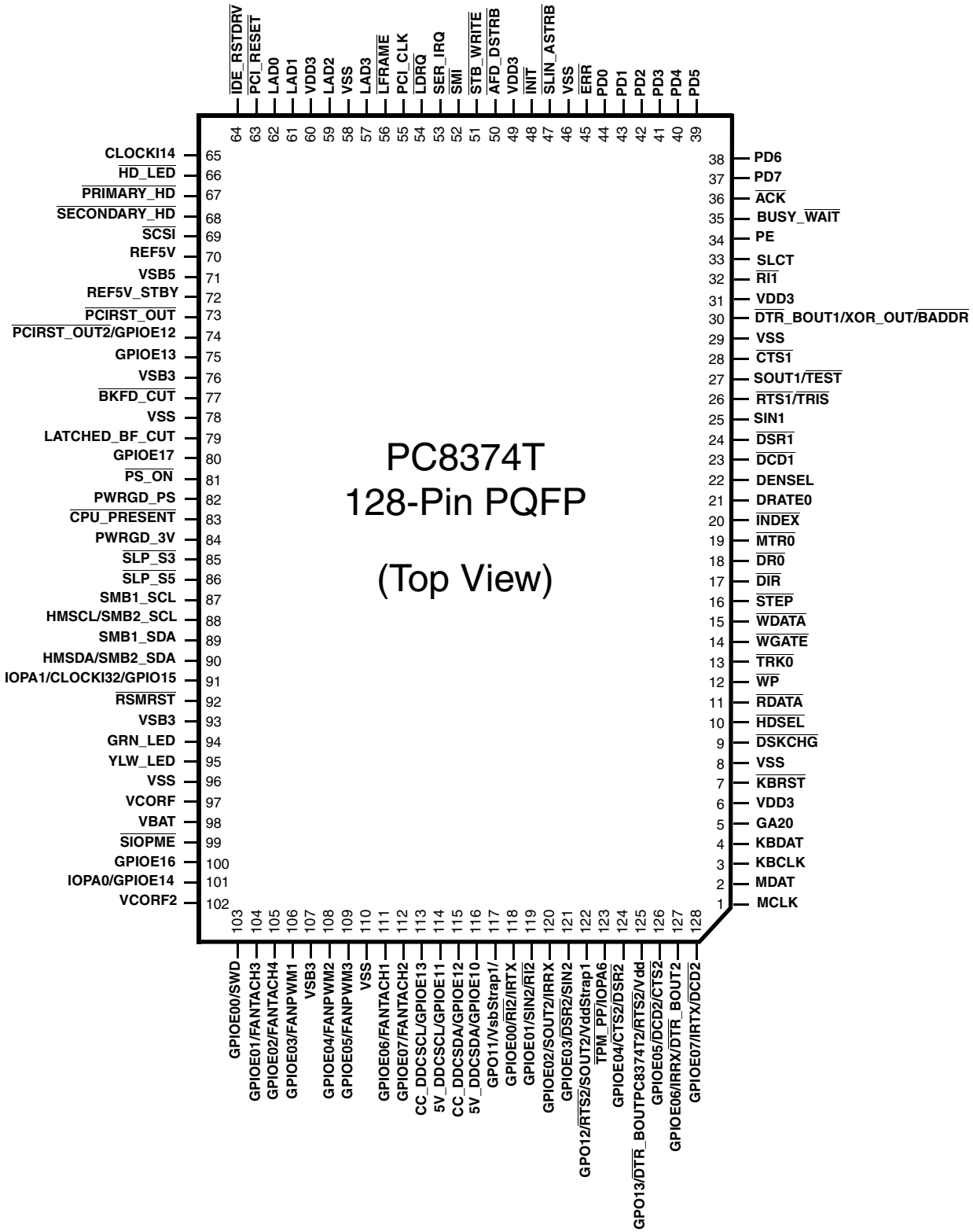
Features (Continued)

Clocking, Supply, and Package Information

- Clocks
  - On-chip Low-Frequency Clock Generator:
    - Generates 32.768 KHz internal clock
  - On-chip SuperI/O Clock Generator:
    - Generates 48 MHz
    - V_{DD3} powered
- Protection
  - All device pins are 5V tolerant and back-drive protected (except LPC bus pins)
  - High ESD protection of all the device pins
  - Pin multiplexing selection lock
  - Configuration register lock
- Testability
  - XOR tree structure
    - Includes all the device pins (except the supply and the analog pins)
    - Selected at power-up by strap input ($\overline{TEST}$)
  - TRI-STATE device pins, selected at power-up by strap input ($\overline{TRIS}$)
- Power Supply
  - 3.3V supply operation
  - Separate pin pairs for main (V_{DD3}) and standby (V_{SB3}) power supplies
  - Backup battery input (V_{BAT}) for SWC indications
  - Low standby power consumption
  - Very low power consumption from backup battery (less than 1 μA)
- Package
  - 128-pin PQFP

1.0 Signal/Pin Connection and Description

1.1 CONNECTION DIAGRAM



Plastic Quad Flatpack (PQFP), JEDEC

Order Number PC8374T0xxx/VLA

Package Number VLA128A

Note: 'xxx' stands for the following Keyboard Controller Microcodes:
IBW - for AMI IBU - for Intel
IBM - for IBM ICG - for Dell
ICK - for Phoenix

1.0 Signal/Pin Connection and Description (Continued)

Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
1	MCLK	33	SLCT	65	CLOCKI14	97	V_{CORF}
2	MDAT	34	PE	66	$\overline{HD\_LED}$	98	V_{BAT}
3	KBCLK	35	BUSY_$\overline{WAIT}$	67	$\overline{PRIMARY\_HD}$	99	$\overline{SIOPME}$
4	KBDAT	36	$\overline{ACK}$	68	$\overline{SECONDARY\_HD}$	100	GPIOE16
5	GA20	37	PD7	69	$\overline{SCSI}$	101	IOPA0/GPIOE14
6	V_{DD3}	38	PD6	70	REF5V	102	V_{CORF2}
7	$\overline{KBRST}$	39	PD5	71	V_{SB5}	103	GPIOE00/SWD
8	V_{SS}	40	PD4	72	REF5V_STBY	104	GPIOE01/FANTACH3
9	$\overline{DSKCHG}$	41	PD3	73	$\overline{PCIRST\_OUT}$	105	FANTACH4/GPIOE02
10	$\overline{HDSEL}$	42	PD2	74	$\overline{PCIRST\_OUT2}$/GPIOE12	106	GPIOE03/FANPWM1
11	$\overline{RDATA}$	43	PD1	75	GPIOE13	107	V_{SB3}
12	$\overline{WP}$	44	PD0	76	V_{SB3}	108	GPIOE04/FANPWM2
13	$\overline{TRK0}$	45	$\overline{ERR}$	77	$\overline{BKFD\_CUT}$	109	GPIOE05/FANPWM3
14	$\overline{WGATE}$	46	V_{SS}	78	V_{SS}	110	V_{SS}
15	$\overline{WDATA}$	47	$\overline{SLIN\_ASTRB}$	79	LATCHED_BF_CUT	111	GPIOE06/FANTACH1
16	$\overline{STEP}$	48	$\overline{INIT}$	80	GPIOE17	112	GPIOE07/FANTACH2
17	$\overline{DIR}$	49	V_{DD3}	81	$\overline{PS\_ON}$	113	CC_DDCSCL/GPIOE13
18	$\overline{DR0}$	50	$\overline{AFD\_DSTRB}$	82	PWRGD_PS	114	5V_DDCSCL/GPIOE11
19	$\overline{MTR0}$	51	$\overline{STB\_WRITE}$	83	$\overline{CPU\_PRESENT}$	115	CC_DDCSDA/GPIOE12
20	$\overline{INDEX}$	52	$\overline{SMI}$	84	PWRGD_3V	116	5V_DDCSDA/GPIOE10
21	DRATE0	53	SER_IRQ	85	$\overline{SLP\_S3}$	117	GPO11/VsbStrap1
22	DENSEL	54	$\overline{LDRQ}$	86	$\overline{SLP\_S5}$	118	GPIOE00/$\overline{RI2}$/IRTX
23	$\overline{DCD1}$	55	PCI_CLK	87	SMB1_SCL	119	GPIOE01/SIN2/$\overline{RI2}$
24	$\overline{DSR1}$	56	$\overline{LFRAME}$	88	SMB2_SCL/HMSCL	120	GPIOE02/SOUT2/IRRX
25	SIN1	57	LAD3	89	SMB1_SDA	121	GPIOE03/$\overline{DSR2}$/SIN2
26	$\overline{RTS1}$/$\overline{TRIS}$	58	V_{SS}	90	SMB2_SDA/HMSDA	122	GPO12/$\overline{RTS2}$/SOUT2/ VddStrap1
27	SOUT1/$\overline{TEST}$	59	LAD2	91	IOPA1/CLOCKI32/GPIO15	123	$\overline{TPM\_PP}$/IOPA6
28	$\overline{CTS1}$	60	V_{DD3}	92	$\overline{RSMRST}$	124	GPIOE04/$\overline{CTS2}$/$\overline{DSR2}$
29	V_{SS}	61	LAD1	93	V_{SB3}	125	GPO13/$\overline{DTR}$_BOUT2/ $\overline{RTS2}$/VddStrap2
30	$\overline{DTR}$_BOUT1/$\overline{BADDR}$/ XOR_OUT	62	LAD0	94	GRN_LED	126	GPIOE05/$\overline{DCD2}$/$\overline{CTS2}$
31	V_{DD3}	63	$\overline{PCI\_RESET}$	95	YLW_LED	127	GPIOE06/IRRX/ $\overline{DTR}$_BOUT2
32	$\overline{RI1}$	64	$\overline{IDE\_RSTDRV}$	96	V_{SS}	128	GPIOE07/IRTX/$\overline{DCD2}$

1.0 Signal/Pin Connection and Description (Continued)

1.2 BUFFER TYPES AND SIGNAL/PIN DIRECTORY

The signal DC characteristics of the pins described in Section 1.4 on page 10 are denoted by buffer type symbols, which are defined in Table 1 and described in further detail in Section 2.2 on page 22.

Table 1. Buffer Types

Symbol	Description
IN_T	Input, TTL compatible
IN_{TS}	Input, TTL compatible, with 250 mV Schmitt Trigger
IN_{TS2}	Input, TTL compatible, with 200 mV Schmitt Trigger
IN_{TS4}	Input, TTL compatible, with 400 mV Schmitt Trigger
IN_{PCI}	Input, PCI 3.3V compatible
IN_{SM}	Input, SMBus compatible
IN_{ULR}	Input, power, resistor protected (not characterized)
AI	Input, analog (0-5.5V tolerant)
$O_{p/n}$	Output, TTL/CMOS compatible, push-pull buffer capable of sourcing *p* mA and sinking *n* mA
OD_n	Output, TTL/CMOS compatible, open-drain buffer capable of sinking *n* mA
O_{PCI}	Output, PCI 3.3V compatible,
AO	Output, analog (0-5.5V tolerant)
SW_{SM}	Input/Output switch, SMBus compatible
PWR	Power pin
GND	Ground pin

1.3 PIN MULTIPLEXING

Table 2 shows only multiplexed pins, their associated functional blocks and the configuration bits for the selection of the multiplexed options used in the PC8374T.

Table 2. Pin Multiplexing Configuration

Pin	Default Signal	Function Block	Alternate Signal	Function Block	Alternate Signal	Function Block	Configuration Select	Strap or Wake-Up	Function Block
26	$\overline{\text{RTS1}}$	Serial Port 1						$\overline{\text{TRIS}}$	Config (Straps)
27	SOUT1							$\overline{\text{TEST}}$	
30	$\overline{\text{DTR}}$_BOUT1		XOR_OUT	Config			$\overline{\text{TEST}}$ (strap)	$\overline{\text{BADDR}}$	
74	$\overline{\text{PCIRST\_OUT2}}$	Glue	GPIOE12	GPIO			SIOCF4.nPCIRSTO2	GPIOE12	SWC
75	GPIOE13	GPIO						GPIOE13	
91	GPIO15	GPIO	CLOCKI32	TPM	IOPA1	TPM	TPM Firmware Controlled		
101	GPIOE14	GPIO	IOPA0	TPM			TPM Firmware Controlled	GPIOE14	
103	SWD	HM	GPIOE00	GPIO			SIOCF4.nSWD	GPIOE00	SWC
104	GPIOE01	GPIO	FANTACH3	HM			SIOCF2.TACH3EN	GPIOE01	SWC
105	GPIOE02		FANTACH4				SIOCF2.TACH4EN	GPIOE02	
106	GPIOE03		FANPWM1				SIOCF3.PWM1EN	GPIOE03	
108	GPIOE04		FANPWM2				SIOCF3.PWM2EN	GPIOE04	
109	GPIOE05		FANPWM3				SIOCF3.PWM3EN	GPIOE05	
111	GPIOE06		FANTACH1				SIOCF2.TACH1EN	GPIOE06	
112	GPIOE07		FANTACH2				SIOCF2.TACH2EN	GPIOE07	
113	CC_DDCSCL	Glue	GPIOE13	GPIO			SIOCF2.GPIO03EN	GPIOE13	
114	5V_DDCSCL		GPIOE11					GPIOE11	
115	CC_DDCSDA		GPIOE12					GPIOE12	
116	5V_DDCSDA		GPIOE10					GPIOE10	
117	GPO11	GPIO						VsbStrap1[1]	Strap

Table 2. Pin Multiplexing Configuration (Continued)

Pin	Default Signal	Function Block	Alternate Signal	Function Block	Alternate Signal	Function Block	Configuration Select	Strap or Wake-Up	Function Block
118	GPIOE00	GPIO	$\overline{RI2}$	Serial Port 2	IRTX	InfraRed	SIOCF3.373COMP AND SIOCF3.SP2EN AND SIOCF3.IREN	$\overline{RI2}$	SWC
119	GPIOE01		SIN2		$\overline{RI2}$	Serial Port 2	SIOCF3.373COMP AND SIOCF3.SP2EN	$\overline{RI2}$	
120	GPIOE02		SOUT2		IRRX	InfraRed	SIOCF3.373COMP AND SIOCF3.SP2EN AND SIOCF3.IREN		
121	GPIOE03		$\overline{DSR2}$		SIN2	Serial Port 2	SIOCF3.373COMP AND SIOCF3.SP2EN		
122	GPO12		$\overline{RTS2}$		SOUT2			VddStrap1[2]	Config (Straps)
124	GPIOE04		$\overline{CTS2}$		$\overline{DSR2}$				
125	GPO13		$\overline{DTR}$_BOUT2		$\overline{RTS2}$			VddStrap2	Config (Straps)
126	GPIOE05		$\overline{DCD2}$		$\overline{CTS2}$				
127	GPIOE06		IRRX	InfraRed	$\overline{DTR}$_BOUT2		SIOCF3.373COMP AND SIOCF3.SP2EN AND SIOCF3.IREN		
128	GPIOE07		IRTX		$\overline{DCD2}$				
123	$\overline{TPM\_PP}$	TPM	IOPA6	TPM			TPM Firmware controlled		

1. V_{SB} strap input. Reserved for National use.
2. V_{DD} strap input. Reserved for National use.

1.0 Signal/Pin Connection and Description (Continued)

1.4 DETAILED SIGNAL/PIN DESCRIPTIONS

This section describes all signals of the PC8374T device. The signals are organized by functional group.

1.4.1 LPC Interface

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
LAD3-0	57, 59, 61-62	I/O	IN_{PCI}/O_{PCI}	V_{DD3}	**LPC Address-Data.** Multiplexed command, address bi-directional data and cycle status.
PCI_CLK	55	I	IN_{PCI}	V_{DD3}	**LPC Clock.** PCI clock used for the LPC bus (up to 33 MHz).
$\overline{\text{LFRAME}}$	56	I	IN_{PCI}	V_{DD3}	**LPC Frame.** Low pulse indicates the beginning of a new LPC cycle or termination of a broken cycle.
$\overline{\text{LDRQ}}$	54	O	O_{PCI}	V_{DD3}	**LPC DMA Request.** Encoded DMA request for LPC interface.
$\overline{\text{PCI\_RESET}}$	63	I	IN_{PCI}	V_{DD3}	**LPC Reset.** PCI system reset used for the LPC bus (Hardware Reset).
SER_IRQ	53	I/O	IN_{PCI}/O_{PCI}	V_{DD3}	**Serial IRQ.** The interrupt requests are serialized over a single pin, where each IRQ level is delivered during a designated time slot.
$\overline{\text{SMI}}$	52	O	OD_6	V_{DD3}	**System Management Interrupt.** Active (low) level indicates that an SMI occurred. External pull-up resistor to V_{DD3} is required.

1.4.2 Serial Port 1 and Serial Port 2 (UART1 and UART2)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
$\overline{\text{CTS1}}$	28	I	IN_{TS}	V_{DD3}	**Clear to Send.** When low, indicates that the modem or other data transfer device is ready to exchange data.
$\overline{\text{CTS2}}$	124 or 126	I	IN_{TS}	V_{DD3}	
$\overline{\text{DCD1}}$	23	I	IN_{TS}	V_{DD3}	**Data Carrier Detected.** When low, indicates that the modem or other data transfer device has detected the data carrier.
$\overline{\text{DCD2}}$	126 or 128	I	IN_{TS}	V_{DD3}	
$\overline{\text{DSR1}}$	24	I	IN_{TS}	V_{DD3}	**Data Set Ready.** When low, indicates that the data transfer device, e.g., modem, is ready to establish a communications link.
$\overline{\text{DSR2}}$	121 or 124	I	IN_{TS}	V_{DD3}	
$\overline{\text{DTR}}$_BOUT1	30	O	$O_{4/8}$	V_{DD3}	**Data Terminal Ready.** When low, indicates to the modem or other data transfer device that the corresponding UART is ready to establish a communications link. After a system reset, these pins provide the $\overline{\text{DTR}}$ function and set these signals to inactive high. **Baud Output.** Provides the associated serial channel baud rate generator output signal if test mode is selected, i.e., bit 7 of EXCR1 register is set.
$\overline{\text{DTR}}$_BOUT2	125 or 127	O	$O_{4/8}$	V_{DD3}	
$\overline{\text{RI1}}$	32	I	IN_{TS}	V_{DD3}	**Ring Indicator.** When low, indicates that a telephone ring signal was received by the modem. These pins are monitored during V_{DD} power-off for wake-up event detection.
$\overline{\text{RI2}}$	118 or 119	I	IN_{TS}	V_{DD3}	
$\overline{\text{RTS1}}$	26	O	$O_{4/8}$	V_{DD3}	**Request to Send.** When low, indicates to the modem or other data transfer device that the corresponding UART device is ready to exchange data. A system reset sets these signals to inactive high.
$\overline{\text{RTS2}}$	122 or 125	O	$O_{4/8}$	V_{DD3}	
SIN1	25	I	IN_{TS}	V_{DD3}	**Serial Input.** Receives composite serial data from the communications link (peripheral device, modem or other data transfer device).
SIN2	119 or 121	I	IN_{TS}	V_{DD3}	

1.0 Signal/Pin Connection and Description (Continued)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
SOUT1	27	O	$O_{4/8}$	V_{DD3}	**Serial Output.** Sends composite serial data to the communications link (peripheral device, modem or other data transfer device). These signals are set active high after a system reset.
SOUT2	120 or 122	O	$O_{4/8}$	V_{DD3}	

1.4.3 InfraRed Port

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
IRRX	127 or 120	I	IN_{TS}	V_{DD3}	**InfraRed Receive.** InfraRed serial input data.
IRTX	128 or 118	O	$O_{6/12}$	V_{DD3}	**InfraRed Transmit.** InfraRed serial output data.

1.4.4 Parallel Port

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
$\overline{ACK}$	36	I	IN_T	V_{DD3}	**Acknowledge.** Pulsed low by the printer to indicate that it has received data from the parallel port.
$\overline{AFD\_DSTRB}$	50	O	OD_{14}, $O_{14/14}$	V_{DD3}	**$\overline{AFD}$ - Automatic Feed.** When low, instructs the printer to automatically feed a line after printing each line. This pin is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor must be connected to this pin. **$\overline{DSTRB}$ - Data Strobe (EPP).** Active low; used in EPP mode to denote a data cycle. When the cycle is aborted, $\overline{DSTRB}$ becomes inactive (high).
BUSY_$\overline{WAIT}$	35	I	IN_T	V_{DD3}	**Busy.** Set high by the printer when it cannot accept another character. **Wait.** In EPP mode, the parallel port device uses this active low signal to extend its access cycle.
$\overline{ERR}$	45	I	IN_T	V_{DD3}	**Error.** Set active low by the printer when it detects an error.
$\overline{INIT}$	48	O	OD_{14}, $O_{14/14}$	V_{DD3}	**Initialize.** When low, initializes the printer. This signal is in TRI-STATE after a 1 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor must be connected to this pin.
PD7-0	37-44	I/O	$IN_T/O_{14/14}$	V_{DD3}	**Parallel Port Data.** Transfers data to and from the peripheral data bus and the appropriate parallel port data register. These signals have a high current drive capability.
PE	34	I	IN_T	V_{DD3}	**Paper End.** Set high by the printer when it is out of paper. This pin has an internal weak pull-up or pull-down resistor.
SLCT	33	I	IN_T	V_{DD3}	**Select.** Set active high by the printer when the printer is selected.
$\overline{SLIN\_ASTRB}$	47	O	OD_{14}, $O_{14/14}$	V_{DD3}	**$\overline{SLIN}$ - Select Input.** When low, selects the printer. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor must be connected to this pin. **$\overline{ASTRB}$ - Address Strobe (EPP).** Active low, used in EPP mode to denote an address cycle. When the cycle is aborted, $\overline{ASTRB}$ becomes inactive (high).

1.0 Signal/Pin Connection and Description (Continued)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
$\overline{\text{STB\_WRITE}}$	51	O	OD_{14}, $O_{14/14}$	V_{DD3}	**$\overline{\text{STB}}$ - Data Strobe.** When low, Indicates to the printer that valid data is available at the printer port. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor must be connected to this pin. **$\overline{\text{WRITE}}$ - Write Strobe.** Active low, used in EPP mode to denote an address or data write cycle. When the cycle is aborted, $\overline{\text{WRITE}}$ becomes inactive (high).

1.4.5 Floppy Disk Controller (FDC)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
DENSEL	22	O	OD_{12} $O_{6/12}$	V_{DD3}	**Density Select.** Indicates that a high FDC density data rate (500 Kbps, 1 Mbps or 2 Mbps) or a low density data rate (250 or 300 Kbps) is selected.
$\overline{\text{DIR}}$	17	O	OD_{12} $O_{6/12}$	V_{DD3}	**Direction.** Determines the direction of the Floppy Disk Drive (FDD) head movement (active = step in; inactive = step out) during a seek operation.
$\overline{\text{DR0}}$	18	O	OD_{12} $O_{6/12}$	V_{DD3}	**Drive Select.** Active low signal controlled by bit 0 of the Digital Output Register (DOR).
DRATE0	21	O	OD_{12} $O_{6/12}$	V_{DD3}	**Data Rate.** Reflects the value of bit 0 of either Configuration Control Register (CCR) or Data Rate Select Register (DSR), whichever was written to last.
$\overline{\text{DSKCHG}}$	9	I	IN_{TS}	V_{DD3}	**Disk Change.** Indicates that the drive door was opened.
$\overline{\text{HDSEL}}$	10	O	OD_{12} $O_{6/12}$	V_{DD3}	**Head Select.** Selects which side of the FDD is accessed. Active (low) selects side 1; inactive selects side 0.
$\overline{\text{INDEX}}$	20	I	IN_{TS}	V_{DD3}	**Index.** Indicates the beginning of an FDD track.
$\overline{\text{MTR0}}$	19	O	OD_{12} $O_{6/12}$	V_{DD3}	**Motor Select.** Active low motor enable signal for drive 0, controlled by bit D4 of the Digital Output Register (DOR).
$\overline{\text{RDATA}}$	11	I	IN_{TS}	V_{DD3}	**Read Data.** Raw serial input data stream read from the FDD.
$\overline{\text{STEP}}$	16	O	OD_{12} $O_{6/12}$	V_{DD3}	**Step.** Issues pulses to the disk drive at a software programmable rate to move the head during a seek operation.
$\overline{\text{TRK0}}$	13	I	IN_{TS}	V_{DD3}	**Track 0.** Indicates to the controller that the head of the selected floppy disk drive is at track 0.
$\overline{\text{WDATA}}$	15	O	OD_{12} $O_{6/12}$	V_{DD3}	**Write Data.** Carries out the pre-compensated serial data that is written to the FDD. Pre-compensation is software selectable.
$\overline{\text{WGATE}}$	14	O	OD_{12} $O_{6/12}$	V_{DD3}	**Write Gate.** Enables the write circuitry of the selected FDD. $\overline{\text{WGATE}}$ is designed to prevent glitches during power-up and power-down. This prevents writing to the disk when power is cycled.
$\overline{\text{WP}}$	12	I	IN_{TS}	V_{DD3}	**Write Protected.** Indicates that the disk in the selected drive is write protected.

1.0 Signal/Pin Connection and Description (Continued)

1.4.6 Keyboard and Mouse Controller (KBC)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
KBCLK	3	I/O	IN_{TS}/OD_{14}	V_{DD3}	**Keyboard Clock.** Keyboard clock signal. External pull-up resistor is required for PS/2 compliance. This pin is monitored during V_{DD3} power-off for wake-up event detection.
KBDAT	4	I/O	IN_{TS}/OD_{14}	V_{DD3}	**Keyboard Data.** Keyboard data signal. External pull-up resistor is required for PS/2 compliance. This pin is monitored during V_{DD3} power-off for wake-up event detection.
MCLK	1	I/O	IN_{TS}/OD_{14}	V_{DD3}	**Mouse Clock.** Mouse clock signal. External pull-up resistor is required for PS/2 compliance. This pin is monitored during V_{DD3} power-off for wake-up event detection.
MDAT	2	I/O	IN_{TS}/OD_{14}	V_{DD3}	**Mouse Data.** Mouse data signal. External pull-up resistor is required for PS/2 compliance. This pin is monitored during V_{DD3} power-off for wake-up event detection.
$\overline{KBRST}$	7	I/O	IN_T/OD_8, $O_{4/8}$	V_{DD3}	**KBD Reset.** Keyboard reset (P20) quasi-bidirectional output.
GA20	5	I/O	IN_T/OD_8, $O_{4/8}$	V_{DD3}	**Gate A20.** KBC gate A20 (P21) quasi-bidirectional output.

1.4.7 General-Purpose I/O (GPIO)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
GPIOE00	103	I/O	IN_{TS}/ OD_8, $O_{4/8}$	V_{SB3}	**General-Purpose I/O Ports.** Each pin is configured independently as input or I/O, with or without static pull-up (and some also with or without static pull-down) and with either open-drain or push-pull output type. These pins have event detection capability to generate a wake-up event or an interrupt. **Note:** If GPIOE12 is configured (on pin 74) make sure that the pin's default function does not interfere with the circuit connected to the GPIO. Failure to do so may result in irreversible damage to the chip.
	118		IN_{TS}/ OD_{12}, $O_{6/12}$	V_{DD3}	
GPIOE01-06	104-106, 108-109, 111		IN_{TS}/ OD_8, $O_{4/8}$	V_{SB3}	
	119-121, 124, 126-127			V_{DD3}	
GPIOE07	112		IN_{TS}/ OD_8, $O_{4/8}$	V_{SB3}	
	128		IN_{TS}/ OD_{12}, $O_{6/12}$	V_{DD3}	
GPIOE10-13	116, 114, 115, 113		IN_{TS2}/ OD_6, $O_{3/6}$	V_{SB3}	
GPIOE12-13	74-75		IN_{TS}/ OD_8, $O_{4/8}$		
GPIOE14, GPIOE16-17	101, 100, 80				
GPIO15	91		IN_{TS}/ OD_8, $O_{4/8}$		**General-Purpose I/O Port.** This pin is configured independently as input or I/O with or without static pull-up and with either open-drain or push-pull output type.
GPO11	117	O	OD_8, $O_{4/8}$		**General-Purpose Output Port.** This pin is configured independently as output, with or without static pull-up and with either open-drain or push-pull output type.
GPO12-13	122, 125			V_{DD3}	

1.0 Signal/Pin Connection and Description (Continued)

1.4.8 Health Management (HM)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
SWD	103	I/O	IN_{SM}/OD_6	V_{SB3}	**SensorPath™ Data.** Bidirectional, SensorPath Data interface signal to LMxx sensor device(s). An internal pull-up for this pin is optional.
HMSCL	88	I/O	IN_{SM}/OD_6	V_{SB3}	**Health Management SMBus Serial Clock.** Serial clock signal. External pull-up resistor is required.
HMSDA	90	I/O	IN_{SM}/OD_6	V_{SB3}	**Health Management SMBus Serial Data.** Serial data signal. External pull-up resistor is required.
FANTACH1-4	111-112, 104-105	I	IN_{TS}	V_{DD3}	**Fan Inputs.** Used to feed the fan's tachometer pulse to the Fan Speed Monitor.
FANPWM1-3	106, 108-109	O	OD_{12},$O_{6/12}$	V_{DD3}	**Fan Outputs.** Pulse Width Modulation (PWM) signals, used to control the speed of cooling fans by controlling the voltage supplied to the fan motors.

1.4.9 Trusted Platform Module (TPM)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
$\overline{TPM\_PP}$	123	I	IN_{TS}	V_{SB3}	**Physical Presence Input.** Indicates owner's physical presence.
IOPA0, IOPA1, IOPA6	101, 91, 123	I/O	IN_{TS}/ OD_8, $O_{4/8}$	V_{SB3}	**General-Purpose I/O Ports.** Each pin is configured independently as input or I/O, with or without static pull-up and with either open-drain or push-pull output type. These pins have event detection capability to generate a wake-up event or an interrupt.

1.4.10 System Wake-Up Control (SWC)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
GPIOE00-07	103-106, 108-109, 111-112	I	IN_{TS}	V_{SB3}	**Wake-Up Inputs.** Generates a wake-up event. These pins have programmable debouncing. When the pin is not used, the internal pull-up resistor must be enabled to allow the pin to be left not connected.
	118-121, 124, 126-128			V_{DD3}	
GPIOE10-13	116, 114, 115, 113		IN_{TS2}	V_{SB3}	
GPIOE12-13	74-75		IN_{TS}		
GPIOE14, GPIOE16-17	101, 100, 80				
$\overline{RI1}$ $\overline{RI2}$	32, 118 or 119	I	IN_{TS}	V_{SB3}	**Ring Indicator Wake-Up.** When low, generates a wake-up event, indicating that a telephone ring signal was received by the modem.
KBCLK	3	I	IN_{TS}	V_{SB3}	**Keyboard Clock Wake-Up.** Generates a wake-up event when a specific keyboard sequence is detected.
KBDAT	4	I	IN_{TS}	V_{SB3}	**Keyboard Data Wake-Up.** Generates a wake-up event when a specific keyboard sequence is detected.
MCLK	1	I	IN_{TS}	V_{SB3}	**Mouse Clock Wake-Up.** Generates a wake-up event when a specific mouse action is detected.

1.0 Signal/Pin Connection and Description (Continued)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
MDAT	2	I	IN_{TS}	V_{SB3}	**Mouse Data Wake-Up.** Generates a wake-up event when a specific mouse action is detected.
$\overline{SIOPME}$	99	O	OD_8, $O_{4/8}$	V_{SB3}	**Power Management Event (SCI).** Active level indicates that a wake-up event occurred, causing the system to exit its current sleep state. This signal has programmable polarity (default is active low).
$\overline{SLP\_S3}$, $\overline{SLP\_S5}$	85, 86	I	IN_{TS4}	V_{SB3}	**Sleep States 3 to 5.** Active (low) level indicates the system is in one of the sleep states S3 or S5. These signals are generated by an external ACPI controller.
YLW_LED, GRN_LED	95, 94	O	OD_{24}	V_{SB3}	**Power LEDs.** Yellow and green LED drivers. Each indicates the Main power status or blinks under software control.

1.4.11 Clocks

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
CLOCKI32	91	I	IN_{TS}	V_{SB3}	**Low-Frequency Clock Input.** 32.768 KHz clock for the TPM timing.
CLOCKI14	65	I	IN_{TS}	V_{DD3}	**High-Frequency Clock Input.** 14.31818 MHz clock for the on-chip, 48 MHz Clock Generator (for the Legacy modules).

1.4.12 Glue Functions

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
REF5V	70	O	AO	V_{SB3}	**Main Highest Active Supply, Reference Output.** Reference voltage equal to the highest voltage between V_{DD5} and V_{DD3}. External pull-up resistor to V_{DD5} is required.
REF5V_STBY	72	O	AO	V_{SB3}	**Standby Highest Active Supply, Reference Output.** Reference voltage equal to the highest voltage between V_{SB5} and V_{SB3}. External pull-up resistor to V_{SB5} is required.
$\overline{PS\_ON}$	81	O	OD_6	V_{SB3}	**Main Power Supply On/Off Control.** Active (low) level turns the main power supply (V_{DD}) on. External pull-up resistor to V_{SB5} is required.
PWRGD_PS	82	I	IN_{TS4}	V_{SB3}	**Power Good Signal from the Power Supply.** Active level indicates the Main power supply voltage is valid.
PWRGD_3V	84	O	$O_{3/6}$	V_{SB3}	**Power Good Output.** Active level indicates: Main supply voltage is valid and the system is in a higher than S3 sleep state.
$\overline{CPU\_PRESENT}$	83	I	IN_{TS4}	V_{SB3}	**CPU Present.** Active (low) level indicates a processor is currently plugged in.
$\overline{BKFD\_CUT}$	77	O	OD_6	V_{SB3}	**Backfeed-Cut Control.** Power distribution control (when switching between main and standby regulators) for system transition into and out of the S3 sleep state. External pull-up resistor to V_{SB5} is required.
LATCHED_BF_CUT	79	O	$O_{14/14}$	V_{SB3}	**Latched Backfeed-Cut.** Power distribution control (when switching between main and standby regulators) for system transition into and out of the S5 sleep state.
VSB5	71	I	AI	V_{SB3}	**Standby 5V Power Supply.** Used for Resume Reset generation (Range: 0-5.5V, Backdrive protected).
$\overline{RSMRST}$	92	O	$O_{3/6}$	V_{SB3}	**Resume Reset.** Power-Up reset signal based on the V_{SB5} supply voltage.

1.0 Signal/Pin Connection and Description (Continued)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
$\overline{\text{PRIMARY\_HD}}$	67	I	IN_{TS4}	V_{DD3}	**Primary Drive.** Active (low) level indicates that the primary IDE drive is active.
$\overline{\text{SECONDARY\_HD}}$	68	I	IN_{TS4}	V_{DD3}	**Secondary Drive.** Active (low) level indicates that the secondary IDE drive is active.
$\overline{\text{SCSI}}$	69	I	IN_{TS4}	V_{DD3}	**SCSI Drive.** Active (low) level indicates that the SCSI drive is active.
$\overline{\text{HD\_LED}}$	66	O	OD_{12}	V_{DD3}	**Hard Drive LED.** Red LED driver. When low, indicates that at least one drive is active.
CC_DDCSCL	113	I/O	SW_{SM}	V_{SB3}	**Chipset Cluster (2.5V or 3.3V) Level DDC Serial Clock.** SMBus serial clock signal with 2.5V or 3.3V logic levels for Data Display Channel (DDC) interface. External pull-up resistor to V_{DD3} or 2.5V is required.
5V_DDCSCL	114	I/O	SW_{SM}	V_{SB3}	**5V Level DDC Serial Clock.** SMBus serial clock signal with 5V logic levels for VGA monitor interface. External pull-up resistor to V_{DD5} is required.
CC_DDCSDA	115	I/O	SW_{SM}	V_{SB3}	**Chipset Cluster (2.5V or 3.3V) Level DDC Serial Data.** SMBus serial data signal with 2.5V or 3.3V logic levels for DDC interface. External pull-up resistor to V_{DD3} or 2.5V is required.
5V_DDCSDA	116	I/O	SW_{SM}	V_{SB3}	**5V Level DDC Serial Data.** SMBus serial data signal with 5V logic levels for VGA monitor interface. External pull-up resistor to V_{DD5} is required.
SMB1_SCL	87	I/O	SW_{SM}	V_{SB3}	**Bus 1 Serial Clock.** Serial clock signal of SMBus 1 (3.3V logic levels). External pull-up resistor to the 3.3V supply is required.
SMB2_SCL	88	I/O	SW_{SM}	V_{SB3}	**Bus 2 Serial Clock.** Serial clock signal of SMBus 2 (3.3V logic levels). External pull-up resistor to the 3.3V supply is required.
SMB1_SDA	89	I/O	SW_{SM}	V_{SB3}	**Bus 1 Serial Data.** Serial data signal of SMBus 1 (3.3V logic levels). External pull-up resistor to the 3.3V supply is required.
SMB2_SDA	90	I/O	SW_{SM}	V_{SB3}	**Bus 2 Serial Data.** Serial data signal of SMBus 2 (3.3V logic levels). External pull-up resistor to the 3.3V supply is required.
$\overline{\text{PCIRST\_OUT}}$	73	O	$O_{14/14}$	V_{SB3}	**PCI Reset Output.** PCI system reset. $\overline{\text{PCIRST\_OUT}}$ is a buffered copy of $\overline{\text{PCI\_RESET}}$ when V_{DD3} is on, and it is held at low level when V_{DD3} is off.
$\overline{\text{PCIRST\_OUT2}}$	74	O	$O_{14/14}$	V_{SB3}	**PCI Reset Output 2.** PCI system reset (same behavior as $\overline{\text{PCIRST\_OUT}}$ above).
$\overline{\text{IDE\_RSTDRV}}$	64	O	OD_6	V_{DD3}	**IDE Reset Output.** IDE drive reset. $\overline{\text{IDE\_RSTDRV}}$ is a buffered copy of $\overline{\text{PCI\_RESET}}$ when V_{DD3} is on, and it is floating when V_{DD3} is off.

1.0 Signal/Pin Connection and Description (Continued)

1.4.13 Configuration Straps and Testing

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
$\overline{\text{BADDR}}$	30	I	IN_{TS}	V_{DD3}	**Base Address.** Sampled at V_{DD} Power-Up reset to determine the base address of the configuration Index-Data register pair, as follows: – No pull-down resistor (default) - 2Eh-2Fh – 10 KΩ[1] external pull-down resistor - 4Eh-4Fh The external pull-down resistor must be connected to V_{SS}.
VsbStrap1	117	I	IN_{TS}	V_{SB3}	**Vsb Strap 1.** Reserved strap input function for National use.
VddStrap1	122	I	IN_{TS}	V_{DD3}	**Vdd Strap 1.** Reserved strap input function for National use.
VddStrap2	125	I	IN_{TS}	V_{DD3}	**Vdd Strap 2.** General-Purpose strap input function.
$\overline{\text{TRIS}}$	26	I	IN_{TS}	V_{DD3}	**TRI-STATE Device.** Sampled at V_{DD} Power-Up reset to force the device to float all its output and I/O pins, as follows: – No pull-down resistor (default) - normal pin operation – 10 KΩ[1] external pull-down resistor - floating device pins The external pull-down resistor must be connected to V_{SS}. When $\overline{\text{TRIS}}$ is set to 0 (by an external pull-down resistor), $\overline{\text{TEST}}$ must be 1 (left unconnected).
$\overline{\text{TEST}}$	27	I	IN_{TS}	V_{DD3}	**XOR Tree Test Mode.** Sampled at V_{DD} Power-Up reset to force the device pins into a XOR tree configuration, as follows: – No pull-down resistor (default) - normal device operation – 10 KΩ[1] external pull-down resistor - pins configured as XOR tree. When $\overline{\text{TEST}}$ is set to 0 (by an external pull-down resistor), $\overline{\text{TRIS}}$ must be 1 (left unconnected).
XOR_OUT	30	O	$O_{4/8}$	V_{DD3}	**XOR Tree Output.** All the device pins (except power type and analog type pins) are internally connected in a XOR tree structure.

1. Because the strap function is multiplexed with the Serial Port pins, a CMOS transceiver device is recommended for Serial Port functionality; in this case, the value of the external pull-down resistor is 10 KΩ. If, however, a TTL transceiver device is used, the value of the external pull-down resistor must be 470Ω, and since the Serial Port pins are not able to drive this load, the external pull-down resistor must be disconnected t_{EPLV} after V_{DD3} power-up (see "VDD Power-Up Reset" on page 30).

1.4.14 Power and Ground

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
V_{SS}	8, 29, 46, 58, 78, 96, 110	I	GND		**Ground.** Ground connection for both core logic and I/O buffers, for the Main, Standby and Battery power supplies.
V_{DD3}	6, 31, 49, 60	I	PWR		**Main 3.3V Power Supply.** Powers the I/O buffers of the legacy peripherals and the LPC interface.
V_{SB3}	76, 93, 107	I	PWR		**Standby 3.3V Power Supply.** Powers the I/O buffers of the GPIO ports, SWC, Glue Functions, TPM Health Management and the on-chip Core power converter.
V_{CORF}	97	I/O	PWR		**On-Chip Core Power Converter Filter.** On-chip Core power converter output. An external 1 µF ceramic filter capacitor must be connected between this pin and V_{SS}.
V_{CORF2}	102	I/O	PWR		**On-Chip Core Power Converter Filter.** On-chip Core power converter output. An external 1 µF ceramic filter capacitor must be connected between this pin and V_{SS}.

1.0 Signal/Pin Connection and Description (Continued)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
V_{BAT}	98	I	IN_{ULR}		**Battery Power Supply.** When V_{SB3} is off, this supply provides battery back-up to some of the SWC registers. When the functions powered by V_{BAT} are not used, the V_{BAT} pin must be connected to V_{SB3}. The pin is connected to the internal logic through a series resistor and diode for UL-compliant protection.
V_{SB5}	71	I	PWR		**Standby 5V Power Supply.** Used for Resume Reset generation in the Glue Logic.

1.0 Signal/Pin Connection and Description (Continued)

1.5 INTERNAL PULL-UP AND PULL-DOWN RESISTORS

The signals listed in Table 3 have internal pull-up (PU) and/or pull-down (PD) resistors. The internal resistors are optional for those signals indicated as “Programmable”. See Section 2.3 on page 27 for the values of each resistor type.

Table 3. Internal Pull-Up and Pull-Down Resistors

Signal	Pin(s)	Power Well	Type	Comments
Health Management (HM)				
SWD	103	V_{SB}	PU_{1K25}	Programmable[1]
Parallel Port				
$\overline{ACK}$	36	V_{DD3}	PU_{220}	
$\overline{AFD\_DSTRB}$	50	V_{DD3}	PU_{440}	
BUSY_$\overline{WAIT}$	35	V_{DD3}	PD_{120}	
$\overline{ERR}$	45	V_{DD3}	PU_{220}	
$\overline{INIT}$	48	V_{DD3}	PU_{440}	
PE	34	V_{DD3}	PU_{220}/PD_{120}	Programmable
SLCT	33	V_{DD3}	PD_{120}	
$\overline{SLIN\_ASTRB}$	47	V_{DD3}	PU_{440}	
$\overline{STB\_WRITE}$	51	V_{DD3}	PU_{440}	
Keyboard and Mouse Controller (KBC)				
$\overline{KBRST}$	7	V_{DD3}	PU_{30}	
GA20	5	V_{DD3}	PU_{30}	
System Wake-Up Control (SWC)				
$\overline{SIOPME}$	99	V_{SB3}	PU_{30}	Programmable[2]
General-Purpose Input/Output (GPIO) Ports				
GPIOE00	103	V_{SB}	PU_{1K25}	Programmable[3]
	118	V_{DD3}	PU_{30}/PD_{30}	Programmable[4]
GPIOE01-06	104-106, 108-109, 111	V_{SB3}	PU_{30}	Programmable[1]
	119-121, 124, 126-127	V_{DD3}		
GPIOE07	112	V_{SB3}	PU_{30}	Programmable[5]
	128	V_{DD3}	PU_{30}/PD_{30}	Programmable[4]
GPIOE10-11	116, 114	V_{SB3}	PU_{30}	Programmable[6]
GPIOE12	115	V_{SB3}	PU_{30}	Programmable[6]
	74			
GPIOE13	113	V_{SB3}	PU_{30}	Programmable[6]
	75		PU_{90}	Programmable[1]
GPIOE14	101	V_{SB3}	PU_{30}/PD_{30}	Programmable[4]
GPIO15, GPIOE16	91, 100	V_{SB3}	PU_{30}	Programmable[5]
GPIOE17	80	V_{SB3}	PU_{30}	Programmable[1]

1.0 Signal/Pin Connection and Description (Continued)

Table 3. Internal Pull-Up and Pull-Down Resistors (Continued)

Signal	Pin(s)	Power Well	Type	Comments
GPO11	117	V_{SB3}	PU_{30}	Programmable[1]
GPO12-13	122, 125	V_{DD3}	PU_{30}	Programmable[1]
Glue Functions				
PWRGD_PS	82	V_{SB3}	PU_{90}	
$\overline{\text{CPU\_PRESENT}}$	83	V_{SB3}	PU_{90}	
$\overline{\text{PRIMARY\_HD}}$	67	V_{DD3}	PU_{90}	
$\overline{\text{SECONDARY\_HD}}$	68	V_{DD3}	PU_{90}	
$\overline{\text{SCSI}}$	69	V_{DD3}	PU_{90}	
Trusted Platform Module (TPM)				
$\overline{\text{TPM\_PP}}$	123	V_{SB3}	PD_{30}	Programmable[7]
IOPA6	123	V_{SB3}	PU_{30}/PD_{30}	Programmable[8]
IOPA0, IOPA1	101, 91	V_{SB3}	PU_{30}	Programmable[8]
Strap Configuration				
$\overline{\text{BADDR}}$	30	V_{DD3}	PU_{30}	Strap[9]
$\overline{\text{TRIS}}$	26	V_{DD3}	PU_{30}	Strap[9]
$\overline{\text{TEST}}$	27	V_{DD3}	PU_{30}	Strap[9]
VsbStrap1	117	V_{SB3}	PU_{30}	Strap[10]
VddStrap1	122	V_{DD3}	PU_{30}	Strap[9]
VddStrap2	125	V_{DD3}	PU_{30}	Strap[9]

1. Default at reset: enabled.
2. Enabled only when the OD_6 buffer type is selected (OD_6 is the default at reset).
3. Alternate function at reset: enabled.
4. Default at reset: PD enabled.
5. Default at reset: disabled.
6. Alternate function at reset: disabled.
7. Controlled by TPM. Default at reset: enabled.
8. Controlled by TPM. Default at reset: disabled.
9. Active only during V_{DD} Power-Up reset.
10. Active only during V_{SB} Power-Up reset.

2.0 Device Characteristics

2.1 GENERAL DC ELECTRICAL CHARACTERISTICS

2.1.1 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD3}	Main 3V Supply Voltage	3.0	3.3	3.6	V
V_{SB3}	Standby 3V Supply Voltage	3.0	3.3	3.6	V
V_{BAT}	Battery Backup Supply Voltage	2.4	3.0	3.6	V
T_A	Operating Temperature	0		+70	°C

2.1.2 Absolute Maximum Ratings

Absolute maximum ratings are values beyond which damage to the device may occur. Unless otherwise specified, all voltages are relative to ground (V_{SS}).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{SUP}	Supply Voltage[1]		−0.5	+4.1	V
V_I	Input Voltage	All other pins	−0.5	5.5	V
		LAD3-0, $\overline{\text{LFRAME}}$, SERIRQ	−0.5	V_{DD3} + 0.5	V
V_O	Output Voltage	All other pins	−0.5	5.5	V
		LAD3-0, $\overline{\text{LDRQ}}$, SERIRQ	−0.5	V_{DD3} + 0.5	V
T_{STG}	Storage Temperature		−65	+165	°C
P_D	Power Dissipation			1	W
T_L	Lead Temperature Soldering (10 s)			+260	°C
	ESD Tolerance	C_{ZAP} = 100 pF R_{ZAP} = 1.5 KΩ[2]	2000		V

1. V_{SUP} is V_{DD3}, V_{SB3}.
2. Value based on test complying with RAI-5-048-RA human body model ESD testing.

2.1.3 Capacitance

Symbol	Parameter	Conditions	Min[2]	Typ[1]	Max[2]	Unit
C_{IN}	Input Pin Capacitance			4	5	pF
C_{INC}	LPC Clock Input Capacitance	PCI_CLK	5	8	12	pF
C_{PCI}	LPC Pin Capacitance	LAD3-0, $\overline{\text{LFRAME}}$, $\overline{\text{PCI\_RESET}}$, SERIRQ, $\overline{\text{LDRQ}}$		8	10	pF
C_{IO}	I/O Pin Capacitance			8	10	pF
C_O	Output Pin Capacitance			6	8	pF

1. T_A = 25°C; f = 1 MHz.
2. Not tested. Guaranteed by characterization.

2.0 Device Characteristics (Continued)

2.1.4 Power Consumption under Recommended Operating Conditions

Symbol	Parameter	Conditions[1]	Typ	Max[2]	Unit
I_{DD3}	V_{DD3} Average Supply Current	V_{IL} = 0.5V, V_{IH} = 2.4V, No Load	14	20	mA
I_{DD3LP}	V_{DD3} Quiescent Supply Current in Low Power Mode[3]	V_{IL} = V_{SS}, V_{IH} = V_{DD3}, No Load	0.5	0.8	mA
I_{SB3}	V_{SB3} Average Supply Current	V_{IL} = 0.5V, V_{IH} = 2.4V, No Load	25	100	mA
I_{SB3LP}	V_{SB3} Quiescent Supply Current in Low Power Mode[3]	V_{IL} = V_{SS}, V_{IH} = V_{SB3}, No Load	5	TBD	mA
I_{BAT}	V_{BAT} Battery Supply Current	V_{DD3}, V_{SB3} = 0V, V_{BAT} = 3V	0.4	0.9	µA

1. All parameters specified for 0°C ≤ T_A ≤ 70°C; V_{DD3} and V_{SB3} = 3.3V ±10% unless otherwise specified.
2. Not tested. Guaranteed by characterization.
3. All the modules disabled; no LPC bus activity.

2.1.5 Voltage Thresholds

Symbol	Parameter[1]	Min[2]	Typ	Max[2]	Unit
V_{DD3ON}	V_{DD3} Detected as Power-on	2.3	2.6	2.9	V
V_{DD3OFF}	V_{DD3} Detected as Power-off	2.1	2.5	2.8	V
V_{SB3ON}	V_{SB3} Detected as Power-on	2.3	2.6	2.9	V
V_{SB3OFF}	V_{SB3} Detected as Power-off	2.1	2.5	2.8	V
V_{PPSW}	V_{PP} Switching between V_{SB3} and V_{BAT}	2.0	2.3	2.6	V
V_{BATLOW}	V_{BAT} Detected as “Low”			2.3	V

1. All parameters specified for 0°C ≤ T_A ≤ 70°C.
2. Not tested. Guaranteed by characterization.

2.2 DC CHARACTERISTICS OF PINS, BY I/O BUFFER TYPES

The following tables summarize the DC characteristics of all device pins described in Section 1.2 on page 7. The characteristics describe the general I/O buffer types defined in Table 1 on page 7. For exceptions, refer to Section 2.2.13 on page 26. The DC characteristics of the LPC interface meet the *PCI Local Bus Specification (Rev 2.2 December 18, 1998)* for 3.3V DC signaling.

2.2.1 Input, TTL Compatible

Symbol: IN_T

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	5.5[1]	V
V_{IL}	Input Low Voltage		−0.5[1]	0.8	V
I_{IL}[2]	Input Leakage Current	0 < V_{IN} < V_{SUP}[3]		±1	µA

1. Not tested. Guaranteed by design.
2. Input leakage current includes the output leakage of the bi-directional buffers with TRI-STATE outputs.
3. V_{SUP} is V_{DD3} or V_{SB3} according to the input power well.

2.0 Device Characteristics (Continued)

2.2.2 Input, TTL Compatible, with Schmitt Trigger

Symbol: IN_{TS}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	5.5[1]	V
V_{IL}	Input Low Voltage		−0.5[1]	0.8	V
V_{HY}	Input Hysteresis		250[2]		mV
I_{IL}[3]	Input Leakage Current	$0 < V_{IN} < V_{SUP}$[4]		±1	µA

1. Not tested. Guaranteed by design.
2. Not tested. Guaranteed by characterization.
3. Input leakage current includes the output leakage of the bi-directional buffers with TRI-STATE outputs.
4. V_{SUP} is V_{DD3} or V_{SB3} according to the input power well.

2.2.3 Input, TTL Compatible, with 200 mV Schmitt Trigger

Symbol: IN_{TS2}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	5.5[1]	V
V_{IL}	Input Low Voltage		−0.5[1]	0.8	V
V_{HY}	Input Hysteresis		200[2]		mV
I_{IL}[3]	Input Leakage Current	$0 < V_{IN} < V_{SUP}$[4]		±1	µA

1. Not tested. Guaranteed by design.
2. Not tested. Guaranteed by characterization.
3. Input leakage current includes the output leakage of the bi-directional buffers with TRI-STATE outputs.
4. V_{SUP} is V_{DD3} or V_{SB3} according to the input power well.

2.2.4 Input, TTL Compatible, with 400 mV Schmitt Trigger

Symbol: IN_{TS4}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	5.5[1]	V
V_{IL}	Input Low Voltage		−0.5[1]	0.8	V
V_{HY}	Input Hysteresis		400[2]		mV
I_{IL}[3]	Input Leakage Current	$0 < V_{IN} < V_{SUP}$[4]		±1	µA

1. Not tested. Guaranteed by design.
2. Not tested. Guaranteed by characterization.
3. Input leakage current includes the output leakage of the bi-directional buffers with TRI-STATE outputs.
4. V_{SUP} is V_{DD3} or V_{SB3} according to the input power well.

2.0 Device Characteristics (Continued)

2.2.5 Input, PCI 3.3V Compatible

Symbol: IN_{PCI}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		0.5 V_{DD}	V_{DD} + 0.5[1]	V
V_{IL}	Input Low Voltage		−0.5[1]	0.3 V_{DD}	V
I_{IL}[2]	Input Leakage Current	0 < V_{IN} < V_{DD3}		±1	µA

1. Not tested. Guaranteed by design.
2. Input leakage current includes the output leakage of the bi-directional buffers with TRI-STATE outputs.

2.2.6 Input, SMBus Compatible

Symbol: IN_{SM}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		1.4	5.5[1]	V
V_{IL}	Input Low Voltage		−0.5[1]	0.8	V
I_{IL}[2]	Input Leakage Current	0 < V_{IN} < V_{SB}		±1	µA

1. Not tested. Guaranteed by design.
2. Input leakage current includes the output leakage of the bidirectional buffers with TRI-STATE outputs.

2.2.7 Analog Input

Symbol: AI

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IR}	Input Voltage Range		0	5.5[1]	V
I_{IL}	Input Leakage Current	V_{IN} = V_{IR}		300	µA

1. Not tested. Guaranteed by characterization.

2.2.8 Output, TTL/CMOS Compatible, Push-Pull Buffer

Symbol: $O_{p/n}$

Output, TTL/CMOS Compatible, rail-to-rail push-pull buffer that is capable of sourcing *p* mA and sinking *n* mA

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −*p* mA	2.4		V
		I_{OH} = −50 µA	V_{SUP} − 0.2[1]		V
V_{OL}	Output Low Voltage	I_{OL} = *n* mA		0.4	V
		I_{OL} = 50 µA		0.2	V

1. V_{SUP} is V_{DD3} or V_{SB3} according to the output power well.

2.0 Device Characteristics (Continued)

2.2.9 Output, TTL/CMOS Compatible, Open-Drain Buffer

Symbol: OD_n

Output, TTL/CMOS-compatible open-drain output buffer capable of sinking *n* mA. Output from these signals is open-drain and is never forced high.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output Low Voltage	I_{OL} = *n* mA		0.4	V
		I_{OL} = 50 µA		0.2	V

2.2.10 Output, PCI 3.3V Compatible

Symbol: O_{PCI}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{out} = –500 µA	0.9 V_{DD3}		V
V_{OL}	Output Low Voltage	I_{out} = 1500 µA		0.1 V_{DD3}	V

2.2.11 Analog Output

Symbol: AO

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OR}	Output Voltage Range		0	5.5[1]	V
V_{OD}	Output Drive Voltage	I_{out} = –3.6 mA	V_{SUP}[2] – 150 mV		
I_{OL}	Output Leakage Current	$V_{OUT} = V_{OR}$, $V_{SUP} < V_{OUT}$		20	µA

1. Not tested. Guaranteed by characterization.
2. V_{SUP} is V_{DD3} or V_{SB3} according to the pin power well.

2.2.12 Input/Output Switch, SMBus Compatible

Symbol: SW_{SM}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRP}	Pin-to-Pin Voltage Drop	I_{SW} = ±3 mA, Switch Closed		150[1]	mV
V_{ISC}	Input Voltage for Switch Closed	I_{SW} = ±3 mA	1.5[1]		V
V_{ISO}	Input Voltage for Switch Open	I_{SW} = ±20 µA		2.25	V
I_{IL}	Input Leakage Current	$V_{ISO} < V_{IN} < 5.5V$		±20[1]	µA

1. Not tested. Guaranteed by characterization.

2.0 Device Characteristics (Continued)

2.2.13 Exceptions

1. All pins are 5V tolerant except for the output pins with PCI (O_{PCI}) buffer types.
2. All pins are back-drive protected except for the output pins with PCI (O_{PCI}) buffer types.
3. The following pins have an internal static pull-up resistor (when enabled) and therefore may have leakage current from V_{SUP} (when V_{IN} = 0): SWD, $\overline{ACK}$, $\overline{AFD\_DSTRB}$, $\overline{ERR}$, $\overline{INIT}$, PE, $\overline{SLIN\_ASTRB}$, $\overline{STB\_WRITE}$, $\overline{KBRST}$, GA20, $\overline{SIOPME}$, GPIOE00-07, GPIOE10-17, GPO11-13 PWRGD_PS, $\overline{CPU\_PRESENT}$, $\overline{PRIMARY\_HD}$, $\overline{SECONDARY\_HD}$, $\overline{SCSI}$, IOPA0, IOPA1, IOPA6.
4. The following pins have an internal static pull-down resistor (when enabled) and therefore may have leakage current to V_{SS} (when $V_{IN} = V_{SUP}$): BUSY_$\overline{WAIT}$, PE and SLCT, GPIOE14, GPIOE00 (on pin 118), GPIOE07 (on pin 128), $\overline{TPM\_PP}$,.
5. The following strap pins have an internal static pull-up resistor enabled during Power-Up reset and therefore may have leakage current to V_{SUP} (when V_{IN} = 0): $\overline{BADDR}$, $\overline{TRIS}$, $\overline{TEST}$, VsbStrap1, VddStrap1, VddStrap2.
6. When V_{DD3} = 0V, the following pins present a DC load to V_{SS} of 30 KΩ minimum (not tested, guaranteed by design) for a pin voltage of 0V to 3.6V: $\overline{CTS1}$, $\overline{CTS2}$, $\overline{DCD1}$, $\overline{DCD2}$, $\overline{DSR1}$, $\overline{DSR2}$, $\overline{DTR\_BOUT1}$, $\overline{DTR\_BOUT2}$, $\overline{RI1}$, $\overline{RI2}$, $\overline{RTS1}$, $\overline{RTS2}$, SIN1, SIN2, SOUT1, SOUT2.
7. Output from SLCT, BUSY_$\overline{WAIT}$ (and PE if bit 2 of PP Confg0 register is 0) is open-drain in all SPP modes except in SPP-Compatible mode when the setup mode is ECP-based FIFO and bit 4 of the Control2 parallel port register is 1. Otherwise, output from these signals is level 2. External 4.7 KΩ pull-up resistors should be used.
8. Output from $\overline{ACK}$, $\overline{ERR}$ (and PE if bit 2 of PP Confg0 register is set to 1) is open-drain in all SPP modes except in SPP-Compatible mode when the setup mode is ECP-based FIFO and bit 4 of the Control2 parallel port register is set to 1. Otherwise, output from these signals is level 2. External 4.7 KΩ pull-up resistors should be used.
9. Output from $\overline{STB}$, $\overline{AFD}$, $\overline{INIT}$ and $\overline{SLIN}$ is open-drain in all SPP modes, except in SPP-Compatible mode when the setup mode is ECP-based (FIFO). Otherwise, output from these signals is level 2. External 4.7 KΩ pull-up resistors should be used.
10. I_{OH} is valid for a GPIO pin only when it is not configured as open-drain.
11. In XOR Tree mode, the buffer type of the input pins participating in the XOR Tree is IN_T (Input, TTL compatible), regardless of the buffer type of these pins in normal device operation mode (see Section 1.4 on page 10).

2.2.14 Terminology

Back-Drive Protection. A pin that is back-drive protected does not sink current into the supply when an input voltage higher than the supply, but below the pin's maximum input voltage, is applied to the pin. This is true even when the supply is inactive. Note that active pull-up resistors and active output buffers are typically not back-drive protected.

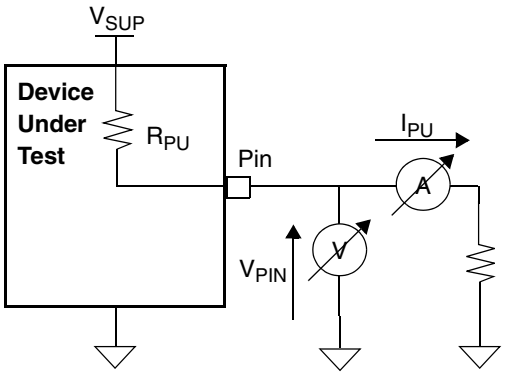
5-Volt Tolerance. An input signal that is 5V tolerant can operate with input voltage of up to 5V even though the supply to the device is only 3.3V. The actual maximum input voltage allowed to be supplied to the pin is indicated by the maximum high voltage allowed for the input buffer. Note that some pins have multiple buffers, not all of which are 5V tolerant. In such cases, there is a note that indicates at what conditions a 5V input may be applied to the pin; if there is no note, the low maximum voltage among the buffers is the maximum voltage allowed for the pin.

2.0 Device Characteristics (Continued)

2.3 INTERNAL RESISTORS

DC Test Conditions

Pull-Up Resistor Test Circuit



Pull-Down Resistor Test Circuit

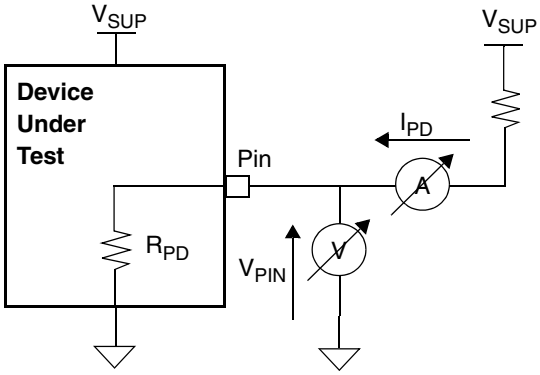


Figure 1. Internal Resistor Test Conditions, T_A = 0°C to 70°C, V_{SUP} = 3.3V

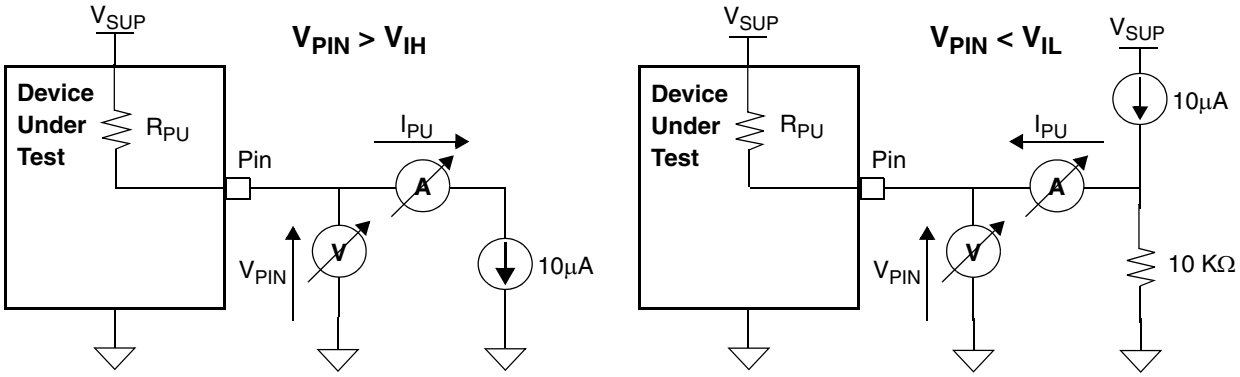


Figure 2. Internal Pull-Down Resistor for Straps, T_A = 0°C to 70°C, V_{SUP} = 3.3V

Notes for Figures 1 and 2:

1. V_{SUP} is V_{DD3} or V_{SB3} according to the pin power well.
2. The equivalent resistance of the pull-up resistor is calculated by $R_{PU} = (V_{SUP} - V_{PIN}) / I_{PU}$.
3. The equivalent resistance of the pull-down resistor is calculated by $R_{PD} = V_{PIN} / I_{PD}$.

2.3.1 Pull-Up Resistor

Symbol: PU_{nn}

Symbol	Parameter	Conditions[1]	Min[2]	Typical	Max[2]	Unit
R_{PU}	Pull-up equivalent resistance	V_{PIN} = 0V	*nn* – 30%	*nn*	*nn* + 30%	KΩ
		V_{PIN} = 0.8 V_{SUP}[3]			*nn* – 38%	KΩ
		V_{PIN} = 0.17 V_{SUP}[3]	*nn* – 35%			KΩ

1. TA = 0°C to 70°C, V_{SUP} = 3.3V.
2. Not tested. Guaranteed by characterization.
3. For strap pins only.

2.3.2 Pull-Down Resistor

Symbol: PD_{nn}

Symbol	Parameter	Conditions[1]	Min[2]	Typical	Max[2]	Unit
R_{PD}	Pull-down equivalent resistance	V_{PIN} = V_{SUP}	*nn* – 30%	*nn*	*nn* + 30%	KΩ

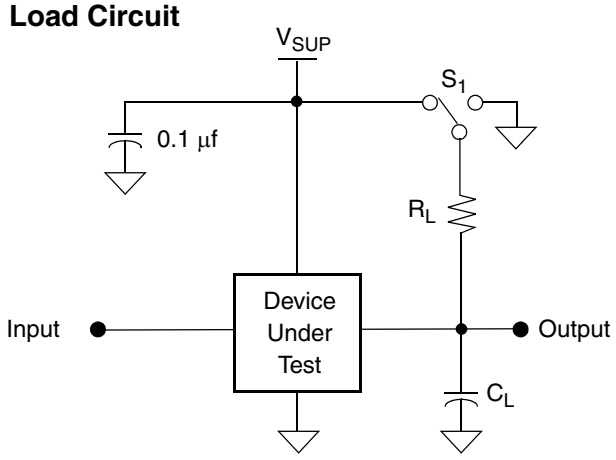
1. TA = 0°C to 70°C, V_{SUP} = 3.3V.
2. Not tested. Guaranteed by characterization.

2.0 Device Characteristics (Continued)

2.4 AC ELECTRICAL CHARACTERISTICS

2.4.1 AC Test Conditions

Load Circuit



AC Testing Input, Output Waveform

(unless otherwise specified)

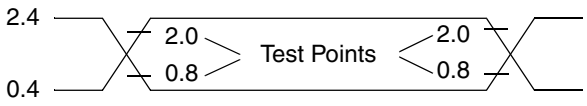


Figure 3. AC Test Conditions, T_A = 0°C to 70°C, V_{SUP} = 3.3V ±10%

Notes:

1. V_{SUP} is either V_{DD3} or V_{SB3}, according to the pin power well.
2. C_L = 50 pF for all output pins except the following pin groups:
   – C_L = 100 pF for Serial Port 1 and 2 pins (see Section 1.4.2 on page 10), Parallel Port pins (see Section 1.4.4 on page 11) and Floppy Disk Controller pins (see Section 1.4.5 on page 12).
   – C_L = 40 pF for $\overline{\text{IDE\_RSTDRV}}$ pin.
   – C_L = 400 pF for SMBus pins (see "SMBus Voltage Translation and Isolation Timing" on page 44).
   These values include both jig and oscilloscope capacitance.
3. S_1 = Open – for push-pull output pins.
   S_1 = V_{SUP} – for high impedance to active low and active low to high-impedance transition measurements.
   S_1 = GND – for high impedance to active high and active high to high-impedance transition measurements.
   R_L = 1.0 KΩ – for all the pins
4. For the FDC open-drain interface pins, S_1 = V_{DD3} and R_L = 150Ω.

2.4.2 Reset Timing

V_{SB} Power-Up Reset

Symbol	Figure	Description	Reference Conditions		Min[1]	Max[1]
t_{IRST}	4	Internal Power-Up Reset Time	V_{SB3} power-up to end of internal reset	Ended by 32 KHz Clock Domain		$t_{32KW} + t_{32KVAL}$[2] + 17 * t_{CP}
	5			Ended by $\overline{\text{PCI\_RESET}}$		t_{LRST}
t_{LRST}	5	$\overline{\text{PCI\_RESET}}$ active time	V_{SB3} power-up to end of $\overline{\text{PCI\_RESET}}$		10 ms	
t_{IPLV}	5	Internal VsbStrap1 strap pull-up resistor, valid time[3]	Before end of internal reset		t_{IRST}	
t_{EPLV}	5	External VsbStrap1 strap pull-down resistor, valid time	Before end of internal reset		t_{IRST}	

1. Not tested. Guaranteed by design.
2. t_{32KW} + t_{32KVAL} from V_{SB3} power-up to 32 KHz domain toggling; see "Low-Frequency Clock Timing" on page 32.
3. Active only during V_{SB3} Power-Up reset.

2.0 Device Characteristics (Continued)

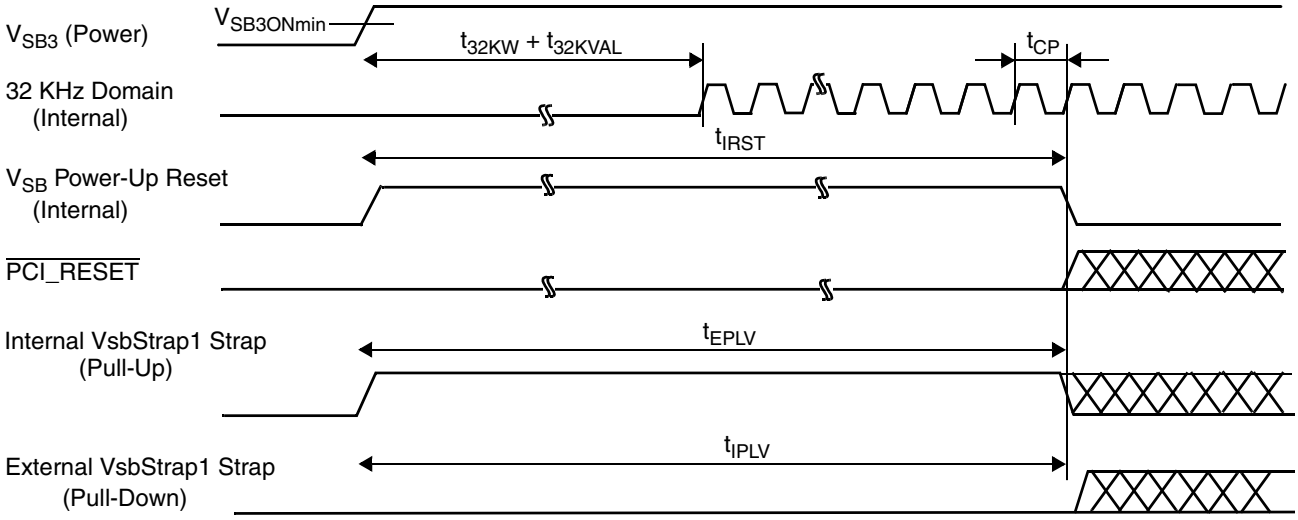


Figure 4. Internal V_{SB} Power-Up Reset - Ended by 32 KHz Clock

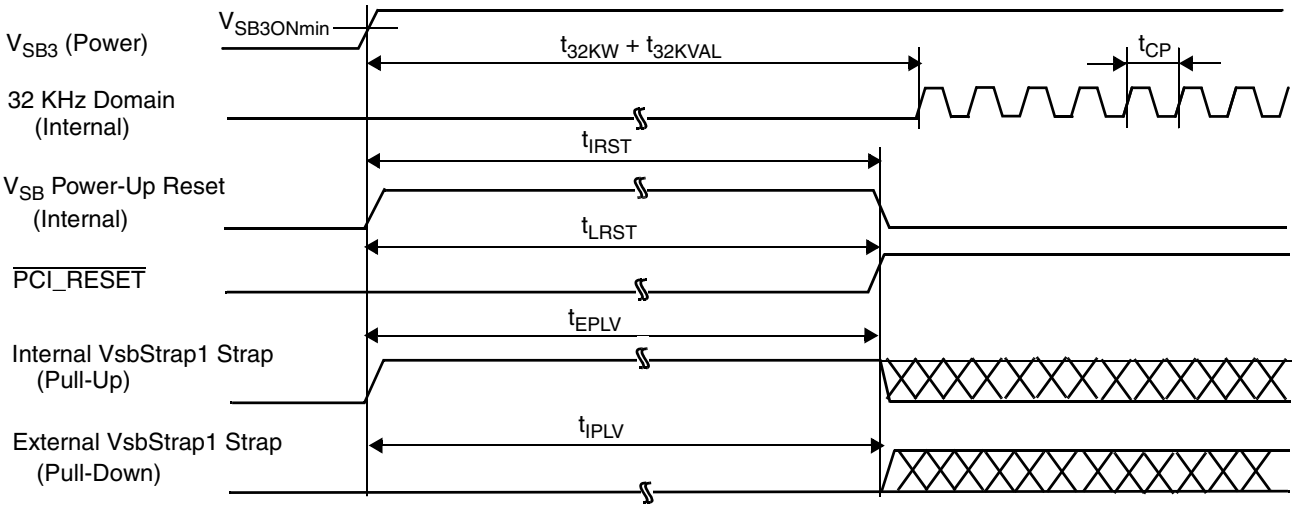


Figure 5. Internal V_{SB} Power-Up Reset - Ended by $\overline{\text{PCI\_RESET}}$

2.0 Device Characteristics (Continued)

V_{DD} Power-Up Reset

Symbol	Figure	Description	Reference Conditions	Min[1]	Max[1]
t_{IRST}	6	Internal Power-Up reset time	V_{DD3} power-up to end of internal reset		t_{LRST}
t_{LRST}	6	$\overline{PCI\_RESET}$ active time	V_{DD3} power-up to end of $\overline{PCI\_RESET}$	10 ms	2.5 s
t_{IPLV}	6	Internal strap pull-up resistor, valid time[2]	Before end of internal reset	t_{IRST}	
t_{EPLV}	6	External strap pull-down resistor, valid time	Before end of internal reset	t_{IRST}	

1. Not tested. Guaranteed by design.
2. Active only during V_{DD3} Power-Up reset.

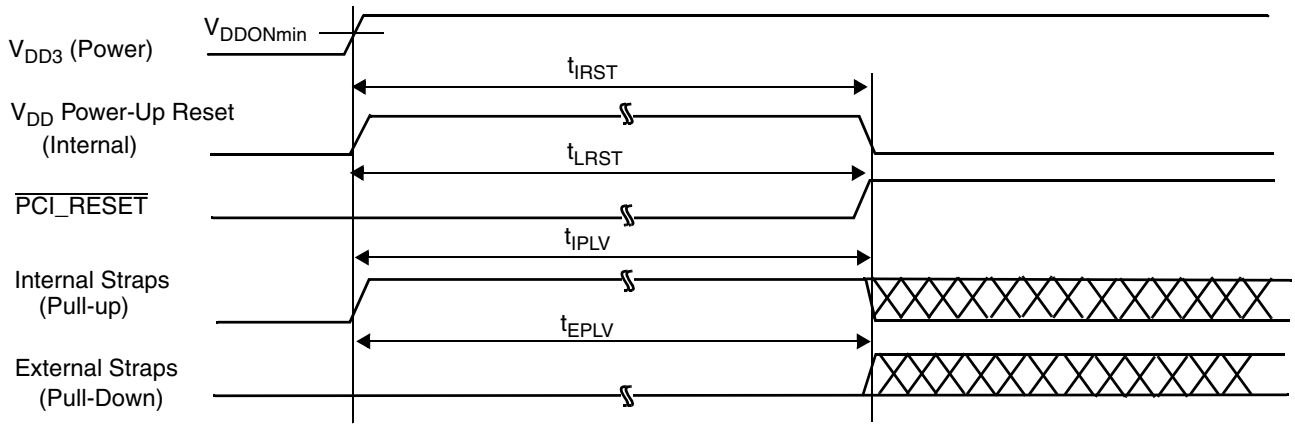


Figure 6. Internal V_{DD} Power-Up Reset

Hardware Reset

Symbol	Figure	Description	Reference Conditions	Min	Max
t_{WRST}	7	$\overline{PCI\_RESET}$ pulse width		100 ns	

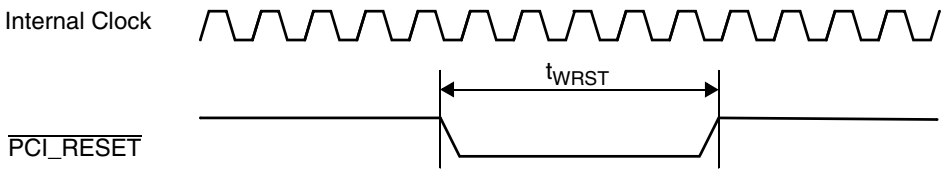


Figure 7. Hardware Reset

2.0 Device Characteristics (Continued)

2.4.3 Clock Timing

High-Frequency Clock Timing

Symbol	Figure	Clock Input Parameters	Reference Conditions	CLOCKI14			Units
				Min	Typ	Max	
t_{CH}	8	Clock High Pulse Width[1]		20			ns
t_{CL}	8	Clock Low Pulse Width[1]		20			ns
t_{CP}	8	Clock Period[1] (50%-50%)		69.14	69.84	70.54	ns
F_{CK}	–	Clock Frequency		F_{CKTYP} – 1%	14.31818	F_{CKTYP} + 1%	MHz
t_{CR}	8	Clock Rise Time[1] (V_{IL} to V_{IH})				5[2]	ns
t_{CF}	8	Clock Fall Time[1] (V_{IH} to V_{IL})				5[2]	ns
t_{CE}	9	Clock Generator Enable	RE $\overline{\text{PCI\_RESET}}$ to Clock Generator enabled			80	µs

1. Not tested. Guaranteed by design.
2. Recommended value.

Sym.	Fig.	Internal Clock Parameter	Reference Conditions	INT48M			Units
				Min	Typ	Max	
t_{CP}	8	Clock Period[1] (50%-50%)			20.83		ns
F_{CK}	–	Clock Frequency			48		MHz
t_{48MD}	9	Clock Wake-Up Time[1]	After Clock Generator enabled			500	µs

1. Not tested. Guaranteed by characterization.

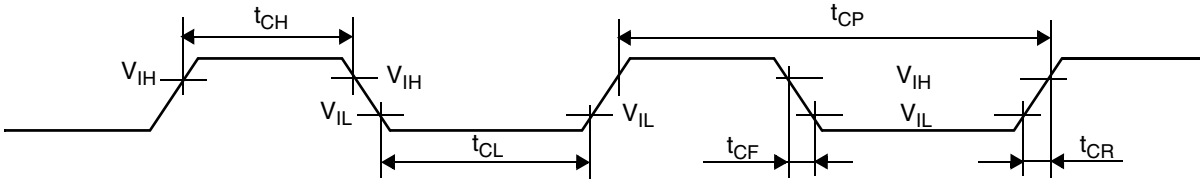


Figure 8. High-Frequency Clock Waveform Timing

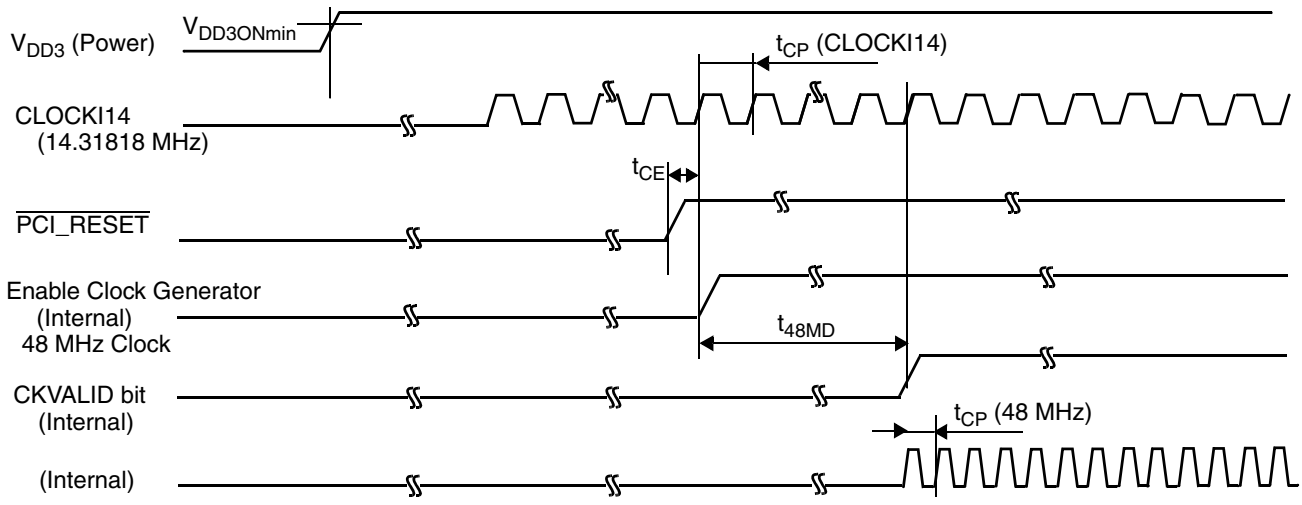


Figure 9. CLOCKI14 and Internal 48 MHz Clock Timing

2.0 Device Characteristics (Continued)

Low-Frequency Clock Timing

Symbol	Figure	Internal Clock Parameters	Reference Conditions	INT32K			Units
				Min	Typ	Max	
t_{CP}	10	Clock Period[1] (50%-50%)	After V_{SB3} power-up	21.3623	30.517578	39.6728	µs
t_{CPL}	10	Clock Period[1] (50%-50%)	After CLOCKI14 valid	30.2124	30.517578	30.8227	µs
			When V_{DD3} does not exist	27.465820	30.517578	33.569336	
F_{CK}	–	Clock Frequency	After V_{SB3} power-up	F_{32TYP} – 30%	32.768 (F_{32TYP})	F_{32TYP} + 30%	KHz
F_{CKL}		Clock Frequency	After CLOCKI14 valid	F_{32TYP} – 1%	32.768 (F_{32TYP})	F_{32TYP} + 1%	
			When V_{DD3} does not exist	F_{32TYP} – 10%	32.768 (F_{32TYP})	F_{32TYP} + 10%	
t_{32KW}	10	Clock wake-up time[1]	V_{SB3} stable to clock start toggling			5	ms
t_{32KVAL}	10	Clock valid time[1]	Clock start toggling to clock valid			1	ms

1. Not tested. Guaranteed by characterization.

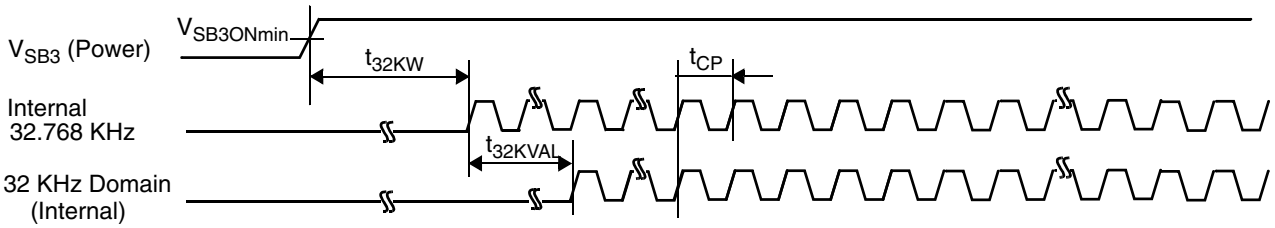


Figure 10. Internal 32 KHz (INT32K) and CLOCKO32 Timing

2.0 Device Characteristics (Continued)

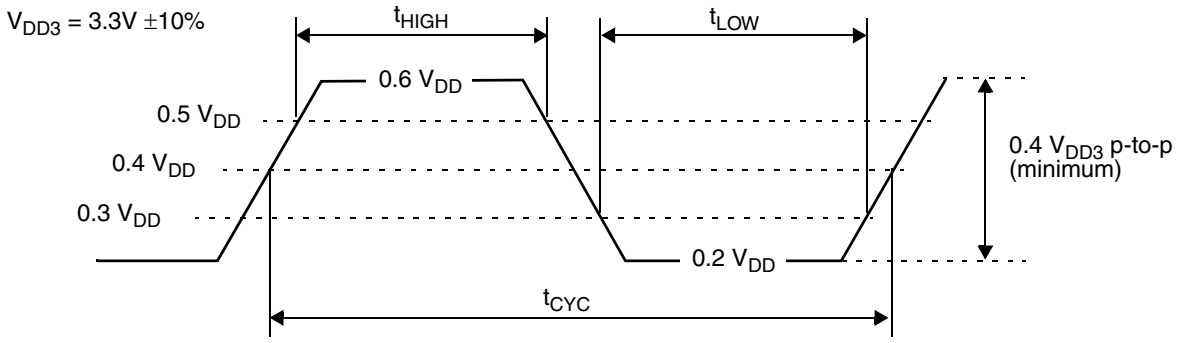
2.4.4 LPC Interface Timing

The AC characteristics of the LPC interface meet the PCI Local Bus Specification *(Rev 2.2 December 18, 1998)* for 3.3V DC signaling.

PCI_CLK and $\overline{\text{PCI\_RESET}}$

Symbol	Parameter	Min	Max	Units
t_{CYC}[1]	PCI_CLK Cycle Time	30		ns
t_{HIGH}	PCI_CLK High Time[2]	11		ns
t_{LOW}	PCI_CLK Low Time[2]	11		ns
–	PCI_CLK Slew Rate[2,3]	1	4	V/ns
–	$\overline{\text{PCI\_RESET}}$ Slew Rate[2,4]	50		mV/ns

1. The PCI may have any clock frequency between nominal DC and 33 MHz. Device operational parameters at frequencies under 16 MHz are guaranteed by design rather than by testing. The clock frequency may be changed at any time during the operation of the system as long as the clock edges remain “clean” (monotonic) and the minimum cycle high and low times are not violated. The clock may only be stopped in a low state.
2. Not tested. Guaranteed by characterization.
3. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock wavering (0.2 * V_{DD3} to 0.6 * V_{DD3}) as shown below.
4. The minimum $\overline{\text{PCI\_RESET}}$ slew rate applies only to the rising (de-assertion) edge of the reset signal and ensures that system noise cannot make an otherwise monotonic signal appear to bounce in the switching range.



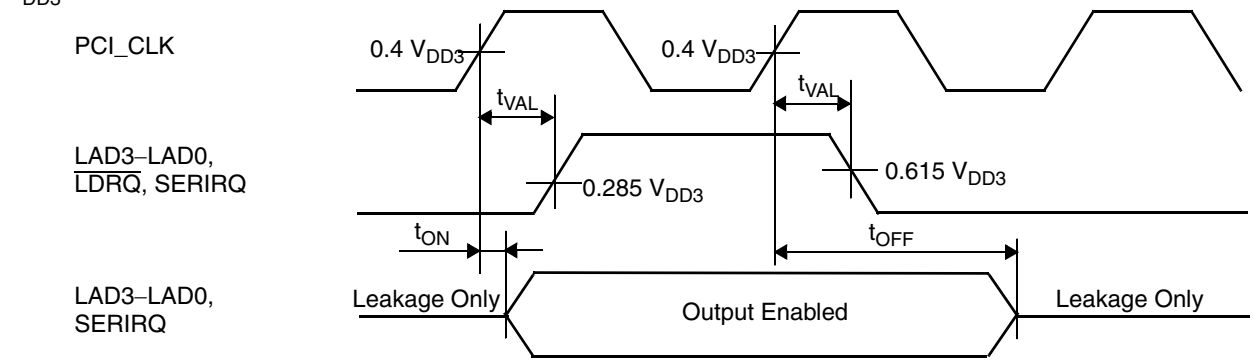
2.0 Device Characteristics (Continued)

LPC Signals

Symbol	Figure	Description	Reference Conditions	Min	Max	Unit
t_{VAL}	Outputs	Output Valid Delay	After RE of CLK	2	11	ns
t_{ON}	Outputs	Float to Active Delay	After RE of CLK	2		ns
t_{OFF}	Outputs	Active to Float Delay	After RE of CLK		28	ns
t_{SU}	Inputs	Input Setup Time	Before RE of CLK	7		ns
t_{HL}	Inputs	Input Hold Time	After RE of CLK	0		ns

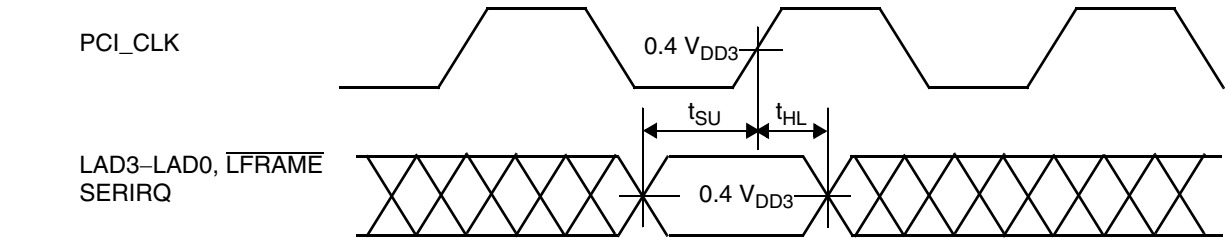
Outputs

V_{DD3} = 3.3V ±10%



Inputs

V_{DD3} = 3.3V ±10%



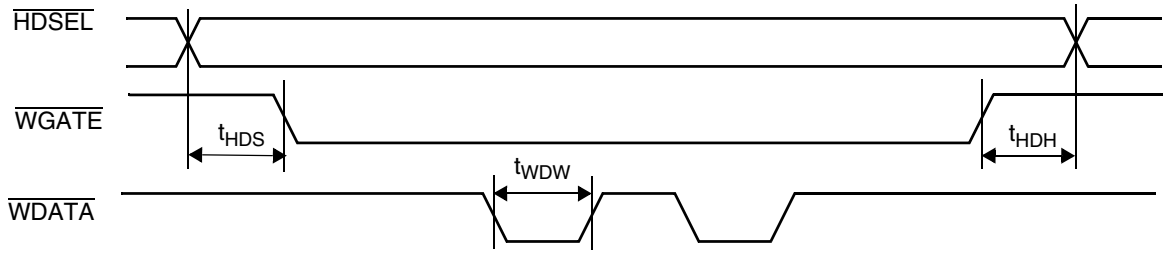
2.0 Device Characteristics (Continued)

2.4.5 FDC Timing

FDC Write Data Timing

Symbol	Parameter	Min	Max	Unit
t_{HDH}	$\overline{HDSEL}$ Hold from $\overline{WGATE}$ Inactive[1]	100		µs
t_{HDS}	$\overline{HDSEL}$ Setup to $\overline{WGATE}$ Active[1]	100		µs
t_{WDW}	Write Data Pulse Width[1]	See t_{DRP}, t_{ICP} and t_{WDW} values in table below		

1. Not tested. Guaranteed by design.



t_{DRP}, t_{ICP}, t_{WDW} Values

Data Rate	t_{DRP}	t_{ICP}	t_{ICP} Nominal	t_{WDW}	t_{WDW} Minimum	Unit
1 Mbps	1000	6 x t_{CP}[1]	125	2 x t_{ICP}	250	ns
500 Kbps	2000	6 x t_{CP}[1]	125	2 x t_{ICP}	250	ns
300 Kbps	3333	10 x t_{CP}[1]	208	2 x t_{ICP}	375	ns
250 Kbps	4000	12 x t_{CP}[1]	250	2 x t_{ICP}	500	ns

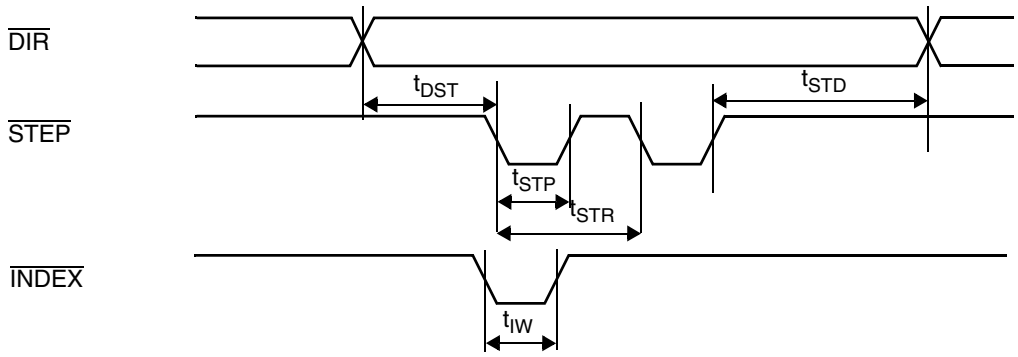
1. t_{CP} is the clock period defined for CLOCKI in “Clock Timing” on page 31.

FDC Drive Control Timing

Symbol	Parameter	Min	Max	Unit
t_{DST}	$\overline{DIR}$ Setup to $\overline{STEP}$ Active[1]	6		µs
t_{IW}	Index Pulse Width	100		ns
t_{STD}	$\overline{DIR}$ Hold from $\overline{STEP}$ Inactive	t_{STR}		ms
t_{STP}	$\overline{STEP}$ Active (Low) Pulse Width[1]	8		µs
t_{STR}	$\overline{STEP}$ Rate Time[1]	0.5		ms

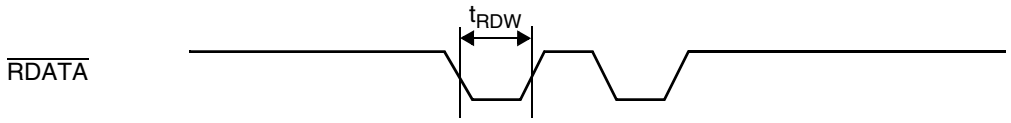
1. Not tested. Guaranteed by design.

2.0 Device Characteristics (Continued)



FDC Read Data Timing

Symbol	Parameter	Min	Max	Unit
t_{RDW}	Read Data Pulse Width	50		ns

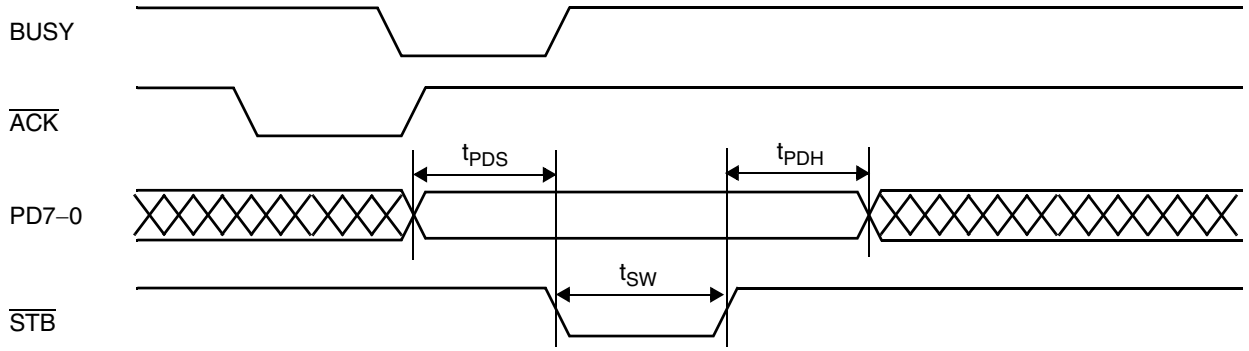


2.0 Device Characteristics (Continued)

2.4.6 Parallel Port Timing

Standard Parallel Port Timing

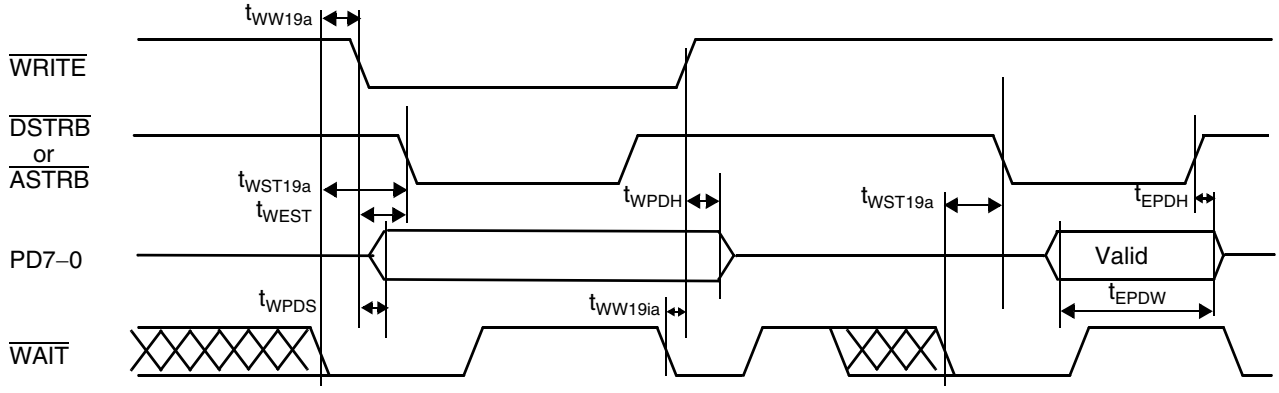
Symbol	Parameter	Conditions	Min	Max	Unit
t_{PDH}	Port Data Hold	SPP Mode 0 and Mode 1, ECP Mode 0 and Mode1: system dependent; ECP Mode 2: device dependent.	750		ns
t_{PDS}	Port Data Setup	SPP Mode 0 and Mode 1, ECP Mode 0 and Mode1: system dependent; ECP Mode 2: device dependent.	750		ns
t_{SW}	Strobe Width	SPP Mode 0 and Mode 1, ECP Mode 0 and Mode1: system dependent; ECP Mode 2: device dependent.	750		ns



Enhanced Parallel Port Timing

Symbol	Parameter	Min	Max	EPP 1.7[1]	EPP 1.9[1]	Unit
t_{WW19a}	$\overline{WRITE}$ Active from $\overline{WAIT}$ Low		45		✔	ns
t_{WW19ia}	$\overline{WRITE}$ Inactive from $\overline{WAIT}$ Low		45		✔	ns
t_{WST19a}	$\overline{DSTRB}$ or $\overline{ASTRB}$ Active from $\overline{WAIT}$ Low		65		✔	ns
t_{WEST}	$\overline{DSTRB}$ or $\overline{ASTRB}$ Active after $\overline{WRITE}$ Active	10		✔	✔	ns
t_{WPDH}	PD7–0 Hold after $\overline{WRITE}$ Inactive	0		✔	✔	ns
t_{WPDS}	PD7–0 Valid after $\overline{WRITE}$ Active		15	✔	✔	ns
t_{EPDW}	PD7–0 Valid Width	80		✔	✔	ns
t_{EPDH}	PD7–0 Hold after $\overline{DSTRB}$ or $\overline{ASTRB}$ Inactive	0		✔	✔	ns

1. Also in ECP Mode 4.



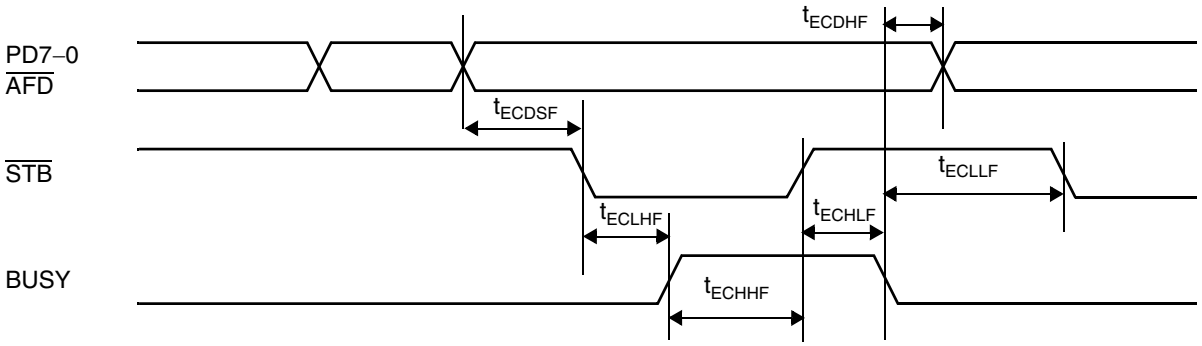
2.0 Device Characteristics (Continued)

Extended Capabilities Port (ECP) Timing

Forward Mode

Symbol	Parameter	Min	Max	Unit
t_{ECDSF}	Data Setup before $\overline{STB}$ Active	0		ns
t_{ECDHF}	Data Hold after BUSY Inactive	0		ns
t_{ECLHF}	BUSY Active after $\overline{STB}$ Active	75		ns
t_{ECHHF}	$\overline{STB}$ Inactive after BUSY Active[1]	0	1	s
t_{ECHLF}	BUSY Inactive after $\overline{STB}$ Inactive[1]	0	35	ms
t_{ECLLF}	$\overline{STB}$ Active after BUSY Inactive	0		ns

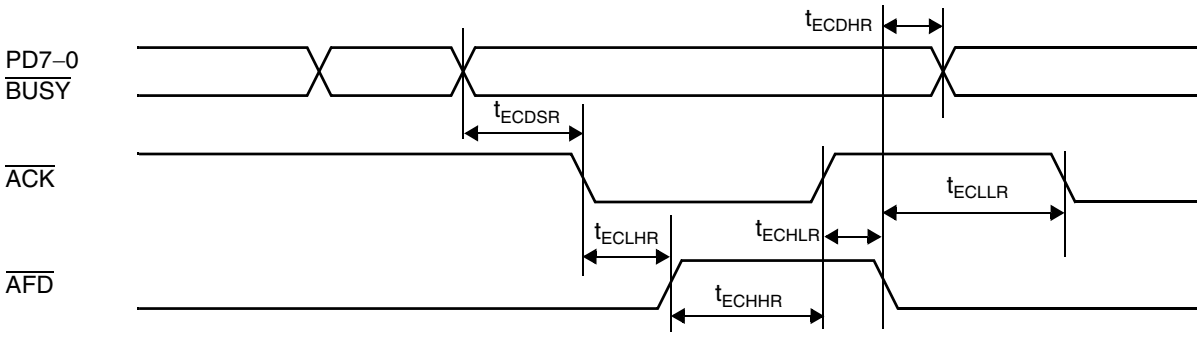
1. Not tested. Guaranteed by design.



Reverse Mode

Symbol	Parameter	Min	Max	Unit
t_{ECDSR}	Data Setup before $\overline{ACK}$ Active	0		ns
t_{ECDHR}	Data Hold after $\overline{AFD}$ Active	0		ns
t_{ECLHR}	$\overline{AFD}$ Inactive after $\overline{ACK}$ Active	75		ns
t_{ECHHR}	$\overline{ACK}$ Inactive after $\overline{AFD}$ Inactive[1]	0	35	ms
t_{ECHLR}	$\overline{AFD}$ Active after $\overline{ACK}$ Inactive[1]	0	1	s
t_{ECLLR}	$\overline{ACK}$ Active after $\overline{AFD}$ Active	0		ns

1. Not tested. Guaranteed by design.



2.0 Device Characteristics (Continued)

2.4.7 Serial Ports 1 and 2 Timing

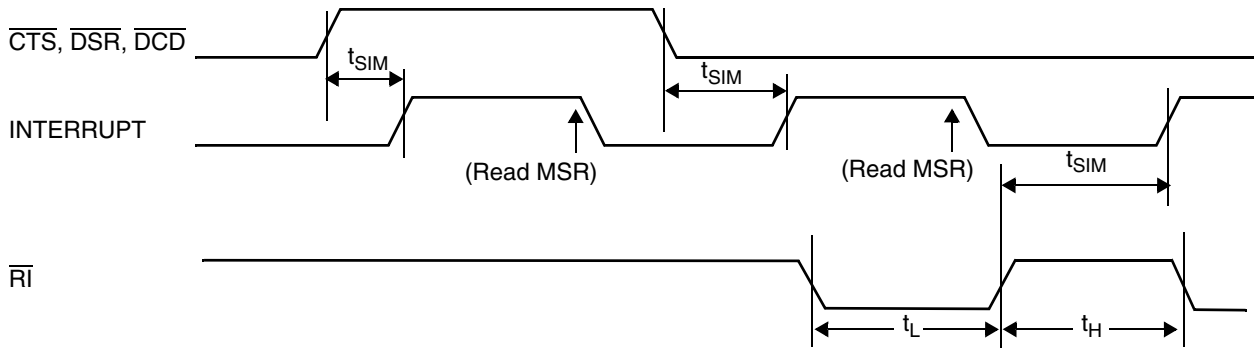
Serial Port Data Timing

See Section 2.4.8 on page 40.

Modem Control Timing

Symbol	Parameter	Min	Max	Unit
t_L	$\overline{RI1,2}$ Low Time[1,2]	10		ns
t_H	$\overline{RI1,2}$ High Time[1,2]	10		ns
t_{SIM}	Delay to Set IRQ from Modem Input		40	ns

1. Not tested. Guaranteed by characterization.
2. The value also applies to $\overline{RI1,2}$ wake-up detection in the SWC module.

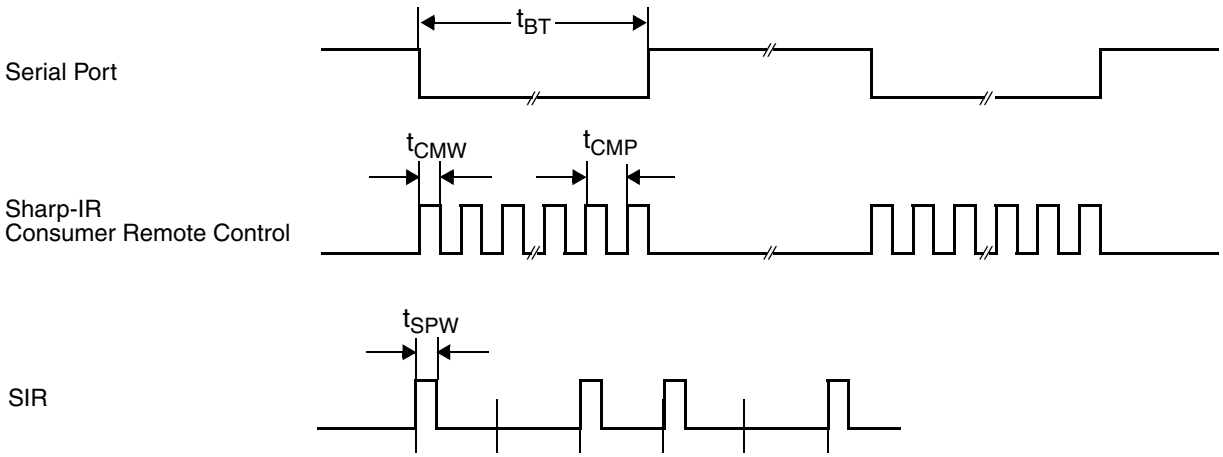


2.0 Device Characteristics (Continued)

2.4.8 Serial Port, Sharp-IR, SIR and Consumer Remote Control Timing

Symbol	Parameter	Conditions	Min[1]	Max[1]	Unit
t_{BT}	Single Bit Time in Serial Port and Sharp-IR	Transmitter	$t_{BTN} - 25$[2]	$t_{BTN} + 25$	ns
		Receiver	$t_{BTN} - 2\%$	$t_{BTN} + 2\%$	ns
t_{CMW}	Modulation Signal Pulse Width in Sharp-IR and Consumer Remote Control	Transmitter	$t_{CWN} - 25$[3]	$t_{CWN} + 25$	ns
		Receiver	500		ns
t_{CMP}	Modulation Signal Period in Sharp-IR and Consumer Remote Control	Transmitter	$t_{CPN} - 25$[4]	$t_{CPN} + 25$	ns
		Receiver	t_{MMIN}[5]	t_{MMAX}[5]	ns
t_{SPW}	SIR Signal Pulse Width	Transmitter, Variable	$(3/16) \times t_{BTN} - 15$[2]	$(3/16) \times t_{BTN} + 15$[2]	ns
		Transmitter, Fixed	1.48	1.78	µs
		Receiver	1		µs
S_{DRT}	SIR Data Rate Tolerance. % of Nominal Data Rate.	Transmitter		± 0.87%	
		Receiver		± 2.0%	
t_{SJT}	SIR Leading Edge Jitter. % of Nominal Bit Duration.	Transmitter		± 2.5%	
		Receiver		± 6.5%	

1. Not tested. Guaranteed by design.
2. t_{BTN} is the nominal bit time in Serial Port, Sharp-IR, SIR and Consumer Remote Control modes. It is determined by the setting of the Baud Generator Divisor registers.
3. t_{CWN} is the nominal pulse width of the modulation signal for Sharp-IR and Consumer Remote Control modes. It is determined by MCPW field (bits 7-5) of IRTXMC register and TXHSC bit (bit 2) of RCCFG register.
4. t_{CPN} is the nominal period of the modulation signal for Sharp-IR and Consumer Remote Control modes. It is determined by MCFR field (bits 4-0) of IRTXMC register and the TXHSC bit (bit 2) of RCCFG register.
5. t_{MMIN} and t_{MMAX} define the time range within which the period of the incoming subcarrier signal has to fall in order for the signal to be accepted by the receiver. These time values are determined by the contents of the IRRXDC register and the setting of RXHSC bit (bit 5) of RCCFG register.



2.0 Device Characteristics (Continued)

2.4.9 Glue Function Timing

Highest Active Main and Standby Supply Reference

Symbol	Figure	Description	Reference Conditions	Min	Max
Main					
t_{PD}	11	V_{DD3} to REF5V Propagation Delay[1]	V_{DD5} = 0; V_{DD3} slew rate > 10 V/ms		1 ms
Standby					
t_{PD}	11	V_{SB3} to REF5V_STBY Propagation Delay[1]	V_{SB5} = 0; V_{SB3} slew rate > 10 V/ms		1 ms

1. Not tested. Guaranteed by design.

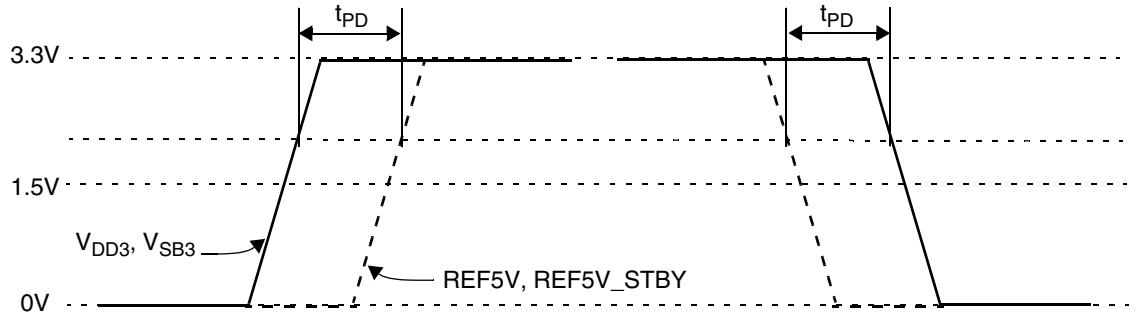


Figure 11. REF5V and REF5V_STBY (AC Characteristics)

Resume Reset

Symbol	Figure	Description	Reference Conditions	Min	Max	Units
t_{RD}	12	Rising Supply Delay[1] (typ. 32 ms)	$V_{SB5} > V_{TRIP}$ and $V_{SB3} > V_{SB3ON}$	20	100	ms
t_{FD5}	12	Falling V_{SB5} Supply Delay[1]	$V_{SB5} < V_{TRIP}$ and $V_{SB3} > V_{SB3ON}$		100	ns
t_{GA}	12	V_{SB5} and V_{SB3} Glitch Allowance[1]	$V_{SB5} < V_{TRIP}$ or $V_{SB3} < V_{SB3OFF}$		100	ns
t_{FD3}	12	Falling V_{SB3} Supply Delay[1]	$V_{SB3} < V_{SB3OFF}$ and $V_{SB5} > V_{TRIP}$		100	ns
t_R	12	Rise Time[2]	$V_{SB3} > V_{SB3ON}$		100	ns
t_F	12	Fall Time[2]	$V_{SB3} > V_{SB3ON}$		100	ns

1. Not tested. Guaranteed by characterization.
2. Not tested. Guaranteed by design.

2.0 Device Characteristics (Continued)

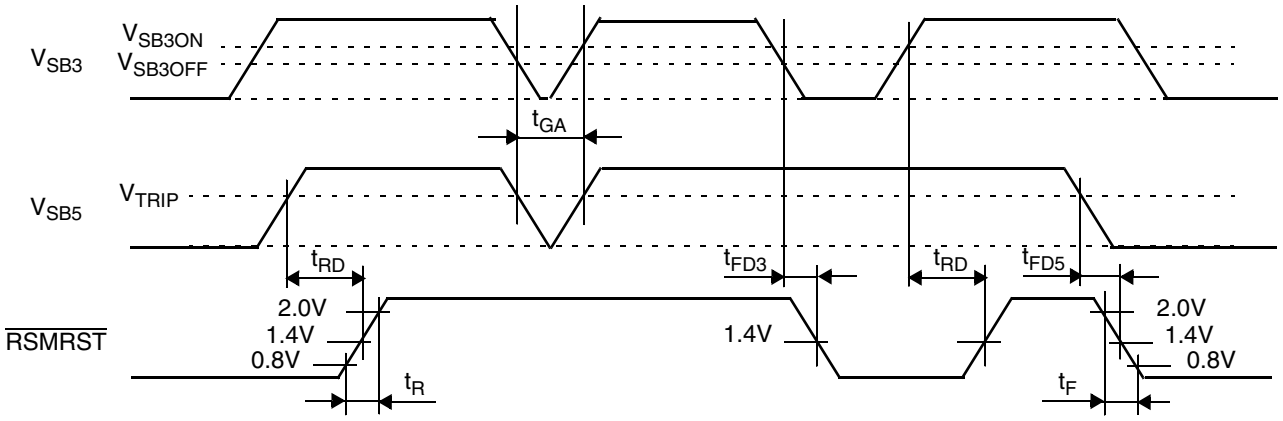


Figure 12. $\overline{\text{RSMRST}}$ (AC Characteristics)

PCI Reset Buffering

Symbol	Figure	Description	Reference Conditions	Min	Max	Units
t_{PDR}	13	Rise Propagation Delay	From RE of $\overline{\text{PCI\_RESET}}$ to RE of $\overline{\text{PCIRST\_OUT}}$, $\overline{\text{PCIRST\_OUT2}}$		30	ns
t_R	13	Rise Time	$\overline{\text{PCIRST\_OUT}}$, $\overline{\text{PCIRST\_OUT2}}$		50	ns
t_{PDF}	13	Fall Propagation Delay	From FE of $\overline{\text{PCI\_RESET}}$ to FE of $\overline{\text{IDE\_RSTDRV}}$		20	ns
t_F	13	Fall Time	$\overline{\text{IDE\_RSTDRV}}$		15	ns

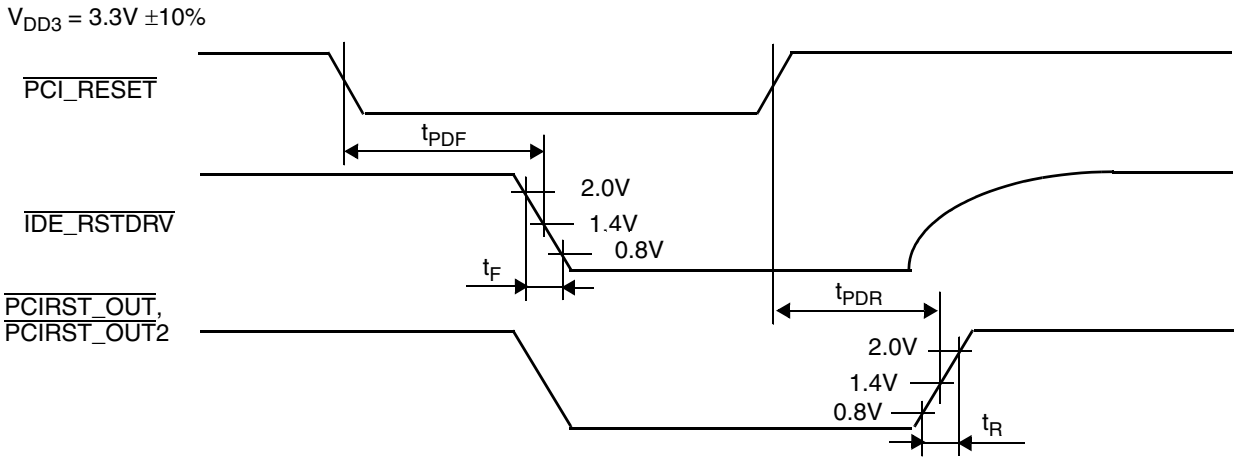


Figure 13. Reset Outputs

2.0 Device Characteristics (Continued)

Main Power Good

Symbol	Figure	Description	Reference Conditions	Min	Max	Units
t_{PSD}	–	Low-to-High Delay[1]	After RE of PWRGD_PS	100	120	ms
t_{S3D}	–	High-to-Low Delay[1]	After FE of $\overline{SLP\_S3}$		20	ns
t_R	–	PWRGD_3V Rise Time[1]	0.8V to 2.0V		50	ns
t_F	–	PWRGD_3V Fall Time[1]	2.0V to 0.8V		50	ns

1. Not tested. Guaranteed by design.

Power Distribution Control

Symbol	Figure	Description	Reference Conditions	Min	Max	Units
t_{PB}	–	$\overline{BKFD\_CUT}$ Propagation Delay[1]	PWRGD_PS or $\overline{SLP\_S3}$ to $\overline{BKFD\_CUT}$		1	µs
t_{TB}	–	$\overline{BKFD\_CUT}$ Transition Time[1]	0.8V to 2.0V		50	ns
t_{PL}	14	LATCHED_BF_CUT Propagation Delay[1]	$\overline{BKFD\_CUT}$ or $\overline{SLP\_S5}$ to LATCHED_BF_CUT		1	µs
t_{TL}	14	LATCHED_BF_CUT Transition Time[1]	0.8V to 2.0V		50	ns

1. Not tested. Guaranteed by design.

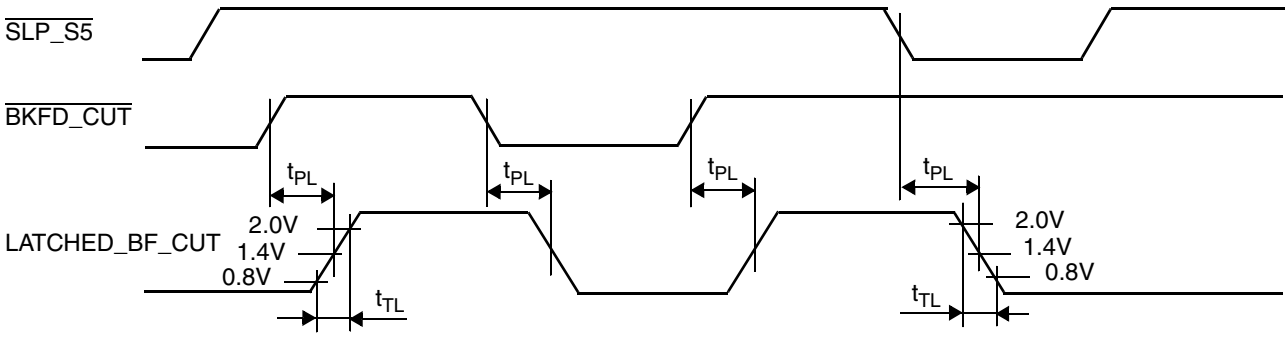


Figure 14. $\overline{BKFD\_CUT}$ and LATCHED_BF_CUT (AC Characteristics)

2.0 Device Characteristics (Continued)

Main Power Supply Control

Symbol	Figure	Description	Reference Conditions	Min	Max	Units
t_{PR}	–	Rise Propagation Delay[1,2]	($\overline{CPU\_PRESENT}$ = 1) or ($\overline{SLP\_S3}$ = 0) or (ETC event occurred) to RE of $\overline{PS\_ON}$		1	µs
t_{PF}	–	Fall Propagation Delay[1]	From whichever occurs last: ($\overline{CPU\_PRESENT}$ = 0), ($\overline{SLP\_S3}$ = 1), (No ETC event and RE on $\overline{SLP\_S3}$) to FE of $\overline{PS\_ON}$		1	µs
t_R	–	Rise Time[1,2]	0.8V to 2.0V		50	ns
t_F	–	Fall Time[1]	2.0V to 0.8V		50	ns

1. Not tested. Guaranteed by design.
2. Test conditions: C_L = 50 pF and 1 KΩ external resistor to V_{SB5}.

SMBus Voltage Translation and Isolation Timing

Symbol	Figure	Description	Type of Requirement[1]	Min	Max	Unit
t_{SMBR}	–	Rise Time (all signals)	Input		1000[2,3]	ns
t_{SMBF}	–	Fall Time (all signals)	Input		250[3]	ns
			Output		300[2,4]	ns
t_{SMBD}	–	Propagation Delay (each signal pair, in both directions)	Output		500[2,4]	ns

1. An “Input” type is a value the PC8374T device expects from the system; an “Output” type is a value the PC8374T device provides to the system.
2. Test conditions: R_L = 1 KΩ to V_{DD3} = 2.25V or 3.3V, or R_L = 1.5 KΩ to V_{DD5} = 5V and C_L = 400 pF to GND.
3. Not tested. Guaranteed by design.
4. Not tested. Guaranteed by characterization.

2.0 Device Characteristics (Continued)

2.4.10 SWC Timing

Wake-Up Inputs at V_{SB3} Power Switching

Symbol	Figure	Description	Reference Conditions	Min	Max
t_{EWIV}	15	External Wake-Up Inputs Valid[1]	At V_{SB3} power on, after the 32 KHz Domain is toggling	24576 * t_{CP}[2]	32768 * t_{CP}

1. Not tested. Guaranteed by characterization.
2. t_{CP} is the cycle time of the 32 KHz clock domain (see "Low-Frequency Clock Timing" on page 32).

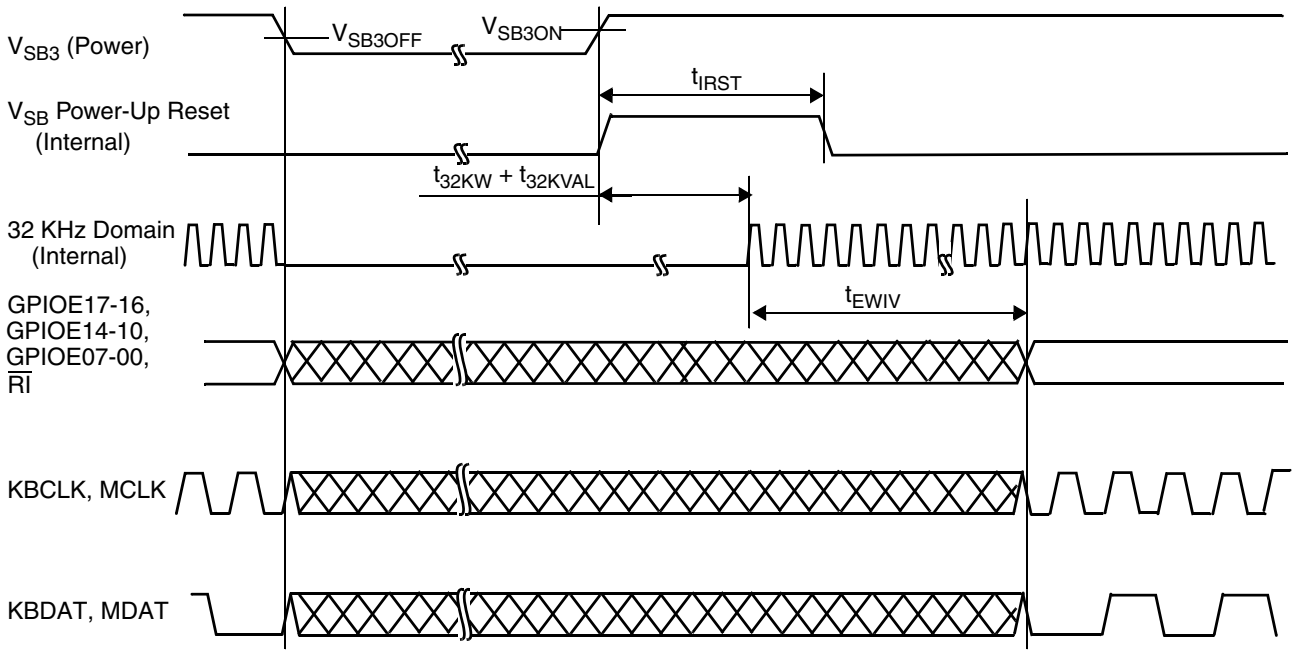


Figure 15. Inputs at V_{SB3} Power Switching

Wake-Up Inputs at V_{DD3} Power Switching

Symbol	Figure	Description	Reference Conditions	Min	Max
t_{EWIV}	16	External Wake-Up Inputs Valid[1]	After V_{DD3} power on[2]	24576 * t_{CP}[3]	32768 * t_{CP}

1. Not tested. Guaranteed by characterization.
2. The 32 KHz clock domain is assumed to be toggling at V_{DD3} power stable.
3. t_{CP} is the cycle time of the 32 KHz clock domain (see "Low-Frequency Clock Timing" on page 32).

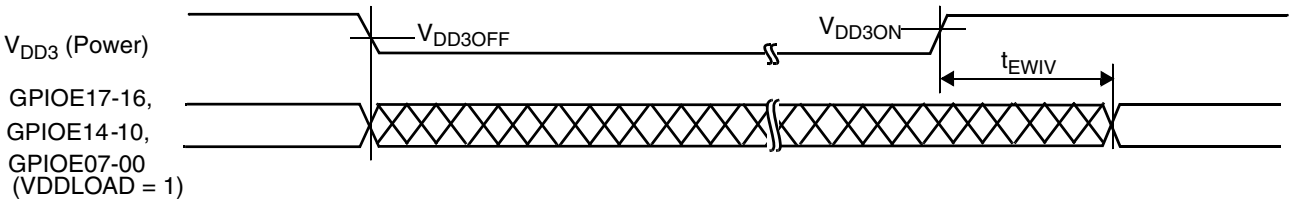


Figure 16. Wake-Up Inputs at V_{DD3} Power Switching

2.0 Device Characteristics (Continued)

2.4.11 SMBus Timing

Symbol	Figure	Description	Type of Requirement[1]	Min	Max	Unit
t_{SMBR}	17	Rise time (HMSCL and HMSDA)	Input[2]		1000[3]	ns
t_{SMBF}	17	Fall time (HMSCL and HMSDA)	Input		300[3]	ns
			Output[2]		250[4]	ns
t_{SMBCKL}	17	Clock low period (HMSCL)	Input	4.7		µs
t_{SMBCKH}	17	Clock high period (HMSCL)	Input	4		µs
t_{SMBCY}	18	Clock cycle (HMSCL)	Input	10		µs
t_{SMBDS}	18	Data setup time (before clock rising edge)	Input	250		ns
			Output[2]	250		ns
t_{SMBDH}	18	Data hold time (after clock falling edge)	Input	0		ns
			Output[2]	300		ns
t_{SMBPS}	19	Stop condition setup time (clock before data)	Input	4		µs
t_{SMBSH}	19	Start condition hold time (clock after data)	Input	4		µs
t_{SMBBUF}	19	Bus free time between Stop and Start conditions (HMSDA)	Input	4.7		µs
t_{SMBRS}	20	Restart condition setup time (clock before data)	Input	4.7		µs
t_{SMBRH}	20	Restart condition hold time (clock after data)	Input	4		µs
t_{SMBLEX}	-	Cumulative clock low extend time from Start to Stop (HMSCL)	Output		25[3]	ms
t_{SMBTO}	-	Clock low time-out (HMSCL)	Input	25[3,5]		ms
			Output		35[3,6]	ms

1. An “Input” type is a value the PC8374T expects from the system; an “Output” type is a value the PC8374T provides to the system.
2. Test conditions: R_L = 1 KΩ to V_{SB} = 3.3V, C_L = 400 pF to GND.
3. Not tested. Guaranteed by design.
4. Not tested. Guaranteed by characterization.
5. The PC8374T detects a time-out condition if HMSCL is held low for more than t_{SMBTO}.
6. On detection of a time-out condition, the PC8374T resets the SMBus Interface no later than t_{SMBTO}.

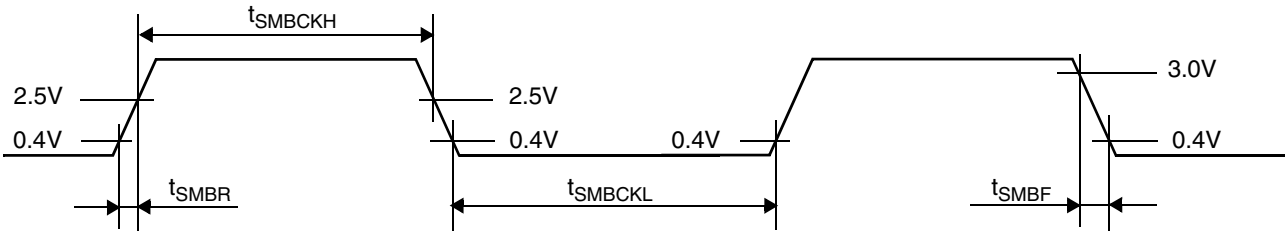


Figure 17. SMBus Signals (HMSCL and HMSDA) Rising Time and Falling Time

2.0 Device Characteristics (Continued)

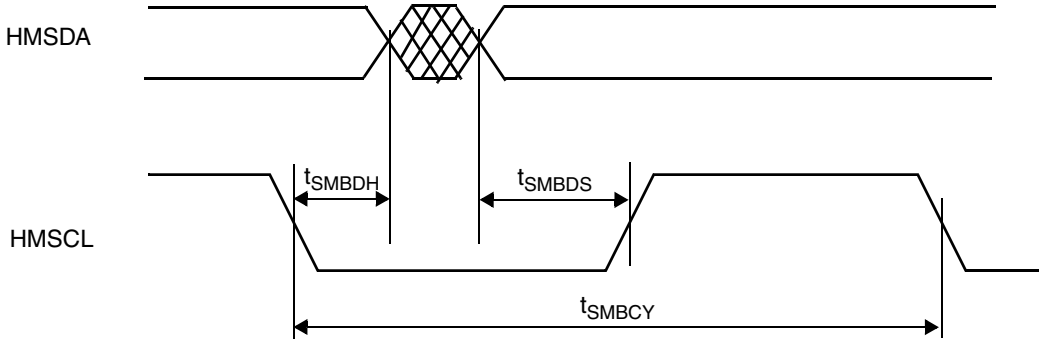


Figure 18. SMBus Data Bit Timing

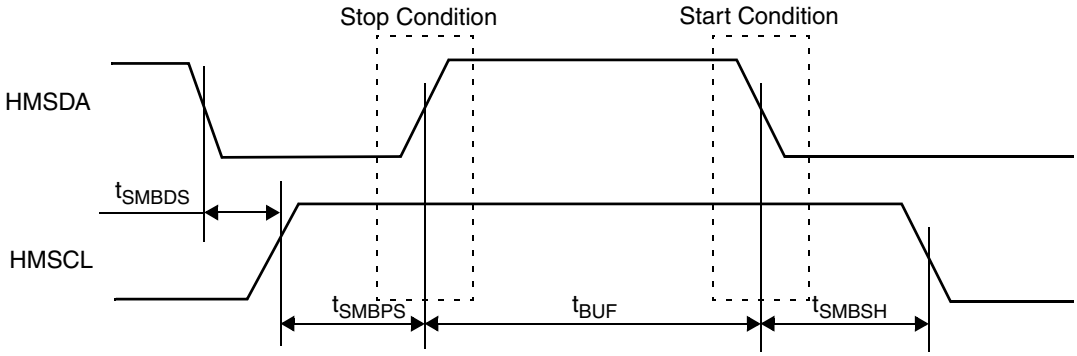


Figure 19. SMBus Start and Stop Condition Timing

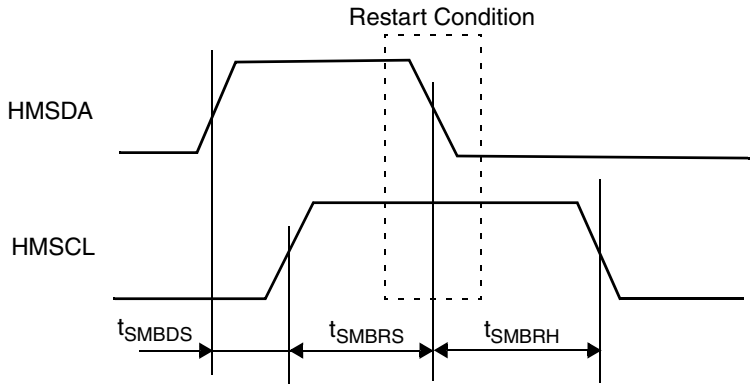


Figure 20. SMBus Restart Condition TIming

2.5 PACKAGE THERMAL INFORMATION

Thermal resistance (degrees C/W) $Theta_{JC}$ and $Theta_{JA}$ values for the PC8374T package are as follows:

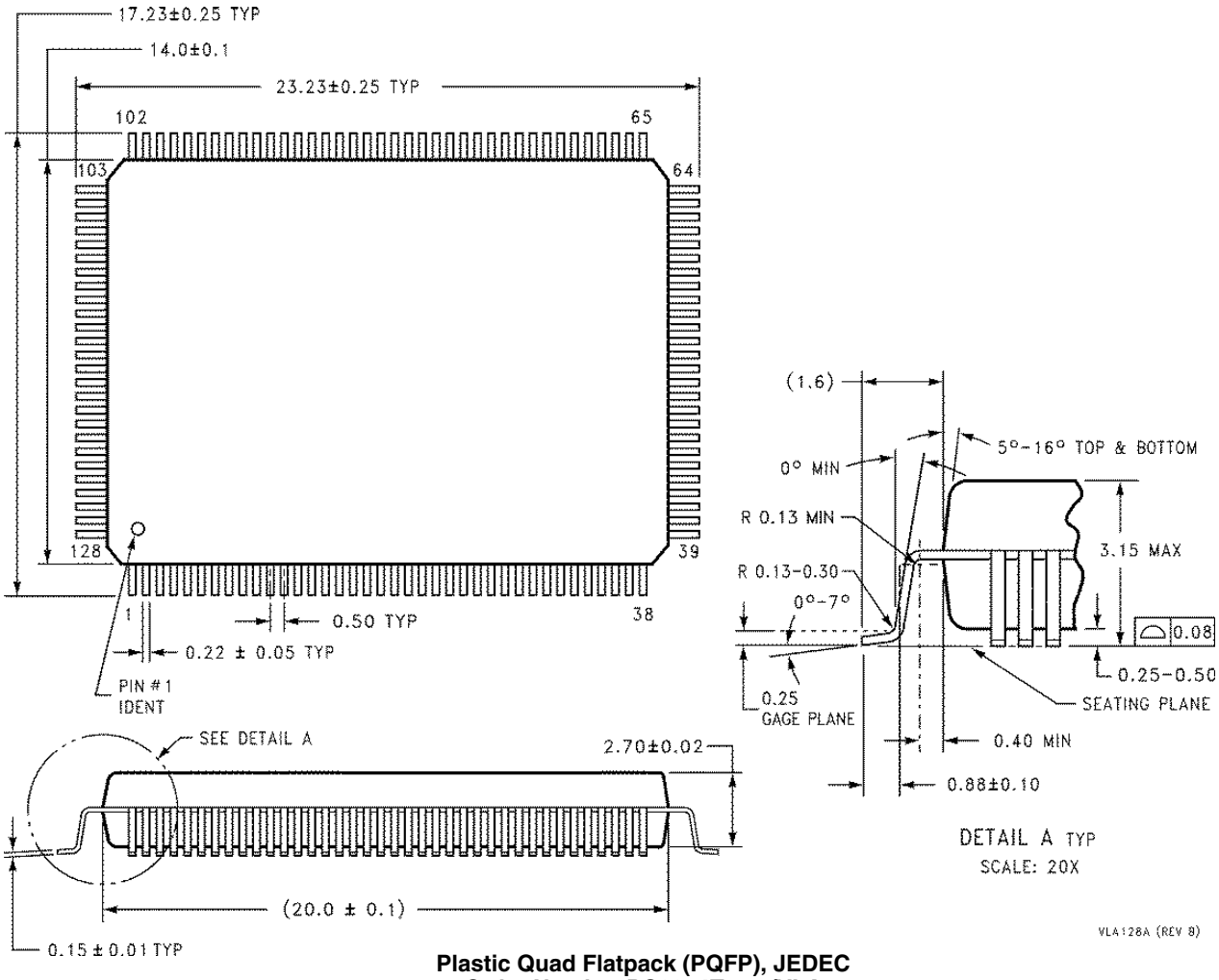
Table 4. Theta (Θ) J Values

Package Type	$Theta_{JA}$@0 lfpm	$Theta_{JA}$@225 lfpm	$Theta_{JA}$@500 lfpm	$Theta_{JA}$@900 lfpm	$Theta_{JC}$
128-PQFP	41.5	33.7	30.1	27.7	16.8

Note: Airflow for $Theta_{JA}$ values is measured in linear feet per minute (lfpm).

Physical Dimensions

All dimensions are in millimeters



Plastic Quad Flatpack (PQFP), JEDEC
Order Number PC8374T-xxx/VLA
NS Package Number VLA128A

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