National Semiconductor

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Revision 1.1

PC87373
LPC SuperI/O with Glue Functions

General Description

The National Semiconductor® PC87373 Advanced I/O product is a member of the PC8737x SuperI/O family. All PC8737x devices are highly integrated and are pin and software compatible, thus providing drop-in interchangeability and enabling a variety of assembly options using only a single motherboard and BIOS.

PC87373 integration allows for a smaller system board size and saves on total system cost.

The PC87373 includes legacy SuperI/O functions, system glue functions, fan monitoring and control, commonly used functions such as GPIO, and ACPI-compliant Power Management support.

The PC87373 integrates miscellaneous analog and digital system glue functions to reduce the number of discrete components required. The host communicates with the functions integrated in the PC87373 device through an LPC Bus Interface.

The PC87373 Legacy functions are: two serial ports, a fully compliant IEEE 1284 Parallel Port, a Floppy Disk Controller (FDC), a Keyboard/Mouse Controller (KBC), a Game Port and a MIDI Port.

The Fan Speed Control and Monitor (FSCM) module allows the system to monitor and control three fans.

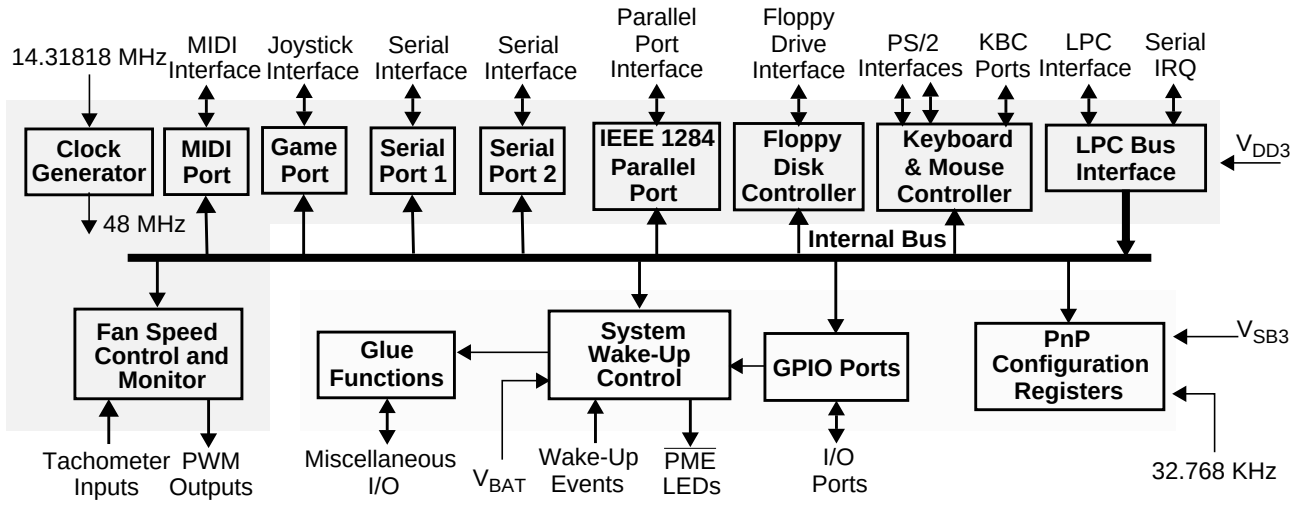
The PC87373 extended wake-up support complements the ACPI controller in the chipset. The System Wake-Up Control (SWC) module, powered by V_{SB3}, supports a flexible wake-up mechanism.

There are 13 General-Purpose Input/Output (GPIO) ports; these allow system control and wake-up on system events.

Outstanding Features

- Legacy modules: Parallel Port, Floppy Disk Controller (FDC), two Serial Ports, Keyboard and Mouse Controller (KBC), Game Port and MIDI Port
- Glue functions to complement the South Bridge functionality
- Fan Speed monitoring and control of three fans
- V_{SB3}-powered Power Management with 20 wake-up sources
- Controls three LED indicators
- 13 GPIO ports with a variety of wake-up options
- LPC interface, based on Intel's *LPC Interface Specification Revision 1.0, September 29th, 1997*
- *PC01 Revision 1.0* and *Advanced Configuration and Power Interface (ACPI) Specification Revision 2.0* compliant
- 128-pin PQFP package

Block Diagram



Device-Specific Information

The following table shows a comparison of features between the PC87372 and the PC87373 devices.

Function		PC87372	PC87373
Keyboard and Mouse Controller (KBC) Floppy Disk Controller (FDC) Parallel Port (PP)		✓	✓
Serial Ports	Serial Port 1 (SP1)	✓	✓
	Serial Port 2 (SP2)		✓
MIDI Port and Game Port			✓
General-Purpose Input/Output Ports (GPIO)		13	13
System Wake-Up Control (SWC)	Basic Functionality	✓	✓
	Last power state indication & Special LED blinking		✓
Fan Speed Control and Monitor (FSCM)	Fan Speed Monitor (Tacho)	2	3
	Fan Speed Control (PWM)		3
Glue Functions		✓	✓

Features

Bus Interface

- LPC Bus Interface
  - Based on Intel's *LPC Interface Specification Revision 1.0, September 29, 1997*
  - Synchronous cycles using up to 33 MHz bus clock
  - 8-bit I/O read and write cycles
  - Up to four 8-bit DMA channels
  - Serial IRQ (SERIRQ)
  - Reset input ($\overline{\text{PCI\_RESET}}$)
  - Optional power-down support ($\overline{\text{LPCPD}}$)
- Configuration Control
  - PnP Configuration Register structure
  - Compliant with *PC01 Specification Revision 1.0, 1999-2000*
  - Base Address strap ($\overline{\text{BADDR}}$) to setup the address of the Index-Data register pair (defaults to 2Eh/2Fh)
  - Flexible resource allocation for all logical devices:
    - Relocatable base address
    - 15 IRQ routing options to serial IRQ
    - Up to four optional 8-bit DMA channels
  - Configurable feature sets:
    - Software selectable
    - V_{SB3}-powered pin multiplexing

Legacy Modules

- Serial Ports 1 and 2
  - Software compatible with the NS16550A and the NS16450
  - Support shadow register for write-only bit monitoring
  - Data rates up to 1.5 Mbaud
- IEEE 1284-compliant Parallel Port
  - ECP, with Level 2 (14 mA sink and source output buffers)
  - Software or hardware control
  - Enhanced Parallel Port (EPP) compatible with EPP 1.7 and EPP 1.9
  - Supports EPP as mode 4 of the Extended Control Register (ECR)
  - Selection of internal pull-up or pull-down resistor for Paper End (PE) pin
  - Supports a demand DMA mode mechanism and a DMA fairness mechanism for improved bus utilization
  - Protection circuit that prevents damage to the parallel port when a printer connected to it is powered up or is operated at high voltages (in both cases, even if the PC87373 is in power-down state)
- Floppy Disk Controller (FDC)
  - Software compatible with the PC8477 (the PC8477 contains a superset of the FDC functions in the µDP8473, NEC µPD765A/B and N82077 devices)
  - Error-free handling of data overrun and underrun
  - Programmable write protect
  - Supports FM and MFM modes
  - Supports Enhanced mode command for three-mode Floppy Disk Drive (FDD)
  - Perpendicular recording drive support for 2.88 MBytes
  - Burst (16-byte FIFO) and Non-Burst modes
  - Full support for IBM Tape Drive Register (TDR) implementation of AT and PS/2 drive types
  - High-performance digital separator
  - Supports fast tape drives (2 Mbps) and standard tape drives (1 Mbps, 500 Kbps and 250 Kbps)
- Keyboard and Mouse Controller (KBC)
  - 8-bit microcontroller, software compatible with 8042AH and PC87911
  - Standard interface (60h, 64h, IRQ1 and IRQ12)
  - Supports two external swapable PS/2 interfaces for keyboard and mouse
  - Programmable, dedicated quasi-bidirectional I/O lines (GA20/P21, $\overline{\text{KBRST}}$/P20)

Features (Continued)

- Musical Instrument Digital Interface (MIDI) Port
  - Compatible with MPU-401 UART mode
  - 16-byte Receive and Transmit FIFOs
  - Loopback mode support
- Game Port (GMP)
  - Compatible with the Legacy Game Port definition
  - Full digital implementation
  - Supports up to two analog joysticks

General-Purpose Modules

- General-Purpose I/O (GPIO) Ports
  - 13 GPIO ports powered by V_{SB3}
  - Each pin individually configured as input or output
  - Programmable features for each output pin:
    - Drive type (open-drain, push-pull or TRI-STATE)
    - TRI-STATE on detection of falling V_{DD3} for V_{SB3}-powered pins driving V_{DD}-supplied devices
  - Programmable option for internal pull-up resistor on each input pin
  - Lock option for the configuration and data of each output pin
  - 12 GPIO ports generate IRQ/$\overline{\text{SIOPME}}$ for wake-up events; each GPIO has separate:
    - Enable control of event status routing to IRQ
    - Enable control of event status routing to $\overline{\text{SIOPME}}$
    - Polarity and edge/level selection
    - Programmable debouncing
- Glue Functions
  - Software selectable alternative functionality, through pin multiplexing
  - Generates the power-related signals:
    - Main Power good
    - Power distribution control (for switching between Main and Standby regulators)
    - Resume reset (Master Reset) according to the 5V standby supply status
    - Main power supply turn on ($\overline{\text{PS\_ON}}$)
    - Rambus SCK clock gating
  - Voltage translation between 3.3V levels (DDC) and 5V levels (VGA) for the SMBus serial clock and data signals
  - Isolation circuitry for the SMBus serial clock and data signals
  - Buffers $\overline{\text{PCI\_RESET}}$ to generate three reset output signals
  - Generates “highest active supply” reference voltage
    - Based on 3.3V and 5V Main supplies
    - Based on 3.3V and 5V Standby supplies
  - High-current LED driver control for Hard Disk Drive activity indication
  - CNR downstream codec, dynamic control
- Fan Speed Control and Monitor (FSCM)
  - Supports tachometers with one or two pulses per revolution
  - Speed monitoring for three fans, including:
    - Digital filtering of the tachometer input signal
    - 16-bit fan speed data
    - Alarm for fan speed slower than programed threshold
    - Alarm for fan stopped
  - Speed control lines with Pulse Width Modulation (PWM) for three fans
    - Output signal in the range of 6 Hz to 93.75 KHz
    - Duty cycle resolution of 1/256

Power Management

- Supports *ACPI Specification Revision 2.0b, July 27, 2000*
- System Wake-Up Control (SWC)
  - Optional routing of events to generate SCI ($\overline{\text{SIOPME}}$) on detection of:
    - Keyboard or Mouse events
    - Ring Indication $\overline{\text{RI}}$ on each of the two serial ports
    - General-Purpose Input Events from the 12 GPIO pins
    - IRQs of the Keyboard and Mouse Controller
    - IRQs of the other internal modules
  - Optional routing of the SCI ($\overline{\text{SIOPME}}$) to generate IRQ (SERIRQ)
  - Implements the GPE1_BLK of the ACPI General Purpose (Generic) Register blocks with “child” events
  - V_{SB3}-powered event detection and event-logic configuration
- Enhanced Power Management (PM), including:
  - Special configuration registers for power down
  - Low-leakage pins
  - Low-power CMOS technology
  - Ability to disable all modules
  - High-current LED drivers control (two LEDs) for power status indication with:
    - Standard blinking, controlled by software
    - Advanced blinking, controlled by power supply status, sleep state or software
    - Special blinking, controlled by power supply status, sleep state and software bit
  - V_{BAT}-powered indication of the Main power supply state before an AC power failure

Features (Continued)

- Keyboard Events
  - Wake-up on any key
  - Supports programmable 8-byte sequence “Password” or “Special Keys” for Power Management
  - Simultaneous recognition of three programmable keys (sequences): “Power”, “Sleep” and “Resume”
  - Wake-up on mouse movement and/or button click

Clocking, Supply, and Package Information

- Clocks
  - LPC (PCI) clock input (up to 33 MHz)
  - Low-frequency 32.768 KHz clock input, active also in S3-S5 (when V_{DD3} is off), for:
    - System Wake-Up Control (SWC) wake-up timing
    - LED blink timing
    - Glue Functions timing
  - On-chip Clock Generator:
    - Generates 48 MHz for the SuperI/O modules and FSCM
    - Based on the 14.31818 MHz clock input
    - V_{DD3} powered
- Protection
  - All device pins are 5V tolerant and back-drive protected (except LPC bus pins
  - High ESD protection of all the device pins
  - Pin multiplexing selection lock
  - Configuration register lock
- Testability
  - XOR tree structure
    - Includes all the device pins (except the supply and the analog pins)
    - Selected at power-up by strap input ($\overline{TEST}$)
  - TRI-STATE device pins, selected at power-up by strap input ($\overline{TRIS}$)
- Power Supply
  - 3.3V supply operation
  - Separate pin pairs for main (V_{DD3}) and standby (V_{SB3}) power supplies
  - Backup battery input (V_{BAT}) for SWC indications
  - Low standby power consumption
  - Very low power consumption from backup battery (less than 0.5 μA)
- Package
  - 128-pin PQFP

Datasheet Revision Record

Revision Date	Status	Comments
August 2002	Preliminary Datasheet	First issue - Revision 1.0
October 2002	Preliminary Datasheet	Second issue - Revision 1.1

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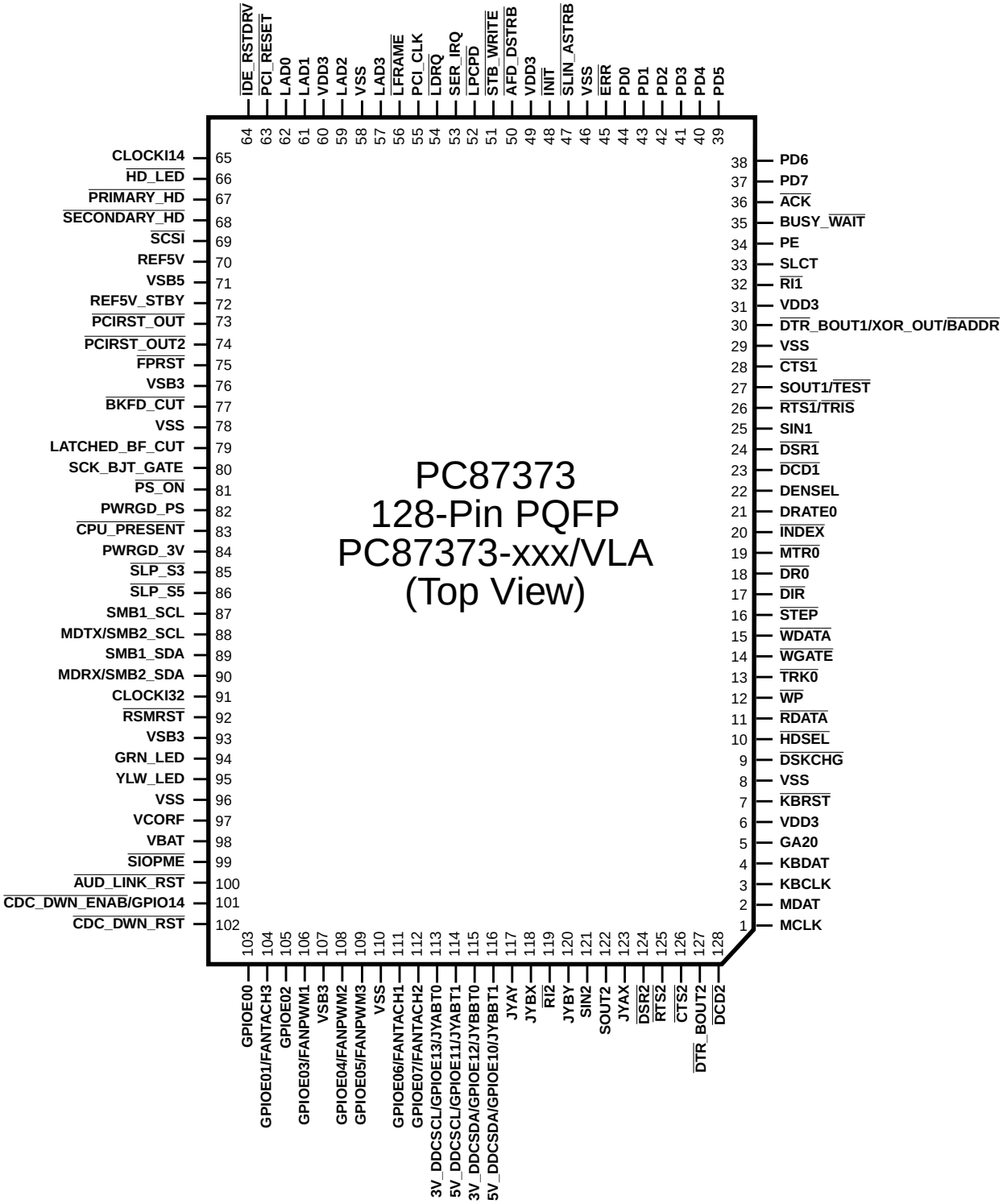
1.0 Signal/Pin Connection and Description

1.1 CONNECTION DIAGRAMS



Plastic Quad Flatpack (PQFP), JEDEC
Order Number PC87373-xxx/VLA
See NS Package Number VLA128A

xxx = Three-character identifier for National data, and keyboard ROM and/or customer identification code

1.0 Signal/Pin Connection and Description (Continued)

1.2 BUFFER TYPES AND SIGNAL/PIN DIRECTORY

The signal DC characteristics of the pins described in Section 1.4 on page 16 are denoted by buffer type symbols, which are defined in Table 1 and described in further detail in Section 13.2 on page 153. The pin multiplexing information refers to two different types of multiplexing:

- Multiplexed, denoted by a slash (/) between pins in the diagrams in Section 1.1. Pins are shared between two different functions. Each function is associated with different board connectivity. Normally, the function selection is determined by the board design and cannot be changed dynamically. The multiplexing options must be configured by the BIOS on power-up in order to comply with the board implementation.
- Multiple Mode, denoted by an underscore (_) between pins in the diagrams in Section 1.1. Pins have two or more modes of operation within the same function. These modes are associated with the same external (board) connectivity. Mode selection may be controlled by the device driver through the registers of the functional block and do not require a special BIOS setup on power-up. These pins are not considered multiplexed pins from the PC87373 configuration perspective. The mode selection method (registers and bits), as well as the signal specification in each mode, are described within the functional description of the relevant functional block.

Table 1. Buffer Types

Symbol	Description
IN_{GP}	Input, Game Port compatible, with Schmitt Trigger
IN_{T}	Input, TTL compatible
IN_{TS}	Input, TTL compatible, with Schmitt Trigger
IN_{TS4}	Input, TTL compatible, with 400 mV Schmitt Trigger
IN_{PCI}	Input, PCI 3.3V compatible
IN_{ULR}	Input, power, resistor protected (not characterized)
AI	Input, analog (0-5.5V tolerant)
$O_{p/n}$	Output, TTL/CMOS compatible, push-pull buffer capable of sourcing *p* mA and sinking *n* mA
OD_{n}	Output, TTL/CMOS compatible, open-drain buffer capable of sinking *n* mA
O_{PCI}	Output, PCI 3.3V compatible,
AO	Output, analog (0-5.5V tolerant)
SW_{SM}	Input/Output switch, SMBus compatible
PWR	Power pin
GND	Ground pin

1.0 Signal/Pin Connection and Description (Continued)

1.3 PIN MULTIPLEXING

Table 2 shows only multiplexed pins, their associated functional blocks and the configuration bits for the selection of the multiplexed options used in the PC87373.

Table 2. Pin Multiplexing Configuration

Pin	Default Signal	Function Block	Alternate Signal	Function Block	Alternate Signal	Function Block	Configuration Select	Strap or Wake-Up	Function Block
30	$\overline{\text{DTR\_BOUT1}}$	Serial Port 1	XOR_OUT	Config			$\overline{\text{TEST}}$ (strap)	$\overline{\text{BADDR}}$	Config (Straps)
26	$\overline{\text{RTS1}}$							$\overline{\text{TRIS}}$	
27	SOUT1							$\overline{\text{TEST}}$	
32	$\overline{\text{RI1}}$							$\overline{\text{RI1}}$	SWC
119	$\overline{\text{RI2}}$	Serial Port 2						$\overline{\text{RI2}}$	
3	KBCLK	KBC						KBCLK	
4	KBDAT							KBDAT	
1	MCLK							MCLK	
2	MDAT							MDAT	
103	GPIOE00	GPIO						GPIOE00	
104	GPIOE01		FANTACH3	FSCM			SIOCF2.TACH3EN	GPIOE01	
105	GPIOE02							GPIOE02	
106	GPIOE03		FANPWM1	FSCM			SIOCF3.PWM1EN	GPIOE03	
108	GPIOE04		FANPWM2	FSCM			SIOCF3.PWM2EN	GPIOE04	
109	GPIOE05		FANPWM2	FSCM			SIOCF3.PWM2EN	GPIOE05	
111	GPIOE06		FANTACH1	FSCM			SIOCF2.TACH1EN	GPIOE06	
112	GPIOE07		FANTACH2				SIOCF2.TACH2EN	GPIOE07	
116	5V_DDCSDA	Glue Functions	GPIOE10	GPIO	JYBBT1	Game Port	SIOCF2.GPIO03EN, SIOCF3.GMPEN	GPIOE10	
114	5V_DDCSCL		GPIOE11		JYABT1			GPIOE11	
115	3V_DDCSDA		GPIOE12		JYBBT0			GPIOE12	
113	3V_DDCSCL		GPIOE13		JYABT0			GPIOE13	
101	$\overline{\text{CDC\_DWN\_ENAB}}$		GPIO14				Note[1]		
88	SMB2_SCL	Glue Functions	MDTX	MIDI			SIOCF4.MIDIEN		
90	SMB2_SDA		MDRX						

1. Both $\overline{\text{CDC\_DWN\_ENAB}}$ and GPIO14 are simultaneously available at the device pin.

1.0 Signal/Pin Connection and Description (Continued)

1.4 DETAILED SIGNAL/PIN DESCRIPTIONS

This section describes all signals of the PC87373 device. The signals are organized by functional group.

1.4.1 LPC Interface

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
LAD3-0	57,59 61,62	I/O	IN_{PCI}/O_{PCI}	V_{DD3}	**LPC Address-Data.** Multiplexed command, address bi-directional data and cycle status.
PCI_CLK	55	I	IN_{PCI}	V_{DD3}	**LPC Clock.** PCI clock used for the LPC bus (up to 33 MHz).
$\overline{\text{LFRAME}}$	56	I	IN_{PCI}	V_{DD3}	**LPC Frame.** Low pulse indicates the beginning of a new LPC cycle or termination of a broken cycle.
$\overline{\text{LDRQ}}$	54	O	O_{PCI}	V_{DD3}	**LPC DMA Request.** Encoded DMA request for LPC interface.
$\overline{\text{PCI\_RESET}}$	63	I	IN_{PCI}	V_{DD3}	**LPC Reset.** PCI system reset used for the LPC bus (Hardware Reset).
SER_IRQ	53	I/O	IN_{PCI}/O_{PCI}	V_{DD3}	**Serial IRQ.** The interrupt requests are serialized over a single pin, where each IRQ level is delivered during a designated time slot.
$\overline{\text{LPCPD}}$	52	I	IN_{PCI}	V_{DD3}	**Power Down.** Indicates that power to the LPC interface is about to be turned off. When $\overline{\text{LPCPD}}$ functionality is not required, an internal pull-up resistor allows this pin to be left floating.
$\overline{\text{PCIRST\_OUT}}$	73	O	$O_{14/14}$	V_{SB3}	**PCI Reset Output.** PCI system reset. $\overline{\text{PCIRST\_OUT}}$ is a buffered copy of $\overline{\text{PCI\_RESET}}$ when V_{DD3} is on, and it is held at low level when V_{DD3} is off.
$\overline{\text{PCIRST\_OUT2}}$	74	O	$O_{14/14}$	V_{SB3}	**PCI Reset Output 2.** PCI system reset (same behavior as $\overline{\text{PCIRST\_OUT}}$ above).
$\overline{\text{IDE\_RSTDRV}}$	64	O	OD_6	V_{DD3}	**IDE Reset Output.** IDE drive reset. $\overline{\text{IDE\_RSTDRV}}$ is a buffered copy of $\overline{\text{PCI\_RESET}}$ when V_{DD3} is on, and it is floating when V_{DD3} is off.

1.0 Signal/Pin Connection and Description (Continued)

1.4.2 Serial Port 1 and Serial Port 2 (UART1 and UART2)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
$\overline{CTS1}$ $\overline{CTS2}$	28 126	I	IN_{TS}	V_{DD3}	**Clear to Send.** When low, indicates that the modem or other data transfer device is ready to exchange data.
$\overline{DCD1}$ $\overline{DCD2}$	23 128	I	IN_{TS}	V_{DD3}	**Data Carrier Detected.** When low, indicates that the modem or other data transfer device has detected the data carrier.
$\overline{DSR1}$ $\overline{DSR2}$	24 124	I	IN_{TS}	V_{DD3}	**Data Set Ready.** When low, indicates that the data transfer device, e.g., modem, is ready to establish a communications link.
$\overline{DTR}$_BOUT1 $\overline{DTR}$_BOUT2	30 127	O	$O_{4/8}$	V_{DD3}	**Data Terminal Ready.** When low, indicates to the modem or other data transfer device that the UART is ready to establish a communications link. After a system reset, these pins provide the $\overline{DTR}$ function and set these signals to inactive high. Loopback operation holds them inactive. **Baud Output.** Provides the associated serial channel baud rate generator output signal if test mode is selected, i.e., bit 7 of EXCR1 register is set.
$\overline{RI1}$ $\overline{RI2}$	32 119	I	IN_{TS}	V_{DD3}	**Ring Indicator.** When low, indicates that a telephone ring signal was received by the modem. These pins are monitored during V_{DD} power-off for wake-up event detection.
$\overline{RTS1}$ $\overline{RTS2}$	26 125	O	$O_{4/8}$	V_{DD3}	**Request to Send.** When low, indicates to the modem or other data transfer device that the corresponding UART is ready to exchange data. A system reset sets these signals to inactive high, and loopback operation holds them inactive.
SIN1 SIN2	25 121	I	IN_{TS}	V_{DD3}	**Serial Input.** Receives composite serial data from the communications link (peripheral device, modem or other data transfer device).
SOUT	27	O	$O_{4/8}$	V_{DD3}	**Serial Output.** Sends composite serial data to the communications link (peripheral device, modem or other data transfer device). These signals are set active high after a system reset.
SOUT2	122		$O_{6/12}$		

1.0 Signal/Pin Connection and Description (Continued)

1.4.3 Parallel Port

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
$\overline{ACK}$	36	I	IN_T	V_{DD3}	**Acknowledge.** Pulsed low by the printer to indicate that it has received data from the parallel port.
$\overline{AFD}$_DSTRB	50	O	OD_{14}, $O_{14/14}$	V_{DD3}	**$\overline{AFD}$ - Automatic Feed.** When low, instructs the printer to automatically feed a line after printing each line. This pin is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor must be connected to this pin. **$\overline{DSTRB}$ - Data Strobe (EPP).** Active low; used in EPP mode to denote a data cycle. When the cycle is aborted, $\overline{DSTRB}$ becomes inactive (high).
BUSY_$\overline{WAIT}$	35	I	IN_T	V_{DD3}	**Busy.** Set high by the printer when it cannot accept another character. **Wait.** In EPP mode, the parallel port device uses this active low signal to extend its access cycle.
$\overline{ERR}$	45	I	IN_T	V_{DD3}	**Error.** Set active low by the printer when it detects an error.
$\overline{INIT}$	48	O	OD_{14}, $O_{14/14}$	V_{DD3}	**Initialize.** When low, initializes the printer. This signal is in TRI-STATE after a 1 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor must be connected to this pin.
PD7-0	37-44	I/O	$IN_T/O_{14/14}$	V_{DD3}	**Parallel Port Data.** Transfers data to and from the peripheral data bus and the appropriate parallel port data register. These signals have a high current drive capability.
PE	34	I	IN_T	V_{DD3}	**Paper End.** Set high by the printer when it is out of paper. This pin has an internal weak pull-up or pull-down resistor.
SLCT	33	I	IN_T	V_{DD3}	**Select.** Set active high by the printer when the printer is selected.
$\overline{SLIN}$_ASTRB	47	O	OD_{14}, $O_{14/14}$	V_{DD3}	**$\overline{SLIN}$ - Select Input.** When low, selects the printer. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor must be connected to this pin. **$\overline{ASTRB}$ - Address Strobe (EPP).** Active low, used in EPP mode to denote an address or data cycle. When the cycle is aborted, $\overline{ASTRB}$ becomes inactive (high).
$\overline{STB}$_WRITE	51	O	OD_{14}, $O_{14/14}$	V_{DD3}	**$\overline{STB}$ - Data Strobe.** When low, Indicates to the printer that valid data is available at the printer port. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor must be connected to this pin. **$\overline{WRITE}$ - Write Strobe.** Active low, used in EPP mode to denote an address or data cycle. When the cycle is aborted, $\overline{WRITE}$ becomes inactive (high).

1.0 Signal/Pin Connection and Description (Continued)

1.4.4 Floppy Disk Controller (FDC)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
DENSEL	22	O	OD_{12} $O_{6/12}$	V_{DD3}	**Density Select.** Indicates that a high FDC density data rate (500 Kbps, 1 Mbps or 2 Mbps) or a low density data rate (250 or 300 Kbps) is selected.
$\overline{DIR}$	17	O	OD_{12} $O_{6/12}$	V_{DD3}	**Direction.** Determines the direction of the Floppy Disk Drive (FDD) head movement (active = step in; inactive = step out) during a seek operation.
$\overline{DR0}$	18	O	OD_{12} $O_{6/12}$	V_{DD3}	**Drive Select.** Active low signal controlled by bit 0 of the Digital Output Register (DOR).
DRATE0	21	O	OD_{12} $O_{6/12}$	V_{DD3}	**Data Rate.** Reflects the value of bit 0 of either Configuration Control Register (CCR) or Data Rate Select Register (DSR), whichever was written to last.
$\overline{DSKCHG}$	9	I	IN_{TS}	V_{DD3}	**Disk Change.** Indicates that the drive door was opened.
$\overline{HDSEL}$	10	O	OD_{12} $O_{6/12}$	V_{DD3}	**Head Select.** Selects which side of the FDD is accessed. Active (low) selects side 1; inactive selects side 0.
$\overline{INDEX}$	20	I	IN_{TS}	V_{DD3}	**Index.** Indicates the beginning of an FDD track.
$\overline{MTR0}$	19	O	OD_{12} $O_{6/12}$	V_{DD3}	**Motor Select.** Active low motor enable signal for drive 0, controlled by bit D4 of the Digital Output Register (DOR).
$\overline{RDATA}$	11	I	IN_{TS}	V_{DD3}	**Read Data.** Raw serial input data stream read from the FDD.
$\overline{STEP}$	16	O	OD_{12} $O_{6/12}$	V_{DD3}	**Step.** Issues pulses to the disk drive at a software programmable rate to move the head during a seek operation.
$\overline{TRK0}$	13	I	IN_{TS}	V_{DD3}	**Track 0.** Indicates to the controller that the head of the selected floppy disk drive is at track 0.
$\overline{WDATA}$	15	O	OD_{12} $O_{6/12}$	V_{DD3}	**Write Data.** Carries out the pre-compensated serial data that is written to the FDD. Pre-compensation is software selectable.
$\overline{WGATE}$	14	O	OD_{12} $O_{6/12}$	V_{DD3}	**Write Gate.** Enables the write circuitry of the selected FDD. $\overline{WGATE}$ is designed to prevent glitches during power-up and power-down. This prevents writing to the disk when power is cycled.
$\overline{WP}$	12	I	IN_{TS}	V_{DD3}	**Write Protected.** Indicates that the disk in the selected drive is write protected.

1.0 Signal/Pin Connection and Description (Continued)

1.4.5 Keyboard and Mouse Controller (KBC)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
KBCLK	3	I/O	IN_{TS}/OD_{14}	V_{DD3}	**Keyboard Clock.** Keyboard clock signal. External pull-up resistor is required for PS/2 compliance. This pin is monitored during V_{DD3} power-off for wake-up event detection.
KBDAT	4	I/O	IN_{TS}/OD_{14}	V_{DD3}	**Keyboard Data.** Keyboard data signal. External pull-up resistor is required for PS/2 compliance. This pin is monitored during V_{DD3} power-off for wake-up event detection.
MCLK	1	I/O	IN_{TS}/OD_{14}	V_{DD3}	**Mouse Clock.** Mouse clock signal. External pull-up resistor is required for PS/2 compliance. This pin is monitored during V_{DD3} power-off for wake-up event detection.
MDAT	2	I/O	IN_{TS}/OD_{14}	V_{DD3}	**Mouse Data.** Mouse data signal. External pull-up resistor is required for PS/2 compliance. This pin is monitored during V_{DD3} power-off for wake-up event detection.
$\overline{KBRST}$	7	I/O	IN_T/OD_8, $O_{4/8}$	V_{DD3}	**KBD Reset.** Keyboard reset (P20) quasi-bidirectional output.
GA20	5	I/O	IN_T/OD_8, $O_{4/8}$	V_{DD3}	**Gate A20.** KBC gate A20 (P21) quasi-bidirectional output.

1.4.6 Game Port (GMP)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
JYAX	123	I/O	IN_{GP}/OD_{12}	V_{DD3}	**Joystick A X-Axis.** Indicates X-axis position of joystick A.
JYAY	117	I/O	IN_{GP}/OD_{12}	V_{DD3}	**Joystick A Y-Axis.** Indicates Y-axis position of joystick A.
JYABT0	113	I	IN_{TS}	V_{DD3}	**Joystick A Button 0.** Indicates button 0 status of joystick A.
JYABT1	114	I	IN_{TS}	V_{DD3}	**Joystick A Button 1.** Indicates button 1 status of joystick A.
JYBX	118	I/O	IN_{GP}/OD_{12}	V_{DD3}	**Joystick B X-Axis.** Indicates X-axis position of joystick B.
JYBY	120	I/O	IN_{GP}/OD_{12}	V_{DD3}	**Joystick B Y-Axis.** Indicates Y-axis position of joystick B.
JYBBT0	115	I	IN_{TS}	V_{DD3}	**Joystick B Button 0.** Indicates button 0 status of joystick B.
JYBBT1	116	I	IN_{TS}	V_{DD3}	**Joystick B Button 1.** Indicates button 1 status of joystick B.

1.4.7 Musical Instrument Digital Interface (MIDI) Port

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
MDTX	88	O	$O_{4/8}$	V_{DD3}	**MIDI Transmit.** MIDI serial data output.
MDRX	90	I	IN_{TS}	V_{DD3}	**MIDI Receive.** MIDI serial data input.

1.0 Signal/Pin Connection and Description (Continued)

1.4.8 General-Purpose I/O (GPIO)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
GPIOE00-07 GPIOE10-13	103-106, 108-109, 111-112 116, 114, 115, 113	I/O	IN_{TS}/ OD_8, $O_{4/8}$	V_{SB3}	**General-Purpose I/O Ports.** Each pin is configured independently as input or I/O, with or without static pull-up and with either open-drain or push-pull output type. These pins have event detection capability to generate a wake-up event or an interrupt.
GPIO14	101	I/O	IN_{TS}/ OD_{12}, $O_{6/12}$		**General-Purpose I/O Port.** This pin is configured independently as input or I/O with or without static pull-up and with either open-drain or push-pull output type.

1.4.9 Fan Speed Control and Monitor (FSCM)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
FANTACH1 FANTACH2 FANTACH3	111, 112, 104	I	IN_{TS}	V_{DD3}	**Fan Tachometer Inputs.** Input to the Fan Speed Monitor for the fan tachometer pulse. The rising edge indicates the completion of either a half or full fan revolution.
FANPWM1 FANPWM2 FANPWM3	106, 108, 109	O	$O_{4/8}$	V_{DD3}	**Fan Control Outputs.** Pulse Width Modulation (PWM) signals, used to control the speed of cooling fans by controlling the On/Off duty cycle, and thus the voltage supplied to the fan motor.

1.0 Signal/Pin Connection and Description (Continued)

1.4.10 System Wake-Up Control (SWC)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
GPIOE00-07, GPIOE10-13	103-106, 108-109, 111-116	I	IN_{TS}	V_{SB3}	**Wake-Up Inputs.** Generates a wake-up event. These pins have programmable debouncing. When GPIOE functionality of a pin is not required, the internal pull-up resistor must be enabled to allow the pin to be left floating.
$\overline{RI1}$ $\overline{RI2}$	32, 119	I	IN_{TS}	V_{SB3}	**Ring Indicator Wake-Up.** When low, generates a wake-up event, indicating that a telephone ring signal was received by the modem.
KBCLK	3	I	IN_{TS}	V_{SB3}	**Keyboard Clock Wake-Up.** Generates a wake-up event, when a specific keyboard sequence is detected.
KBDAT	4	I	IN_{TS}	V_{SB3}	**Keyboard Data Wake-Up.** Generates a wake-up event, when a specific keyboard sequence is detected.
MCLK	1	I	IN_{TS}	V_{SB3}	**Mouse Clock Wake-Up.** Generates a wake-up event, when a specific mouse action is detected.
MDAT	2	I	IN_{TS}	V_{SB3}	**Mouse Data Wake-Up.** Generates a wake-up event, when a specific mouse action is detected.
$\overline{SIOPME}$	99	O	OD_8, $O_{4/8}$	V_{SB3}	**Power Management Event (SCI).** Active level indicates that a wake-up event occurred, causing the system to exit its current sleep state. This signal has programmable polarity (default is active low).
$\overline{SLP\_S3}$, $\overline{SLP\_S5}$	85 86	I	IN_{TS4}	V_{SB3}	**Sleep States 3 to 5.** Active (low) level indicates the system is in one of the sleep states S3 or S5. These signals are generated by an external ACPI controller. **Pins** **$\overline{SLPS3}$ $\overline{SLPS5}$ Functionality** 1 1: Working state (S0) or Sleep states S1 or S2 0 1: Sleep state S3 0 0: Sleep state S5 1 0: Illegal combination
YLW_LED, GRN_LED	95, 94	O	OD_{24}	V_{SB3}	**Power LEDs.** Yellow and green LED drivers. Each indicates the Main power status or blinks under software control.

1.4.11 Clocks

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
CLOCKI32	91	I	IN_{TS}	V_{SB3}	**Low-Frequency Clock Input.** 32.768 KHz clock for the SWC and Glue Functions timing.
CLOCKI14	65	I	IN_{TS}	V_{DD3}	**High-Frequency Clock Input.** 14.31818 MHz clock for the on-chip, 48 MHz Clock Generator (for the Legacy modules and FSCM).

1.0 Signal/Pin Connection and Description (Continued)

1.4.12 Glue Functions

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
REF5V	70	O	AO	V_{SB3}	**Main Highest Active Supply, Reference Output.** Reference voltage equal to the highest voltage between V_{DD5} and V_{DD3}. External pull-up resistor to V_{DD5} is required.
REF5V_STBY	72	O	AO	V_{SB3}	**Standby Highest Active Supply, Reference Output.** Reference voltage equal to the highest voltage between V_{SB5} and V_{SB3}. External pull-up resistor to V_{SB5} is required.
$\overline{\text{PS\_ON}}$	81	O	OD_6	V_{SB3}	**Main Power Supply On/Off Control.** Active (low) level turns the main power supply (V_{DD}) on. External pull-up resistor to V_{SB5} is required.
PWRGD_PS	82	I	IN_{TS4}	V_{SB3}	**Power Good Signal from the Power Supply.** Active level indicates the Main power supply voltage is valid.
PWRGD_3V	84	O	$O_{3/6}$	V_{SB3}	**Power Good Output.** Active level indicates the Main supply voltage is valid and the reset button is not pressed.
$\overline{\text{CPU\_PRESENT}}$	83	I	IN_{TS4}	V_{SB3}	**CPU Present.** Active (low) level indicates a processor is currently plugged in.
$\overline{\text{BKFD\_CUT}}$	77	O	OD_6	V_{SB3}	**Backfeed-Cut Control.** Power distribution control (when switching between main and standby regulators) for system transition into and out of the S3 sleep state. External pull-up resistor to V_{DD5} is required.
LATCHED_BF_ CUT	79	O	$O_{14/14}$	V_{SB3}	**Latched Backfeed-Cut.** Power distribution control (when switching between main and standby regulators) for system transition into and out of the S5 sleep state.
$\overline{\text{FPRST}}$	75	I	IN_{TS4}	V_{SB3}	**Front Panel Reset.** Active (low) level indicates that the reset button on the front panel is pressed.
V_{SB5}	71	I	AI	V_{SB3}	**Standby 5V Power Supply.** Used for Resume Reset generation (Range: 0-5.5V, Backdrive protected).
$\overline{\text{RSMRST}}$	92	O	$O_{3/6}$	V_{SB3}	**Resume Reset.** Power-Up reset signal based on the V_{SB5} supply voltage.
SCK_BJT_GATE	80	O	OD_6	V_{SB3}	**Rambus SCK Clock Gate Control.** Gates an external circuit that disables the SCK clock to the Rambus socket when the Main supply voltage is invalid. External pull-up resistor to V_{SB5} is required.
$\overline{\text{PRIMARY\_HD}}$	67	I	IN_{TS4}	V_{DD3}	**Primary Drive.** Active (low) level indicates that the primary IDE drive is active.
$\overline{\text{SECONDARY\_HD}}$	68	I	IN_{TS4}	V_{DD3}	**Secondary Drive.** Active (low) level indicates that the secondary IDE drive is active.
$\overline{\text{SCSI}}$	69	I	IN_{TS4}	V_{DD3}	**SCSI Drive.** Active (low) level indicates that the SCSI drive is active.
$\overline{\text{HD\_LED}}$	66	O	OD_{12}	V_{DD3}	**Hard Drive LED.** Red LED driver. When low, indicates that at least one drive is active.
$\overline{\text{AUD\_LINK\_RST}}$	100	I	IN_T	V_{SB3}	**Audio Link Reset.** Controls the downstream codec.
$\overline{\text{CDC\_DWN\_ENAB}}$	101	I	IN_T	V_{SB3}	**Downstream Codec Enable.** Controls the downstream codec. The GPIO14 signal is also connected to this pin, allowing the software to control both this input and external input pins connected to it.
$\overline{\text{CDC\_DWN\_RST}}$	102	O	$O_{6/12}$	V_{SB3}	**Downstream Codec Reset.** Enables the audio CNR Board.

1.0 Signal/Pin Connection and Description (Continued)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
3V_DDCSCL	113	I/O	SW_{SM}	V_{SB3}	**3.3V Level DDC Serial Clock.** SMBus serial clock signal with 3.3V logic levels for Data Display Channel interface. External pull-up resistor to V_{DD3} is required.
5V_DDCSCL	114	I/O	SW_{SM}	V_{SB3}	**5V Level DDC Serial Clock.** SMBus serial clock signal with 5V logic levels for VGA monitor interface. External pull-up resistor to V_{DD5} is required.
3V_DDCSDA	115	I/O	SW_{SM}	V_{SB3}	**3.3V Level DDC Serial Data.** SMBus serial data signal with 3.3V logic levels for Data Display Channel interface. External pull-up resistor to V_{DD3} is required.
5V_DDCSDA	116	I/O	SW_{SM}	V_{SB3}	**5V Level DDC Serial Data.** SMBus serial data signal with 5V logic levels for VGA monitor interface. External pull-up resistor to V_{DD5} is required.
SMB1_SCL	87	I/O	SW_{SM}	V_{SB3}	**Bus 1 Serial Clock.** Serial clock signal of SMBus 1 (3.3V logic levels). External pull-up resistor to the 3.3V supply is required.
SMB2_SCL	88	I/O	SW_{SM}	V_{SB3}	**Bus 2 Serial Clock.** Serial clock signal of SMBus 2 (3.3V logic levels). External pull-up resistor to the 3.3V supply is required.
SMB1_SDA	89	I/O	SW_{SM}	V_{SB3}	**Bus 1 Serial Data.** Serial data signal of SMBus 1 (3.3V logic levels). External pull-up resistor to the 3.3V supply is required.
SMB2_SDA	90	I/O	SW_{SM}	V_{SB3}	**Bus 2 Serial Data.** Serial data signal of SMBus 2 (3.3V logic levels). External pull-up resistor to the 3.3V supply is required.

1.4.13 Configuration Straps and Testing

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
$\overline{BADDR}$	30	I	IN_{TS}	V_{DD3}	**Base Address.** Sampled at V_{DD} Power-Up reset to determine the base address of the configuration Index-Data register pair, as follows: – No pull-down resistor (default) - 2Eh-2Fh – 10 KΩ[1] external pull-down resistor - 4Eh-4Fh The external pull-down resistor must be connected to V_{SS}.
$\overline{TRIS}$	26	I	IN_{TS}	V_{DD3}	**TRI-STATE Device.** Sampled at V_{DD} Power-Up reset to force the device to float all its output and I/O pins. No pull-down resistor (default) - normal pin operation – 10 KΩ[1] external pull-down resistor - floating device pins – The external pull-down resistor must be connected to V_{SS}. When $\overline{TRIS}$ is set to 0 (by an external pull-down resistor), $\overline{TEST}$ must be 1 (left unconnected).
$\overline{TEST}$	27	I	IN_{TS}	V_{DD3}	**XOR Tree Test Mode.** Sampled at V_{DD} Power-Up reset to force the device pins into a XOR tree configuration. – No pull-down resistor (default) - normal device operation – 10 KΩ[1] external pull-down resistor - pins configured as XOR tree. The external pull-down resistor must be connected to V_{SS}. When $\overline{TEST}$ is set to 0 (by an external pull-down resistor), $\overline{TRIS}$ must be 1 (left unconnected).

1.0 Signal/Pin Connection and Description (Continued)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
XOR_OUT	30	O	$O_{4/8}$	V_{DD3}	**XOR Tree Output.** All the device pins (except power type and analog type pins) are internally connected in a XOR tree structure.

1. Because the strap function is multiplexed with the Serial Port pins, a CMOS transceiver device is recommended for Serial Port functionality; in this case, the value of the external pull-down resistor is 10 KΩ. If, however, a TTL transceiver device is used, the value of the external pull-down resistor must be 470Ω, and since the Serial Port pins are not able to drive this load, the external pull-down resistor must be disconnected t_{EPLV} after V_{DD3} power-up (see "VDD Power-Up Reset" on page 160).

1.4.14 Power and Ground

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
V_{SS}	8, 29, 46, 58, 78, 96, 110	I	GND		**Ground.** Ground connection for both core logic and I/O buffers, for the Main and Standby power supplies.
V_{DD3}	6, 31, 49, 60	I	PWR		**Main 3.3V Power Supply.** Powers the I/O buffers of the legacy peripherals and the LPC interface.
V_{SB3}	76, 93, 107	I	PWR		**Standby 3.3V Power Supply.** Powers the I/O buffers of the GPIO ports, SWC, Glue Functions and the on-chip Core power converter.
V_{CORF}	97	I/O	PWR		**On-chip Core Power Converter Filter.** On-chip Core power converter output. Powers the core logic of all the device modules. An external 1 µF ceramic filter capacitor must be connected between this pin and V_{SS}.
V_{BAT}	98	I	IN_{ULR}		**Battery Power Supply.** When V_{SB3} is off, this supply provides battery back-up to some of the SWC registers. When the functions powered by V_{BAT} are not used, the V_{BAT} pin must be connected to V_{SS} through an external 10 KΩ pull-down resistor. The pin is connected to the internal logic through a series resistor for UL-compliant protection.

1.5 INTERNAL PULL-UP AND PULL-DOWN RESISTORS

The signals listed in Table 3 have internal pull-up (PU) and/or pull-down (PD) resistors. The internal resistors are optional for those signals indicated as "Programmable". See Section 13.3 on page 157 for the values of each resistor type.

Table 3. Internal Pull-Up and Pull-Down Resistors

Signal	Pin(s)	Power Well	Type	Comments
LPC Interface				
$\overline{LPCPD}$	52	V_{DD3}	PU_{30}	
Parallel Port				
$\overline{ACK}$	36	V_{DD3}	PU_{220}	
$\overline{AFD\_DSTRB}$	50	V_{DD3}	PU_{440}	
BUSY_$\overline{WAIT}$	35	V_{DD3}	PD_{120}	
$\overline{ERR}$	45	V_{DD3}	PU_{220}	
$\overline{INIT}$	48	V_{DD3}	PU_{440}	
PE	34	V_{DD3}	PU_{220}/ PD_{120}	Programmable

1.0 Signal/Pin Connection and Description (Continued)

Table 3. Internal Pull-Up and Pull-Down Resistors (Continued)

Signal	Pin(s)	Power Well	Type	Comments
SLCT	33	V_{DD3}	PD_{120}	
$\overline{\text{SLIN\_ASTRB}}$	47	V_{DD3}	PU_{440}	
$\overline{\text{STB\_WRITE}}$	51	V_{DD3}	PU_{440}	
Keyboard and Mouse Controller (KBC)				
$\overline{\text{KBRST}}$	7	V_{DD3}	PU_{30}	
GA20	5	V_{DD3}	PU_{30}	
System Wake-Up Control (SWC)				
$\overline{\text{SIOPME}}$	99	V_{SB3}	PU_{30}	Programmable[1]
Game Port (GMP)				
JYABT0	113	V_{DD3}	PU_{30}	Programmable[2]
JYABT1	114	V_{DD3}	PU_{30}	Programmable[2]
JYBBT0	115	V_{DD3}	PU_{30}	Programmable[2]
JYBBT1	116	V_{DD3}	PU_{30}	Programmable[2]
Musical Instrument Digital Interface (MIDI) Port				
MDRX	90	V_{DD3}	PU_{30}	Programmable[2]
General-Purpose Input/Output (GPIO) Ports				
GPIOE00-07	106-103, 108, 109, 111, 112	V_{SB3}	PU_{30}	Programmable[2]
GPIOE10-13	116, 114, 115, 113	V_{SB3}	PU_{30}	Programmable[2]
GPIO14	101	V_{SB3}	PU_{30}	Programmable[2]
Glue Functions				
PWRGD_PS	82	V_{SB3}	PU_{90}	
$\overline{\text{CPU\_PRESENT}}$	83	V_{SB3}	PU_{90}	
$\overline{\text{FPRST}}$	75	V_{SB3}	PU_{90}	
$\overline{\text{PRIMARY\_HD}}$	67	V_{DD3}	PU_{90}	
$\overline{\text{SECONDARY\_HD}}$	68	V_{DD3}	PU_{90}	
$\overline{\text{SCSI}}$	69	V_{DD3}	PU_{90}	
Strap Configuration				
$\overline{\text{BADDR}}$	30	V_{DD3}	PU_{30}	Strap[3]
$\overline{\text{TRIS}}$	26	V_{DD3}	PU_{30}	Strap[3]
$\overline{\text{TEST}}$	27	V_{DD3}	PU_{30}	Strap[3]

1. Enabled only when the OD_6 buffer type is selected (OD_6 is the default at reset).
2. Default at reset: disabled.
3. Active only during V_{DD} Power-Up reset.

2.0 Power, Reset and Clocks

2.1 POWER

2.1.1 Power Planes

The PC87373 device has four power planes (wells), as shown in the table below:

Table 4. Power Planes

Power Plane	Description	Power Pins	Ground Pins
Main	Powers the I/O buffers for the external signals[1] of the Legacy modules (Serial Ports, Parallel Port, FDC, KBC, MIDI Port, Game Port), on-chip High-Frequency Clock Generator, FSCM and the LPC interface, including the buffered reset outputs	V_{DD3}	V_{SS}
Standby	Powers the I/O buffers for the external signals[1] of the GPIO ports, SWC, Glue Functions and the on-chip Core power converter	V_{SB3}	V_{SS}
Core	Powers the internal (core) logic of all the device modules	V_{CORF}[2]	V_{SS}
Backup	Powers some of the SWC functions	V_{BAT}	V_{SS}

1. See the tables in Section 1.4 (pages 16–25), specifically the *Power Well* column.
2. V_{CORF} is generated from V_{SB3} by an on-chip power converter.

For correct operation, V_{SB3} must be applied before V_{DD3}.

The battery backup voltage (V_{BAT}) powers some of the SWC functions even when the V_{SB3} voltage is absent due to either power failure or disconnection of the external AC input power. When the functions powered by V_{BAT} are not used, the V_{BAT} pin must be connected to V_{SS} through an external pull-down resistor.

To meet the UL standard requirements, a series resistor (R_{UL}) is implemented.

2.1.2 Power States

The PC87373 device has four power states:

- **Battery Fail** - Backup power plane is powered off (V_{BAT} is inactive). This power state applies only to the SWC functions powered by V_{BAT}.
- **Power Fail** - Main, Standby and Core power planes are powered off (V_{DD3}, V_{SB3} and V_{CORF} are inactive).
- **Power Off** - Main power plane is powered off; the Standby and Core power planes are on (V_{DD3} is inactive; V_{SB3} and V_{CORF} are active).
- **Power On** - Main, Standby and Core power planes are powered on (V_{DD3}, V_{SB3} and V_{CORF} are active).

The following power state is illegal:

- The Main power plane is powered on and the Standby and Core power planes are off (i.e., V_{DD3} is active; V_{SB} and V_{CORF} are inactive). Operation is not guaranteed; however, at power-on/off, the device may temporarily enter this power state due to the different rise/fall times of the V_{DD3} and V_{SB3} power supplies.

Table 5 summarizes the power states described above.

2.0 Power, Reset and Clocks (Continued)

Table 5. Power States and Related Power Planes

Power State	Main (V_{DD3})	Standby (V_{SB3})	Core (V_{CORF})[1]	V_{BAT}
Battery Fail[2]	On or Off	On or Off	On or Off	Off
Power Fail	Off	Off	Off	On or Off
Power Off	Off	On	On	On or Off
Power On	On	On	On	On or Off
Illegal[3]	On	Off	Off	On or Off

1. V_{CORF} is generated from V_{SB3}; therefore, both voltages are on or off at approximately the same time.
2. This power state applies only to the SWC functions powered by V_{BAT}.
3. Operation is not guaranteed and register data may be corrupted. However, at power-on/off, the device may temporarily enter this power state due to the different rise/fall times of the V_{DD3} and V_{SB3} power supplies.

Figure 1 shows the power state transitions:

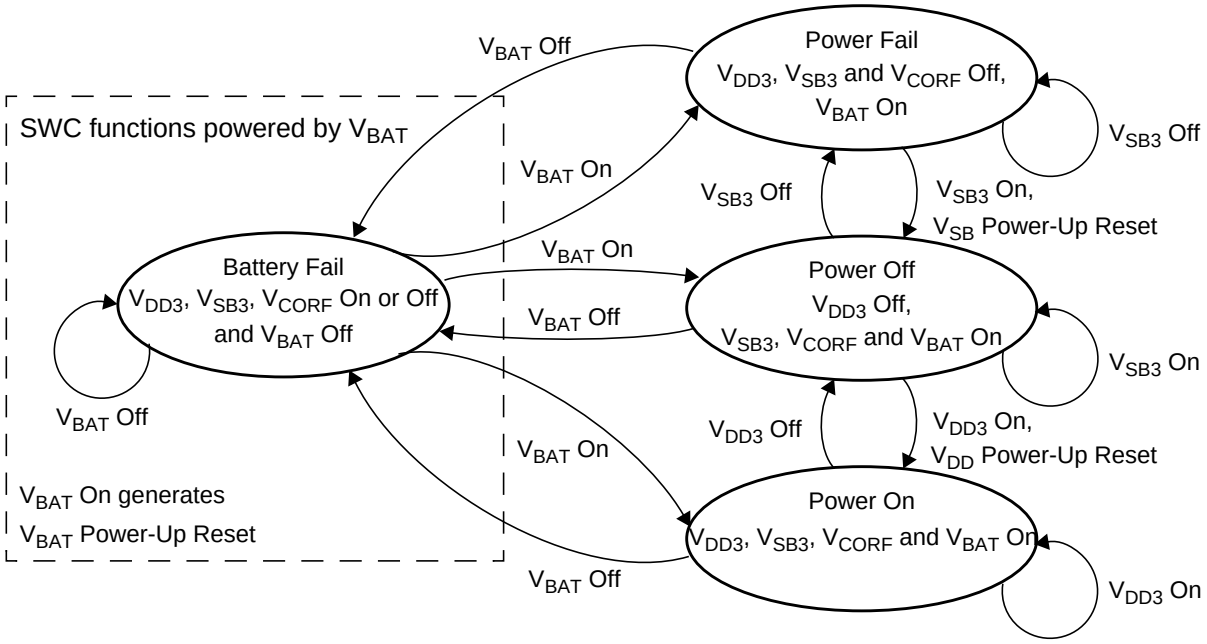


Figure 1. Power State Transitions

2.1.3 Power Connection and Layout Guidelines

The PC87373 requires a power supply voltage of 3.3V ± 10% for both the V_{DD3} and V_{SB3} supplies. The on-chip Core power converter generates a voltage below 3V for the internal logic. The device is designed to operate with a Lithium backup battery supplying up to 3.6V. Therefore, it includes an internal current-limiting resistor on the V_{BAT} input to prevent the battery from shorting, as required by the UL regulations. If the system implementation does not require backup power for the PC87373 device, the V_{BAT} pin must be connected to V_{SS} through an external pull-down resistor.

V_{DD3}, V_{SB3}, V_{CORF} and V_{BAT} use a common ground return marked V_{SS}.

To obtain the best performance, bear in mind the following recommendations.

Ground Connection. The following items must be connected to the ground layer (V_{SS}) as close to the device as possible:

- The ground return (V_{SS}) pins
- The decoupling capacitors of the Main power supply (V_{DD3}) pins
- The decoupling capacitors of the Standby power supply (V_{SB3}) pins

2.0 Power, Reset and Clocks (Continued)

- The decoupling capacitor of the Standby 5V supply (V_{SB5}) pin
- The decoupling capacitor of the on-chip Core power converter (V_{CORF}) pin
- The decoupling capacitor of the Backup battery (V_{BAT}) pin

Note that a low-impedance ground layer also improves noise isolation.

Decoupling Capacitors. The following decoupling capacitors must be used in order to reduce EMI and ground bounce:

- Main power supply (V_{DD3}): Place one capacitor of 0.1 µF on each V_{DD3}-V_{SS} pin pair as close to the pin as possible. In addition, place one 10–47 µF tantalum capacitor on the common net as close to the chip as possible.
- Standby power supply (V_{SB3}): Place one capacitor of 0.1 µF on each V_{SB3}-V_{SS} pin pair as close to the pin as possible. In addition, place one 10–47 µF tantalum capacitor on the common net as close to the chip as possible.
- Standby 5V supply (V_{SB5}): Place one capacitor of 0.1 µF on the V_{SB5}-V_{SS} pin pair as close to the pin as possible.
- On-chip Core power converter (V_{CORF}): Place one 1 µF ceramic capacitor on the V_{CORF}-V_{SS} pin pair as close to the pin as possible.
- Backup battery (V_{BAT}): Place one capacitor of 0.1 µF on the V_{BAT} pin as close to the pin as possible.

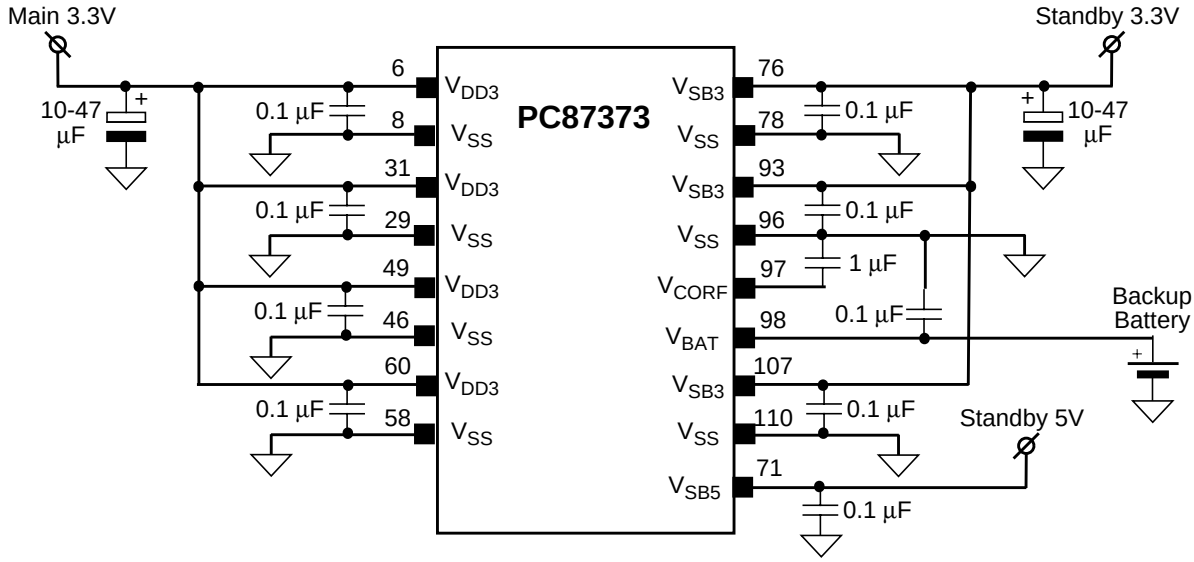


Figure 2. Decoupling Capacitors Connection

2.2 RESET SOURCES AND TYPES

The PC87373 device has five reset sources:

- **V_{BAT} Power-Up Reset** - activated when V_{BAT} is powered up.
- **V_{SB} Power-Up Reset** - activated when V_{SB3} is powered up.
- **V_{DD} Power-Up Reset** - activated when V_{DD3} is powered up.
- **Hardware Reset** - activated when the $\overline{\text{PCI\_RESET}}$ input is asserted (low).
- **Software Reset** - triggered by SWRST bit in SIOCF1 register (see Section 3.7.2 on page 44); SWRST bit is set by the host through the LPC interface.

2.0 Power, Reset and Clocks (Continued)

Unless otherwise noted, reset references throughout the modules of the PC87373 devices default to the following resets:

- For V_{BAT}-retained functions (some SWC): V_{BAT} Power-Up reset (within the limitations described in Section 2.2.1).
- For V_{SB3}-powered functions (GPIO ports, SWC, Glue Functions and some Configuration Control): V_{SB} Power-Up reset (within the limitations described in Section 2.2.2).
- For V_{DD3}-powered functions (Legacy modules, LPC, on-chip Clock Generator, FSCM and some Configuration Control): V_{DD} Power-Up reset, Hardware Reset or Software Reset (within the limitations described in Sections 2.2.3, 2.2.4 and 2.2.5).

The following sections detail the sources and effects of the various PC87373 resets.

2.2.1 V_{BAT} Power-Up Reset

V_{BAT} Power-Up reset is generated by an internal circuit when V_{BAT} power is applied. An active V_{BAT} Power-Up reset signal is generated following a rise in the V_{BAT} until the level of the V_{BAT} power higher than V_{BATLOW} is detected (see Section 13.1.5 on page 152). A V_{BAT} Power-Up reset is generated independently of the state of the other PC87373 power supplies (V_{SB3}, V_{DD3}). When V_{BAT} Power-Up reset is active, it resets the registers whose values are retained by V_{BAT} (some of the SWC).

2.2.2 V_{SB} Power-Up Reset

V_{SB} Power-Up reset is generated by an internal circuit when V_{SB3} power is applied. The V_{SB} Power-Up reset time (t_{IRST}) lasts either 17 cycles of the 32 KHz clock domain or until the PCI_RESET signal is de-asserted, whichever occurs first. External devices must wait at least t_{IRST} before accessing the PC87373 device.

Note that the 32 KHz clock domain starts toggling $t_{32KW} + t_{32KVAL}$ after V_{SB3} power-up. This delay must be added to the 17 clock cycles (see *Low-Frequency Clock Timing on page 162*).

V_{SB} Power-Up reset performs the actions listed below and all the actions performed by V_{DD} Power-Up reset (see Section 2.2.3). Note that V_{DD3} must be active during V_{SB3} power-up for all V_{DD} Power-Up reset actions to be performed:

- Samples the levels of the V_{BAT} power pin
- Activates the relevant circuits in SWC according to the level of the V_{BAT} power pin
- Resets all lock bits in configuration registers and SWC
- Loads default values to VDDLOAD bits in the GPIO configuration registers
- Loads default values to the V_{SB3}-powered bits in the configuration registers, SWC and GPIO
- Sets up the pull-up option and the default source for the V_{SB3}-powered multiplexed output pins

2.2.3 V_{DD} Power-Up Reset

V_{DD} Power-Up reset is generated by an internal circuit when V_{DD3} power is turned on. V_{DD} Power-Up reset time (t_{IRST}) lasts until the PCI_RESET signal is de-asserted. The Hardware reset (PCI_RESET) must be asserted for a minimum of 10 ms to ensure that the PC87373 device operates correctly.

External devices must wait at least t_{IRST} before accessing the PC87373. If the host processor accesses the PC87373 during this time, the PC87373 LPC interface ignores the transaction (that is, it does not return a SYNC handshake).

V_{DD} Power-Up reset performs the following actions:

- Puts pins with strap options into TRI-STATE and enables their internal pull-up resistors
- Samples the logic levels of the strap pins
- Executes all the actions performed by the Hardware reset (see Section 2.2.4)

2.2.4 Hardware Reset

Hardware reset is activated by the assertion (low) of the PCI_RESET input while V_{DD3} is "good". When V_{DD3} power is off, the PC87373 device ignores the level of the PCI_RESET input. However, the PCIRST_OUT and PCIRST_OUT2 outputs reflect the PCI_RESET input and thus are active (low). In addition, the Hardware reset (PCI_RESET) must be asserted after V_{SB} power-up, as described in Section 2.2.2.

Hardware reset performs the following actions:

- Resets all lock bits in configuration registers and SWC
- Sets up the pull-up option and the default source for the V_{DD3}-powered multiplexed output pins
- Executes all the actions performed by the Software reset (see Section 2.2.5)

2.0 Power, Reset and Clocks (Continued)

2.2.5 Software Reset

The Software reset is triggered by the host setting SWRST bit in SIOCF1 register (see Section 3.7.2 on page 44) via the LPC interface. The Host Software reset performs the following actions:

- Loads default values to the V_{DD3}-powered unlocked bits in the Configuration Control.
- Loads default values to the V_{SB3}-powered unlocked GPIO Configuration and Data bits for those GPIO ports with VDDLOAD = 1. VDDLOAD bit is not affected.
- Resets all the V_{DD3}-powered Legacy logical devices.
- Loads default values to all the V_{DD3}-powered Legacy module registers.

2.3 CLOCK DOMAINS

The PC87373 device has three clock domains, as shown in Table 6.

Table 6. Clock Domains of the PC87373

Clock Domain	Frequency	Power Plane	Source	Usage
LPC	Up to 33 MHz	V_{DD3}	LPC clock input (PCI_CLK)	LPC bus Interface and Configuration Registers
48 MHz	48 MHz	V_{DD3}	On-chip Clock Generator	Legacy functions (Serial Ports, Parallel Port, FDC, KBC, MIDI, Game Port) and FSCM
32 KHz	32.768 KHz	V_{SB3}	Clock input (CLOCKI32)	SWC, GPIO and Glue Functions

The LPC and 48 MHz clock domains, and the modules using them, are supplied by the Main power plane. Therefore, these two clock domains are active only when the V_{DD3} power supply is on.

2.3.1 LPC Domain

The LPC clock signal at the PCI_CLK pin must become valid (to the extent specified in *PCI_CLK and PCI_RESET* on page 163) before the end of the V_{DD} Power-Up reset (see Section 2.2.3).

2.3.2 48 MHz Domain

The 48 MHz clock domain is sourced by the on-chip Clock Generator (supplied by the Main power plane).

Following a V_{DD} Power-Up reset, the software waits a period of $t_{14MW} + t_{14MVAL}$ until a valid 14.31818 MHz clock signal is available at the CLOCKI14 pin. Then, the software can set the HFCGEN bit in the CLOCKCF register to 1. This bit enables the operation of the Clock Generator.

After the Clock Generator is enabled for operation, its output clock is frozen to a low level until the generator provides an internal clock signal that meets all requirements. When the requirements are met, the 48 MHz clock domain starts toggling. The status of the Clock Generator output clock is indicated by CKVALID bit in CLOCKCF register. While the Clock Generator is stabilizing, this bit is 0, indicating a 48 MHz clock domain frozen at low level. After t_{48MD}, the 48 MHz clock domain starts toggling and this bit is set to 1. The software must wait for CKVALID bit to be set before it enables the FSCM or the Legacy functions (Serial Ports, Parallel Port, FDC, KBC, MIDI, Game Port).

The on-chip Clock Generator multiplies the frequency of the clock signal (received through the CLOCKI14 pin) by a constant value to obtain the 48 MHz output frequency.

Figure 3 shows a simplified diagram of the 32 KHz and the 48 MHz clock domains.

2.0 Power, Reset and Clocks (Continued)

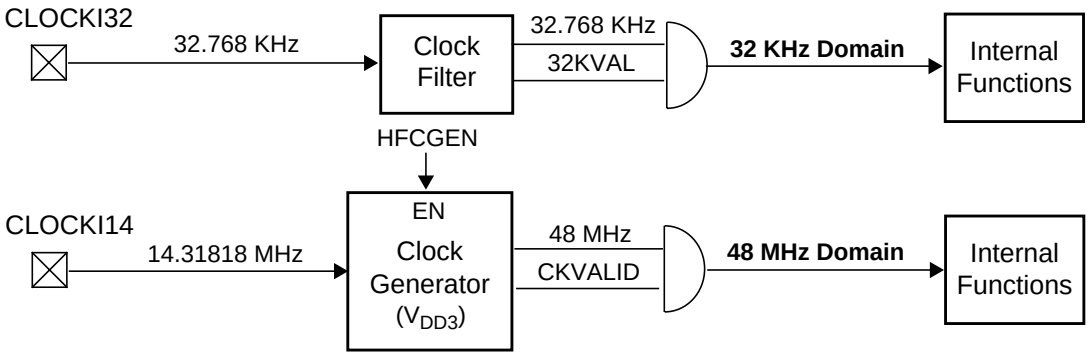


Figure 3. 32 KHz and 48 MHz Clock Domains (Simplified Diagram)

2.3.3 32 KHz Domain

The 32 KHz clock domain, and the modules using it, are supplied by the Standby and Core power planes. Therefore, this clock domain is active whenever the V_{SB3} and V_{CORF} power supplies are on.

The 32 KHz clock domain is sourced by the CLOCKI32 pin. The clock signal from the CLOCKI32 pin passes through a Clock Filter. The 32 KHz clock domain signal is held low by the 32KVAL output of the Clock Filter until a valid 32.768 KHz clock is available at the CLOCKI32 pin. The 32 KHz clock domain signal starts toggling t_{32KW} + t_{32KVAL} after V_{SB3} Power-Up (*Low-Frequency Clock Timing on page 162*).

2.4 TESTABILITY SUPPORT

The PC87373 device supports two testing techniques:

- In-Circuit Testing (ICT)
- XOR Tree Testing

2.4.1 ICT

The In-Circuit Testing (ICT) technique, also known as “bed-of-nails”, injects logic patterns to the input pins of the devices mounted on the tested board. It then checks their outputs for the correct logic levels.

The PC87373 supports this testing technique by floating (TRI-STATing) all the device pins. This prevents “back-driving” the PC87373 pins by the ICT tester when a device normally controlled by PC87373 is tested (device inputs are driven by the ICT tester).

To enter TRI-STATE mode, the $\overline{\text{TRIS}}$ pin must be pulled low (by a 10 KΩ resistor to V_{SS}), and the $\overline{\text{TEST}}$ pin must be left unconnected after both V_{DD3} and V_{SB3} power supplies are turned on. In addition, the $\overline{\text{PCI\_RESET}}$ pin must be held low for at least 10 ms (see *VSB Power-Up Reset* on page 159 and *VDD Power-Up Reset* on page 160). After $\overline{\text{PCI\_RESET}}$ is de-asserted, all the device output and I/O pins are floated (TRI-STATEd); exceptions to this are the power supply pins (V_{DD3}, V_{SB3}, V_{SS}, V_{CORF}, V_{BAT}), analog pins (V_{SB5}, REF5V, REF5V_STBY), $\overline{\text{RSMRST}}$, which do not float in TRI-STATE mode.

2.0 Power, Reset and Clocks (Continued)

2.4.2 XOR Tree Testing

When the PC87373 device is mounted on a board, it can be tested using the XOR Tree technique. This test also checks the correct connection of the device pins to the board.

To enter XOR Tree mode, the $\overline{TEST}$ pin must be pulled low (by a 10 KΩ resistor to V_{SS}), and the $\overline{TRIS}$ pin must be left unconnected after both V_{DD3} and V_{SB3} power supplies are turned on. In addition, the $\overline{PCI\_RESET}$ pin must be held low for at least 10 ms (see *VSB Power-Up Reset* on page 159 and *VDD Power-Up Reset* on page 160). After $\overline{PCI\_RESET}$ is de-asserted, the device pins (including the $\overline{PCI\_RESET}$, $\overline{TRIS}$ and $\overline{TEST}$ pins) are connected in a XOR Tree configuration and are isolated from the internal PC87373 functions.

In XOR Tree mode, all PC87373 device pins are configured as inputs, except the last pin in the tree, which is the XOR_OUT output. The buffer type of the input pins participating in the XOR tree, is IN_T (Input, TTL compatible), regardless of the buffer type of these pins in normal device operation mode (see Section 1.4 on page 16). The input pins are chained through XOR gates, as shown in Figure 4. The power supply pins (V_{DD3}, V_{SB3}, V_{SS}, V_{CORF}, V_{BAT}), the analog pins (V_{SB5}, REF5V, REF5V_STBY), $\overline{RSMRST}$ are excluded from the XOR tree.

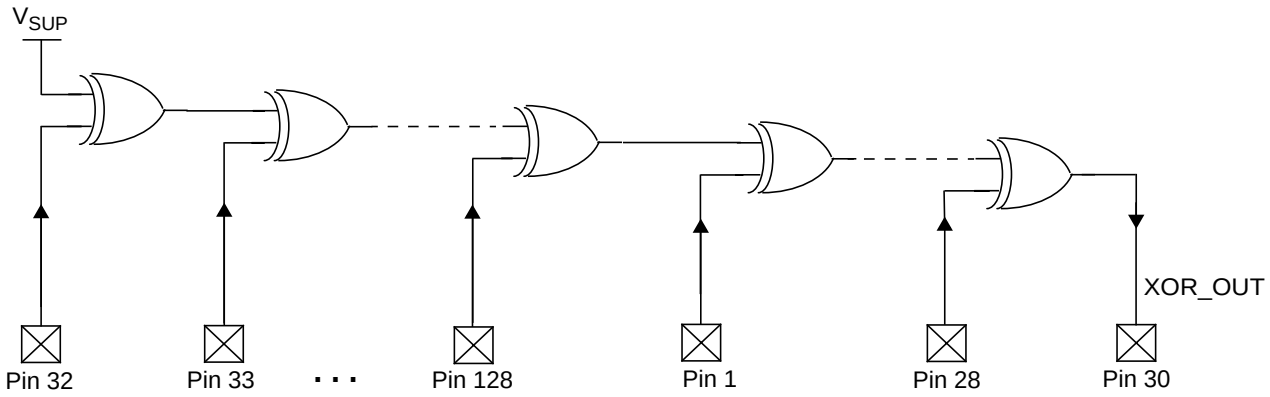


Figure 4. XOR Tree (Simplified Diagram)

The XOR tree starts with pin 32, continues incrementally with pin 33 (the next pin in ascending order) through pins 128, 1, and 28, and ends with pin 30 (XOR_OUT).

The maximum propagation delay through the XOR tree, from pin 32 to XOR_OUT is TBD.

3.0 Device Architecture and Configuration

The PC87373 device includes a collection of legacy and proprietary functional blocks. Each functional block is described in a separate chapter. This chapter describes the structure of the PC87373 device and provides all logical device specific information, including specific implementation of generic blocks, system interface and device configuration.

3.1 OVERVIEW

The PC87373 consists of the following: up to 11 logical devices, the host interface, the Glue Functions and a central set of configuration registers. All of these components are built around a central internal bus. The internal bus is similar to an 8-bit ISA bus protocol. See the Block Diagram on page 1, which illustrates the blocks and the internal bus.

The host, via the LPC Bus interface, can access the modules connected to the internal bus. This interface supports 8-bit I/O Read/Write and 8-bit DMA transactions of the LPC bus (see Section 4.2 on page 72).

The central configuration register set is ACPI compliant and supports PnP configuration. The configuration registers are structured as a subset of the Plug and Play Standard registers, defined in Appendix A of the *Plug and Play ISA Specification, Revision 1.0a* by Intel® and Microsoft®. All system resources assigned to the functional blocks (I/O address space, IRQ numbers and DMA channels) are configured in and managed by the central configuration register set. In addition, some function-specific parameters are configurable through the configuration registers and distributed to the functional blocks through special control signals.

3.2 CONFIGURATION STRUCTURE AND ACCESS

The configuration structure is based on a set of banked registers that are accessed via a pair of specialized registers.

3.2.1 The Index-Data Register Pair

Access to the PC87373 configuration registers is via an Index-Data register pair, using only two system I/O byte locations. The base address of this register pair is determined during reset according to the state of the hardware strapping option on the $\overline{\text{BADDR}}$ pin. Table 7 shows the selected base addresses as a function of $\overline{\text{BADDR}}$.

Table 7. $\overline{\text{BADDR}}$ Strapping Options

$\overline{\text{BADDR}}$	I/O Address	
	Index Register	**Data Register**
1 (default)	2Eh	2Fh
0	4Eh	4Fh

The Index register is an 8-bit read/write register located at the selected base address (Base+0). It is used as a pointer to the configuration register file and holds the index of the configuration register that is currently accessible via the Data register. Reading the Index register returns the last value written to it (or the default of 00h after reset).

The Data register is an 8-bit register (Base+1) used as a data path to any configuration register. Accessing the Data register actually accesses the configuration register that is currently pointed to by the Index register.

3.0 Device Architecture and Configuration (Continued)

3.2.2 Banked Logical Device Registers Structure

Each functional block is associated with a Logical Device Number (LDN). The configuration registers are grouped into banks, where each bank holds the standard configuration registers of the corresponding logical device. Table 8 shows the LDN values of the PC87373 functional blocks. Any value not listed is reserved.

Figure 5 shows the structure of the standard configuration register file. The LDN and PC87373 configuration registers are not banked and are accessed by the Index-Data register pair only, as described above. However, the device control and device configuration registers are duplicated over 11 banks, corresponding to the 11 logical devices. Therefore, accessing a specific register in a specific bank is performed by two-dimensional indexing, where the LDN register selects the bank (or logical device) and the Index register selects the register within the bank. Accessing the Data register while the Index register holds a value of 30h or higher actually accesses the configuration registers of the logical device selected by the LDN register and pointed to by the Index register.

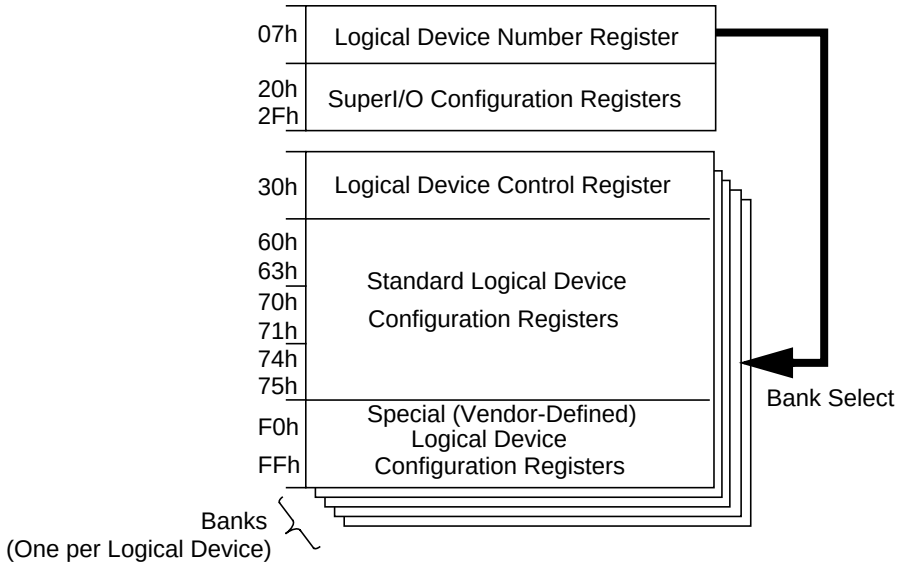


Figure 5. Structure of Standard Configuration Register File

Table 8. Logical Device Number (LDN) Assignments

LDN	Functional Block
00h	Floppy Disk Controller (FDC)
01h	Parallel Port (PP)
02h	Serial Port 2 (SP2)
03h	Serial Port 1 (SP1)
04h	System Wake-Up Control (SWC)
05h	Keyboard and Mouse Controller (KBC) - Mouse Interface
06h	Keyboard and Mouse Controller (KBC) - Keyboard Interface
07h	General-Purpose I/O (GPIO) Ports
09h	Fan Speed Control and Monitor (FSCM)
0Bh	Game Port (GMP)
0Ch	Musical Instrument Digital Interface (MIDI) Port

3.0 Device Architecture and Configuration (Continued)

Write accesses to unimplemented registers (i.e., accessing the Data register while the Index register points to a non-existing register) are ignored. Read accesses return 00h on all addresses, except for 74h and 75h (DMA configuration registers), which returns 04h (indicating no DMA channel). The configuration registers are accessible immediately after reset.

3.2.3 Standard Configuration Register Definitions

In the registers below, any undefined bit is reserved. Unless otherwise noted, the following definitions also hold true:

- All registers are read/write.
- All reserved bits return 0 on reads, except where noted otherwise. To prevent unpredictable results, do not modify these bits. Use read-modify-write to prevent the values of reserved bits from being changed during write.
- Write-only registers must not use read-modify-write during updates.

Table 9. Standard General Configuration Registers

Index	Register Name	Description
07h	Logical Device Number	This register selects the current logical device. See Table 8 for valid numbers. All other values are reserved.
20h-2Fh	PC87373 Configuration	PC87373 configuration registers and ID registers.

Table 10. Logical Device Activate Register

Index	Register Name	Description
30h	Activate	Bits 7-1: Reserved Bit 0: Logical device activation control (see Section 3.3 on page 40) 0: Disabled 1: Enabled

Table 11. I/O Space Configuration Registers

Index	Register Name	Description
60h	I/O Port Base Address Bits 15–8 Descriptor 0	Indicates selected I/O lower limit address bits 15–8 for I/O Descriptor 0.
61h	I/O Port Base Address Bits 7–0 Descriptor 0	Indicates selected I/O lower limit address bits 7–0 for I/O Descriptor 0.
62h	I/O Port Base Address Bits 15–8 Descriptor 1	Indicates selected I/O lower limit address bits 15–8 for I/O Descriptor 1.
63h	I/O Port Base Address Bits 7–0 Descriptor 1	Indicates selected I/O lower limit address bits 7–0 for I/O Descriptor 1.

3.0 Device Architecture and Configuration (Continued)

Table 12. Interrupt Configuration Registers

Index	Register Name	Description
70h	Interrupt Number and Wake-Up on IRQ Enable	Indicates selected interrupt number. Bits 7-5: Reserved. Bit 4: Enables a Power Management event ($\overline{\text{SIOPME}}$) from the IRQ of the logical device. When enabled, IRQ assertion sets the respective *XXX*_IRQ_STS bit (*XXX* is MOD, MS or KBD) in the GPE1_STS_3 register (see Section 6.4.7 on page 101). 0: Disabled (default) 1: Enabled **Note:** If the BIOS routine that sets IRQ does not use a Read-Modify-Write sequence, it might reset bit 4. To ensure that the system wakes up, the BIOS must set bit 4 before the system goes to sleep. Bits 3-0: These bits select the interrupt number. A value of 1 selects IRQ1. A value of 15 selects IRQ15. IRQ0 is not a valid interrupt selection and represents no interrupt selection. **Note:** Avoid selecting the same interrupt number (except 0) for different Logical Devices, as it causes the PC87373 device to behave unpredictably.
71h	Interrupt Request Type Select	Indicates the type and polarity of the interrupt request number selected in the previous register. If a logical device supports only one type of interrupt, the corresponding bit is read only. Bits 7-2: Reserved. Bit 1: Polarity of interrupt request selected in previous register 0: Low polarity 1: High polarity Bit 0: Type of interrupt request selected in previous register 0: Edge 1: Level

Table 13. DMA Configuration Registers

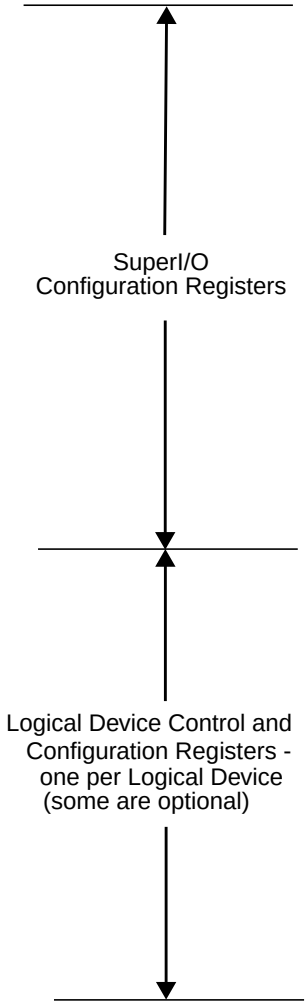
Index	Register Name	Description
74h	DMA Channel Select 0	Indicates selected DMA channel for DMA 0 of the logical device (0 is the first DMA channel if more than one DMA channel is used). Bits 7-3: Reserved. Bits 2-0: These select the DMA channel for DMA 0. The valid choices are 3-0, where: - A value of 0 selects DMA channel 0, 1 selects channel 1, etc. - A value of 4 indicates that no DMA channel is active. - The values 5-7 are reserved. **Note:** Avoid selecting the same DMA channel (except 4) for different logical devices, as it causes the PC87373 device to behave unpredictably.
75h	DMA Channel Select 1	Indicates selected DMA channel for DMA 1 of the logical device (1 is the second DMA channel if more than one DMA channel is used). Bits 7-3: Reserved. Bits 2-0: These select the DMA channel for DMA 1. The valid choices are 3-0, where: - A value of 0 selects DMA channel 0, 1 selects channel 1, etc. - A value of 4 indicates that no DMA channel is active. - The values 5–7 are reserved. **Note:** Avoid selecting the same DMA channel (except 4) for different logical devices, as it causes the PC87373 device to behave unpredictably.

3.0 Device Architecture and Configuration (Continued)

Table 14. Special Logical Device Configuration Registers

Index	Register Name	Description
F0h-FFh	Logical Device Configuration	Special (vendor-defined) configuration options.

3.2.4 Standard Configuration Registers



Index	Register Name
07h	Logical Device Number
20h	SuperI/O ID
21h	SuperI/O Configuration 1
22h	SuperI/O Configuration 2
23h	SuperI/O Configuration 3
24h	SuperI/O Configuration 4
25h	Reserved
26h	SuperI/O Configuration 6
27h	SuperI/O Revision ID
28h	Reserved
29h	Clock Generator Control
2Ah-2Fh	Reserved exclusively for National use
30h	Logical Device Control (Activate)
60h	I/O Base Address Descriptor 0 Bits 15-8
61h	I/O Base Address Descriptor 0 Bits 7-0
62h	I/O Base Address Descriptor 1 Bits 15-8
63h	I/O Base Address Descriptor 1 Bits 7-0
70h	Interrupt Number and Wake-Up on IRQ Enable
71h	IRQ Type Select
74h	DMA Channel Select 0
75h	DMA Channel Select 1
F0h-FFh	Vendor-Defined Logical Device Configuration

Figure 6. Configuration Register Map

SuperI/O Configuration Registers

The PC87373 configuration registers at indexes 20h (SuperI/O ID) and 27h (SuperI/O Revision ID) are used for part identification. The other configuration registers are used for global power management and selecting pin multiplexing options. For details, see Section 3.7 on page 43.

Logical Device Control and Configuration Registers

A subset of these registers is implemented for each logical device. See functional block descriptions in the following sections.

3.0 Device Architecture and Configuration (Continued)

Control Registers

The only implemented control register for each logical device is the Activate register at index 30h. Bit 0 of the Activate register controls the activation of the associated functional block. Activation enables access to the functional block's runtime registers and attaches its system resources, which are unassigned as long as it is not activated. Other effects may apply on a function-specific basis (such as clock enable and active pinout signaling). Access to the configuration register of the logical device is enabled even when the logical device is not activated.

Standard Configuration Registers

The standard configuration registers manage the PnP resource allocation to the functional blocks. The I/O port base address descriptor 0 is a pair of registers at Index 60–61h that hold the first 16-bit base address for the register set of the functional block. An optional 16-bit second base-address (descriptor 1) at index 62–63h is used for logical devices with more than one continuous register set. Interrupt Number and Wake-Up on IRQ Enable (index 70h) and IRQ Type Select (index 71h) allocate an IRQ line to the block and control its type. DMA Channel Select 0 (index 74h) allocates a DMA channel to the block, where applicable. DMA Channel Select 1 (index 75h) allocates a second DMA channel, where applicable.

Vendor-Defined Logical Device Configuration Register

The vendor-defined logical device registers start at index F0h and control function-specific parameters such as operation modes, power saving modes, pin TRI-STATE, clock rate selection and non-standard extensions to generic functions.

3.2.5 Default Configuration Setup

The default configuration setup of the PC87373 device is determined by the four reset types described in Section 2.2 on page 29. See the specific register descriptions for the bits affected by each reset source.

In the event of a V_{SB} Power-Up reset, the following default configuration is set up:

- All lock bits in the configuration registers are reset (the protected bits are unlocked).
- All the unlocked bits in the configuration registers powered by the V_{SB3} plane are reset to their default values.

In the event of a V_{DD} Power-Up (also induced by V_{SB} Power-Up reset) or Hardware reset, the PC87373 device wakes up with the following default configuration setup:

- The configuration base address is 2Eh or 4Eh, according to the $\overline{\text{BADDR}}$ strap pin value, as shown in Table 7 on page 34.
- All lock bits in the configuration registers are reset (the protected bits are unlocked).
- All the actions performed by the Software reset are executed.

If a Software reset occurs, the PC87373 device wakes up with the following default configuration setup:

- All the unlocked bits in the configuration registers powered by the V_{DD3} plane are reset to their default values.
- All logical devices are disabled (the Activation bit is reset) and the V_{SB}-powered logical devices (GPIO and SWC) remain functional but their registers cannot be accessed by the host.
- Standard configuration registers of all logical devices are set to their default values.
- National Semiconductor proprietary functions are not assigned with any default resources, and the default values of their base addresses are all 00h.
- All Legacy devices (Serial Ports, Parallel Port, Floppy Disk Controller, Keyboard and Mouse Controller, MIDI Port and Game Port) and the FSCM device are reset. Default values are loaded into the Legacy module runtime registers.

3.0 Device Architecture and Configuration (Continued)

3.3 MODULE CONTROL

Module control is performed primarily through the Activation bit (bit 0 of index 30h) of each logical device.

3.3.1 Module Enable/Disable

Module control is performed primarily through the Activation bit (bit 0 of index 30h) of each logical device. The operation of each module can be controlled by the host through the LPC bus.

Module enable/disable by the host through the LPC bus is controlled by the following bits:

- Activation bit (bit 0) in index 30h of the Standard configuration registers (see Section 3.2.3 on page 36)
- Fast Disable bit in SIOCF6 register; for the FDC, Parallel Port and Serial Port (1 and 2) modules only (see Section 3.7.6 on page 47)
- Global Enable bit (GLOBEN) in SIOCF1 register (see Section 3.7.2 on page 44)

A module is enabled only if all of these bits are set to their “enable” value.

When a V_{DD3}-powered module (FDC, Parallel Port, Serial Ports, KBC, MIDI Port and Game Port, FSCM) is disabled, the following takes place:

- The host system resources of the logical device (IRQ, DMA and runtime address range) are unassigned.
- Access to the standard- and device-specific Logical Device configuration registers through the LPC bus remains enabled.
- Access to the module’s runtime registers through the LPC bus is disabled (transactions are ignored; SYNC cycle is not generated).
- The module’s internal clock is disabled (the module is not functional) to lower the power consumption.

When a V_{SB3}-powered module (GPIO and SWC) is disabled, the following takes place:

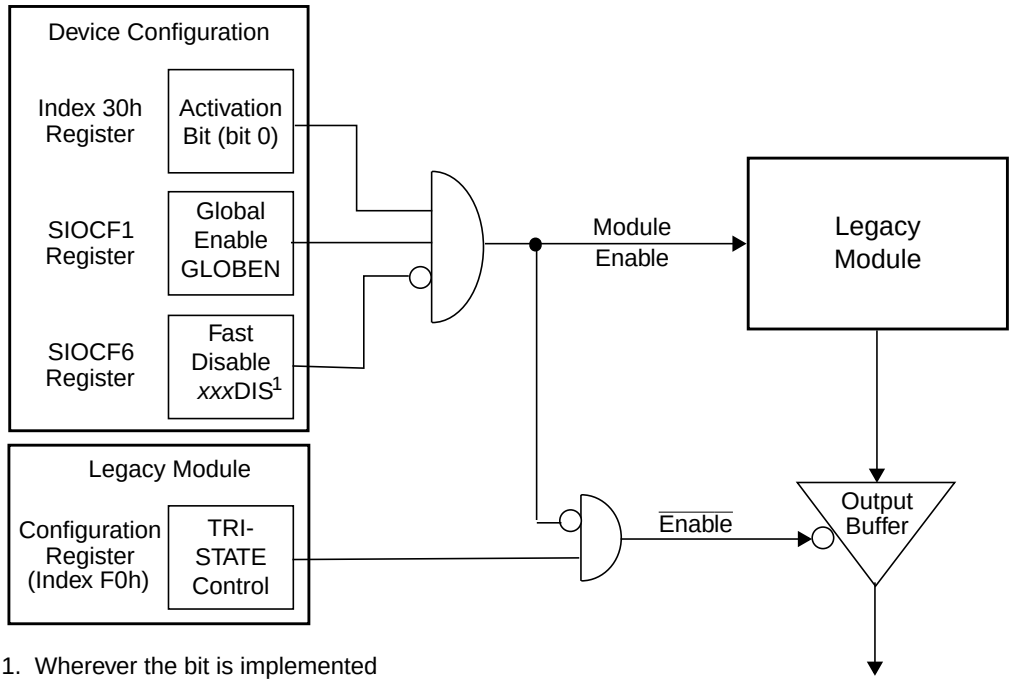
- The host system resources of the logical device (IRQ and runtime address range) are unassigned.
- Access to the standard and device specific Logical Device configuration registers through the LPC bus remains enabled.
- Access to the module’s runtime registers through the LPC bus is disabled (transactions are ignored; SYNC cycle is not generated).
- The module is functional.

3.0 Device Architecture and Configuration (Continued)

3.3.2 TRI-STATing Module Output

The pins of the Legacy modules (Serial Ports, Parallel Port, Floppy Disk Controller, Keyboard and Mouse Controller, MIDI Port, Game Port) and FSCM module can be floated (TRI-STATEd). When the TRI-STATE Control bit (bit 0) is set in the specific module configuration register (at index F0h of the specific Logical Device in the configuration space) **and** the module is disabled (see Section 3.3.1), the module output signals are floated (TRI-STATEd) and the I/O signals are configured as inputs (note that the logic level at the inputs is ignored by the module, which is disabled).

Figure 7 shows the control mechanism for TRI-STATing the pins of a Legacy module.



1. Wherever the bit is implemented

Figure 7. Control of TRI-STATing Legacy Module Pins

3.4 INTERNAL ADDRESS DECODING

A full 16-bit address decoding is applied when accessing the configuration I/O space as well as the registers of the functional blocks. However, the number of configurable bits in the base address registers varies for each logical device.

The lower 1, 2, 3, 4 or 5 address bits are decoded in the functional block to determine the offset of the accessed register within the logical device's I/O range of 2, 4, 8, 16 or 32 bytes, respectively. The rest of the bits are matched with the base address register to decode the entire I/O range allocated to the logical device. Therefore, the lower bits of the base address register are forced to 0 (read only), and the base address is forced to be 2, 4, 8, 16 or 32 byte-aligned, according to the size of the I/O range.

The base address of the FDC, Serial Port 1, Serial Port 2, and KBC are limited to the I/O address range of 00h to 7FXh only (bits 15-11 are forced to 0). The Parallel Port base address is limited to the I/O address range of 00h to 3F8h. The addresses the MIDI Port, Game Port and all of the non-legacy logical devices, including the FSCM, SWC and GPIO, are configurable within the full 16-bit address range (up to FFFXh).

In some special cases, other address bits are used for internal decoding (such as bit 2 in the KBC and bit 10 in the Parallel Port). The KBC has two I/O base addresses with some implied dependency between them. For more details, see the description of the base address register for each logical device.

3.0 Device Architecture and Configuration (Continued)

3.5 PROTECTION

The PC87373 device provides features to protect the hardware configuration from changes made by application software running on the host.

The protection is activated by the software setting a “sticky” lock bit. Each lock bit protects a group of configuration bits located either in the same register or in different registers. When the lock bit is set, the lock bit and all the protected bits become read only and cannot be further modified by the host through the LPC bus. All the lock bits are reset by Power-Up reset, thus unlocking the protected configuration bits.

The bit locking protection mechanism is optional.

The protected groups of configuration bits are described below.

3.5.1 Multiplexed Pins Configuration Lock

Protects the configuration of all the multiplexed device pins.

Lock bit: LOCKMCF in SIOCF1 register (Device Configuration).

Protected bits: IOWAIT in SIOCF1 register and all bits of the SIOCF2, SIOCF3 and SIOCF4 registers (Device Configuration).

3.5.2 GPIO Ports Configuration Lock

Protects the configuration (but not the data) of all the GPIO Ports.

Lock bit: LOCKGCF in SIOCF1 register (Device Configuration).

Protected bits for each GPIO Port: All bits of GPCFG1, GPEVR, GPCFG2 and GPMODE registers except LOCKCFP bit (Device Configuration).

3.5.3 Fast Disable Configuration Lock

Protects the Fast Disable bits for all the Legacy modules.

Lock bit: LOCKFDS in SIOCF6 register (Device Configuration).

Protected bits: All bits of the SIOCF6 register, except General-Purpose Scratch bits and GLOBEN bit in SIOCF1 register (Device Configuration).

3.5.4 Clock Control Lock

Protects the Clock Generator control bits.

Lock bit: HFCGEN in CLOCKCF register (Device Configuration).

Protected bits: All bits of the CLOCKCF register (Device Configuration).

3.5.5 GPIO Ports Lock

Protects the configuration **and** data of all the GPIO Ports.

Lock bit: LOCKCFP in GPCFG1 register, for each GPIO Port (Device Configuration).

Protected bits for each GPIO Port: PUPCTL, OUTTYPE and OUTENA in GPCFG1 register; all bits of the GPCFG2 register (Device Configuration); the corresponding bit (to the port pin) in GPDO and GPDIO registers (GPIO Ports).

3.5.6 Fan Speed Configuration Lock

Protects the Fan Speed Control and Monitor configuration bits.

Lock bit: LOCKFCF in FSCMCF1 register (Device Configuration).

Protected bits: All bits of the FSCMCF1 and FSCMCF2 registers (Device Configuration).

3.5.7 SWC Configuration Lock

Protects the configuration of the SWC module, including the Keyboard and Mouse wake-up configuration.

Lock bit: LOCKSCF in SWC_CTL register (System Wake-Up Control).

Protected bits: BLINK and GRN_YLW bits in the SLEDCTL register;
all bits of the SWC_CTL, ALEDCTL, LEDBLNK, XLEDCTL, KBDWKCTL, PS2CTL and PS2KEY0–7 registers (System Wake-Up Control).

3.0 Device Architecture and Configuration (Continued)

3.6 REGISTER TYPE ABBREVIATIONS

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from register (data written to this address is sent to a different register).
- W = Write (see above).
- RO = Read Only.
- WO = Write Only. Reading from the bit returns 0.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

In the registers below, use one of the following methods to handle the reserved bits:

- Write 0 to reserved bits, unless another “required value” is specified. This method can be used for registers containing bits of all types.
- Use read-modify-write to preserve the values of the reserved bits. This method can be used only for registers containing bits of R/W, RO, R/W1C and R/W1S types.

3.7 PC87373 CONFIGURATION REGISTERS

This section describes the PC87373 configuration and ID registers (i.e., registers with first level indexes in the range of 20h–2Fh). See Table 15 for a summary and directory of these registers.

Table 15. SuperI/O Configuration Registers

Index	Mnemonic	Register Name	Power Well	Type	Section
20h	SID	SuperI/O ID	V_{SB3}	RO	3.7.13.7.1
21h	SIOCF1	SuperI/O Configuration 1	V_{DD3}	Varies per bit	3.7.2
22h	SIOCF2	SuperI/O Configuration 2	V_{SB3}	R/W or RO	3.7.3
23h	SIOCF3	SuperI/O Configuration 3	V_{SB3}	R/W or RO	3.7.4
24h	SIOCF4	SuperI/O Configuration 4	V_{SB3}	R/W or RO	3.7.5
25h	Reserved				
26h	SIOCF6	SuperI/O Configuration 6	V_{DD3}	Varies per bit	3.7.6
27h	SRID	SuperI/O Revision ID	V_{SB3}	RO	3.7.7
28h	Reserved				
29h	CLOCKCF	Clock Generator Control	V_{SB3}	Varies per bit	3.7.8
2Ah-2Fh	Reserved for National use				

3.7.1 SuperI/O ID Register (SID)

This register contains the identity number of the device family. The PC87373 family is identified by the value F3h.

Power Well: V_{SB3}

Location: Index 20h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Family ID**							
Reset	F3h							

Bit	Description
7–0	**Family ID.** Identifies a family of devices with similar functionality but with different implemented options.

3.0 Device Architecture and Configuration (Continued)

3.7.2 SuperI/O Configuration 1 Register (SIOCF1)

Power Well: V_{DD3}

Location: Index 21h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**LOCKMCF**	**LOCKGCF**	**Reserved (must be '01')**		**IOWAIT**		**SWRST**	**GLOBEN**
Reset	0	0	0	1	0	0	0	1

Bit	Type	Description
7	R/W1S	**LOCKMCF (Lock Multiplexing Configuration).** When set to 1, this bit locks the configuration of registers SIOCF1, SIOCF2, SIOCF3 and SIOCF4 by disabling writing to all bits in these registers (including the LOCKMCF bit itself), except for the LOCKGCF, SWRST and GLOBEN bits in SIOCF1. Once set, this bit can be cleared by V_{DD3} Power-Up reset (or Hardware reset). 0: R/W bits are enabled for write (default) 1: All bits are RO
6	R/W1S	**LOCKGCF (Lock GPIO Pins Configuration).** When set to 1, this bit locks the configuration registers of all GPIO pins (see Section 3.14.2 on page 63) by disabling writes to all their bits (including the LOCKGCF bit itself). The locked registers include the GPCFG1 (except LOCKCFP bit), GPEVR, GPCFG2 and GPMODE registers of all GPIO pins. Once set, this bit can be cleared by V_{DD3} Power-Up reset (or Hardware reset). 0: R/W bits are enabled for write (default) 1: All bits are RO
5-4	–	**Reserved.** These bits must be '01'.
3-2	R/W or RO	**IOWAIT (Number of I/O Wait States).** These bits set the number of wait states for I/O transactions through the LPC bus. **Bits 3 2 Number of Wait States** 0 0: 0 (default) 0 1: 2 1 0: 6 1 1: 12
1	R/W	**SWRST (Software Reset).** When set to 1, this bit triggers the Software reset sequence (see Section 2.2.5 on page 31), after which it returns to 0. Read always returns 0. This bit is not influenced by the value of LOCKMCF. 0: Inactive (default) 1: Trigger the Software reset sequence
0	R/W or RO	**GLOBEN (Global Device Enable).** This bit makes it possible to disable all logical devices by setting a single bit (to 0). In addition, when the bit is set to 1, it enables the operation of all the logical devices of the PC87373, as long as the logical device is itself enabled (see Table 8 on page 35). The behavior of the different devices is explained in Section 3.3 on page 40. 0: All logical devices in the PC87373 device are forced to be disabled and their resources are released. 1: Enables each PC87373 logical device that is itself enabled (default); see Section 3.3.1 on page 40.

3.0 Device Architecture and Configuration (Continued)

3.7.3 SuperI/O Configuration 2 Register (SIOCF2)

Power Well: V_{SB3}

Location: Index 22h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**PMEPOL**	**PMETYPE**	**TACH2EN**	**TACH1EN**	**Reserved**		**TACH3EN**	**GPIO03EN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**PMEPOL ($\overline{\text{SIOPME}}$ Polarity).** Selects the polarity of the $\overline{\text{SIOPME}}$ signal. 0: $\overline{\text{SIOPME}}$ is active low (default) 1: $\overline{\text{SIOPME}}$ is active high
6	**PMETYPE ($\overline{\text{SIOPME}}$ Buffer Type).** Selects the output buffer type of the $\overline{\text{SIOPME}}$ pin. 0: Output is open-drain and the pull-up resistor is enabled (default) 1: Output is push-pull (the pull-up resistor is disabled)
5	**TACH2EN (FANTACH2 Multiplex Control).** Selects the function connected to pin 112. 0: GPIOE07 port: GPIO (default) 1: FANTACH2: FSCM
4	**TACH1EN (FANTACH1 Multiplex Control).** Selects the function connected to pin 111. 0: GPIOE06 port: GPIO (default) 1: FANTACH1: FSCM
3-2	**Reserved.**
1	**TACH3EN (FANTACH3 Multiplex Control).** Selects the function connected to the GPIOE01/FANTACH3 pin. 0: GPIOE01 port: GPIO (default) 1: FANTACH3: FSCM
0	**GPIO03EN (GPIOE10-GPIOE13 Multiplex Control).** Selects the functions connected to pins 113-116. 0: 5V_DDCSDA, 5V_DDCSCL, 3V_DDCSDA, 3V_DDCSCL: Glue Functions (default) 1: GPIOE10-GPIOE13 ports: GPIO

3.0 Device Architecture and Configuration (Continued)

3.7.4 SuperI/O Configuration 3 Register (SIOCF3)

Power Well: V_{SB3}

Location: Index 23h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**PWM3EN**	**PWM2EN**	**PWM1EN**	**GMPEN**	**Reserved**			
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**PWM3EN (FANPWM3 Multiplex Control).** Selects the function connected to the GPIOE05/FANPWM3 pin. 0: GPIOE05 port: GPIO (default) 1: FANPWM3: FSCM
6	**PWM2EN (FANPWM2 Multiplex Control).** Selects the function connected to the GPIOE04/FANPWM2 pin. 0: GPIOE04 port: GPIO (default) 1: FANPWM2: FSCM
5	**PWM1EN (FANPWM1 Multiplex Control).** Selects the function connected to the GPIOE03/FANPWM1 pin. 0: GPIOE03 port: GPIO (default) 1: FANPWM1: FSCM
4	**GMPEN (Game Port Multiplex Control).** Selects the functions connected to the following pins: 3V_DDCSCL/GPIOE13/JYABT0, 5V_DDCSCL/GPIOE11/JYABT1, 3V_DDCSDA/GPIOE12/JYBBT0, 5V_DDCSDA/GPIOE10/JYBBT1. 0: 3V_DDCSCL, 5V_DDCSCL, 3V_DDCSDA, 5V_DDCSDA (Glue Functions) **or** GPIOE13, GPIOE11, GPIOE12, GPIOE10 ports (GPIO), respectively, according to GPIO103EN bit in SIOCF2 register (see Section 3.7.3 on page 45) (default) 1: JYABT0, JYABT1, JYBBT0, JYBBT1: Game Port
3-0	**Reserved.**

3.7.5 SuperI/O Configuration 4 Register (SIOCF4)

Power Well: V_{SB3}

Location: Index 24h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**MIDIEN**	**Reserved**					
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Reserved.**
6	**MIDIEN (MIDI Port Multiplex Control).** Selects the function connected to pins SMB2_SCL/MDTX and SMB2_SDA/MDRX. 0: SMB2_SCL, SMB2_SDA: Glue Functions (default) 1: MDTX, MDRX: MIDI Port
5-0	**Reserved.**

3.0 Device Architecture and Configuration (Continued)

3.7.6 SuperI/O Configuration 6 Register (SIOCF6)

This register provides a fast way to disable one or more modules without having to access the Activate register of each (see Section 3.3.1 on page 40).

Power Well: V_{DD3}

Location: Index 26h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**LOCKFDS**	**General-Purpose Scratch**		**Reserved**	**SER1DIS**	**SER2DIS**	**PARPDIS**	**FDCDIS**
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
7	R/W1S	**LOCKFDS (Lock Fast Disable Configuration).** When set to 1, this bit locks itself, SER1DIS, SER2DIS, PARPDIS and FDCDIS bits in this register and GLOBEN bit in SIOCF1 register by disabling writing to all of these bits. Once set, this bit can be cleared by V_{DD3} Power-Up reset (or Hardware reset). 0: R/W bits are enabled for write (default) 1: All bits are RO
6-5	R/W	**General-Purpose Scratch.**
4	–	**Reserved.**
3	R/W or RO	**SER1DIS (Serial Port 1 Disable).** When set to 1, this bit forces the Serial Port 1 module to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled
2	R/W or RO	**SER2DIS (Serial Port 2 Disable).** When set to 1, this bit forces the Serial Port 2 module to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled
1	R/W or RO	**PARPDIS (Parallel Port Disable).** When set to 1, this bit forces the Parallel Port module to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled
0	R/W or RO	**FDCDIS (Floppy Disk Controller Disable).** When set to 1, this bit forces the Floppy Disk Controller module to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled

3.0 Device Architecture and Configuration (Continued)

3.7.7 SuperI/O Revision ID Register (SRID)

This register contains the ID number of the specific family member (Chip ID) and the chip revision number (Chip Rev). The PC87373 is identified by the value '000'. The Chip Rev is incremented on each revision.

Power Well: V_{SB3}

Location: Index 27h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Chip ID**			**Chip Rev**				
Reset	0	0	0	X	X	X	X	X

Bit	Description
7-5	**Chip ID.** These bits identify a specific device of a family.
4-0	**Chip Rev.** These bits identify the device revision.

3.7.8 Clock Generator Control Register (CLOCKCF)

Power Well: V_{SB3}

Location: Index 29h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**HFCGEN**	**Reserved**		**CKVALID**	**Reserved**			
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
7	R/W1S	**HFCGEN (Clock Generator Enable).** When set to 1, this bit enables the operation of the Clock Generator, and locks the configuration register CLOCKCF by disabling writing to all its bits (including to the HFCGEN bit itself). Once set, this bit can be cleared by V_{DD3} Power-Up reset (or Hardware reset). 0: Clock Generator disabled; the R/W bits are enabled for write (default). 1: Clock Generator enabled; all the bits are RO.
6-5	–	**Reserved.**
4	RO	**CKVALID (Valid Clock Generator, Clock Status).** This bit indicates the status of the on-chip, 48 MHz Clock Generator and controls the generator output clock signal. The PC87373 modules using this clock may be enabled (see Section 3.3.1 on page 40) only after this bit is read high (generator clock is valid). 0: Generator output clock frozen (default) 1: Generator output clock active (stable and toggling)
3-0	–	**Reserved.**

3.0 Device Architecture and Configuration (Continued)

3.8 FLOPPY DISK CONTROLLER (FDC) CONFIGURATION

3.8.1 General Description

The generic FDC is a standard FDC with a digital data separator and is DP8473 and N82077 software compatible. The PC87373 FDC supports 14 of the 17 standard FDC signals described in the generic Floppy Disk Controller (FDC) chapter, including the following (see Section 12.1 on page 140):

- FM and MFM modes are supported. To select either mode, set bit 6 of the first command byte when writing to/reading from a diskette, where:
  0 = FM mode
  1 = MFM mode
- A logic 1 is returned during LPC I/O read cycles by all register bits reflecting the state of floating (TRI-STATE) FDC pins.

Exceptions to standard FDC are:

- Automatic media sense using MSEN0 and MSEN1 signals is not supported.
- DRATE1 is not supported.
- $\overline{DR1}$ is not supported.
- $\overline{MTR1}$ is not supported.

The FDC functional block registers are shown in Section 12.1 on page 140. All of these registers are V_{DD3} powered.

3.8.2 Logical Device 0 (FDC) Configuration

Table 16 lists the configuration registers that affect the FDC. Only the last two registers (F0h and F1h) are described here. See Section 3.2.3 on page 36 for descriptions of the other configuration registers. All of these registers are V_{DD3} powered.

Table 16. FDC Configuration Register

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.3.1 on page 40)	R/W	V_{DD3}	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read only, ‘00000’.	R/W	V_{DD3}	03h
61h	Base Address LSB register. Bits 2 and 0 (for A2 and A0) are read only, ‘00’.	R/W	V_{DD3}	F2h
70h	Interrupt Number and Wake-Up on IRQ Enable register	R/W	V_{DD3}	06h
71h	Interrupt Type. Bit 1 is read/write; other bits are read only.	R/W	V_{DD3}	03h
74h	DMA Channel Select	R/W	V_{DD3}	02h
75h	Report no second DMA assignment	RO	V_{DD3}	04h
F0h	FDC Configuration register	R/W	V_{DD3}	24h
F1h	Drive ID register	R/W	V_{DD3}	00h
F8h	FDC Configuration register (mirror of the register at index F0h)	R/W	V_{DD3}	24h

3.0 Device Architecture and Configuration (Continued)

3.8.3 FDC Configuration Register

This register is reset to 24h.

Power Well: V_{DD3}

Location: Indexes F0h and F8h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**TDR Register Mode**	**DENSEL Polarity Control**	**FDC 2Mbps Enable**	**Write Protect**	**PC-AT or PS/2 Drive Mode Select**	**Reserved**	**TRI-STATE Control**
Reset	0	0	1	0	0	1	0	0

Bit	Description
7	**Reserved.**
6	**TDR Register Mode.** 0: PC-AT-Compatible Drive mode; i.e., bits 7-2 of the TDR are '111111' (default) 1: Enhanced Drive mode
5	**DENSEL Polarity Control.** 0: Active low for 500 Kbps or 1 or 2 Mbps data rates 1: Active high for 500 Kbps or 1 or 2 Mbps data rates (default)
4	**FDC 2Mbps Enable.** This bit is set only when a 2 Mbps drive is used. 0: 2 Mbps disabled and the FDC clock is 24 MHz (default) 1: 2 Mbps enabled and the FDC clock is 48 MHz
3	**Write Protect.** This bit enables forcing of write protect functionality by software. When set, writes to the floppy disk drive are disabled. This effect is identical to an active $\overline{WP}$ signal. 0: Write protected according to $\overline{WP}$ signal (default) 1: Write protected regardless of value of $\overline{WP}$ signal
2	**PC-AT or PS/2 Drive Mode Select.** 0: PS/2 Drive mode 1: PC-AT Drive mode (default)
1	**Reserved.**
0	**TRI-STATE Control.** When this bit is set to 1 and the logical device is inactive, the logical device output pins are in TRI-STATE (see Section 3.3.2 on page 41). 0: Normal outputs (default) 1: TRI-STATE outputs when the logical device is inactive

3.0 Device Architecture and Configuration (Continued)

3.8.4 Drive ID Register

This register is reset to 00h. This register controls bits 5 and 4 of the TDR register in Enhanced mode.

Power Well: V_{DD3}
Location: Index F1h
Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**Drive 1 ID**		**Drive 0 ID**	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved.**
3-2	**Drive 1 ID.** When drive 1 is accessed, these bits are reflected on bits 5-4 of the TDR register, respectively.
1-0	**Drive 0 ID.** When drive 0 is accessed, these bits are reflected on bits 5-4 of the TDR register, respectively.

Usage Hints: Some BIOS implementations support FDDs with automatic media sense; in this case, bit 5 of TDR register in Enhanced mode is interpreted as valid media sense when it is cleared to 0. If drive 0 and/or drive 1 do not support automatic media sense, bits 1 and/or 3 of the Drive ID register must be set to 1 (to indicate non-valid media sense). When Drive 0 or Drive 1 is selected, the Drive ID bit is reflected on bit 5 of TDR register in Enhanced mode.

3.0 Device Architecture and Configuration (Continued)

3.9 PARALLEL PORT (PP) CONFIGURATION

3.9.1 General Description

The PC87373 Parallel Port supports all IEEE1284 standard communication modes: Compatibility (also known as Standard or SPP), Bi-directional (known also as PS/2), FIFO, EPP (also known as mode 4) and ECP (with an optional Extended ECP mode).

The Parallel Port includes two groups of runtime registers (see Section 12.2 on page 142):

- A group of 21 registers at first level offset, sharing 14 entries. Three of these registers (at offsets 403h, 404h and 405h) are used only in Extended ECP mode.
- A group of four registers, used only in Extended ECP mode, is accessed by a second level offset.

The desired mode is selected by the ECR runtime register (offset 402h). The selected mode determines which runtime registers are used and which address bits are used for the base address. The Parallel Port functional block registers are shown in Section 12.2 on page 142. All of these registers are V_{DD3} powered.

3.9.2 Logical Device 1 (PP) Configuration

Table 17 lists the configuration registers that affect the Parallel Port. Only the last register (F0h) is described here. See Section 3.2.3 on page 36 for descriptions of the other configuration registers. All of these registers are V_{DD3} powered.

Table 17. Parallel Port Configuration Registers

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.3.1 on page 40)	R/W	V_{DD3}	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read only, '00000'. Bit 2 (for A10) must be '0'.	R/W	V_{DD3}	02h
61h	Base Address LSB register. Bits 1 and 0 (A1 and A0) are read only, '00'. For ECP mode 4 (EPP) or when using Extended registers, bit 2 (A2) must also be '0'.	R/W	V_{DD3}	78h
70h	Interrupt Number and Wake-Up on IRQ Enable register	R/W	V_{DD3}	07h
71h	Interrupt Type: - Bits 7-2 are read only. - Bit 1 is a read/write bit. - Bit 0 is read only. It reflects the interrupt type dictated by the Parallel Port operation mode. This bit is set to 1 (level interrupt) in Extended mode and cleared (edge interrupt) in all other modes.	R/W	V_{DD3}	02h
74h	DMA Channel Select	R/W	V_{DD3}	04h
75h	Report no second DMA assignment	RO	V_{DD3}	04h
F0h	Parallel Port Standard Configuration register	R/W	V_{DD3}	F2h
F8h	Parallel Port Modified Configuration register	R/W	V_{DD3}	07h

3.0 Device Architecture and Configuration (Continued)

3.9.3 Parallel Port Standard Configuration Register

This register is reset to F2h.

Power Well: V_{DD3}

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Parallel Port Mode Select**			**Extended Register Access**	**Reserved**		**Power Mode Control**	**TRI-STATE Control**
Reset	1	1	1	1	0	0	1	0

Bit	Description
7-5	**Parallel Port Mode Select.** The mode selected by writing to these bits, is reflected by bits 3-0 in the Parallel Port Modified Configuration Register (see Section 3.9.4 on page 54). **Bits 7 6 5 Mode** 0 0 0: SPP-Compatible mode. PD7-0 are always output signals 0 0 1: SPP Extended mode. PD7-0 direction is controlled by software 0 1 0: EPP 1.7 mode 0 1 1: EPP 1.9 mode 1 0 0: ECP mode (IEEE1284 register set), with no support for EPP mode 1 0 1: Reserved 1 1 0: Reserved 1 1 1: ECP mode (IEEE1284 register set), with EPP mode selectable as mode “100” (default) Selection of EPP 1.7 or 1.9 in ECP mode “100” is controlled by bit 4 of the Control2 configuration register of the Parallel Port at offset 02h. **Note**: Before setting bits 7-5, enable the Parallel Port and set CTR/DCR (at base address + 2) to C4h.
4	**Extended Register Access.** 0: Registers at base (address) + 403h, base + 404h and base + 405h are not accessible (reads and writes are ignored) 1: Registers at base (address) + 403h, base + 404h and base + 405h are accessible. This option supports runtime configuration within the Parallel Port address space (default).
3-2	**Reserved.**
1	**Power Mode Control.** When the logical device is active: 0: Parallel Port clock disabled. ECP modes and EPP time-out are not functional when the logical device is active. Registers are maintained. 1: Parallel Port clock enabled. All operation modes are functional when the logical device is active (default).
0	**TRI-STATE Control.** When this bit is set to 1 and the logical device is inactive, the logical device output pins are in TRI-STATE (see Section 3.3.2 on page 41). 0: Normal outputs (default) 1: TRI-STATE outputs when the logical device is inactive

3.0 Device Architecture and Configuration (Continued)

3.9.4 Parallel Port Modified Configuration Register

This register is reset to 07h.

Power Well: V_{DD3}

Location: Index F8h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**Parallel Port Mode Select**			
Reset	0	0	0	0	0	1	1	1

Bit	Description
7-4	**Reserved.**
3-0	**Parallel Port Mode Select.** The mode selected by writing to these bits, is reflected by bits 7-5 in the Parallel Port Standard Configuration Register (see Section 3.9.3 on page 53). **Bits 3 2 1 0 Mode** 0 0 0 1: SPP Extended mode. PD7-0 direction is controlled by software 0 0 1 0: EPP 1.9 mode 0 1 0 0: ECP mode (IEEE1284 register set), with no support for EPP mode 1 0 0 0: SPP-Compatible mode. PD7-0 are always output signals 0 1 1 1: ECP mode (IEEE1284 register set), with EPP mode selectable as mode “0100” (default) 1 0 1 0: EPP 1.7 mode Other: Reserved (writing a reserved value causes unpredictable behavior of the Parallel Port) Selection of EPP 1.7 or 1.9 in ECP mode “0100” is controlled by bit 4 of Control2 configuration register of the Parallel Port at offset 02h. **Note**: Before setting bits 3-0, enable the Parallel Port and set CTR/DCR (at base address + 2) to C4h.

3.0 Device Architecture and Configuration (Continued)

3.10 SERIAL PORT 2 CONFIGURATION

3.10.1 General Description

Serial Port 2 provides UART functionality by supporting serial data communication with remote peripheral device or modem. The functional blocks can function as a standard 16450 or 16550 or as an Extended UART.

Serial Port 2 includes four register banks, each containing eight runtime registers, as shown in Section 12.3 on page 145. All these registers are V_{DD} powered.

3.10.2 Logical Device 2 (SP2) Configuration

Table 18 lists the configuration registers that affect Serial Port 2. Only the last register (F0h) is described here. See Section 3.2.3 on page 36 for descriptions of the other configuration registers. All these registers are V_{DD} powered.

Table 18. Serial Port 2 Configuration Registers

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.3.1 on page 40)	R/W	V_{DD}	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read only, 00000b.	R/W	V_{DD}	02h
61h	Base Address LSB register. Bit 2-0 (for A2-0) are read only, 000b.	R/W	V_{DD}	F8h
70h	Interrupt Number and Wake-Up on IRQ Enable register	R/W	V_{DD}	03h
71h	Interrupt Type. Bit 1 is R/W; other bits are read only	R/W	V_{DD}	03h
74h	Report no DMA Assignment	RO	V_{DD}	04h
75h	Report no DMA Assignment	RO	V_{DD}	04h
F0h	Serial Port 2 Configuration register	R/W	V_{DD}	02h

3.0 Device Architecture and Configuration (Continued)

3.10.3 Serial Port 2 Configuration Register

This register is reset by hardware to 02h.

Power Well: V_{DD}

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Bank Select Enable**	**Reserved**				**Busy Indicator**	**Power Mode Control**	**TRI-STATE Control**
Reset	0	0	0	0	0	0	1	0

Bit	Description
7	**Bank Select Enable**. Enables bank switching for Serial Port 2. 0: All attempts to access the extended registers in Serial Port 2 are ignored (default) 1: Enables bank switching for Serial Port 2
6-3	**Reserved.**
2	**Busy Indicator.** This read only bit can be used by power management software to decide when to power-down the Serial Port 2 logical device. 0: No transfer in progress (default) 1: Transfer in progress
1	**Power Mode Control.** The logical device can be active in two modes: 0: Low Power mode: When the logical device is active in Low Power mode, - The Low Serial Port 2 clock is disabled. - The output signals are set to their default states. - The $\overline{RI}$ input signal can be programed to generate an interrupt. - Registers are maintained (unlike the activation bit in Index 30h, which also prevents access to Serial Port 2 registers). 1: Normal Power mode: When the logical device is active in Normal Power mode, - Serial Port 2 clock enabled. - Serial Port 2 is functional when the logical device is active (default).
0	**TRI-STATE Control.** When this bit is set to 1 and the logical device is inactive, the logical device output pins are in TRI-STATE (see Section 3.3.2 on page 41). 0: Normal outputs (default) 1: TRI-STATE outputs when the logical device is inactive

3.0 Device Architecture and Configuration (Continued)

3.11 SERIAL PORT 1 CONFIGURATION

3.11.1 General Description

Serial Port 1 provides UART functionality by supporting serial data communication with a remote peripheral device or a modem. The functional blocks can function as a standard 16450 or 16550 or as an Extended UART.

Serial Port 1 includes four register banks, each containing eight runtime registers, as shown in Section 12.3 on page 145. All the registers are V_{DD3} powered.

3.11.2 Logical Device 3 (SP1) Configuration

Table 19 lists the configuration registers that affect Serial Port 1. Only the last register (F0h) is described here. See Section 3.2.3 on page 36 for descriptions of the other configuration registers. All these registers are V_{DD3} powered.

Table 19. Serial Port 1 Configuration Registers

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.3.1 on page 40)	R/W	V_{DD3}	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read only, '00000'.	R/W	V_{DD3}	03h
61h	Base Address LSB register. Bits 2-0 (for A2-0) are read only, '000'.	R/W	V_{DD3}	F8h
70h	Interrupt Number and Wake-Up on IRQ Enable register	R/W	V_{DD3}	04h
71h	Interrupt Type. Bit 1 is R/W; other bits are read only.	R/W	V_{DD3}	03h
74h	Report no DMA Assignment	RO	V_{DD3}	04h
75h	Report no DMA Assignment	RO	V_{DD3}	04h
F0h	Serial Port 1 Configuration register	R/W	V_{DD3}	02h

3.0 Device Architecture and Configuration (Continued)

3.11.3 Serial Port 1 Configuration Register

This register is reset to 02h.

Power Well: V_{DD3}

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Bank Select Enable**	**Reserved**				**Busy Indicator**	**Power Mode Control**	**TRI-STATE Control**
Reset	0	0	0	0	0	0	1	0

Bit	Description
7	**Bank Select Enable**. Enables bank switching for Serial Port 1. 0: All attempts to access the extended registers in Serial Port 1 are ignored (default) 1: Enables bank switching for Serial Port 1
6-3	**Reserved.**
2	**Busy Indicator.** This read-only bit can be used by power management software to decide when to power down the Serial Port 1 logical device. 0: No transfer in progress (default) 1: Transfer in progress
1	**Power Mode Control.** The logical device can be active in two modes: 0: Low Power mode: When the logical device is active in Low Power mode, - The Low Serial Port 1 clock is disabled. - The output signals are set to their default states. - The $\overline{RI}$ input signal can be programed to generate an interrupt. - Registers are maintained (unlike the activation bit in Index 30h, which also prevents access to the Serial Port 1 registers). 1: Normal Power mode: When the logical device is active in Normal Power mode, - Serial Port 1 clock enabled. - Serial Port 1 is functional when the logical device is active (default).
0	**TRI-STATE Control.** When this bit is set to 1 and the logical device is inactive, the logical device output pins are in TRI-STATE (see Section 3.3.2 on page 41). 0: Normal outputs (default) 1: TRI-STATE outputs when the logical device is inactive

3.0 Device Architecture and Configuration (Continued)

3.12 SYSTEM WAKE-UP CONTROL (SWC) CONFIGURATION

3.12.1 General Description

System Wake-Up Control provides wake-up and power management functionality according to the ACPI specification (see Section 6.1 on page 80). Its registers are V_{SB3} powered.

3.12.2 Logical Device 4 (SWC) Configuration

Table 20 lists the configuration registers that affect the SWC. See Section 3.2.3 on page 36 for a detailed description of these registers. All these registers are V_{DD3} powered.

Table 20. System Wake-Up Control (SWC) Configuration Registers

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate. When bit 0 is cleared, the runtime registers of this logical device are not accessible (see Section 3.3.1 on page 40).[1]	R/W	V_{DD3}	00h
60h	SWC Base Address MSB register	R/W	V_{DD3}	00h
61h	SWC Base Address LSB register. Bits 3-0 (for A3-0) are read only, '0000'.	R/W	V_{DD3}	00h
62h	GPE1_BLK Base Address MSB register	R/W	V_{DD3}	00h
63h	GPE1_BLK Base Address LSB register. Bits 3-0 (for A3-0) are read only, '0000'.	R/W	V_{DD3}	00h
70h	Interrupt Number	R/W	V_{DD3}	00h
71h	Interrupt Type. Bit 1 is read/write. Other bits are read only	R/W	V_{DD3}	03h
74h	Report no DMA assignment	RO	V_{DD3}	04h
75h	Report no DMA assignment	RO	V_{DD3}	04h

1. The logical device runtime registers are maintained and all wake-up detection mechanisms are functional.

3.0 Device Architecture and Configuration (Continued)

3.13 KEYBOARD AND MOUSE CONTROLLER (KBC) CONFIGURATION

3.13.1 General Description

The KBC is implemented physically as a single hardware module and houses two separate logical devices: a Mouse controller (Logical Device 5) and a Keyboard controller (Logical Device 6). The KBC is functionally equivalent to the industry standard 8042A Keyboard controller. Technical references for the standard 8042A Keyboard Controller may serve as detailed technical references for the KBC.

The Keyboard and Mouse Controller runtime registers are described in Section 12.4 on page 149. All the registers are V_{DD3} powered.

3.13.2 Logical Devices 5 and 6 (Mouse and Keyboard) Configuration

Tables 21 and 22 list the configuration registers that affect the Mouse and Keyboard logical devices. Only the last register (F0h) is described here. See Section 3.2.3 on page 36 for descriptions of the other configuration registers. The KBC module is activated and the access to the runtime registers (pointed at by the base addresses at indexes 60h-63h) is enabled when either the Mouse logical device (5) or the Keyboard logical device (6) is activated (by setting the activation bit at index 30h). Because the IRQ configuration resources are separate for each logical device (Mouse or Keyboard), the specific logical device must be activated to enable its IRQ resources. All of these registers are V_{DD3} powered, with the exception of the KBC Configuration register (F0h), which is both V_{DD3} and V_{SB3} powered.

Table 21. Mouse Configuration Registers

Index	Mouse Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.2.3 on page 36). When the Mouse of the KBC is inactive, the IRQ selected by the Mouse Interrupt Number and Wake-Up on IRQ Enable register (index 70h) are not asserted.	R/W	V_{DD3}	00h
70h	Mouse Interrupt Number and Wake-Up on IRQ Enable register	R/W	V_{DD3}	0Ch
71h	Mouse Interrupt Type. Bits 1,0 are read/write; other bits are read only.	R/W	V_{DD3}	02h
74h	Report no DMA assignment	RO	V_{DD3}	04h
75h	Report no DMA assignment	RO	V_{DD3}	04h

Table 22. Keyboard Configuration Registers

Index	Keyboard Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.2.3 on page 36). When the Keyboard of the KBC is inactive, the IRQ selected by the Keyboard Interrupt Number and Wake-Up on IRQ Enable register (index 70h) are not asserted.	R/W	V_{DD3}	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read only, '00000'.	R/W	V_{DD3}	00h
61h	Base Address LSB register. Bits 2-0 (for A2-0) are read-only, '000'.	R/W	V_{DD3}	60h
62h	Command Base Address MSB register. Bits 7-3 (for A15-11) are read only, '00000'.	R/W	V_{DD3}	00h
63h	Command Base Address LSB. Bits 2-0 (for A2-0) are read-only, '100'.	R/W	V_{DD3}	64h
70h	KBD Interrupt Number and Wake-Up on IRQ Enable register	R/W	V_{DD3}	01h
71h	KBD Interrupt Type. Bits 1,0 are read/write; others are read only.	R/W	V_{DD3}	02h
74h	Report no DMA assignment	RO	V_{DD3}	04h
75h	Report no DMA assignment	RO	V_{DD3}	04h
F0h	KBC Configuration register	R/W	V_{DD3}/V_{SB3}	40h

3.0 Device Architecture and Configuration (Continued)

3.13.3 KBC Configuration Register

This register is reset to 40h.

Power Well: V_{DD3} and V_{SB3} (see Note 1)

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**KBC Clock Source**		**Reserved**		**SWAP[1]**	**Reserved**		**TRI-STATE Control**
Reset	0	1	0	0	0	0	0	0
Required						0		

1. This bit is powered from the V_{SB3} well and is reset by V_{SB3} Power-Up reset.

Bit	Description
7-6	**KBC Clock Source.** The clock source can be changed only when the KBC is inactive (disabled). **Bits 7 6 Source** 0 0: 8 MHz 0 1: 12 MHz (default) 1 0: 16 MHz 1 1: Reserved
5-4	**Reserved.**
3	**SWAP (Swap Keyboard and Mouse Inputs).** When this bit is set, the keyboard signals (KBCLK and KBDAT) are swapped with the mouse signals (MCLK and MDAT). This bit is used both by the KBC module and by the Keyboard/Mouse Wake-Up Detector in the SWC module. This bit is reset to the default value by V_{SB3} Power-Up reset only. 0: No swapping (default) 1: Swaps the keyboard and mouse signals
2-1	**Reserved.**
0	**TRI-STATE Control**. When this bit is set, the Keyboard pins (KBCLK, KBDAT) and the Mouse pins (MCLK, MDAT) are in TRI-STATE (see Section 3.3.2 on page 41), if both the Keyboard and the Mouse logical devices are inactive. 0: Normal outputs (default) 1: TRI-STATE outputs when the Keyboard and the Mouse logical devices are inactive

Usage Hints:

1. To change the clock frequency of the KBC:
   a. Disable the KBC logical devices.
   b. Change the frequency setting.
   c. Enable the KBC logical devices.
2. Before swapping between the Keyboard and Mouse Interface pins, disable the KBC logical devices and their pins. After swapping, the software must issue a synchronization command to the Keyboard and Mouse through the KBC to regain synchronization with these devices.

3.0 Device Architecture and Configuration (Continued)

3.14 GENERAL-PURPOSE INPUT/OUTPUT (GPIO) PORTS CONFIGURATION

3.14.1 General Description

The GPIO functional block includes 13 pins arranged in two ports:

- Port 0 contains eight GPIOE pins (i.e., GPIO pins with event detection).
- Port 1 contains four GPIOE pins and one GPIO pin.

The pins of Ports 0 and 1 have full event detection capability (see Section 1.3 on page 15), enabling them to trigger an IRQ. In addition, through the SWC functional block, the pins of Ports 0 and 1 can trigger the $\overline{\text{SIOPME}}$ signal. An exception is the GPIO14 pin of Port 1, which has no event detection and therefore cannot trigger IRQ or $\overline{\text{SIOPME}}$.

All 13 GPIO pins are powered from the V_{SB3} well. The 10 runtime registers associated with the two ports are arranged in the GPIO address space as shown in Table 23. Each GPIO port with wake-up event detection capability has five runtime registers. The GPIO base address is 32-byte aligned. Address bits 4-0 are used to indicate the register offset.

The specific runtime registers implemented in the PC87373 devices are shown in Table 23. All of these registers are V_{SB3} powered.

Table 23. Runtime Registers in GPIO Address Space

Offset	Mnemonic	Register Name	Port	Power Well	Type	
					SEPDIO[1] = 1	SEPDIO = 0
00h	GPDO0	GPIO Data Out 0	0	V_{SB3}	R/W	RO
01h	GPDI0	GPIO Data In 0		V_{SB3}	RO	RO
02h	GPEVEN0	GPIO Event Enable 0		V_{SB3}	R/W	RO
03h	GPEVST0	GPIO Event Status 0		V_{SB3}	R/W1C	RO
04h	GPDO1	GPIO Data Out 1	1	V_{SB3}	R/W	RO
05h	GPDI1	GPIO Data In 1		V_{SB3}	RO	RO
06h	GPEVEN1	GPIO Event Enable 1		V_{SB3}	R/W	RO
07h	GPEVST1	GPIO Event Status 1		V_{SB3}	R/W1C	RO
15h	GPDIO0	GPIO Data In/Out 0	0	V_{SB3}	R/W	R/W
16h	GPDIO1	GPIO Data In/Out 1	1	V_{SB3}	R/W	R/W

1. See Section 3.14.7 on page 66

3.0 Device Architecture and Configuration (Continued)

3.14.2 Logical Device 7 (GPIO) Configuration

Table 24 lists the configuration registers that affect the GPIO. Only the last five registers (F0h-F3h and F8h) are described here. See Section 3.2.3 on page 36 for a detailed description of the other configuration registers. The standard configuration registers are powered by V_{DD3}; however, the specific configuration registers are powered by V_{SB3}.

Table 24. GPIO Configuration Register

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.2.3 on page 36)	R/W	V_{DD3}	00h
60h	Base Address MSB register	R/W	V_{DD3}	00h
61h	Base Address LSB register. Bits 4-0 (for A4-0) are read-only, '00000'.	R/W	V_{DD3}	00h
70h	Interrupt Number and Wake-Up on IRQ Enable register	R/W	V_{DD3}	00h
71h	Interrupt Type. Bit 1 is read/write. Other bits are read only.	R/W	V_{DD3}	03h
74h	Report no DMA assignment	RO	V_{DD3}	04h
75h	Report no DMA assignment	RO	V_{DD3}	04h
F0h	GPIO Pin Select register (GPSEL)	R/W	V_{SB3}	00h
F1h	GPIO Pin Configuration register 1 (GPCFG1)	Varies per bit	V_{SB3}	00h
F2h	GPIO Pin Event Routing register (GPEVR)	R/W or RO	V_{SB3}	00h
F3h	GPIO Pin Configuration register 2 (GPCFG2)	R/W or RO	V_{SB3}	00h
F8h	GPIO Mode Select register (GPMODE)	R/W or RO	V_{SB3}	01h

Figure 8 shows the organization of registers GPCFG1-2, GPEVR and GPMODE:

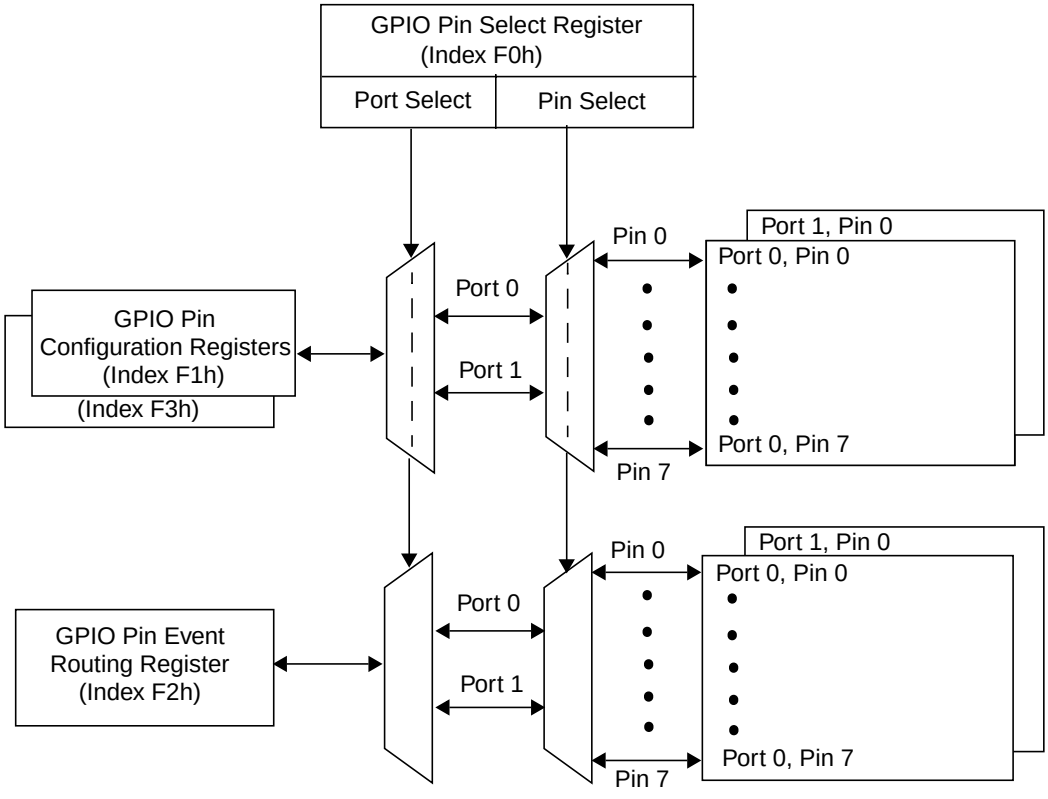


Figure 8. Organization of GPIO Pin Registers GPCFG1-2, GPEVR and GPMODE

3.0 Device Architecture and Configuration (Continued)

3.14.3 GPIO Pin Select Register (GPSEL)

This register selects the GPIO pin (port number and bit number) to be configured (i.e., which register is accessed via the GPIO pin configuration registers). GPSEL is reset to 00h.

Power Well: V_{SB3}

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**PORTSEL**		**Reserved**	**PINSEL**		
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-6	**Reserved.**
5-4	**PORTSEL (Port Select).** These bits select the GPIO port to be configured: 00: Port 0 (default) 01: Port 1 (all other values are reserved)
3	**Reserved.**
2-0	**PINSEL (Pin Select).** These bits select the GPIO pin of the selected port to be configured: 000: Pin 0 (default) 001-111: Binary value of pin numbers 1-7, respectively

3.14.4 GPIO Pin Configuration Register 1 (GPCFG1)

This register reflects, for both read and write, the register currently selected by the GPIO Pin Select register. All of the GPIO pin configuration registers have a common bit structure, as shown below. An exception to this is GPIO14 pin of Port 1, which lacks the EVDBNC, EVPOL and EVTYPE bits (the bits are reserved). All of the GPCFG1 registers are reset to 00h.

Power Well: V_{SB3}

Location: Index F1h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**EVDBNC[1]**	**EVPOL[1]**	**EVTYPE[1]**	**LOCKCFP**	**PUPCTL**	**OUTTYPE**	**OUTENA**
Reset	0	0	0	0	0	0	0	0

1. This bit is reserved for the GPIO14 pin in Port 1.

Bit	Type	Description
7	–	**Reserved.**
6	R/W or RO	**EVDBNC (Event Debounce Enable).** This bit enables the debounce circuit in the event input path of the selected GPIO pin. The event is detected after a predetermined debouncing period (see Section 5.3 on page 75). 0: Disabled (default) 1: Enabled
5	R/W or RO	**EVPOL (Event Polarity).** This bit defines the polarity of the wake-up signal that issues an event from the selected GPIO pin (see Section 5.3 on page 75). 0: Falling edge or low level input (default) 1: Rising edge or high level input

Bit	Type	Description
4	R/W or RO	**EVTYPE (Event Type).** This bit defines the type of the wake-up signal that issues an event from the selected GPIO pin (see Section 5.3 on page 75). 0: Edge input (default) 1: Level input
3	R/W1S	**LOCKCFP (Lock Configuration of Pin)**. When set to 1, this bit locks the GPIO pin configuration and data (see also Section 5.4 on page 77) by disabling writing to itself, to GPCFG1 register bits PUPCTL, OUTTYPE and OUTENA, to all of the bits of GPCFG2 register and to the corresponding bit in GPDO and GPDIO registers. Once set, this bit can be cleared by V_{DD3} Power-Up reset (or Hardware reset). 0: R/W bits are enabled for write (default) 1: All bits are RO
2	R/W or RO	**PUPCTL (Pull-Up Control**). This bit controls the internal pull-up resistor of the selected GPIO pin (see Section 5.2 on page 74). 0: Disabled (default) 1: Enabled
1	R/W or RO	**OUTTYPE (Output Type).** This bit controls the output buffer type of the selected GPIO pin (see Section 5.2 on page 74). 0: Open-drain (default) 1: Push-pull
0	R/W or RO	**OUTENA (Output Enable).** This bit controls the output buffer of the selected GPIO pin (see Section 5.2 on page 74). 0: TRI-STATE (default) 1: Output buffer enabled

3.14.5 GPIO Event Routing Register (GPEVR)

This register enables the routing of the GPIO event (see Section 5.3.2 on page 76) to an IRQ. An exception to this is GPIO14 pin of Port 1, which lacks the GPEVR register (the register is reserved). GPEVR is reset to 00h.

Power Well: V_{SB3}

Location: Index F2h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**							**EV2IRQ**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-1	**Reserved.**
0	**EV2IRQ (Event to IRQ Routing).** Controls the routing of the event from the selected GPIO pin to IRQ (see Section 5.3.2 on page 76). 0: Disabled (default) 1: Enabled

3.0 Device Architecture and Configuration (Continued)

3.14.6 GPIO Pin Configuration Register 2 (GPCFG2)

This register controls the connection of the GPIO pin to a V_{DD}-powered load. An exception to this is GPIO14 pin of Port 1, which lacks the GPCFG2 configuration register (the register is reserved and the pin is configured for V_{SB3}-powered load). GPCFG2 is reset to 00h.

Power Well: V_{SB3}
Location: Index F3h
Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**VDDLOAD**	**Reserved**			
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-5	**Reserved.**
4	**VDDLOAD (V_{DD3}-Powered Load).** This bit indicates that the selected GPIO pin is connected to a device powered by V_{DD3}. The input and output buffers (including the internal pull-up) of the selected GPIO pin are disabled whenever V_{DD3} power to the PC87373 device falls below a certain value (see Section 13.1.5 on page 152). 0: GPIO pin connected to a V_{SB3}-powered load (default): The configuration and data of the GPIO pin are reset by V_{SB} Power-Up reset (see Section 2.2 on page 29). 1: GPIO pin connected to a V_{DD3}-powered load: The configuration (excepting the VDDLOAD bit) and data of the GPIO pin are reset by V_{DD} Power-Up reset, Hardware reset or Software reset (see Section 2.2 on page 29).
3-0	**Reserved.**

3.14.7 GPIO Mode Select Register (GPMODE)

This register controls the operation mode of the GPIO runtime registers (see Section 5.1 on page 73). GPMODE is reset to 01h.

Power Well: V_{SB3}
Location: Index F8h
Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**							**SEPDIO**
Reset	0	0	0	0	0	0	0	1

Bit	Description
7-1	**Reserved.**
0	**SEPDIO (Separate Data I/O Select).** This bit selects the operation mode of the GPIO runtime registers by controlling the GPDO*n*, GPEVEN*n* and GPEVST*n* runtime registers to read-only (*n* is the Port number, 0 or 1). 0: Common Data I/O mode (GPDO*n*, GPEVEN*n* and GPEVST*n* registers are read-only, and data written to them is ignored) 1: Separate Data I/O mode (default)

3.0 Device Architecture and Configuration (Continued)

3.15 FAN SPEED CONTROL AND MONITOR (FSCM) CONFIGURATION

3.15.1 General Description

This module includes three Fan Speed Control units (see Section 7 on page 107) and three Fan Speed Monitor units (see Section 8 on page 110). The 21 runtime registers of the six functional blocks are arranged in the address space shown in Table 25. The base address is 32-byte aligned. Address bits 0–4 are used to indicate the register offset.

Table 25. Runtime Registers in FSCM Address Space

Offset	Mnemonic	Register Name	Function
00h	FMTHRL1	Fan Monitor 1 Threshold Low	Fan Speed Monitor 1
01h	FMTHRH1	Fan Monitor 1 Threshold High	
02h	FMSPRL1	Fan Monitor 1 Speed Low	
03h	FMSPRH1	Fan Monitor 1 Speed High	
04h	FMCSR1	Fan Monitor 1 Control & Status	
05h	FMTHRL2	Fan Monitor 2 Threshold Low	Fan Speed Monitor 2
06h	FMTHRH2	Fan Monitor 2 Threshold High	
07h	FMSPRL2	Fan Monitor 2 Speed Low	
08h	FMSPRH2	Fan Monitor 2 Speed High	
09h	FMCSR2	Fan Monitor 2 Control & Status	
0Ah	FMTHRL3	Fan Monitor 3 Threshold Low	Fan Speed Monitor 3
0Bh	FMTHRH3	Fan Monitor 3 Threshold High	
0Ch	FMSPRL3	Fan Monitor 3 Speed Low	
0Dh	FMSPRH3	Fan Monitor 3 Speed High	
0Eh	FMCSR3	Fan Monitor 3 Control & Status	
0Fh	Reserved		
10h	FCPSR1	Fan Control 1 Pre-Scale	Fan Speed Control 1
11h	FCDCR1	Fan Control 1 Duty Cycle	
12h	FCPSR2	Fan Control 2 Pre-Scale	Fan Speed Control 2
13h	FCDCR2	Fan Control 2 Duty Cycle	
14h	FCPSR3	Fan Control 3 Pre-Scale	Fan Speed Control 3
15h	FCDCR3	Fan Control 3 Duty Cycle	
16h-1Fh	Reserved		

3.15.2 Logical Device 9 (FSCM) Configuration

Table 26 lists the configuration registers that affect the Fan Speed Control and Monitor. Only the last registers (F0h and F1h) are described here. See Section 3.2.3 on page 36 for a detailed description of the other registers.

Table 26. FSCM Configuration Registers

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate. When bit 0 is cleared, the runtime registers of this logical device are not accessible (see Section 3.3.1 on page 40).[1]	R/W	V_{DD3}	00h
60h	FSCM Base Address MSB register	R/W	V_{DD3}	00h
61h	FSCM Base Address LSB register. Bits 4-0 (for A4-0) are read only, '00000'.	R/W	V_{DD3}	00h
70h	Interrupt Number and Wake-Up on IRQ Enable register	R/W	V_{DD3}	00h
71h	Interrupt Type. Bit 1 is read/write. Other bits are read only.	R/W	V_{DD3}	03h

3.0 Device Architecture and Configuration (Continued)

Table 26. FSCM Configuration Registers (Continued)

Index	Configuration Register or Action	Type	Power Well	Reset
74h	Report no DMA assignment	RO	V_{DD3}	04h
75h	Report no DMA assignment	RO	V_{DD3}	04h
F0h	Fan Speed Control and Monitor Configuration register 1 (FSCMCF1)	R/W	V_{DD3}	00h
F1h	Fan Speed Control and Monitor Configuration register 2 (FSCMCF2)	R/W	V_{DD3}	00h

1. The logical device runtime registers are maintained and all detection mechanisms are functional.

3.15.3 Fan Speed Control and Monitor Configuration Register 1 (FSCMCF1)

This register is reset to 00h.

Power Well: V_{DD3}

Location: Index F0h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**LOCKFCF**	**FANCTL_INV2**	**FANCTL_EN2**	**FANMON_EN2**	**FANCTL_INV1**	**FANCTL_EN1**	**FANMON_EN1**	**TRI-STATE Control**
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
7	R/W1S	**LOCKFCF (Lock Fan Speed Configuration).** When set to 1, this bit locks the bits of the FSCMCF1 and FSCMCF2 registers by disabling writing to them (including the LOCKFCF bit itself). Once set, this bit can be cleared by V_{DD3} Power-Up reset (or Hardware reset). 0: R/W bits are enabled for write (default) 1: All bits are RO
6	R/W or RO	**FANCTL_INV2 (Fan Control Output Invert 2).** When this bit is set to 1, the signal at the FANPWM2 control output is inverted (pin GPIOE4/FANPWM2). 0: Normal signal at FANPWM2 (default) 1: Inverted signal at FANPWM2
5	R/W or RO	**FANCTL_EN2 (Fan Control Enable 2).** When this bit is set to 1, the Fan Speed Controller 2 is enabled and a PWM signal is generated at the FANPWM2 control output (pin GPIOE4/FANPWM2). 0: Disabled (default) 1: Enabled
4	R/W or RO	**FANMON_EN2 (Fan Monitor Enable 2).** When this bit is set to 1, the Fan Speed Monitor 2 is enabled and the rate of pulses received at the FANTACH2 tachometer input is measured. 0: Disabled (default) 1: Enabled
3	R/W or RO	**FANCTL_INV1 (Fan Control Output Invert 1).** When this bit is set to 1, the signal at the FANPWM1 control output is inverted (pin GPIOE3/FANPWM1). 0: Normal signal at FANPWM1 (default) 1: Inverted signal at FANPWM1
2	R/W or RO	**FANCTL_EN1 (Fan Control Enable 1).** When this bit is set to 1, the Fan Speed Controller 1 is enabled and a PWM signal is generated at the FANPWM1 control output (pin GPIOE3/FANPWM1). 0: Disabled (default) 1: Enabled

Bit	Type	Description
1	R/W or RO	**FANMON_EN1 (Fan Monitor Enable 1).** When this bit is set to 1, the Fan Speed Monitor 1 is enabled and the rate of pulses received at the FANTACH1 tachometer input is measured. 0: Disabled (default) 1: Enabled
0	R/W or RO	**TRI-STATE Control.** When this bit is set to 1 and the logical device is inactive, the logical device output pins are in TRI-STATE (see Section 3.3.2 on page 41). 0: Normal outputs (default) 1: TRI-STATE outputs when the logical device is inactive

3.15.4 Fan Speed Control and Monitor Configuration Register 2 (FSCMCF2)

This register is reset by hardware to 00h.

Power Well: V_{DD3}

Location: Index F1h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**FANCTL_INV3**	**FANCTL_EN3**	**FANMON_EN3**	**Reserved**
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
7-4	-	**Reserved.**
3	R/W or RO	**FANCTL_INV3 (Fan Control Output Invert 3).** When this bit is set to 1, the signal at the FANPWM3 control output is inverted (pin GPIOE5/FANPWM3). 0: Normal signal at FANPWM3 (default) 1: Inverted signal at FANPWM3
2	R/W or RO	**FANCTL_EN3 (Fan Control Enable 3).** When this bit is set to 1, the Fan Speed Controller 3 is enabled and a PWM signal is generated at the FANPWM3 control output (pin GPIOE5/FANPWM3). 0: Disabled (default) 1: Enabled
1	R/W or RO	**FANMON_EN3 (Fan Monitor Enable 3).** When this bit is set to 1, the Fan Speed Monitor 3 is enabled and the rate of pulses, received at the FANTACH3 tachometer input, is measured. 0: Disabled (default) 1: Enabled
0	-	**Reserved.**

3.0 Device Architecture and Configuration (Continued)

3.16 GAME PORT (GMP) CONFIGURATION

3.16.1 Logical Device B (GMP) Configuration

Table 27 lists the configuration registers that affect the Game Port. Only the last register (F0h) is described here. See Section 3.2.3 on page 36 for descriptions of the other configuration registers. All of these registers are V_{DD3} powered.

Table 27. GMP Configuration Registers

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.3.1 on page 40)	R/W	V_{DD3}	00h
60h	Base Address MSB register	R/W	V_{DD3}	02h
61h	Base Address LSB register	R/W	V_{DD3}	01h
70h	Interrupt Number and Wake-Up on IRQ Enable register	RO	V_{DD3}	00h
71h	Interrupt Type	RO	V_{DD3}	03h
74h	Report no DMA Assignment	RO	V_{DD3}	04h
75h	Report no DMA Assignment	RO	V_{DD3}	04h
F0h	Game Port Configuration register	R/W	V_{DD3}	00h

3.16.2 Game Port Configuration Register

This register is reset by hardware to 00h.

Power Well: V_{DD3}

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**DBNC_EN**	**Reserved**	**INT_PU_EN**	**Reserved**	**TRI-STATE Control**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-5	**Reserved.**
4	**DBNC_EN (Debounce Enable).** When set to 1, this bit enables a 16 ms input debouncer on the Button 0 and Button 1 input pins of Device A and Device B (pins 3V_DDCSCL/GPIOE13/JYABT0, 5V_DDCSCL/GPIOE11/JYABT1, 3V_DDCSDA/GPIOE12/JYBBT0, 5V_DDCSDA/GPIOE10/JYBBT1). 0: Disabled (default) 1: Enabled
3	**Reserved.**
2	**INT_PU_EN (Internal Pull-Up Enable).** When the GMP functionality is selected, this bit controls the internal pull-up resistor on pins 3V_DDCSCL/GPIOE13/JYABT0, 5V_DDCSCL/GPIOE11/JYABT1, 3V_DDCSDA/GPIOE12/JYBBT0, 5V_DDCSDA/GPIOE10/JYBBT1. 0: Disabled (default) 1: Enabled
1	**Reserved.**
0	**TRI-STATE Control.** When the bit is set and the GMP is inactive, the GMP output pins are in TRI-STATE. 0: Disabled (default) 1: Enabled

3.0 Device Architecture and Configuration (Continued)

3.17 MUSICAL INSTRUMENT DIGITAL INTERFACE (MIDI) PORT CONFIGURATION

3.17.1 Logical Device C (MIDI) Configuration

Table 27 lists the configuration registers that affect the MIDI Port. Only the last register (F0h) is described here. See Section 3.2.3 on page 36 for descriptions of the other configuration registers. All of these registers are V_{DD3} powered.

Table 28. MIDI Configuration Registers

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.3.1 on page 40)	R/W	V_{DD3}	00h
60h	Base Address MSB register	R/W	V_{DD3}	03h
61h	Base Address LSB register. Bit 0 (for A0) is read only, 0b.	R/W	V_{DD3}	30h
70h	Interrupt Number and Wake-Up on IRQ Enable register	R/W	V_{DD3}	00h
71h	Interrupt Type. Bit 1 is R/W; other bits are read only	R/W	V_{DD3}	03h
74h	Report no DMA Assignment	RO	V_{DD3}	04h
75h	Report no DMA Assignment	RO	V_{DD3}	04h
F0h	MIDI Port Configuration register	R/W	V_{DD3}	00h

3.17.2 MIDI Port Configuration Register

This register is reset by hardware to 00h.

Power Well: V_{DD3}

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**					**INT_PU_EN**	**Reserved**	**TRI-STATE Control**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved.**
3	**Enhanced Mode Enable.** See Usage Hints below. 0: Disabled - Legacy mode (default) 1: Enabled - Enhanced mode
2	**INT_PU_EN (Internal Pull-Up Enable).** When the MIDI Port functionality is selected, this bit controls the internal pull-up resistor on pin SMB2_SDA/MDRX. 0: Disabled (default) 1: Enabled
1	**Reserved.**
0	**TRI-STATE Control.** When this bit is set and the MIDI is inactive, the MIDI output pins are in TRI-STATE. 0: Disabled (default) 1: Enabled

Usage Hints:

To use MIDI enhanced features, locate the MIDI base address within the LPC Wide Generic address range.

In Legacy mode, only the MIDI IN, MIDI OUT, MIDI Status and MIDI Command registers of the MIDI are user-accessible (see Section 11.3 on page 136).

In Enhanced mode, all the registers listed in the MIDI chapter are accessible (see Section 11.3 on page 136).

4.0 LPC Bus Interface

With the exception of the Glue Functions, the host can access all the functional blocks of the PC87373 device through the LPC bus.

4.1 OVERVIEW

The LPC host interface supports 8-bit I/O Read, 8-bit I/O Write and 8-bit DMA transactions, as defined in Intel's *LPC Interface Specification, Revision 1.0*.

4.2 LPC TRANSACTIONS

The LPC interface of the PC87373 device responds to the following LPC transactions:

- 8-bit I/O read and write cycles
- 8-bit DMA read and write cycles
- DMA request cycles

4.3 $\overline{\text{LPCPD}}$ FUNCTIONALITY

The PC87373 device supports $\overline{\text{LPCPD}}$ functionality. $\overline{\text{LPCPD}}$ is used when the V_{DD3} power supply is not shared by all the devices connected to the LPC bus. The $\overline{\text{LPCPD}}$ signal conforms with Intel's *LPC Interface Specification, Revision 1.00.* Note that if the PC87373 power supply is on while $\overline{\text{LPCPD}}$ is active (indicating the LPC bus is powered down), the PC87373 does not have to be reset when $\overline{\text{LPCPD}}$ is de-asserted (indicating that power is returned to the LPC bus).

When the $\overline{\text{LPCPD}}$ functionality is not required, the $\overline{\text{LPCPD}}$ pin must be left unconnected. Connecting the $\overline{\text{LPCPD}}$ pin to the V_{DD3} power supply is not recommended.

4.4 INTERRUPT SERIALIZER

The Interrupt Serializer translates parallel interrupt request (PIRQ) signals received from internal IRQ sources into serial interrupt request data transmitted over the SERIRQ bus. This enables devices that support only parallel IRQs to be integrated into a system that supports only serial IRQs like the LPC bus.

Each internal IRQ is fed into a Mapping, Enable and Polarity Control block, which maps the IRQ to its associated IRQ numbers (see Table 12 on page 37). The resulting IRQs are then fed into the Interrupt Serializer, where they are translated into serial data and then transmitted over the SERIRQ bus. Each interrupt number is assigned a time slot in the SERIRQ frame. Different IRQ sources in the PC87373 device cannot share the same interrupt number and thus cannot share the same time slot in the SERIRQ frame.

When a transition is detected on an IRQ source, the new value of the IRQ source is transmitted over the SERIRQ bus during the corresponding IRQ slot. For example, when a transition on the Serial Port IRQ is detected, the new value of the Serial Port IRQ is transmitted during time slot n of the SERIRQ bus.

5.0 General-Purpose Input/Output (GPIO) Ports

This chapter describes one 8-bit port. A device may include a combination of several ports with different implementations. For device specific implementation, see Section 3.14 on page 62.

5.1 OVERVIEW

The GPIO port is an 8-bit port, connected to eight pins. It features:

- Software capability to control and read pin levels.
- Flexible system notification by several means, based on the pin level or level transition.
- Ability to capture and route events and their associated status.
- Back-drive protected pins.

GPIO port operation is associated with two sets of registers:

- Pin Configuration registers mapped in the Device Configuration space. These registers are used to configure the logical behavior of each pin. There are three registers for each GPIO pin: GPIO Pin Configuration registers 1 and 2 (GPCFG1, GPCFG2) and the GPIO Pin Event Routing register (GPEVR).
- Four 8-bit runtime registers: GPIO Data Out (GPDO), GPIO Data In (GPDI), GPIO Event Enable (GPEVEN) and GPIO Event Status (GPEVST). These registers are mapped in the GPIO device I/O space (which is determined by the base address registers in the GPIO Device Configuration). They are used to control and/or read the pin values and to handle system notification. Each runtime register corresponds to the 8-pin port, such that bit 'n' in each one of the four registers is associated with GPIOXn pin, where 'X' is the port number.
- An additional optional runtime register: GPIO Data In/Out (GPDIO). This register is also mapped in the GPIO device I/O space, but at a separate location from the above group of four runtime registers. It contains the same data-out value as the GPDO register and the same data-in value as the GPDI register.

Each GPIO pin is associated with configuration bits and the corresponding bit slice of the four runtime registers, as shown in Figure 9.

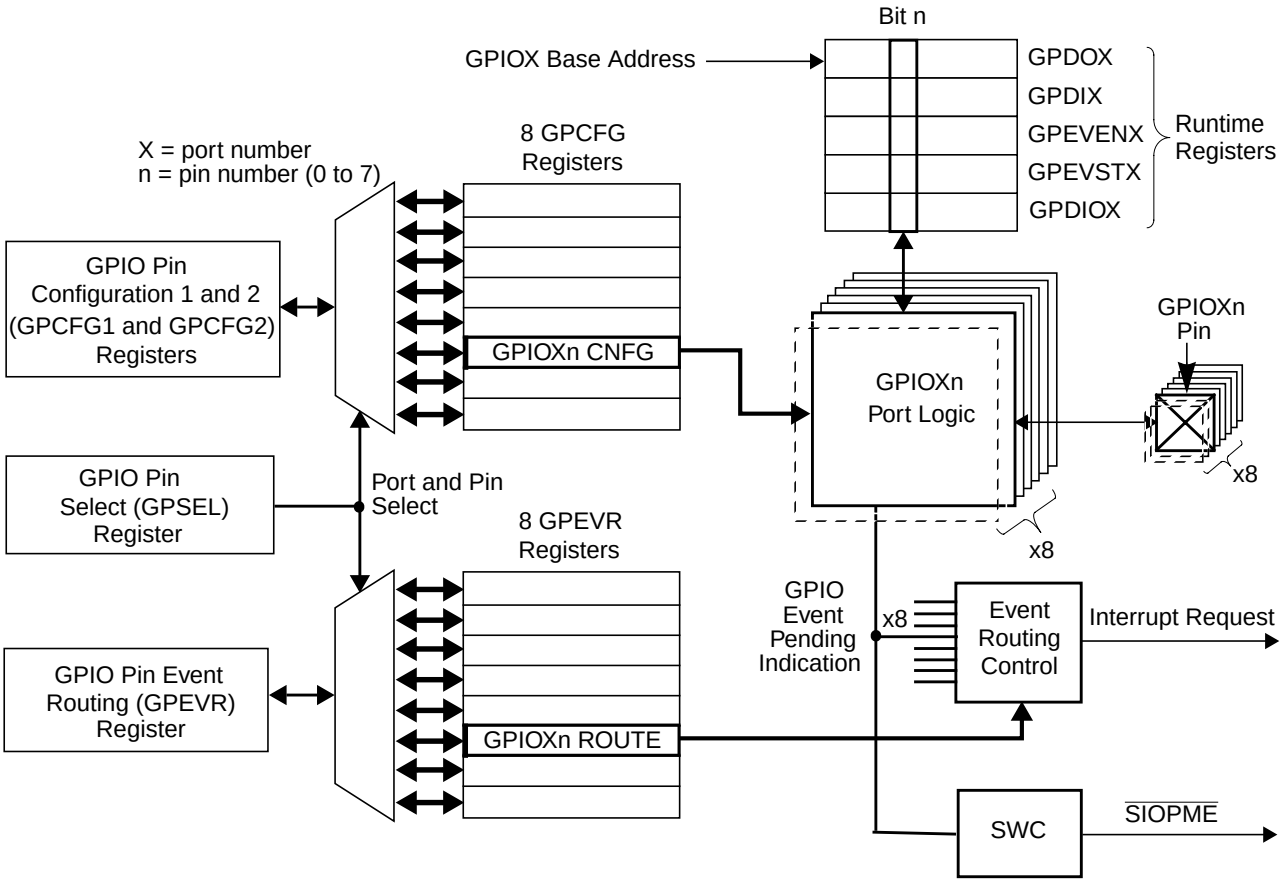


Figure 9. GPIO Port Architecture

5.0 General-Purpose Input/Output (GPIO) Ports (Continued)

The functionality of the GPIO port is divided into:

- Basic functionality: Includes configuration of, writing to and reading from the GPIO pins (described in Section 5.2)
- Enhanced functionality: Includes wake-up event detection and system notification (described in Section 5.3)

In addition, the GPIO port can be operated in one of the following modes:

- Separate Data I/O: Separate registers are available for Data In (GPDI) and for Data Out (GPDO) in addition to the Data In/Out register (GPDIO) and to the enhanced functionality registers (GPEVST and GPEVEN).
- Common Data I/O: Only the Data In/Out register (GPDIO) is available.

5.2 BASIC FUNCTIONALITY

The basic functionality of each GPIO pin is based on four configuration bits and a bit slice of runtime registers GPDO and GPDI (or GPDIO). The configuration and operation of a single pin GPIOXn (pin 'n' in port 'X') is shown in Figure 10.

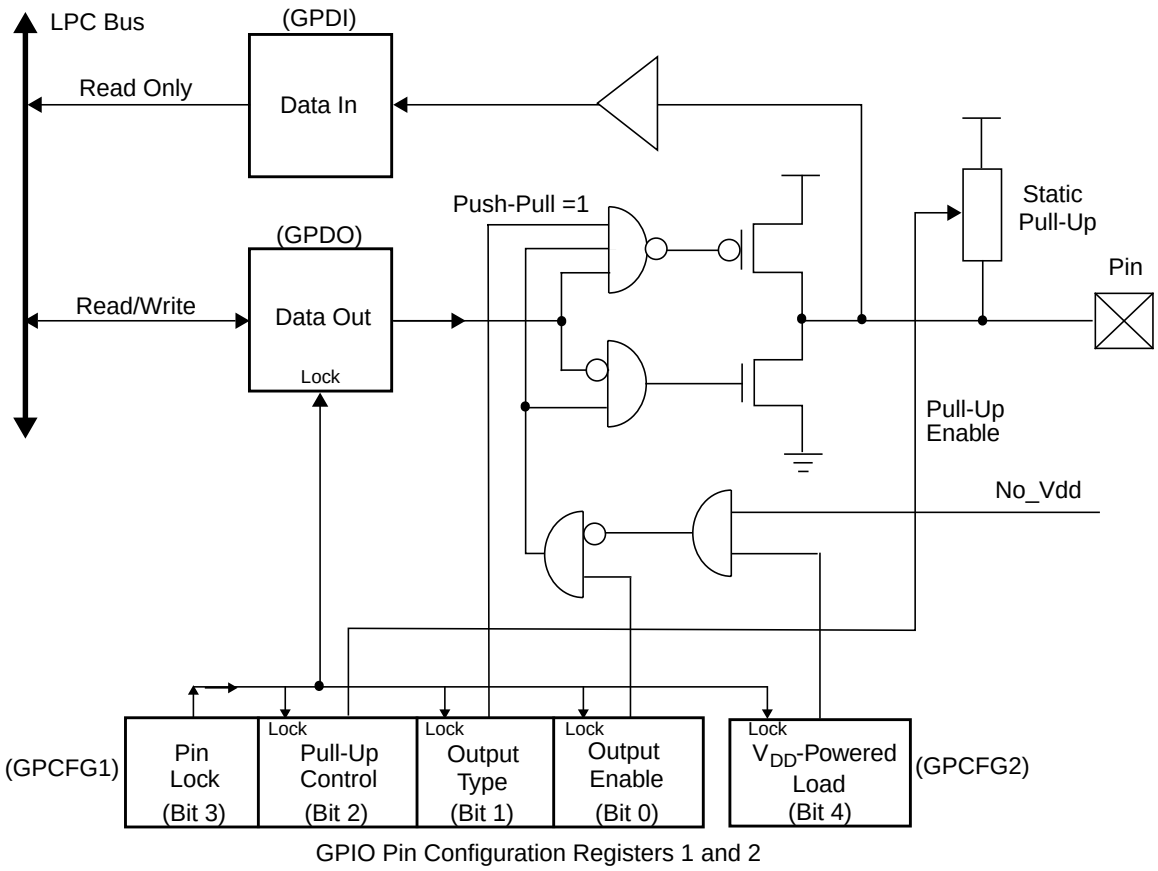


Figure 10. GPIO Basic Functionality

5.2.1 Configuration Options

The GPCFG1 register controls the following basic configuration options, as shown in Figure 10:

- Port Direction: Controlled by Output Enable (bit 0).
- Output Type: Push-pull vs. open-drain; it is controlled by Output Buffer Type (bit 1) by enabling/disabling the upper transistor of the output buffer.
- Static Pull-Up: May be added to any type of port (input, open-drain or push-pull). It is controlled by Pull-Up Control (bit 2).
- Pin Lock: GPIO pin may be locked to prevent any changes in the output value and/or the output configuration. The lock is controlled by bit 3. It disables writes to GPDO and GPDIO registers bits, to bits 3–0 of GPCFG1 register (including the Lock bit itself) and to bit 4 of GPCFG2 register.

5.0 General-Purpose Input/Output (GPIO) Ports (Continued)

The GPCFG2 register controls the Load Protection configuration option:

- V_{DD}-Powered Load: Disables the Output Buffer (if enabled), the Static Pull-Up (if enabled) and the Input Buffer if the specific GPIO pin is connected to a V_{DD}-powered device and V_{DD3} power to the PC87373 is not present (No_Vdd). This function is controlled by the V_{DD}-powered Load bit (bit 4).

5.2.2 Operation

If the output is enabled, the value that is written to the GPDO or GPDIO registers is driven to the pin. Reading from the GPDO register returns its contents regardless of the actual pin value or the port configuration.

The GPDI register is a read-only register. Reading from the GPDI register returns the actual pin value regardless of its source (the port itself or an external device). Writing to this register is ignored.

Reading from the GPDIO register returns the actual pin value regardless of its source.

Activation of the GPIO module is controlled by device-specific configuration bits. When this module is inactive, access through the LPC bus to the runtime registers (GPDI, GPDO and GPDIO) is disabled; however, there is no change in the GPDO and GPDIO values and therefore there is no effect on the outputs of the pins.

The configuration and data registers of each GPIO pin are reset according to the setting of VDDLOAD bit in GPCFG2 register (see Section 3.14.6 on page 66).

5.3 EVENT HANDLING AND SYSTEM NOTIFICATION

The enhanced GPIO port (GPIOE) supports system notification based on event detection. This functionality is based on configuration bits and a bit slice of runtime registers GPEVEN and GPEVST. The configuration and operation of the event detection capability is shown in Figure 11. System notification is described in Section 5.3.2.

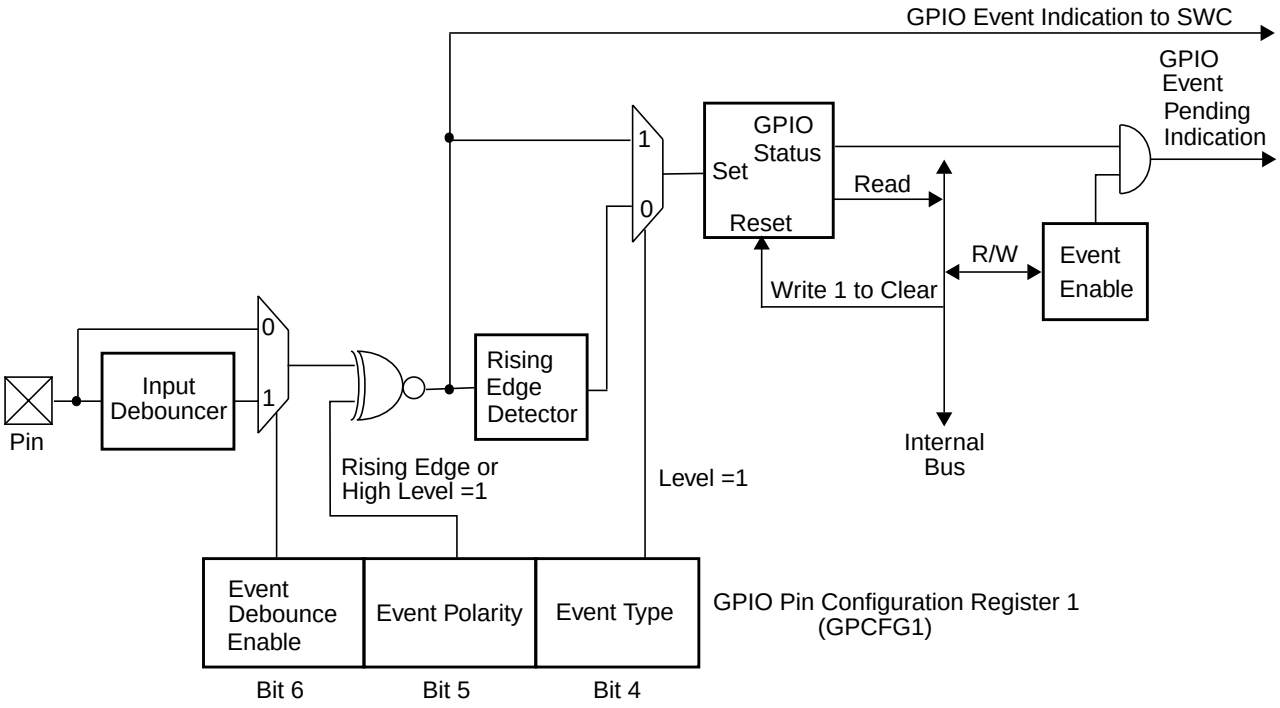


Figure 11. Event Detection

5.3.1 Event Configuration

Each pin in the GPIO port is a potential input event source. The event detection can trigger a system notification upon predetermined behavior of the source pin. The GPCFG1 register determines the event detection trigger type for system notification.

Event Debounce Enable

The input signal can be debounced for at least 16 ms, before entering the detector. To ensure that the signal is stable, the signal state is transferred to the event detector only after a debouncing period during which the signal has no transitions. The debouncer adds a delay equal to the debouncing period to both assertion and de-assertion of the event pending indicator (IRQ, SCI). The debounce is controlled by Event Debounce Enable (bit 6 of GPCFG1 register).

5.0 General-Purpose Input/Output (GPIO) Ports (Continued)

Event Type and Polarity

Two trigger types of event detection are supported: edge and level. An edge event may be detected on a source pin transition either from high to low or low to high. A level event may be detected when the source pin is either at high or low level. The trigger type is determined by Event Type (bit 4 of GPCFG1 register). The direction of the transition (for edge) or the polarity of the active level (for level) is determined by Event Polarity (bit 5 of GPCFG1 register).

Active edge refers to a change in a GPIO pin level that matches the Event Polarity bit (1 for rising edge and 0 for falling edge). *Active level* refers to the GPIO pin level that matches the Event Polarity bit (1 for high level and 0 for low level). The corresponding bit in GPEVST register is set by hardware whenever an active edge or an active level is detected regardless of the GPEVEN register setting. Writing 1 to the Status bit clears it to 0. Writing 0 is ignored.

A GPIO pin is in event pending state if an active event has occurred (the corresponding bit in GPEVST register is set) and the corresponding bit in GPEVEN register is set.

5.3.2 System Notification

System notification on GPIO-triggered events is achieved by asserting an interrupt request via the Interrupt Serializer in the LPC Bus Interface.

The system notification for each GPIO pin is controlled by the corresponding bit in GPEVEN register together with bit 0 of GPEVR register. System notification by a GPIO pin is enabled if the corresponding bit of GPEVEN register is set to 1. The event routing mechanism is shown in Figure 12.

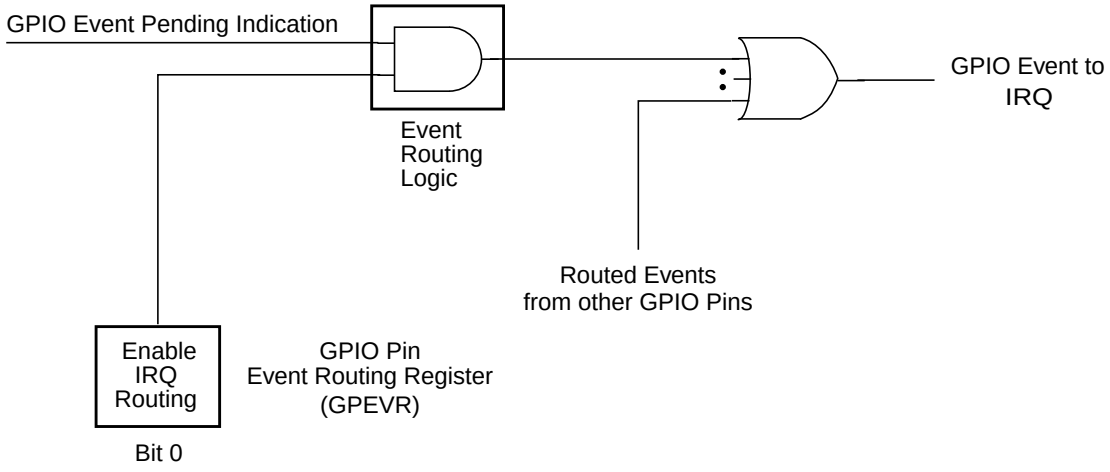


Figure 12. GPIO Event Routing Mechanism for System Notification

The system notification to the target is asserted if at least one GPIO pin is in event pending state.

The selection of the target (for system notification) is determined by the GPEVR register. The specific IRQ number is determined by the IRQ selection procedure of the device configuration. The assertion of IRQ (as a means of system notification) is disabled either when the GPIO functional block is deactivated or when V_{DD3} power is off.

System notification through IRQ or SCI (see Section 6.2.4 on page 84) can be initiated by software by writing to the Data Out bit (in GPDO or GPDIO register) of a GPIO pin. This is possible only if the output of the corresponding GPIO pin is enabled, pin multiplexing is selected for the GPIO function (see Section 1.3 on page 15) and the GPIO event is routed to IRQ or SCI. System notification is asserted according to the actual level at the GPIO pin driven by the GPIO output and/or by external circuitry. The level driven by the GPIO output should not cause a contention with the level driven by the external circuitry.

A pending edge event may be cleared by clearing the corresponding GPEVST bit. However, a level event source may not be released by software (except for disabling the source) as long as the pin is at active level. When level event is used, it is also recommended to disable the input debouncer.

Upon deactivation of the GPIO functional block and while V_{DD3} power is off, access through the LPC bus to the runtime registers (GPEVST and GPEVEN) is disabled. All means of system notification that include the target IRQ number are detached from the GPIO and de-asserted.

When V_{DD3} power is off, the status bits of the GPIO pins connected to a V_{DD}-powered device (VDDLOAD = 1) are cleared, however the status bits of the GPIO pins connected to a V_{SB}-powered device (VDDLOAD = 0) are not affected.

Before enabling any system notification, it is recommended to set the desired event configuration and then verify that the status registers are cleared.

5.0 General-Purpose Input/Output (GPIO) Ports (Continued)

5.4 GPIO PORT REGISTERS

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from register (data written to this address is sent to a different register).
- W = Write (see above).
- RO = Read Only.
- WO = Write Only. Reading from the bit returns 0.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

5.4.1 GPIO Pin Configuration Registers Structure

For each GPIO Port, there is a group of eight identical sets of configuration registers. Each set is associated with one GPIO pin. The entire group is mapped to the PnP configuration space. The mapping scheme is based on the GPSEL register (see Section 3.14.3 on page 64), which functions as an index register for the pin, and the selected GPCFG1, GPEVR and GPCFG2 registers, which reflect the configuration of the currently selected pin (see Table 29). All of these registers are V_{SB3} powered.

Table 29. GPIO Configuration Registers

Index	Configuration Register or Action	Type	Power Well	Reset
F0h	GPIO Pin Select register (GPSEL)	R/W	V_{SB3}	00h
F1h	GPIO Pin Configuration register 1 (GPCFG1)	Varies per bit	V_{SB3}	40h
F2h	GPIO Pin Event Routing register (GPEVR)	R/W or RO	V_{SB3}	01h
F3h	GPIO Pin Configuration register 2 (GPCFG2)	R/W or RO	V_{SB3}	00h
F8h	GPIO Mode Select register (GPMODE)	R/W or RO	V_{SB3}	01h

5.4.2 GPIO Port Runtime Register Map

All of these registers are V_{SB3} powered.

Table 30. GPIO Port Runtime Register Map

Offset	Mnemonic	Register Name	Type		Power Well	Reset	Section
			SEPDIO[1] = 1	SEPDIO = 0			
Device specific[2]	GPDO	GPIO Data Out	R/W	RO	V_{SB3}	FFh	5.4.3
Device specific[2]	GPDI	GPIO Data In	RO	RO	V_{SB3}	–	5.4.4
Device specific[2]	GPEVEN	GPIO Event Enable	R/W	RO	V_{SB3}	00h	5.4.5
Device specific[2]	GPEVST	GPIO Event Status	R/W1C	RO	V_{SB3}	00h	5.4.6
Device specific[2]	GPDIO	GPIO Data In/Out	R/W	R/W	V_{SB3}	FFh[3]	5.4.7

1. See Section 3.14.7 on page 66
2. The location of this register is defined in Section 3.14.1 on page 62.
3. The data read from this register after reset is undefined.

5.0 General-Purpose Input/Output (GPIO) Ports (Continued)

5.4.3 GPIO Data Out Register (GPDO)

Power Well: V_{SB3}

Location: Device specific

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**DATAOUT**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**DATAOUT (Data Out).** Bits 7-0 correspond to pins 7-0 of the specific Port. The value of each bit determines the value driven on the corresponding GPIO pin when its output buffer is enabled. Writing to the bit latches the written data unless the bit is locked by the GPCFG register Lock bit. Reading the bit returns its value regardless of the pin value and configuration. 0: Corresponding pin driven to low 1: Corresponding pin driven or released (according to buffer type selection) to high (default)

5.4.4 GPIO Data In Register (GPDI)

Power Well: V_{SB3}

Location: Device specific

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**DATAIN**							
Reset	X	X	X	X	X	X	X	X

Bit	Description
7-0	**DATAIN (Data In).** Bits 7-0 correspond to pins 7-0 of the specific Port. Reading each bit returns the value of the corresponding GPIO pin. Pin configuration and the GPDO register value may influence the pin value. Write is ignored. 0: Corresponding pin level low 1: Corresponding pin level high

5.0 General-Purpose Input/Output (GPIO) Ports (Continued)

5.4.5 GPIO Event Enable Register (GPEVEN)

Power Well: V_{SB3}

Location: Device specific

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**EVTENA**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**EVTENA (Event Enable).** Bits 7-0 correspond to pins 7-0 of the specific Port. Each bit enables system notification by the corresponding GPIO pin. The bit has no effect on the corresponding Status bit in GPEVST register. 0: Event pending by corresponding GPIO pin masked 1: Event pending by corresponding GPIO pin enabled

5.4.6 GPIO Event Status Register (GPEVST)

Power Well: V_{SB3}

Location: Device specific

Type: R/W1C or RO

Bit	7	6	5	4	3	2	1	0
Name	**EVTSTAT**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7–0	**EVTSTAT (Event Status).** Bits 7–0 correspond to pins 7–0 of the specific Port. The setting of each bit is independent of the Event Enable bit in GPEVEN register. An active event sets the Status bit, which may be cleared only by software writing 1 to the bit. 0: No active edge or level detected since last cleared 1: Active edge or level detected

5.4.7 GPIO Data In/Out Register (GPDIO)

Power Well: V_{SB3}

Location: Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**DATAINOUT**							
Reset Write	1	1	1	1	1	1	1	1
Reset Read	X	X	X	X	X	X	X	X

Bit	Description
7-0	**DATAINOUT (Data In/Out).** Bits 7-0 correspond to pins 7-0 of the specific Port. The value of each bit determines the value driven on the corresponding GPIO pin when its output buffer is enabled. Writing to the bit latches the written data unless the bit is locked by the GPCFG register Lock bit. Reading each bit returns the value of the corresponding GPIO pin. Pin configuration and the data-out value may influence the pin value. 0: Corresponding pin driven to low; pin level read low. 1: Corresponding pin driven or released (according to buffer type selection) to high; pin level read high (default).

6.0 System Wake-Up Control (SWC)

6.1 OVERVIEW

The System Wake-Up Control (SWC) supports the *ACPI Specification, Revision 2.0, Feb. 2, 1999.*

The SWC functional block receives external events from the system; it also receives internal events from the functional blocks of the PC87373 device. Based on these events, the SWC generates the Power Management SCI interrupt ($\overline{\text{SIOPME}}$) and the system interrupt (IRQ). In addition, it controls two LED indicators.

The SWC receives the following external events:

- 12 V_{SB}-powered General-Purpose Input/Output events (GPIOE13-10 and GPIOE07-00).
- Modem Ring events ($\overline{\text{RI1}}$ and $\overline{\text{RI2}}$).
- Mouse movement and button pressing events (via MCLK and MDAT).
- Advanced key pressing events from the Keyboard (via KBCLK and KBDAT).

The SWC receives the following internal events:

- Keyboard and Mouse interrupt event (IRQ).
- Module interrupt (IRQ) event from the Fan Speed Monitor or the Legacy functional blocks (FDC, Parallel Port, Serial Ports 1 and 2, and MIDI Port).

The SWC implements the ACPI generic register group (General-Purpose Event 1 group) with “child” events.

The SWC generates the Power Management Event signal (the ACPI interrupt, $\overline{\text{SIOPME}}$) and the system interrupt (IRQ) based on the external and internal events and on the routing information written into the General-Purpose Event 1 register group. The ACPI-compatible SCI interrupt ($\overline{\text{SIOPME}}$) and the system interrupt (IRQ) are independent of the current sleep state.

The SWC receives sleep state information via the $\overline{\text{SLP\_S3}}$ and $\overline{\text{SLP\_S5}}$ pins from an external ACPI controller and receives power supply status information via PWRGD_PS pin from the system power supply.

In addition, the SWC controls two LED indicators. The Standard LED Control option is used to provide blinking or constantly lit LEDs. The Advanced LED Control option provides programmable blink based on the current sleep state information or on the status of the V_{SB3} and V_{DD3} power supplies. The Special LED Control option provides blinking or constantly lit LEDs, based on the current sleep state information or on the status of the Main Power Supply and on a software controlled bit.

The SWC includes the Last Power State Special Power Management function. This function saves the system power state when an AC power failure occurs.

The SWC module is powered by the V_{SB3} and V_{BAT} planes (see Section 2.1.1 on page 27). However, during Power Fail state (i.e., when only V_{BAT} is present), the module functions (event detection, output generation and LEDs control) are disabled and only the V_{BAT}-powered, Last Power State function is active.

Figure 13 shows the simplified block diagram of the SWC functional block.

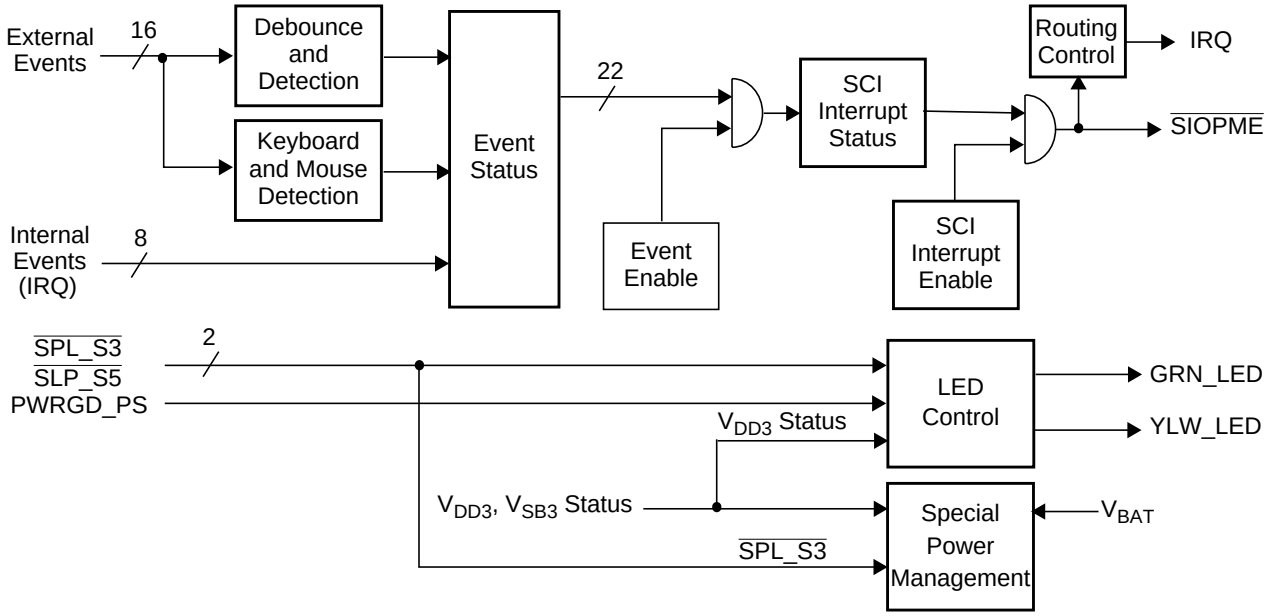


Figure 13. SWC Block Diagram

6.0 System Wake-Up Control (SWC) (Continued)

6.2 FUNCTIONAL DESCRIPTION

6.2.1 External Events

General-Purpose Input/Output Events

The PC87373 device supports 12 V_{SB3}-powered General-Purpose Input/Output events through ports GPIOE00-07 and GPIOE10-13. V_{DD3}- and V_{SB3}-powered signals can be connected to the GPIO pins to become sources of external events. A V_{DD3}-powered signal, when used to generate an event, is internally disabled for event generation while V_{DD3} power is off. It is also disabled for event generation for t_{EWIV} after V_{DD3} power is restored (see *Wake-Up Inputs at VDD3 Power Switching* on page 173), which prevents the detection of false events during power transitions and while the signal driver is unpowered. For the same reasons, a V_{SB3}-powered signal used to generate an event is enabled only t_{EWIV} after V_{SB3} power is on. (When V_{SB3} is off, the whole SWC module is disabled.)

Each GPIOE pin has both programmable polarity and an optional debouncer (see Figure 14). The debouncer is enabled after the reset but can be disabled by software. The debouncing time is longer than 16 ms.

A GPIO event can generate the system interrupt (IRQ) if the event is both enabled and routed to IRQ. The status, event enable and pending event routing bits to IRQ are implemented in the GPIO Port module (see Section 5.3 on page 75). The status bit is set when an event of the programed type (edge or level) is detected.

A GPIO event can also generate the Power Management SCI interrupt ($\overline{\text{SIOPME}}$). The status and event enable bits are implemented in the SWC module (see Figures 14 and 15).

An active level-type event sets the status bit in registers GPE1_STS_0 for ports GPIOE07-00 and GPE1_STS_1 for ports GPIOE13-10 (see Sections 6.4.4 and 6.4.5 on page 99). The status bit remains set even after the event becomes inactive. The status bit is cleared only when the software writes 1 to the bit. If the event is still active when software writes 1, the status bit remains set.

After changing the GPIOE1x pin multiplexing, clear the relevant bits in the GPE1_STS_1 register, to prevent false events (caused by the pin multiplexing switch) from generating a wake-up event.

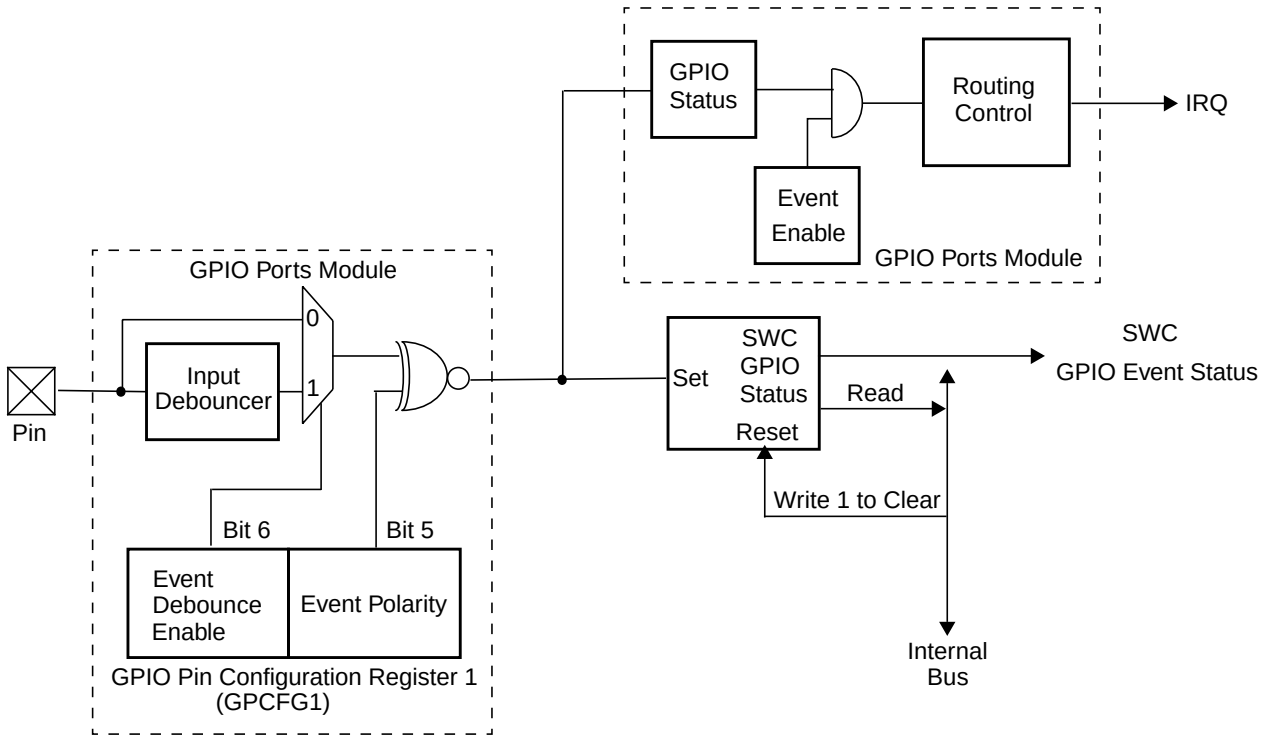


Figure 14. GPIO Events

6.0 System Wake-Up Control (SWC) (Continued)

Modem Ring Events

High-to-low transitions on $\overline{RI1}$ or $\overline{RI2}$ indicate the detection of a ring signal by an external modem connected to the Serial Port 1 or Serial Port 2, respectively. The transitions on $\overline{RI1}$ and $\overline{RI2}$ are detected by the RI Wake-Up Detector powered by V_{SB3}, which works independently of the Serial Port 1 or Serial Port 2 modules (powered by V_{DD3}).

A detected $\overline{RI1}$ or $\overline{RI2}$ transition sets the RI1_EVT_STS or RI2_EVT_STS status bit in GPE1_STS_2 register (see Section 6.4.6 on page 100). The status bit is cleared only when the software writes 1 to it.

The transition detection from $\overline{RI1}$ and $\overline{RI2}$ is enabled (for event generation) t_{EWIV} after V_{SB3} power is on (see *Wake-Up Inputs at VSB3 Power Switching* on page 173). This prevents the detection of false events during V_{SB3} power-On transitions.

Mouse Wake-Up Event

A mouse wake-up event is detected by the Keyboard/Mouse Wake-Up Detector, which monitors the MCLK and MDAT signals. Since the detection mechanisms for keyboard and mouse events are independent, they can be operated simultaneously. Moreover, the Keyboard signals may be swapped with the Mouse signals by setting SWAP bit in KBC Configuration register (see Section 3.13.3 on page 61). The Keyboard/Mouse Wake-Up Detector is powered by V_{SB3} and works independently of the Keyboard Controller module (powered by V_{DD3}).

The mouse event detection mechanism can be programed to detect either a mouse click or movement, a specific mouse click (left or right) or a double-click. To program which mouse action causes an event detection, set MSEVCFG field in PS2CTL register to the required value (see Section 6.3.8 on page 95).

A detected mouse event sets the MS_EVT_STS status bit in GPE1_STS_2 register (see Section 6.4.6 on page 100). The status bit is cleared only when the software writes 1 to it.

Mouse event detection from MCLK and MDAT is enabled (for event generation) t_{EWIV} after V_{SB3} power is on (see *Wake-Up Inputs at VSB3 Power Switching* on page 173). This prevents the detection of false Mouse events during V_{SB3} power-On transitions.

Keyboard Wake-Up Events

Keyboard wake-up events are also detected by the Keyboard/Mouse Wake-Up Detector, which monitors the KBCLK and KBDAT signals. Since the detection mechanisms for keyboard and mouse events are independent, they can be operated simultaneously. Moreover, the Keyboard signals may be swapped with the Mouse signals, by setting SWAP bit in KBC Configuration register (see Section 3.13.3 on page 61). The Keyboard/Mouse Wake-Up Detector is powered by V_{SB3} and works independently of the Keyboard Controller module (powered by V_{DD3}).

The keyboard event detection mechanism can be programed to detect:

- Any keystroke (Fast Any-Key or Special Key Sequence modes).
- A specific programmable sequence of up to eight alphanumeric keystrokes (Password mode).
- Any programmable sequence of up to eight bytes of data received from the keyboard (Special Key Sequence mode).
- Up to three programmable Power Management keys concurrently available, each including a sequence of up to three bytes of data received from the keyboard (Power Management Keys mode).

The Keyboard/Mouse Wake-Up Detector has four operation modes:

- Fast Any-Key mode
- Password mode
- Special Key Sequence mode
- Power Management Keys mode

Up to eight Keyboard Data registers (PS2KEY0-7) are used to define which keyboard data string generates an event. Since the same set of registers is used by three of the four operation modes, only one mode can be selected at a time.

For modes involving more than one keystroke, the maximum delay allowed between pressing two consecutive keys is 4 seconds. A longer delay is interpreted by the Wake-Up Detector as the beginning of a new sequence of keystrokes, which causes the present sequence to be discarded. In all operation modes, pressing a wrong key requires a recovery time of 4 seconds, before a new (correct) sequence may be recognized.

Fast Any-Key Mode. In this mode, pressing any key on the keyboard is identified as a keyboard event and, as a result, KBD_ANYK_STS bit in GPE1_STS_2 register is set (see Section 6.4.6 on page 100). The status bit is cleared only when the software writes 1 to it. The key data contained in the PS2KEY0-7 registers is ignored. To program the Keyboard/Mouse Wake-Up Detector to operate in Fast Any-Key mode, set KBDMODE field in KBDWKCTL register to '01' (see Section 6.3.7 on page 94).

6.0 System Wake-Up Control (SWC) (Continued)

Password Mode. In this mode, the "Break" bytes transmitted by the keyboard are discarded, and only the "Make" keystroke bytes are compared with those programed in the PS2KEY0-7 registers. If the two sets are identical, a keyboard event that sets KBD_EVT1_STS bit in GPE1_STS_2 register is detected (see Section 6.4.6 on page 100). The status bit is cleared only when the software writes 1 to it. Only keys with a "Make" keystroke data of one byte can be included in the sequence to be detected. To program the Keyboard/Mouse Wake-Up Detector to operate in Password mode:

1. Set KBDMODE field in KBDWKCTL register to '00' (see Section 6.3.7 on page 94).
2. Set KBEVCFG field in PS2CTL register to a value that indicates the desired number of alphanumeric keystrokes in the sequence. The programed value = the number of keystrokes + 7. For example, to detect a sequence of two keys, set KBEVCFG to 09h.
3. Program the appropriate subset of the PS2KEY0-7 registers, in sequential order, with the "Make" data bytes of the keys in the sequence. For example, if there are three keys in the sequence and the "Make" keystroke data of these keys are 05h (first), 50h (second) and 44h (third), program PS2KEY0 to 05h, PS2KEY1 to 50h and PS2KEY2 to 44h (the scan codes are only examples).

Special Key Sequence Mode. In this mode, all the bytes transmitted by the keyboard (including "Make" and "Break" bytes) are compared with those programed in the PS2KEY0-7 registers. If the two sets are identical, a keyboard event is detected, as explained in *Password Mode*, above. Special Key Sequence mode enables the detection of any sequence of keystrokes, including "Shift", "Alt" and "Ctl" keys. To program the Keyboard/Mouse Wake-Up Detector to operate in Special Key Sequence mode:

1. Set KBDMODE field in KBDWKCTL register to '00' (see Section 6.3.7 on page 94).
2. Set KBEVCFG field in PS2CTL register to a value that indicates the total number of bytes ("Make" and "Break") in the sequence, minus 1 (i.e., the programed value = the number of bytes - 1). For example, to detect a sequence of three received bytes (i.e., one keystroke), set KBEVCFG to 02h. The minimum value of the KBEVCFG field is 1 (i.e., two bytes).
3. Program the appropriate subset of the PS2KEY0-7 registers, in sequential order, with the data bytes that comprise the sequence. For example, if the number of bytes in the sequence is four, and the values of these bytes are E0h (first), 5Bh (second), E0h (third) and DBh (fourth), program PS2KEY0 to E0h, PS2KEY1 to 5Bh, PS2KEY2 to E0h and PS2KEY3 to DBh (the byte values are only examples).

Special Key Sequence mode also enables detection of any single keystroke. To program the Keyboard/Mouse Wake-Up Detector to wake-up on any single keystroke:

1. Set KBDMODE field in KBDWKCTL register to '00' (see Section 6.3.7 on page 94).
2. Set KBEVCFG field in PS2CTL register to '0001'.
3. Program the PS2KEY0 and PS2KEY1 registers to 00h. This forces the detector to ignore the values of incoming data, thus causing it to detect a keyboard event caused by a single keystroke.

Power Management Mode. In this mode, the PS2KEY0-7 register bank is divided into three groups of registers: PS2KEY0-2, PS2KEY3-5 and PS2KEY6-7. Each group can be programed with different data bytes, allowing the bytes transmitted by the keyboard to be compared simultaneously with three keystroke sequences. If the bytes transmitted by the keyboard (including Make and Break) are identical to the data bytes in one register group, the related keyboard event is detected. The detection of Keyboard Event 1 (data in PS2KEY0-2) sets KBD_EVT1_STS bit; the detection of Keyboard Event 2 (data in PS2KEY3-5) sets KBD_EVT2_STS bit; the detection of Keyboard Event 3 (data in PS2KEY6-7) sets KBD_EVT3_STS bit. All three status bits are in GPE1_STS_2 register (see Section 6.4.6 on page 100). Each status bit is cleared only when the software writes 1 to the bit. This mode enables the detection of any sequence of keys.

To program the Keyboard/Mouse Wake-Up Detector to operate in Power Management Keys mode, proceed as follows:

1. Set KBDMODE field in KBDWKCTL register to '10' (see Section 6.3.7 on page 94).
2. Set each event configuration field (EVT1CFG, EVT2CFG and EVT3CFG) in KBDWKCTL register to a value that indicates the desired number of keystroke data bytes ("Make" and "Break" bytes) in the sequence, for each event. For example, to detect a sequence of two received bytes, set EVTxCFG to 02h.
3. Program each group of the PS2KEY0-7 registers, in sequential order, with the data bytes of the keys in the sequence for each event.

Event Generation. Keyboard event detection from KBCLK and KBDAT is enabled, for event generation, t_{EWIV} after V_{SB3} power is on (see *Wake-Up Inputs at VSB3 Power Switching* on page 173). This prevents the detection of false Keyboard events during V_{SB3} power-On transitions.

Usage Hints:

1. After changing the operation mode of the Keyboard/Mouse Wake-Up Detector, clear the KBD_EVT3_STS, KBD_EVT2_STS, KBD_EVT1_STS, and KBD_ANYK_STS status bits in GPE1_STS_2 register (see Section 6.4.6 on page 100).
2. If a byte sequence that is a "subset" of the byte sequence of another ("superset") Power Management key event is used, the "superset" Power Management key event will never be detected. (The subset sequence has fewer bytes, set by EVTxCFG fields in KBDWKCTL register, than the superset sequence; however, the bytes contained in the subset sequence, as programed in the PS2KEY0-7 registers, are identical to the respective bytes of the superset sequence.)

6.0 System Wake-Up Control (SWC) (Continued)

6.2.2 Internal Events

Keyboard and Mouse IRQ Events

Keyboard and Mouse IRQ events are detected when either the Keyboard IRQ or Mouse IRQ is asserted.

To enable the IRQ of a logical device to generate an IRQ event, the associated Enable bit (bit 4 of the configuration register at index 70h; see Section 3.2.3 on page 36) must be set to 1. Since the Keyboard Controller (KBC) functional block is powered by V_{DD3}, a Keyboard or Mouse IRQ event can occur only when V_{DD3} is present.

An active (level-type) Keyboard IRQ event sets KBD_IRQ_STS status bit; an active Mouse IRQ event sets MS_IRQ_STS status bit. Both status bits are in GPE1_STS_3 register (see Section 6.4.7 on page 101). A status bit is cleared only when the software writes 1 to it. If the IRQ event is active when software writes 1 to the status bit, the status bit remains set.

The ROM code used for the Keyboard Controller generates active high Keyboard and Mouse interrupts, which are used by the SWC module.

Module IRQ Event

A Module IRQ event is detected when one of the Legacy modules (FDC, Parallel Port, Serial Ports 1 and 2, and MIDI Port) or the Fan Speed Control and Monitor, asserts its IRQ.

To enable the IRQ of a logical device to generate an IRQ event, the associated Enable bit (bit 4 of the configuration register at index 70h; see Section 3.2.3 on page 36) must be set to 1. Since the Legacy modules and the Fan Speed Monitor are powered by V_{DD3}, they can assert IRQ only when V_{DD3} is present.

MOD_IRQ_STS status bit in GPE1_STS_3 register is set by an IRQ that is asserted by one of the Legacy modules or the Fan Speed Monitor (see Section 6.4.7 on page 101). The status bit is cleared only when the software writes 1 to it. If the Module IRQ event is active when software writes 1 to the status bit, the status bit remains set.

6.2.3 Sleep States

The PC87373 identifies the current system sleep state, by decoding the levels of the $\overline{\text{SLP\_S3}}$ and $\overline{\text{SLP\_S5}}$ pins. The levels of these pins are generated by the system ACPI controller located in an external device. Table 31 shows the decoding of the logic levels of the $\overline{\text{SLP\_S3}}$ and $\overline{\text{SLP\_S5}}$ pins.

Table 31. $\overline{\text{SLP\_S3}}$, $\overline{\text{SLP\_S5}}$ Decoding

$\overline{\text{SLP\_S3}}$	$\overline{\text{SLP\_S5}}$	System Sleep State
1	1	S0, S1 or S2
0	1	S3
0	0	S5
1	0	Illegal combination

6.2.4 SCI and IRQ Interrupts

The SCI ($\overline{\text{SIOPME}}$) pin is the Power Management interrupt defined by ACPI.

All external and internal events are exclusively processed by the SWC to generate the Power Management interrupt, SCI. Each active event sets a status bit in GPE1_STS_0 to GPE1_STS_3 registers (see Sections 6.4.4 to 6.4.7 on page 99).

For each status bit, the SWC holds an enable bit in GPE1_EN_0 to GPE1_EN_3 registers. A set status bit can set PME_STS bit in GPE1_STS register (see Section 6.4.2 on page 98) only when its related enable bit is set. A set PME_STS bit can cause the assertion of the SCI interrupt only when PME_EN bit in GPE1_EN register is set (see Section 6.4.3 on page 98).

The SCI interrupt is independent of the system sleep state.

The $\overline{\text{SIOPME}}$ signal can be inverted to generate an active high SCI interrupt. In addition, the output buffer of the $\overline{\text{SIOPME}}$ pin can be configured as either push-pull or open-drain, to allow sharing with external SCI interrupt sources.

Figure 15 shows SCI generation.

6.0 System Wake-Up Control (SWC) (Continued)

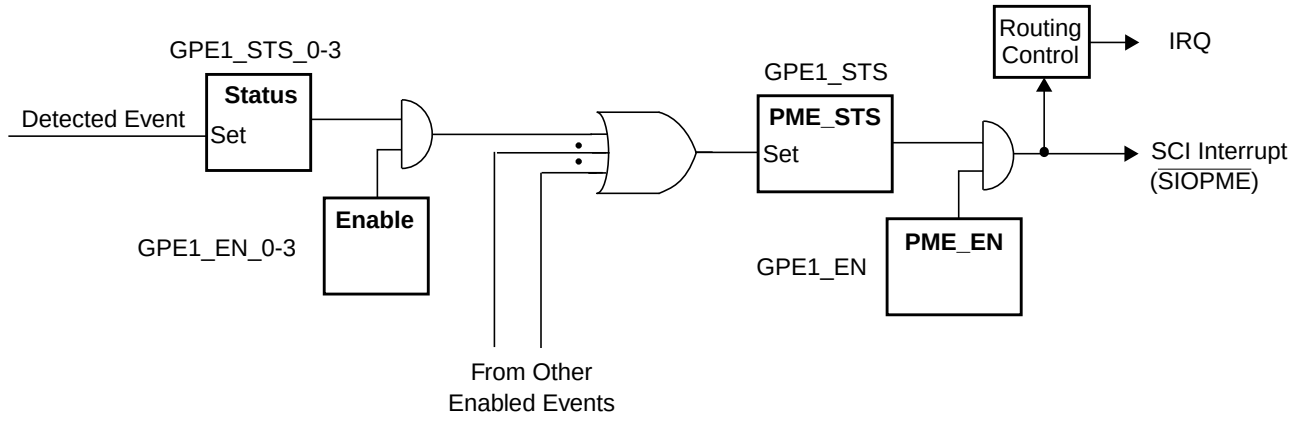


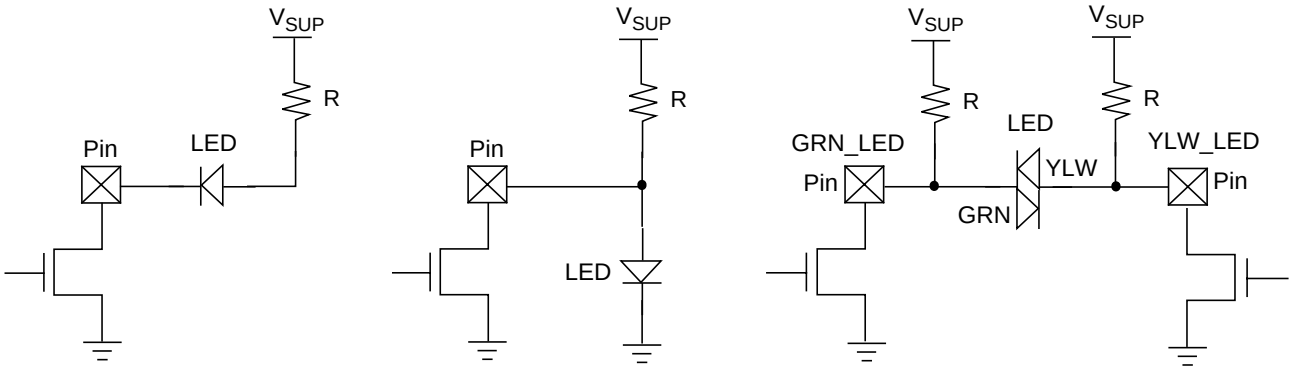
Figure 15. SCI Generation

The SCI interrupt ($\overline{\text{SIOPME}}$) is routed to the system interrupt (IRQ) by setting the Interrupt Number value, in the Interrupt Number register, located at index 70h in the SWC Configuration (see Section 3.12.2 on page 59).

6.2.5 LED Control

The PC87373 device controls the operation of two LED indicators. The two open-drain buffers allow the connection of either two regular LEDs or one dual-color LED.

The LEDs can be connected to PC87373 using one of the configurations shown in Figure 16.



a. Active Low **b. Active High** **c. Dual-Color**

Figure 16. LED Connection Configurations

The LED pins are named GRN_LED (Green LED) and YLW_LED (Yellow LED), although other LED colors can be used.

The PC87373 allows three LED control options, which are selected by LED_OPT field in SWC_CTL register (see Section 6.3.3 on page 90):

- Standard LED control: On/Off and Blink controlled by software or by S5 sleep state
- Advanced LED control: On/Off and Blink controlled by software, by S3 or S5 sleep states, or by the V_{DD3} power supply status
- Special LED control: On/Off and Blink controlled by software, by S3 or S5 sleep states or by the Main power supply status via the PWRGD_PS signal

From the base address of the SWC registers, the register for Standard LED Control is located at offset 00h, the two registers for Advanced LED Control are located at offsets 02h and 03h, and the register for Special LED Control is located at offset 02h (see Section 6.3.1 on page 88). The active control registers are selected by LED_OPT field.

The blink rate and duty cycle of all LED control options are based on a clock, which is obtained by dividing the frequency of the 32 KHz clock domain.

6.0 System Wake-Up Control (SWC) (Continued)

Standard LED Control

The Standard LED control is the default LED control option when V_{BAT} pin is connected to ground (V_{SS}). Two regular LEDs must be connected to the GRN_LED and the YLW_LED pins, according to configuration “b” (Active High) in Figure 16.

In this option, LED operation is controlled by the bits of SLEDCTL register (at offset 00h; see Section 6.3.2 on page 89) and by the $\overline{SLP\_S5}$ pin. When the system is in sleep state S5 ($\overline{SLP\_S5}$ = 0), both LEDs are off. GRN_YLW bit selects the active LED (on or blinking) of the two; the other LED is off. BLINK bit selects the operation mode of the active LED as either constantly on or blinking at 0.667 Hz with a duty cycle of 41.7% (on time percent of the blink cycle).

Table 34 on page 89 shows the states of the GRN_LED and YLW_LED pins. The LEDs are connected according to configuration “b” (see Figure 16); therefore, a LED is on when the pin is TRI-STATEd and off when the pin is at low level (0).

Advanced LED Control

In the Advanced LED control option, one dual-color LED or two regular LEDs can be connected to the GRN_LED and the YLW_LED pins, using any of the configurations shown in Figure 16. LEDCFG and LEDPOL bits in ALEDCTL register (at offset 02h; see Section 6.3.4 on page 91) must be set to reflect the connection configuration of the LEDs.

LEDCFG bit selects either configurations “a” and “b” (two regular LEDs are connected between each pin and ground or V_{SUPP}) or configuration “c” (one dual-color LED is connected between the GRN_LED and YLW_LED pins). LEDPOL bit selects the polarity of the On state at both pins (GRN_LED and YLW_LED). Table 32, shows the value of LEDCFG and LEDPOL bits for each LED connection configuration in Figure 16, and also the state of the GRN_LED and YLW_LED pins for which the LED(s) are On.

Table 32. LEDs “On” Polarity as a Function of LEDCFG and LEDPOL

LEDCFG	LEDPOL	GRN_LED	YLW_LED	Connection (See Figure 16)
0	0	TRI-STATE	0	“c”, Green anode to GRN_LED pin
0	1	0	TRI-STATE	“c”, Yellow anode to GRN_LED pin
1	0	TRI-STATE	TRI-STATE	“b”
1	1	0	0	“a”

The LEDMOD field controls the operation mode of GRN_LED and YLW_LED pins in each system power state (see Table 35 on page 91). The system power state is identified either by the status of the V_{DD3} power supply or by the current system sleep state:

- ‘00’ – The behavior of the GRN_LED and YLW_LED pins is controlled solely by software by the setting of the GRNBLNK and YLWBLNK fields.
- ‘01’ – The behavior of the GRN_LED and YLW_LED pins is controlled by the status of the V_{DD3} supply and by software.
  In the Power Off state (V_{DD3} off), the GRN_LED behaves according to the setting of the GRNBLNK field, but the YLW_LED blinks at a 1 Hz rate with a 50% duty cycle;
  In the Power On state (V_{DD3} on), each LED behaves according to the setting of its xxxBLNK field.
- ‘10’ – The behavior of the GRN_LED and YLW_LED pins is controlled by the S5 sleep state and by software.
  In S5 sleep state, both LEDs are off;
  In S3 - S0 sleep states, each LED behaves according to the setting of its xxxBLNK field.
- ‘11’ – The behavior of the GRN_LED and YLW_LED pins is controlled by the status of the V_{DD3} supply and by software.
  In the Power Off state (V_{DD3} off), both LEDs are off;
  In Power On state (V_{DD3} on), each LED behaves according to the setting of its xxxBLNK field.

The status of the V_{DD3} power supply is detected by internal circuits, which identify the Power Off and Power On states (see Section 2.1.2 on page 27).

The current system sleep state is decoded from the levels of the $\overline{SLP\_S3}$ and $\overline{SLP\_S5}$ pins (see Section 6.2.3 on page 84). Only sleep state S5 is relevant.

The GRNBLNK and YLWBLNK fields in LEDBLNK register (at offset 03h; see Section 6.3.6 on page 93) control the On/Off state or the blinking rate of the GRN_LED and YLW_LED pins, respectively. For each LED pin, a different blink rate can be selected. Different blink rates can also be selected for the dual-color LED mode (LEDCFG = 0).

6.0 System Wake-Up Control (SWC) (Continued)

Special LED Control

The Special LED control is the default LED control option when a Lithium backup battery is connected to V_{BAT} pin ($V_{BAT} > V_{BATLOW}$). Two regular LEDs must be connected to the GRN_LED and the YLW_LED pins, according to configuration "b" (Active High) in Figure 16.

In this option, LED operation is controlled by the bits of XLEDCTL register (at offset 02h; see Section 6.3.5 on page 92) and by the $\overline{SLP\_S3}$, $\overline{SLP\_S5}$ and PWRGD_PS pins. When the system is in sleep state S5 ($\overline{SLP\_S5}$ = 0), both LEDs are off. When the system is in sleep state S3 ($\overline{SLP\_S3}$ = 0) or S1 (SLP_S1 bit is set), the green LED blinks and the yellow LED is off. The green and yellow LED operation is reversed when the system is in the working state (S0) and the Main power supply is not functional (PWRGD_PS = 0). When the system is in working state (S0) and the Main power supply is within the specified limits, SW_CTL bit selects the active LED (On) of the two, and the other LED is turned off.

The blinking rate of the LEDs is 1 Hz with a duty cycle of 50%.

Table 36 on page 92 shows the states of the GRN_LED and YLW_LED pins. The LEDs are connected according to configuration "b" (see Figure 16 on page 85); therefore, a LED is On when the pin is TRI-STATEd; it is Off when the pin is at low level (0).

6.2.6 Special Power Management Functions

Last Power State

Last Power State function saves the system power state when an AC power failure occurs.

When either the V_{DD3} or V_{SB3} power supply falls below the minimum limit, the SWC samples the value of the $\overline{SLP\_S3}$ signal. If $\overline{SLP\_S3}$ is sampled low, this indicates an orderly shutdown of the Main supply through the S3-S5 sleep states; however, if $\overline{SLP\_S3}$ is sampled high, this indicates a Power Fail condition, caused either by turning off the mechanical switch (G2 state) or by an AC power failure. The sampled value is powered by the V_{BAT} backup supply, which preserves its value throughout the Power Fail condition when both V_{DD3} and V_{SB3} supplies are off (see Section 2.1.2 on page 27) and until AC power returns. When the system exits Power Fail (i.e., when V_{SB3} power is back on), this read-only bit serves as a snapshot of the system state before the power was turned off.

The level of the $\overline{SLP\_S3}$ signal is sampled in LAST_PWR_STATE read-only bit in SWC_CTL register (see Section 6.3.3 on page 90).

In case of a power failure, both V_{DD} and V_{SB} power supplies fall simultaneously. Therefore, the power failure is detected either by V_{DD3} falling below V_{DD3OFF}, or by V_{SB3} falling below V_{SB3OFF}, whichever occurs first.

The LAST_PWR_STATE bit is reset to 0 at V_{BAT} Power-Up (see Section 2.2.1 on page 30).

Backup Battery Status

This function detects the status of the backup battery (V_{BAT}). When the battery voltage is below the specification ($V_{BAT} < V_{BATLOW}$), GOOD_BAT and LAST_PWR_STATE bits in SWC_CTL register (see Section 6.3.3 on page 90) are reset. In this case, the value of LAST_PWR_STATE bit is incorrect and must be ignored.

If the battery voltage is within specified limits ($V_{BAT} > V_{BATLOW}$), GOOD_BAT bit is set when either the V_{DD3} or the V_{SB3} power supply falls below the minimum limit.

6.0 System Wake-Up Control (SWC) (Continued)

6.3 SWC REGISTERS

The offsets of the SWC registers are related to the base address determined by the SWC Base Address register at indexes 60h-61h in the SWC Logical Device configuration.

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from register (data written to this address is sent to a different register).
- W = Write (see above).
- RO = Read Only.
- WO = Write Only. Reading from the bit returns 0.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

6.3.1 SWC Register Map

The following table lists the SWC registers. For the SWC register bitmap, see Section 6.5 on page 105. The SWC registers are V_{SB3} powered.

Table 33. SWC Register Map

Offset	Option[1]	Mnemonic	Register Name	Type	Power Well	Section
00h	LED_OPT = 01	SLEDCTL	Standard LED Control	R/W or RO	V_{SB3}	6.3.2
	LED_OPT = other	Reserved				
01h		SWC_CTL	SWC Miscellaneous Control	Varies per bit	Varies per bit	6.3.3
02h	LED_OPT = 00	ALEDCTL	Advanced LED Control	R/W or RO	V_{SB3}	6.3.4
	LED_OPT = 10	XLEDCTL	Special LED Control	R/W or RO	V_{DD3}	6.3.5
	LED_OPT = other	Reserved				
03h	LED_OPT = 00	LEDBLNK	LED Blinking Control	R/W or RO	V_{SB3}	6.3.6
	LED_OPT = other	Reserved				
04h		KBDWKCTL	Keyboard Wake-Up Control	R/W or RO	V_{SB3}	6.3.7
05h		PS2CTL	PS2 Protocol Control	R/W or RO	V_{SB3}	6.3.8
06h		KDSR	Keyboard Data Shift-Register	RO	V_{SB3}	6.3.9
07h		MDSR	Mouse Data Shift-Register	RO	V_{SB3}	6.3.10
08h		PS2KEY0	PS2 Keyboard Key Data 0	R/W, RO	V_{SB3}	6.3.11
09h		PS2KEY1	PS2 Keyboard Key Data 1	R/W, RO	V_{SB3}	6.3.11
0Ah		PS2KEY2	PS2 Keyboard Key Data 2	R/W, RO	V_{SB3}	6.3.11
0Bh		PS2KEY3	PS2 Keyboard Key Data 3	R/W, RO	V_{SB3}	6.3.11
0Ch		PS2KEY4	PS2 Keyboard Key Data 4	R/W, RO	V_{SB3}	6.3.11
0Dh		PS2KEY5	PS2 Keyboard Key Data 5	R/W, RO	V_{SB3}	6.3.11
0Eh		PS2KEY6	PS2 Keyboard Key Data 6	R/W, RO	V_{SB3}	6.3.11
0Fh		PS2KEY7	PS2 Keyboard Key Data 7	R/W, RO	V_{SB3}	6.3.11

1. Selected by LED_OPT field in SWC_CTL register.

6.0 System Wake-Up Control (SWC) (Continued)

6.3.2 Standard LED Control Register (SLEDCTL)

This register configures the standard LED control of the two LEDs connected to pins GRN_LED and YLW_LED of the PC87373 device. It is reset to 03h.

Power Well: V_{SB3}

Location: Offset 00h, when LED_OPT = 01 in the SWC_CTL register

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**						**BLINK**	**GRN_YLW**
Reset	0	0	0	0	0	0	1	1

Bit	Description
7-2	**Reserved.**
1	**BLINK (LEDs Blink Control).** This bit controls the operation mode (either blinking or constantly on) of the LED selected by GRN_YLW bit. Blinking rate is 0.667 Hz with a duty cycle of 41.7%. When the system is in sleep state S5, both LEDs are forced off regardless of BLINK and GRN_YLW bit values; see Table 34. 0: Selected LED blinking 1: Selected LED constantly on (default)
0	**GRN_YLW (Green-Yellow LED Select).** This bit selects which of the two LEDs (GRN_LED or YLW_LED) is active. The LED which is not active is off; see Table 34. 0: Yellow LED (connected to YLW_LED pin) selected 1: Green LED (connected to GRN_LED pin) selected (default)

Table 34. GRN_LED and YLW_LED States

$\overline{\text{SLP\_S5}}$ pin	GRN_YLW bit	BLINK bit	GRN_LED pin	YLW_LED pin
0[1]	X[2]	X	0	0
1	0	0	0	Blink
1	0	1	0	TRI-STATE
1	1	0	Blink	0
1	1	1	TRI-STATE	0

1. $\overline{\text{SLP\_S5}}$ = 0: System is in sleep state S5.
2. X is either logic “0” or logic “1”.

6.0 System Wake-Up Control (SWC) (Continued)

6.3.3 SWC Miscellaneous Control Register (SWC_CTL)

This register contains control and status bits for the SWC module. Its reset value depends on the power well of each bit.

Power Well: V_{SB3}

Location: Offset 01h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**LOCKSCF**	**Reserved**	**GOOD_ BAT**	**Reserved**		**LAST_PWR _STATE**	**LED_OPT**	
Reset	0	0	0	0	0	0	'01' or '10'	
Power Well	V_{SB3}		V_{BAT}			V_{BAT}	V_{SB3}	

Bit	Type	Description
7	R/W1S	**LOCKSCF (Lock SWC Configuration).** When set to 1, this bit locks the BLINK and GRN_YLW bits in SLEDCTL register, and all bits of SWC_CTL, ALEDCTL, LEDBLNK, XLEDCTL, KBDWKCTL, PS2CTL and PS2KEY0–7 registers by disabling writing to them (including to the LOCKSCF bit itself). Once set, this bit can be cleared by V_{DD3} Power-Up reset (or Hardware reset). 0: R/W bits are enabled for write (default) 1: All bits are RO
6		**Reserved.**
5	RO	**GOOD_BAT (Battery Good Status).** This bit indicates the status of the V_{BAT} backup power. The bit is powered by the V_{BAT} backup supply and its value is: • Reset at any time, if $V_{BAT} < V_{BATLOW}$ • Set when either V_{DD3} or V_{SB3} power supply falls below the minimum limit, if $V_{BAT} > V_{BATLOW}$ When the bit is '0', the value of the LAST_PWR_STATE bit is incorrect and must be ignored. 0: Backup battery low, or not connected ($V_{BAT} < V_{BATLOW}$) 1: Backup battery good ($V_{BAT} > V_{BATLOW}$)
4-3		**Reserved.**
2	RO	**LAST_PWR_STATE (Last Power State).** This bit samples the value of the $\overline{SLP\_S3}$ signal when a power failure occurs. It is powered by the V_{BAT} backup supply, thus preserving its value during a Power Fail condition (see Section 2.1.2 on page 27). After the AC power returns, reading from this bit returns the value of the $\overline{SLP\_S3}$ signal at the time the power failure occurred. The value of this bit must be ignored when GOOD_BAT bit is 0. Writing to this bit is ignored. At V_{BAT} Power-Up reset, LAST_PWR_STATE bit is reset to 0. 0: Orderly system shutdown - Main power off by S3 or S5 sleep states (default) 1: Forced system shutdown - Main power off by Mechanical off (G2 state) or by AC power failure
1-0	R/W or RO	**LED_OPT (LED Control Option Select).** Selects the Advanced, Standard or Special LED control option for the two power LEDs (yellow and green). **Bits 1 0 LED Control Option** 0 0: Advanced: LEDs controlled by the ALEDCTL and LEDBLNK registers at offsets 02h and 03h, respectively 0 1: Standard: LEDs controlled by SLEDCTL register at offset 00h (default if $V_{BAT} < V_{BATLOW}$ at V_{SB3} Power-Up reset) 1 0: Special: LEDs controlled by XLEDCTL register at offset 02h (default if $V_{BAT} > V_{PPLOW}$ at V_{SB3} Power-Up reset) 1 1: Reserved

6.0 System Wake-Up Control (SWC) (Continued)

6.3.4 Advanced LED Control Register (ALEDCTL)

This register configures the advanced LED control of the two LEDs connected to pins GRN_LED and YLW_LED of the PC87373 device. It is reset to 00h.

Power Well: V_{SB3}

Location: Offset 02h, when LED_OPT = 00 in the SWC_CTL register

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**LEDCFG**	**LEDPOL**	**Reserved**		**LEDMOD**	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-6	**Reserved.**
5	**LEDCFG (LED Configuration).** This bit enables the use of either two regular LEDs, connected to the GRN_LED and YLW_LED pins or one dual-colored LED, connected between the two pins (see Figure 16 on page 85). 0: One dual-colored LED (default) 1: Two regular LEDs
4	**LEDPOL (LED Polarity).** This bit determines the polarity of GRN_LED and YLW_LED outputs. An active output, according to this bit setting, turns the LED on. For the dual-colored LED configuration, changing the polarity reverses the LED colors. The configurations described here apply to the “two regular LEDs” option only; see Table 32 on page 86). 0: Active high: for connection configuration “b” in Figure 16 on page 85 (default) 1: Active low: for connection configuration “a” in Figure 16 on page 85
3-2	**Reserved.**
1-0	**LEDMOD (LED Operation Mode).** These bits control the operation mode of GRN_LED and YLW_LED in each power state. Table 35 shows the behavior of the two LED outputs as a function of the system power state.

Table 35. GRN_LED and YLW_LED as a Function of the Power State

LEDMOD	V_{DD3} Off[1]	V_{DD3} On[1]	State S5[2]	State S3[2]	States S0 - S2[2]	GRN_LED	YLW_LED
00 (default)	X[3]	X	X	X	X	S/W_GRN[4]	S/W_YLW[5]
01	Yes		X	X	X	S/W_GRN	Blink[6]
		Yes	X	X	X	S/W_GRN	S/W_YLW
10	X	X	Yes			Off	Off
	X	X		Yes		S/W_GRN	S/W_YLW
	X	X			Yes	S/W_GRN	S/W_YLW
11	Yes		X	X	X	Off	Off
		Yes	X	X	X	S/W_GRN	S/W_YLW

1. See Section 2.1.2 on page 27.
2. See Section 6.2.3 on page 84.
3. In this table, X is “Irrelevant”.
4. Controlled by the value of GRNBLNK in the LEDBLNK register.
5. Controlled by the value of YLWBLNK in the LEDBLNK register.
6. Blink rate is 1 Hz with a duty cycle of 50%.

6.0 System Wake-Up Control (SWC) (Continued)

6.3.5 Special LED Control Register (XLEDCTL)

This register configures the Special LED Control of the two LEDs connected to pins GRN_LED and YLW_LED of the PC87373 device. It is reset to 00h.

Power Well: V_{DD3}

Location: Offset 02h, when LED_OPT = 10 in SWC_CTL register

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**						**SLP_S1**	**SW_CTL**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-2	**Reserved.**
1	**SLP_S1 (Sleep State S1 Select).** When set to 1 by the software, this bit indicates that the system will enter an S1 sleep state. The value of this bit controls the operation mode of GRN_LED and YLW_LED, as shown in Table 36. 0: System in working state (S0), or in S3-S5 sleep states (default) 1: System in S1 sleep state
0	**SW_CTL (Software LEDs Control).** This bit controls the operation mode of GRN_LED and YLW_LED, as shown in Table 36. 0: Normal (default) 1: Bit set by software

Table 36. Special control of the GRN_LED and YLW_LED

System State	$\overline{\text{SLP\_S5}}$ Pin	$\overline{\text{SLP\_S3}}$ Pin	SLP_S1 Bit	PWRGD_PS Pin	SW_CTL Bit	GRN_LED Pin	YLW_LED Pin
Soft Off (S5)	0	X[1]	X	X	X	0	0
Sleep State S3	1	0	X	X	X	Blink[2]	0
Sleep State S1	1	1	1	X	X		
Working (S0), Power not good	1	1	0	0	X	0	Blink
Working (S0), Power good, no SW_CTL	1	1	0	1	0	0	TRI-STATE
Working (S0), Power good, and SW_CTL	1	1	0	1	1	TRI-STATE	0

1. In this table, X is either logic “1” or logic “0”.
2. Blink rate is 1 Hz with a duty cycle of 50%.

6.0 System Wake-Up Control (SWC) (Continued)

6.3.6 LED Blink Control Register (LEDBLNK)

This register controls the advanced blinking rate of the two LEDs connected to pins GRN_LED and YLW_LED of the PC87373 device. It is reset to 70h.

Power Well: V_{SB3}

Location: Offset 03h, when LED_OPT = 00 in the SWC_CTL register

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**GRNBLNK**			**Reserved**	**YLWBLNK**		
Reset	0	1	1	1	0	0	0	0

Bit	Description
7	**Reserved.**
6-4	**GRNBLNK (Green LED Blink Rate).** These bits control the blinking rate of GRN_LED output. **Bits 6 5 4 — Rate (Hz) — Duty Cycle** 0 0 0: Off — Always inactive 0 0 1: 0.25 — 12.5% 0 1 0: 0.5 — 25% 0 1 1: 1 — 50% 1 0 0: 2 — 50% 1 0 1: 3 — 50% 1 1 0: 4 — 50% 1 1 1: On — Always active (default)
3	**Reserved.**
2-0	**YLWBLNK (Yellow LED Blink Rate).** These bits control the blinking rate of YLW_LED output. **Bits 2 1 0 — Rate (Hz) — Duty Cycle** 0 0 0: Off — Always inactive (default) 0 0 1: 0.25 — 12.5% 0 1 0: 0.5 — 25% 0 1 1: 1 — 50% 1 0 0: 2 — 50% 1 0 1: 3 — 50% 1 1 0: 4 — 50% 1 1 1: On — Always active

6.0 System Wake-Up Control (SWC) (Continued)

6.3.7 Keyboard Wake-Up Control Register (KBDWKCTL)

This register configures the keyboard events detected by the Keyboard/Mouse Wake-Up Detector. It is reset to 40h.

Power Well: V_{SB3}

Location: Offset 04h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**KBDMODE**		**EVT3CFG**		**EVT2CFG**		**EVT1CFG**	
Reset	0	1	0	0	0	0	0	0

Bit	Description
7-6	**KBDMODE (Keyboard Mode Select).** This field selects one of the keyboard wake-up modes for the Keyboard/Mouse Wake-Up Detector. **Bits 7 6 — Keyboard Wake-Up Mode** 0 0: Special Key Sequence or Password: Configured by bits 3-0 of PS2CTL register 0 1: Fast Any-Key: Indicates that any key was pressed on the keyboard (default) 1 0: Power Management Keys: Configured by bits 5-0 of KBDWKCTL register 1 1: Reserved
5-4	**EVT3CFG (Keyboard Event 3 Configuration).** These bits configure the keyboard data sequence for Keyboard Event 3, which indicates that “PM Key 3” was pressed on the keyboard. The setting of the EVT3CFG field is relevant only if the Keyboard/Mouse Wake-Up Detector is in Power Management Keys mode (KBDMODE = 10). The keyboard data sequence used to detect Keyboard Event 3 is stored in registers PS2KEY6-7, starting with PS2KEY6. **Bits 5 4 — Sequence Length** 0 0: 0 bytes: Keyboard Event 3 disabled (default) 0 1: 1 byte: PS2KEY6 1 0: 2 bytes: PS2KEY6, PS2KEY7 1 1: Reserved
3-2	**EVT2CFG (Keyboard Event 2 Configuration).** These bits configure the keyboard data sequence for Keyboard Event 2, which indicates that “PM Key 2” was pressed on the keyboard. The setting of the EVT2CFG field is relevant only if the Keyboard/Mouse Wake-Up Detector is in Power Management Keys mode (KBDMODE = 10). The keyboard data sequence used to detect Keyboard Event 2 is stored in registers PS2KEY3-5, starting with PS2KEY3. **Bits 3 2 — Sequence Length** 0 0: 0 bytes: Keyboard Event 2 disabled (default) 0 1: 1 byte: PS2KEY3 1 0: 2 bytes: PS2KEY3, PS2KEY4 1 1: 3 bytes: PS2KEY3, PS2KEY4, PS2KEY5
1-0	**EVT1CFG (Keyboard Event 1 Configuration).** These bits configure the keyboard data sequence for Keyboard Event 1, which indicates that “PM Key 1” was pressed on the keyboard. The setting of the EVT1CFG field is relevant only if the Keyboard/Mouse Wake-Up Detector is in Power Management Keys mode (KBDMODE = 10). The keyboard data sequence used to detect Keyboard Event 1 is stored in registers PS2KEY0-2, starting with PS2KEY0. **Bits 1 0 — Sequence Length** 0 0: 0 bytes: Keyboard Event 1 disabled (default) 0 1: 1 byte: PS2KEY0 1 0: 2 bytes: PS2KEY0, PS2KEY1 1 1: 3 bytes: PS2KEY0, PS2KEY1, PS2KEY2

6.0 System Wake-Up Control (SWC) (Continued)

6.3.8 PS2 Protocol Control Register (PS2CTL)

This register configures the keyboard and mouse events detected by the Keyboard/Mouse Wake-Up Detector. It is reset to 10h.

Power Well: V_{SB3}

Location: Offset 05h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**DISPAR**	**MSEVCFG**			**KBEVCFG**			
Reset	0	0	0	1	0	0	0	0

Bit	Description
7	**DISPAR (Disable Parity Check).** This controls the parity checking of the keyboard and mouse data by the Keyboard/Mouse Wake-Up Detector. 0: Enable parity check (default) 1: Disable parity check
6-4	**MSEVCFG (Mouse Event Configuration).** These bits configure the mouse data sequence for the Mouse event. Before setting them to a new value, these bits must be cleared by writing a value of '000'. **Bits 6 5 4 — Event Configuration** 0 0 0: Disable mouse wake-up detection 0 0 1: Wake-up on any mouse movement or button click (default) 0 1 0: Wake-up on left button click 0 1 1: Wake-up on left button double-click 1 0 0: Wake-up on right button click 1 0 1: Wake-up on right button double-click 1 1 0: Wake-up on any button single-click (left, right or middle) 1 1 1: Wake-up on any button double-click (left, right or middle)
3-0	**KBEVCFG (Keyboard Event Configuration).** These bits configure the keyboard data sequence for the Keyboard event indicating that any key or key sequence was pressed on the keyboard. The setting of the KBEVCFG field is relevant only if the Keyboard/Mouse Wake-Up Detector is in either Special Key Sequence or Password mode (KBDMODE = 00). The keyboard data sequence used to detect a Keyboard Event is stored in registers PS2KEY0-7, starting with PS2KEY0. Before setting them to a new value, the KBEVCFG field must be cleared by writing a value of '0000'. **Bits 3 2 1 0 — Event Configuration** 0 0 0 0: Disable keyboard wake-up detection (default) 0 0 0 1 to 0 1 1 1: Special Key Sequence mode consisting of from two to eight PS/2 data bytes, "Make" and "Break" codes (including Shift and Alt keys) 1 0 0 0 to 1 1 1 1: Password Enabled mode with consisting of from one to eight keys "Make" code (excluding Shift and Alt keys)

6.0 System Wake-Up Control (SWC) (Continued)

6.3.9 Keyboard Data Shift Register (KDSR)

When keyboard wake-up detection is enabled, this register stores the keyboard data shifted in from the keyboard during data transmission. It is reset to 00h.

Power Well: V_{SB3}

Location: Offset 06h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Keyboard Data**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**Keyboard Data.**

6.3.10 Mouse Data Shift Register (MDSR)

When mouse wake-up detection is enabled, this register stores the mouse data shifted in from the mouse during data transmission. It is reset to 00h.

Power Well: V_{SB3}

Location: Offset 07h (offset in PC8741x = 17h)

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**					**Mouse Data**		
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-3	**Reserved.**
2-0	**Mouse Data.**

6.3.11 PS2 Keyboard Key Data 0 to 7 Registers (PS2KEY0-7)

These eight registers (PS2KEY0-7) store the data bytes for Special Key Sequence or Password mode (KBDMODE = 00) or for Power Management Keys mode (KBDMODE = 10) of the Keyboard/Mouse Wake-Up Detector.

In Special Key Sequence or in Password modes, the keyboard data is stored as follows:

- PS2KEY0 register stores the data byte for the first key in the sequence.
- PS2KEY1 register stores the data byte for the second key in the sequence.
- PS2KEY2-7 registers store data bytes for the third to eighth key in the sequence.

For keyboard data storage in Power Management Keys mode, see Section 6.3.7 on page 94.

When one of these registers is set to 00h, it indicates that the value of the corresponding data byte is ignored (i.e., it is not compared with the keyboard data). These registers are reset to 00h.

Power Well: V_{SB3}

Location: Offset 08h to 0Fh

Type: R/W, RO

Bit	7	6	5	4	3	2	1	0
Name	**Data Byte of Key**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**Data Byte of Key.**

6.0 System Wake-Up Control (SWC) (Continued)

6.4 ACPI REGISTERS

The ACPI registers are organized in two groups, which are both powered by V_{SB3}. The offsets of the two groups of ACPI registers are related to the base address determined by the Base Address registers at indexes 62h-63h in the SWC device configuration.

The PC87373 device supports the General-Purpose Event 1, ACPI generic register group. This group contains the GPE1_STS and GPE1_EN registers, each with a length of one byte. In addition, the device supports the “child” events of the General-Purpose Event 1 register group in the GPE1_STS_0-GPE1_STS_3 and the GPE1_EN_0-GPE1_EN_3 registers.

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from register (data written to this address is sent to a different register).
- W = Write (see above).
- RO = Read Only.
- WO = Write Only. Reading from the bit returns 0.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

6.4.1 ACPI Register Map

The following table lists the ACPI registers. All of these registers are V_{SB3} powered.

Table 37. ACPI Register Map

Base Registers	Offset	Mnemonic	Register Name	Type	Power Well	Section
At index 62h, 63h	00h	GPE1_STS	General-Purpose Status 1 Register	R/W1C	V_{SB3}	6.4.2
	01h-03h	Reserved				
	04h	GPE1_EN	General-Purpose Enable 1 Register	R/W	V_{SB3}	6.4.3
	05h-07h	Reserved				
	08h	GPE1_STS_0	General-Purpose Status 1 Register 0	R/W1C	V_{SB3}	6.4.4
	09h	GPE1_STS_1	General-Purpose Status 1 Register 1	R/W1C	V_{SB3}	6.4.5
	0Ah	GPE1_STS_2	General-Purpose Status 1 Register 2	R/W1C	V_{SB3}	6.4.6
	0Bh	GPE1_STS_3	General-Purpose Status 1 Register 3	R/W1C	V_{SB3}	6.4.7
	0Ch	GPE1_EN_0	General-Purpose Enable 1 Register 0	R/W	V_{SB3}	6.4.8
	0Dh	GPE1_EN_1	General-Purpose Enable 1 Register 1	R/W	V_{SB3}	6.4.9
	0Eh	GPE1_EN_2	General-Purpose Enable 1 Register 2	R/W	V_{SB3}	6.4.10
	0Fh	GPE1_EN_3	General-Purpose Enable 1 Register 3	R/W	V_{SB3}	6.4.11

6.0 System Wake-Up Control (SWC) (Continued)

6.4.2 General-Purpose Status 1 Register (GPE1_STS)

This register contains the global Power Management Event status bit. This register belongs to the General-Purpose Event 1 register group of the ACPI generic-feature space registers.

The status bit behaves according to the Sticky Status Bit definition in the ACPI Specification (i.e., the bit is set when the level of the hardware signal is high and is only cleared by the software writing 1 to it).

Power Well: V_{SB3}

Location: Offset 00h

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**							**PME_STS**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-1	**Reserved.**
0	**PME_STS (Power Management Event Status).** Indicates that an enabled Power Management event has occurred. This bit is set if at least one enabled event (in GPE1_EN_0 to GPE1_EN_3 registers) is active (in GPE1_STS_0 to GPE1_STS_3 registers). This bit can be reset by writing 1 only if all the enabled events are inactive. 0: Inactive (default) 1: At least one enabled “child” event was active since this bit was last cleared

6.4.3 General-Purpose Enable 1 Register (GPE1_EN)

This register contains the global Power Management Event enable bit. This register belongs to the General-Purpose Event 1 register group of the ACPI generic-feature space registers. It is reset to 00h.

The enable bit behaves according to the Enable Bit definition in the ACPI Specification (i.e., the bit can be read or written by software).

Power Well: V_{SB3}

Location: Offset 04h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**							**PME_EN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-1	**Reserved.**
0	**PME_EN (Power Management Event Enable).** Controls SCI ($\overline{\text{SIOPME}}$) generation by a set PME_STS bit. If this bit is set, a set PME_STS bit in GPE1_STS register generates an SCI interrupt. 0: Disable SCI (default) 1: Enable SCI generation by a set PME_STS bit

6.0 System Wake-Up Control (SWC) (Continued)

6.4.4 General-Purpose Status 1 Register 0 (GPE1_STS_0)

This register contains “child” events 0-7 of the GPE1_STS register.

The status bits behave according to the Sticky Status Bit definition in the ACPI Specification (i.e., the bit is set when the hardware signal is high and is only cleared by the software writing 1 to it).

Power Well: V_{SB3}

Location: Offset 08h

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**GPIOE07_STS**	**GPIOE06_STS**	**GPIOE05_STS**	**GPIOE04_STS**	**GPIOE03_STS**	**GPIOE02_STS**	**GPIOE01_STS**	**GPIOE00_STS**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**GPIOE07_STS (GPIOE07 Event Status).** Indicates that an active event has been detected at pin 7 of GPIOE Port 0. The event has programmable polarity and the debounce option (see Section 5.3 on page 75). The bit is set by an active level at the GPIOE07 pin. Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: An active event has occurred
6-0	**GPIOE06_STS to GPIOE00_STS (GPIOE06 to GPIOE00 Event Status).** Same as above for pins 6-0 of GPIOE Port 0.

6.4.5 General-Purpose Status 1 Register 1 (GPE1_STS_1)

This register contains “child” events 8-15 of the GPE1_STS register.

The status bits behave according to the Sticky Status Bit definition in the ACPI Specification (i.e., the bit is set when the hardware signal is high and is only cleared by the software writing 1 to it).

Power Well: V_{SB3}

Location: Offset 09h

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**GPIOE13_STS**	**GPIOE12_STS**	**GPIOE11_STS**	**GPIOE10_STS**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved.**
3	**GPIOE13_STS (GPIO13 Event Status).** Indicates that an active event has been detected at pin 3 of GPIOE Port 1. The event has programmable polarity and the debounce option (see Section 5.3 on page 75). The bit is set by an active level at the GPIOE13 pin. Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: An active event has occurred
2-0	**GPIOE12_STS to GPIOE10_STS (GPIOE12 to GPIOE10 Event Status).** Same as above for pins 2-0 of GPIOE Port 1.

6.0 System Wake-Up Control (SWC) (Continued)

6.4.6 General-Purpose Status 1 Register 2 (GPE1_STS_2)

This register contains “child” events 16-23 of the GPE1_STS register.

The status bits behave according to the Sticky status bit definition in the ACPI Specification (i.e., the bit is set when the level of the hardware signal is high and is only cleared by the software writing 1 to it).

Power Well: V_{SB3}

Location: Offset 0Ah

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**KBD_EVT3_STS**	**KBD_EVT2_STS**	**KBD_EVT1_STS**	**MS_EVT_STS**	**KBD_ANYK_STS**	**RI1_EVT_STS**	**RI2_EVT_STS**	**Reserved**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**KBD_EVT3_STS (Keyboard Event 3 Status).** Indicates that “PM Key 3” was pressed and that the event was identified by the Keyboard/Mouse Wake-Up Detector. This bit is set only if the Keyboard/Mouse Wake-Up Detector is in Power Management Keys mode (see Section 6.3.7 on page 94). Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: The “PM Key 3” key was pressed on the keyboard
6	**KBD_EVT2_STS (Keyboard Event 2 Status).** Indicates that “PM Key 2” was pressed and that the event was identified by the Keyboard/Mouse Wake-Up Detector. This bit is set only if the Keyboard/Mouse Wake-Up Detector is in Power Management Keys mode (see Section 6.3.7 on page 94). Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: The “PM Key 2” key was pressed on the keyboard
5	**KBD_EVT1_STS (Keyboard Event 1 Status).** This bit indicates that a keyboard event occurred and was identified by the Keyboard/Mouse Wake-Up Detector. The event type depends on the selected operation mode for the Keyboard/Mouse Wake-Up Detector (see Sections 6.3.7 and 6.3.8 on page 94.): • Pressing any key or a sequence of special keys in Special Key Sequence mode • Pressing a sequence of keys in Password mode • Pressing the “PM Key 1” in Power Management Keys mode Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: A keyboard event occurred
4	**MS_EVT_STS (Mouse Event Status).** Indicates that a mouse event occurred and was identified by the Keyboard/Mouse Wake-Up Detector (see Section 6.3.8 on page 95). Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: A mouse event occurred
3	**KBD_ANYK_STS (Keyboard Any-Key Status).** This bit indicates that any key was pressed and that the event was identified by the Keyboard/Mouse Wake-Up Detector. This bit is set only if the Keyboard/Mouse Wake-Up Detector is in Fast Any-Key mode (see Section 6.3.7 on page 94). Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: A keyboard event occurred
2	**RI1_EVT_STS ($\overline{\text{RI1}}$ Event Status).** Indicates that a telephone ring signal was received at Serial Port 1 and the event was identified by the RI Wake-Up Detector. This bit is set by a high-to-low transition at the $\overline{\text{RI1}}$ pin (see Section 6.2.1 on page 81). Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: A telephone ring signal was received at Serial Port 1

Bit	Description
1	**RI2_EVT_STS ($\overline{\text{RI2}}$ Event Status).** Indicates that a telephone ring signal was received at Serial Port 2 and the event was identified by the RI Wake-Up Detector. This bit is set by a high-to-low transition at the $\overline{\text{RI2}}$ pin (see Section 6.2.1 on page 81). Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: A telephone ring signal was received at Serial Port 2
0	**Reserved.**

6.4.7 General-Purpose Status 1 Register 3 (GPE1_STS_3)

This register contains “child” events 24-31 of the GPE1_STS register.

The status bits behave according to the Sticky Status Bit definition in the ACPI Specification (i.e., the bit is set when the level of the hardware signal is high and is only cleared by the software writing 1 to it).

Power Well: V_{SB3}

Location: Offset 0Bh

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**MOD_IRQ _STS**	**MS_IRQ _STS**	**KBD_IRQ _STS**	**Reserved**	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-5	**Reserved.**
4	**MOD_IRQ_STS (Modules IRQ Event Status).** Indicates that an IRQ was generated by one of the Legacy modules (FDC, Parallel Port, Serial Ports 1 and 2, and MIDI Port) or the Fan Speed Control and Monitor. This bit is set only if the IRQ is enabled for wake-up (bit 4 of the Standard configuration register at index 70h) and the related module is active; see Section 3.2.3 on page 36. Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: An enabled IRQ from one of the Legacy modules or the Fan Speed Control and Monitor is active
3	**MS_IRQ_STS (Mouse IRQ Event Status).** Indicates that an IRQ was generated by the mouse interface section of the KBC module. This bit is set only if the IRQ is enabled for wake-up (bit 4 of the Mouse Logical Device configuration register at index 70h) and the KBC module is active (see Section 3.2.3 on page 36). Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: An enabled IRQ from the mouse interface section of the KBC module is active
2	**KBD_IRQ_STS (Keyboard IRQ Event Status).** Indicates that an IRQ was generated by the keyboard interface section of the KBC module. This bit is set only if the IRQ is enabled for wake-up (bit 4 of the Keyboard Logical Device configuration register at index 70h) and the KBC module is active (see Section 3.2.3 on page 36). Writing 1 clears this bit; writing 0 is ignored. 0: Inactive since last cleared (default) 1: An enabled IRQ from the keyboard interface section of the KBC module is active
1-0	**Reserved.**

6.0 System Wake-Up Control (SWC) (Continued)

6.4.8 General-Purpose Enable 1 Register 0 (GPE1_EN_0)

This register contains “child” events 0-7 of the GPE1_EN register.

The enable bits behave according to the Enable Bit definition in the ACPI Specification (i.e., the bit can be read or written by software).

Power Well: V_{SB3}

Location: Offset 0Ch

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**GPIOE07_EN**	**GPIOE06_EN**	**GPIOE05_EN**	**GPIOE04_EN**	**GPIOE03_EN**	**GPIOE02_EN**	**GPIOE01_EN**	**GPIOE00_EN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**GPIOE07_EN (GPIOE07 Event Enable).** Enables an active event at pin 7 of GPIOE Port 0 to set PME_STS bit in GPE1_STS register. 0: Disable event (default) 1: Enable event to set PME_STS
6-0	**GPIOE06_EN to GPIOE00_EN (GPIOE06 to GPIOE00 Event Enable).** Same as above for pins 6-0 of GPIOE Port 0.

6.4.9 General-Purpose Enable 1 Register 1 (GPE1_EN_1)

This register contains “child” events 8-15 of the GPE1_EN register.

The enable bits behave according to the Enable Bit definition in the ACPI Specification (i.e., the bit can be read or written by software).

Power Well: V_{SB3}

Location: Offset 0Dh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**GPIOE13_EN**	**GPIOE12_EN**	**GPIOE11_EN**	**GPIOE10_EN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved.**
3	**GPIOE13_EN (GPIOE13 Event Enable).** Enables an active event at pin 3 of GPIOE Port 1 to set PME_STS bit in GPE1_STS register. 0: Disable event (default) 1: Enable event to set PME_STS
2-0	**GPIOE12_EN to GPIOE10_EN (GPIOE12 to GPIOE10 Event Enable).** Same as above for pins 2-0 of GPIOE Port 1.

6.0 System Wake-Up Control (SWC) (Continued)

6.4.10 General-Purpose Enable 1 Register 2 (GPE1_EN_2)

This register contains “child” events 16-23 of the GPE1_EN register.

The enable bits behave according to the Enable Bit definition in the ACPI Specification (i.e., the bit can be read or written by software).

Power Well: V_{SB3}

Location: Offset 0Eh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**KBD_EVT3_EN**	**KBD_EVT2_EN**	**KBD_EVT1_EN**	**MS_EVT_EN**	**KBD_ANYK_EN**	**RI1_EVT_EN**	**RI2_EVT_EN**	**Reserved**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**KBD_EVT3_EN (Keyboard Event 3 Enable).** Enables the event of pressing “PM Key 3” (on the keyboard) to set PME_STS bit in GPE1_STS register. 0: Disable event (default) 1: Enable event of pressing the “PM Key 3” on the keyboard to set PME_STS
6	**KBD_EVT2_EN (Keyboard Event 2 Enable).** Enables the event of pressing “PM Key 2” (on the keyboard) to set PME_STS bit in GPE1_STS register. 0: Disable event (default) 1: Enable event of pressing the “PM Key 2” on the keyboard to set PME_STS
5	**KBD_EVT1_EN (Keyboard Event 1 Enable).** Enables the event of pressing any key, key sequence or “PM Key 1” (on the keyboard) to set PME_STS bit in GPE1_STS register. 0: Disable event (default) 1: Enable event of pressing a sequence of keys or the “PM Key 1” on the keyboard to set PME_STS
4	**MS_EVT_EN (Mouse Event Enable).** Enables a mouse event identified by the Keyboard/Mouse Wake-Up Detector to set PME_STS bit in GPE1_STS register. 0: Disable event (default) 1: Enable event of mouse event identified by the Keyboard/Mouse Wake-Up Detector to set PME_STS
3	**KBD_ANYK_EN (Keyboard Any-Key Enable).** Enables the event of pressing any key (on the keyboard) to set PME_STS bit in GPE1_STS register. 0: Disable event (default) 1: Enable event of pressing any key on the keyboard to set PME_STS
2	**RI1_EVT_EN ($\overline{\text{RI1}}$ Event Enable).** Enables a telephone ring, received at Serial Port 1 and identified by the RI Wake-Up Detector, to set PME_STS bit in GPE1_STS register. 0: Disable event (default) 1: Enable event of telephone ring event received at Serial Port 1 to set PME_STS
1	**RI2_EVT_EN ($\overline{\text{RI2}}$ Event Enable).** Enables a telephone ring, received at Serial Port 2 and identified by the RI Wake-Up Detector, to set PME_STS bit in GPE1_STS register. 0: Disable event (default) 1: Enable event of telephone ring event received at Serial Port 2 to set PME_STS
0	**Reserved.**

6.0 System Wake-Up Control (SWC) (Continued)

6.4.11 General-Purpose Enable 1 Register 3 (GPE1_EN_3)

This register contains “child” events 24-31 of the GPE1_EN register.

The enable bits behave according to the Enable Bit definition in the ACPI Specification (i.e., the bit can be read or written by software).

Power Well: V_{SB3}

Location: Offset 0Fh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**MOD_IRQ_EN**	**MS_IRQ_EN**	**KBD_IRQ_EN**	**Reserved**	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-5	**Reserved.**
4	**MOD_IRQ_EN (Modules IRQ Event Enable).** Enables an active IRQ from one of the Legacy modules or the Fan Speed Control and Monitor to set PME_STS bit in GPE1_STS register. 0: Disable event (default) 1: Enable event of an active IRQ from one of the Legacy modules or the Fan Speed Control and Monitor to set PME_STS
3	**MS_IRQ_EN (Mouse IRQ Event Enable).** Enables an IRQ generated by the mouse interface section of the KBC module to set PME_STS bit in GPE1_STS register. 0: Disable event (default) 1: Enable event of an IRQ generated by the mouse interface section of the KBC module to set PME_STS
2	**KBD_IRQ_EN (Keyboard IRQ Event Enable).** Enables an IRQ generated by the keyboard interface section of the KBC module to set PME_STS bit in GPE1_STS register. 0: Disable event (default) 1: Enable event of an IRQ generated by the keyboard interface section of the KBC module to set PME_STS
1-0	**Reserved.**

6.0 System Wake-Up Control (SWC) (Continued)

6.5 SYSTEM WAKE-UP CONTROL REGISTER BITMAP

Table 38. SWC Register Map with Base Address at Index 60h, 61h

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	SLEDCTL LED_OPT=01	Reserved						BLINK	GRN_YLW
	Reserved LED_OPT=other	Reserved							
01h	SWC_CTL	LOCKSCF	Reserved	GOOD_ BAT	Reserved		LAST_PW R_STATE	LED_OPT	
02h	ALEDCTL LED_OPT=00	Reserved		LEDCFG	LEDPOL	Reserved		LEDMOD	
	XLEDCTL LED_OPT=10	Reserved						SLP_S1	SW_CTL
	Reserved LED_OPT=other	Reserved							
03h	LEDBLNK LED_OPT=00	Reserved	GRNBLNK			Reserved	YLWBLNK		
	Reserved LED_OPT=other	Reserved							
04h	KBDWKCTL	KBDMODE		EVT3CFG		EVT2CFG		EVT1CFG	
05h	PS2CTL	DISPAR	MSEVCFG			KBEVCFG			
06h	KDSR	Keyboard Data							
07h	MDSR	Reserved					Mouse Data		
08h	PS2KEY0	Data Byte of Key							
09h	PS2KEY1	Data Byte of Key							
0Ah	PS2KEY2	Data Byte of Key							
0Bh	PS2KEY3	Data Byte of Key							
0Ch	PS2KEY4	Data Byte of Key							
0Dh	PS2KEY5	Data Byte of Key							
0Eh	PS2KEY6	Data Byte of Key							
0Fh	PS2KEY7	Data Byte of Key							

6.0 System Wake-Up Control (SWC) (Continued)

Table 39. ACPI Register Map with Base Address at Index 62h, 63h

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	GPE1_STS	Reserved							PME_STS
01h-03h	Reserved	Reserved							
04h	GPE1_EN	Reserved							PME_EN
05h-07h	Reserved	Reserved							
08h	GPE1_STS_0	GPIOE07_STS	GPIOE06_STS	GPIOE05_STS	GPIOE04_STS	GPIOE03_STS	GPIOE02_STS	GPIOE01_STS	GPIOE00_STS
09h	GPE1_STS_1	Reserved				GPIOE13_STS	GPIOE12_STS	GPIOE11_STS	GPIOE10_STS
0Ah	GPE1_STS_2	KBD_EVT3_STS	KBD_EVT2_STS	KBD_EVT1_STS	MS_EVT_STS	KBD_ANYK_STS	RI1_EVT_STS	RI2_EVT_STS	Reserved
0Bh	GPE1_STS_3	Reserved			MOD_IRQ_STS	MS_IRQ_STS	KBD_IRQ_STS	Reserved	
0Ch	GPE1_EN_0	GPIOE07_EN	GPIOE06_EN	GPIOE05_EN	GPIOE04_EN	GPIOE03_EN	GPIOE02_EN	GPIOE01_EN	GPIOE00_EN
0Dh	GPE1_EN_1	Reserved				GPIOE13_EN	GPIOE12_EN	GPIOE11_EN	GPIOE10_EN
0Eh	GPE1_EN_2	KBD_EVT3_EN	KBD_EVT2_EN	KBD_EVT1_EN	MS_EVT_EN	KBD_ANYK_EN	RI1_EVT_EN	RI2_EVT_EN	Reserved
0Fh	GPE1_EN_3	Reserved			MOD_IRQ_EN	MS_IRQ_EN	KBD_IRQ_EN	Reserved	

7.0 Fan Speed Control

This chapter describes a generic Fan Speed Control unit. One or more Fan Speed Control units are included in the Fan Speed Control and Monitor (FSCM) module. For the specific implementation in this device, see Section 3.15.1 on page 67.

7.1 OVERVIEW

The Fan Speed Control is a programmable Pulse Width Modulation (PWM) generator. The PWM generator output is used to control the fan power voltage, which is correlated to the fan speed. Converting a 0 to 100% duty cycle PWM signal to an analog voltage range is performed by an external driver circuit, as shown in Figure 17. Some newer fans accept direct PWM input without any external driver.

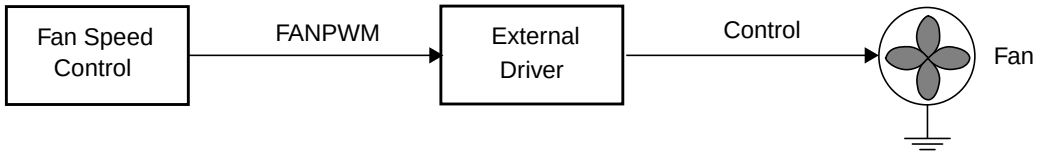


Figure 17. Fan Speed Control - System Configuration

7.2 FUNCTIONAL DESCRIPTION

The PWM generator operation is based on a PWM counter and two registers: the Fan Speed Control Pre-Scale register (FCPSR), used to determine the overall cycle time (or the frequency) of the FANPWM output, and the Fan Speed Control Duty Cycle register (FCDCR), used to determine the duty cycle of the FANPWM between 0 to 100%.

The PWM counter is an 8-bit, free-running counter that runs continuously in a cyclic manner, i.e., its cycle equals 256 clock periods. The PWM output is high, as long as the count is lower than the FCDCR value and it flips to low as the counter exceeds that value. The duty cycle (expressed as a percentage) is therefore (FCDCR/256)*100. In particular, the PWM output is continuously low when FCDCR=0; it is continuously high when FCDCR=FFh. The FANOUT output may be inverted by an external configuration bit (FANCTL_INV in FSCMCF1 or FSCMCF2 register; see Section 3.15.3 on page 68 and Section 3.15.4 on page 69), in which case the FANPWM duty cycle is ([256-FCDCR]/256)*100.

The PWM counter clock is generated by dividing the input clock (either 24 MHz or 200 KHz), using a clock divider. The division factor, which must be between 1 and 124, is defined as PRE-SCALE +1, where PRE-SCALE is the binary value stored in bits 6 to 0 of the FCPSR register. The resulting PWM output frequency is therefore:

(24 MHz or 200 kHz) / ([PRE-SCALE + 1] ***** 256).

The default selection of 24 MHz input clock allows a programmable FANPWM frequency in the range of 756 Hz to 93.75 KHz. For lower frequencies, selecting the 200 KHz input clock allows a frequency range of 6 Hz to 781 Hz (see Figure 18).

The FANPWM frequency must be selected, according to the fan type's specific requirements, prior to enabling the Fan Speed Control. The only register that must be changed at runtime to control the fan speed is the FCDCR register.

Warning! The contents of the FCPSR register must not be changed while the Fan Speed Control is enabled.

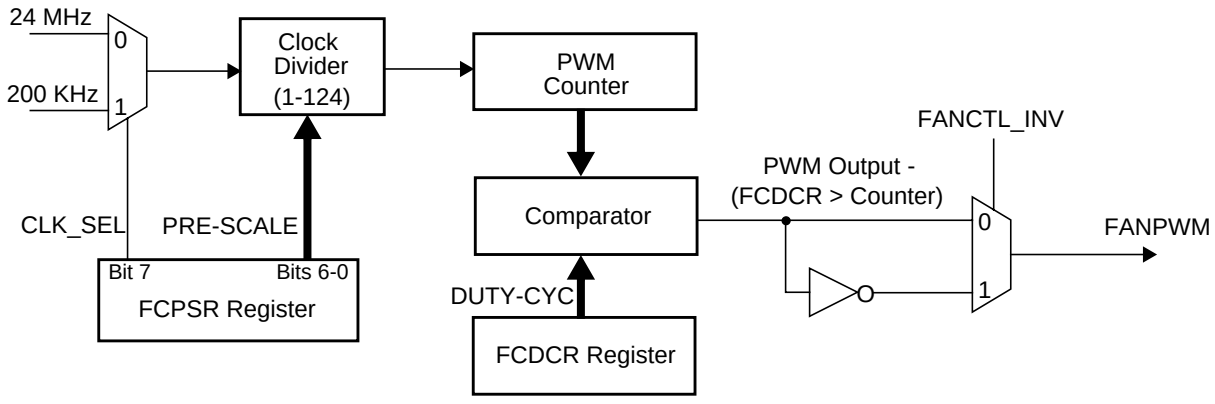


Figure 18. Fan Speed Control - Simplified Diagram

7.0 Fan Speed Control (Continued)

7.3 FAN SPEED CONTROL REGISTERS

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from a specific register (write to the same address is to a different register).
- W = Write (see above).
- RO = Read Only.
- WO = Write Only. Reading from the bit returns 0.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

7.3.1 Fan Speed Control Register Map

Table 40. Fan Speed Control Register Map

Offset	Mnemonic	Register Name	Type	Power Well	Section
Device specific[1]	FCPSR	Fan Speed Control Pre-Scale	R/W	V_{DD3}	7.3.2
Device specific[1]	FCDCR	Fan Speed Control Duty Cycle	R/W	V_{DD3}	7.3.3

1. The location of this register is defined in Section 3.15.1 on page 67.

7.3.2 Fan Speed Control Pre-Scale Register (FCPSR)

This register controls the clock of the PWM counter. It is reset by hardware to 00h.

Note: The contents of this register must not be changed when the corresponding FANCTL_EN bit in FSCMCF1 or FSCMCF2 register is set (see Section 3.15.3 on page 68), as this may produce unpredictable results.

Power Well: V_{DD3}

Location: Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**CLK_SEL**	**PRE-SCALE**						
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**CLK_SEL (Clock Select).** This bit selects the input clock for the clock divider. 0: 24 MHz (default) 1: 200 KHz
6-0	**PRE-SCALE (Pre-Scale Value).** The clock divider for the input clock (24 MHz or 200 KHz) is PRE-SCALE + 1. Writing 0000000b (default) to these bits transfers the input clock directly to the counter. The maximum clock divider is 124 (7Bh +1). These bits must not be programed with the values 7Ch, 7Dh, 7Eh and 7Fh as this may produce unpredictable results.

7.0 Fan Speed Control (Continued)

7.3.3 Fan Speed Control Duty-Cycle Register (FCDCR)

This register controls the duty-cycle of the FANPWM signal. It is reset by hardware to FFh.

Power Well: V_{DD3}

Location: Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**DUTY-CYC**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**DUTY-CYC (Duty-Cycle Value).** The binary value of this 8-bit field determines the number of clock cycles (out of a 256-cycle period) during which the PWM output is high (a high FANPWM is either equal to or the inverse of the PWM output, depending on the FANCTL_INV configuration bit). 00h: The PWM output is continuously low 01h - FEh: The PWM output is high for [DUTY-CYC] number of clock cycles and low for [256-DUTY-CYC] number of clock cycles FFh: The PWM output is continuously high (default)

7.4 FAN SPEED CONTROL REGISTER BITMAP

Table 41. Fans Speed Control Register Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Device Specific[1]	FCPSR	CLK_SEL	PRE-SCALE						
Device Specific[1]	FCDCR	DUTY-CYC							

1. The location of this register is defined in Section 3.15.1 on page 67.

8.0 Fan Speed Monitor

This chapter describes a generic Fan Speed Monitor unit. One or more Fan Speed Monitor units are included in the Fan Speed Control and Monitor (FSCM) module. For the implementation used in this device, see Section 3.15.1 on page 67.

8.1 OVERVIEW

The Fan Speed Monitor measures the fan speed by measuring the time between consecutive “active” tachometer pulses (obtained from the tachometer pulses generated by the fan). The FSM provides to the system a current speed reading; it can also alert the system by interrupt whenever the speed drops below a programmable threshold. The FSM indicates whether the speed is just below the threshold or low enough to consider the fan stopped (i.e., inefficient fan operation).

Figure 19 shows the basic system configuration of the Fan Speed Monitor.

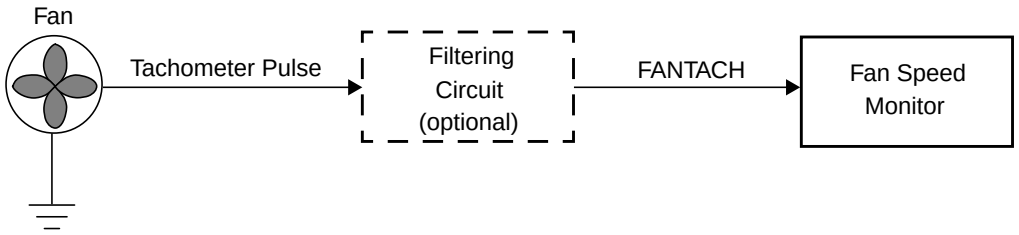


Figure 19. Fan Speed Monitor - System Configuration

8.2 FUNCTIONAL DESCRIPTION

The fan generates a tachometer pulse every half or full revolution (depending on the fan type). These pulses are fed into the Fan Speed Monitor through the FANTACH input pin.

The FANTACH pin has a Schmitt Trigger input buffer. In addition, the FANTACH signal passes through a digital filter, which ignores any tachometer pulses shorter than 750 µs. This filter can be enabled by setting FILTER_DIS bit in FMCSR register to 0.

Speed monitoring is based on measuring the time between tachometer pulses generated by the fan. The Fan Speed Monitor measures the time for a full fan revolution. Since fans generate one or two tachometer pulses per revolution (depending on the fan type), the incoming pulses at the FANTACH pin are either used directly or are divided by 2 to produce the active tachometer pulses. These active pulses eventually control the fan speed counter. Incoming tachometer pulse decimation is controlled by TPPR bit in FMCSR register.

The fan speed measured by the counter during a full fan revolution is stored as a 16-bit FAN_SPD value, where FAN_SPD_HIGH is the high byte and FAN_SPD_LOW is the low byte. The rotational speed of the fan is calculated according to the following relationship:

$$\text{Rotational Speed of Fan (in RPM)} = 60 * \frac{32000}{\text{FAN\_SPD}}$$

The Fan Speed Monitor consists of a 16-bit counter, which measures the fan speed, and two 16-bit registers, FAN_SPD, which holds the current fan speed value, and THRSH, which holds the threshold value. The 16-bit THRSH value is composed of THRSH_HIGH (the high byte) and THRSH_LOW (the low byte). Figure 20 is a simplified diagram of the Fan Speed Monitor.

The Up Counter and the FAN_SPD data are cleared to 0 when the Fan Speed Monitor is disabled.

When the Fan Speed Monitor is enabled (by FANMON_EN bit in FSCMCF1 or FSCMCF2 register; see Section 3.15.3 on page 68 and Section 3.15.4 on page 69) and there is no counter overflow, the Up Counter, which is clocked by a 32.000 KHz internal clock, increments by 1. Starting from the second active FANTACH pulse (after activation) and on every subsequent active FANTACH pulse, the FAN_SPD data is updated with the contents of the counter, the counter is cleared to 0 and SPD_RDY bit in FMCSR register is set to 1.

The above operation continually repeats itself, updating the current speed value as long as the FAN_SPD value is less than or equal to the THRSH value.

When the FAN_SPD value exceeds the THRSH value, OVR_THR bit in FMCSR register is set to 1. An interrupt is also asserted if IRQ_EN bit in FMCSR register is set to 1 (i.e., interrupt is enabled). After OVR_THR bit is set, the FAN_SPD data is no longer updated with new values from the Up Counter. A new value is loaded into FAN_SPD data only after OVR_THR bit is cleared by writing 1. This guarantees that the FAN_SPD value that generated the interrupt remains available for the interrupt handler.

If the Up Counter exceeds FFFFh, OVFLOW bit in FMCSR register is set to 1, the FAN_SPD data is set to FFFFh, and the interrupt is asserted (if enabled). The FAN_SPD data continues to be updated with new values from the Up Counter. OVFLOW bit is cleared to 0 when 1 is written to it.

8.0 Fan Speed Monitor (Continued)

To read the FAN_SPD data:

- Read the FMSPRL register: This reads the low byte of the FAN_SPD data and saves the high byte in a latch. In addition, the SPD_RDY bit in the FMCSR register is cleared to 0.
- Read the FMSPRH register: This reads the high byte of the FAN_SPD data from the latch.

.

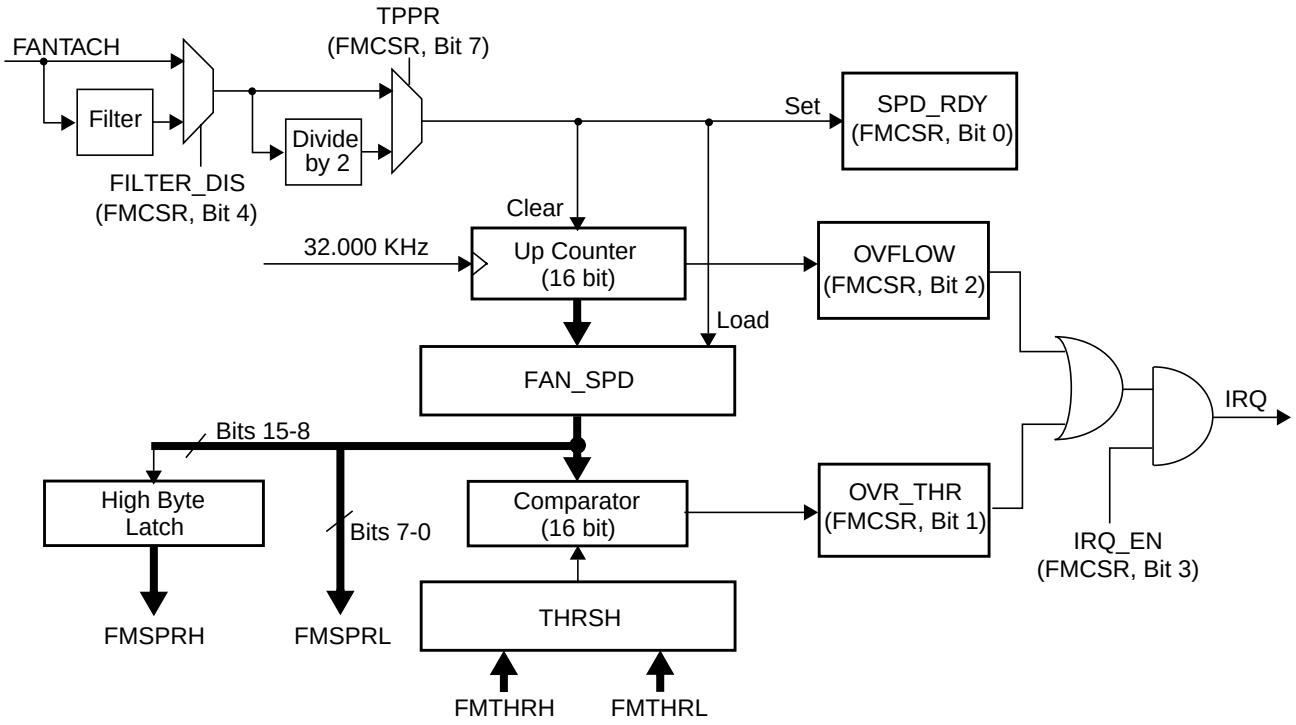


Figure 20. Fan Speed Monitor (Simplified Diagram)

8.0 Fan Speed Monitor (Continued)

8.3 FAN SPEED MONITOR REGISTERS

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from register (write to the same address is to a different register).
- W = Write (see above).
- RO = Read Only.
- WO = Write Only. Reading from the bit returns 0.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

8.3.1 Fan Speed Monitor Register Map

Table 42. Fan Speed Monitor Register Map

Offset	Mnemonic	Register Name	Type	Power Well	Section
Device specific[1]	FMTHRL	Fan Speed Monitor Threshold Low	R/W	V_{DD3}	8.3.2
Device specific[1]	FMTHRH	Fan Speed Monitor Threshold High	R/W	V_{DD3}	8.3.3
Device specific[1]	FMSPRL	Fan Speed Monitor Speed Low	RO	V_{DD3}	8.3.4
Device specific[1]	FMSPRH	Fan Speed Monitor Speed High	RO	V_{DD3}	8.3.5
Device specific[1]	FMCSR	Fan Speed Monitor Control and Status	Varies per bit	V_{DD3}	8.3.6

1. The location of this register is defined in Section 3.15.1 on page 67.

8.3.2 Fan Speed Monitor Threshold Low Register (FMTHRL)

This register holds the low byte (bits 7-0) of the lowest permitted fan speed value. It is reset to FFh.

Power Well: V_{DD3}

Location: Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**THRSH_LOW**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**THRSH_LOW (Fan Speed Threshold Value - Low).** This field contains the low byte of the threshold setting, indicating the lowest permitted fan speed value. If the number of clock cycles counted in one fan revolution is higher than the THRSH value, OVR_THR bit is set in FMCSR register and the FAN_SPD data is “frozen” at its last value. In addition, an interrupt (if enabled) is issued. To prevent unpredictable results, the contents of this register can only be changed when the corresponding FANMON_EN bit in FSCMCF1 or FSCMCF2 register is reset to 0 (see Section 3.15.3 on page 68 and Section 3.15.4 on page 69).

8.0 Fan Speed Monitor (Continued)

8.3.3 Fan Speed Monitor Threshold High Register (FMTHRH)

This register holds the high byte (bits 15-8) of the lowest permitted fan speed value. It is reset to FFh.

Power Well: V_{DD3}

Location: Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**THRSH_HIGH**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**THRSH_HIGH (Fan Speed Threshold Value - High).** This field contains the high byte of the threshold for the lowest permitted fan speed value; see Section 8.3.2 on page 112 for the description of this field.

8.3.4 Fan Speed Monitor Speed Low Register (FMSPRL)

This register contains the low byte (bits 7-0) of the current fan speed value, which is updated once per fan revolution. It is reset to 00h. Whenever the FMSPRL register is read, the high byte of the FAN_SPD data is latched to save the current fan speed value until FMSPRH register is read. Therefore, the FMSPRL register must be read first. When FMSPRL register is read, SPD_RDY bit in FMCSR register is reset.

The FAN_SPD data is reset when one of the following conditions occurs:

- System reset (see Section 2.2 on page 29).
- The corresponding FANMON_EN bit in FSCMCF1 or FSCMCF2 register is reset to 0 (see Section 3.15.3 on page 68 and Section 3.15.4 on page 69).

Power Well: V_{DD3}

Location: Device specific

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**FAN_SPD_LOW**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**FAN_SPD_LOW (Fan Speed Value - Low).** This field contains the low byte of the current fan speed value. The 16-bit FAN_SPD data represents the number of clock cycles counted during one full revolution of the fan, according to the setting of TPPR bit in FMCSR register. When SPD_RDY bit is set in FMCSR register, FAN_SPD contains new speed data that has not yet been read.

8.0 Fan Speed Monitor (Continued)

8.3.5 Fan Speed Monitor Speed High Register (FMSPRH)

This register contains the high byte (bits 15-8) of the current fan speed value, which is updated once per fan revolution. It is reset to 00h. FMSPRH register must be read last; see Section 8.3.4 on page 113.

Power Well: V_{DD3}

Location: Device specific

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**FAN_SPD_HIGH**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**FAN_SPD_HIGH (Fan Speed Value - High).** This field contains the high byte of the current fan speed value. See Section 8.3.4 on page 113 for the description of this field.

8.3.6 Fan Speed Monitor Control and Status Register (FMCSR)

This register contains control and status bits of the Fan Speed Monitor unit. FMCSR is reset to 10h.

Power Well: V_{DD3}

Location: Device specific

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**TPPR**	**Reserved**		**FILTER_DIS**	**IRQ_EN**	**OVFLOW**	**OVR_THR**	**SPD_RDY**
Reset	0	0	0	1	0	0	0	0

Bit	Type	Description
7	R/W	**TPPR (Tachometer Pulses Per Revolution).** This bit selects the number of pulses per fan revolution generated by the tachometer and thus the division factor of the incoming pulses at the FANTACH pin. 0: Two pulses per revolution: division by 2 (default) 1: One pulse per revolution: no division To prevent unpredictable results, the value of this bit can only be changed when the corresponding FANMON_EN bit in FSCMCF1 or FSCMCF2 register is reset to 0 (see Section 3.15.3 on page 68 and Section 3.15.4 on page 69).
6-5	–	**Reserved.**
4	R/W	**FILTER_DIS (Filter Disable).** When this bit is set to 1, the digital Low Pass Filter on the FANTACH input is disabled. 0: Digital Low Pass Filter enabled 1: Digital Low Pass Filter disabled (default) To prevent unpredictable results, the value of this bit can only be changed when the corresponding FANMON_EN bit in FSCMCF1 or FSCMCF2 register is reset to 0 (see Section 3.15.3 on page 68 and Section 3.15.4 on page 69).
3	R/W	**IRQ_EN (Fan Interrupt Enable).** This bit controls the routing of Overflow and Over Threshold events to the FSCM module interrupt. 0: Interrupt disabled (default) 1: Interrupt enabled. An interrupt is asserted when either OVR_THR bit or OVFLOW bit is set to 1.
2	R/W1C	**OVFLOW (Overflow).** This bit indicates that the number of clock cycles counted during one full revolution of the fan exceeds 65536 (FFFFh) clocks. This is equivalent to a fan speed slower than 29.3 RPM. At this speed, fan cooling is inefficient; therefore, the fan is considered stopped and an interrupt (if enabled) is issued. Writing 1 to this bit clears it to 0. 0: No overflow occurred since the last time this bit was cleared by writing 1 (default) 1: Counter overflow (FFFFh) occurred

8.0 Fan Speed Monitor (Continued)

Bit	Type	Description
1	R/W1C	**OVR_THR (Over Threshold).** This bit indicates that the FAN_SPD value (current speed) is higher than the THRSH value. This is equivalent to a fan speed slower than [60 * 32000 / THRSH] RPM. At this speed, the fan cooling is less efficient; therefore, an interrupt (if enabled) is issued. Writing 1 to this bit clears it to 0. 0: No Over Threshold occurred since the last time this bit was cleared by writing 1 (default) 1: FAN_SPD value is higher than THRSH value
0	RO	**SPD_RDY (Speed Data Ready).** This bit indicates that the FAN_SPD data contains a new current speed value that has not yet been read. SPD_RDY is set to 1 on each “active” tachometer pulse (after the division selected by TPPR bit) received at the FANTACH input, starting from the third “active” pulse, if OVR_THR bit is 0. SPD_RDY is cleared to 0 whenever FMSPRL register is read or when OVFLOW bit is set. 0: The FAN_SPD data is either invalid or has already been read (default) 1: FAN_SPD data contains a new value

8.4 FAN SPEED MONITOR REGISTER BITMAP

Table 43. Fan Speed Monitor Register Bitmap

Register		Bits							
Offset[1]	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Device Specific	FMTHRL	THRSH_LOW							
Device Specific	FMTHRH	THRSH_HIGH							
Device Specific	FMSPRL	FAN_SPD_LOW							
Device Specific	FMSPRH	FAN_SPD_HIGH							
Device Specific	FMCSR	TPPR	Reserved		FILTER_DIS	IRQ_EN	OVFLOW	OVR_THR	SPD_RDY

1. The location of these registers is defined in Section 3.15.1 on page 67.

9.0 Glue Functions

This chapter describes the glue functions integrated in the PC87373 device.

9.1 OVERVIEW

This module contains 11 glue functions. Most of them operate independently of the other functions and of the other modules in the PC87373 device.

The 11 glue functions are divided into three groups:

- Power-related functions:
  - Highest active Main supply reference (REF5V)
  - Highest active Standby supply reference (REF5V_STBY)
  - Resume reset ($\overline{\text{RSMRST}}$)
  - Main power good (PWRGD_3V)
  - Rambus SCK clock gate control (SCK_BJT_GATE)
  - Power distribution control ($\overline{\text{BKFD\_CUT}}$, LATCHED_BF_CUT)
  - Main power supply control ($\overline{\text{PS\_ON}}$)
- Miscellaneous functions:
  - CNR downstream codec dynamic control ($\overline{\text{CDC\_DWN\_RST}}$)
  - Hard-disk LED indicator control ($\overline{\text{HD\_LED}}$)
- SMBus support functions:
  - SMBus voltage translation (3V_DDCSCL, 3V_DDCSDA, 5V_DDCSCL, 5V_DDCSDA)
  - SMBus isolation (SMB1_SCL, SMB1_SDA, SMB2_SCL, SMB2_SDA)

Each function is described in the following sections.

9.2 FUNCTIONAL DESCRIPTION

9.2.1 Highest Active Main Supply Reference

This function generates the REF5V analog output signal (see specification in Section 13.2.10 on page 155). When the Main power supply is turned on or off, the REF5V signal tracks either the V_{DD3} or V_{DD5} power supplies, whichever has a higher voltage.

The circuit that generates the REF5V output is composed of two parts:

- One part tracks the V_{DD3} supply voltage and is implemented in the PC87373 device.
- One part tracks the V_{DD5} supply voltage and is implemented by an external resistor connected to the V_{DD5} power supply.

Figure 21 shows a simplified diagram of the circuit that generates the REF5V analog output signal

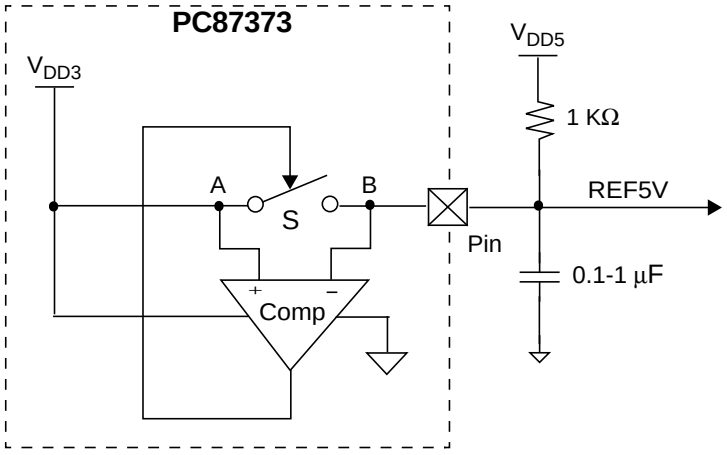


Figure 21. REF5 Generation (Simplified Diagram)

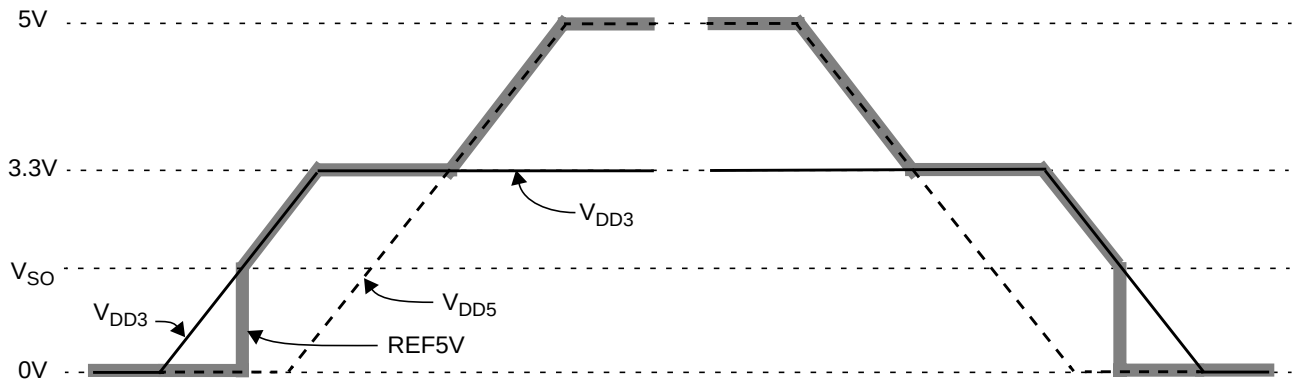
9.0 Glue Functions (Continued)

The voltage levels at both sides of switch “S” are measured by the comparator (“Comp”), which controls the state of the switch as follows:

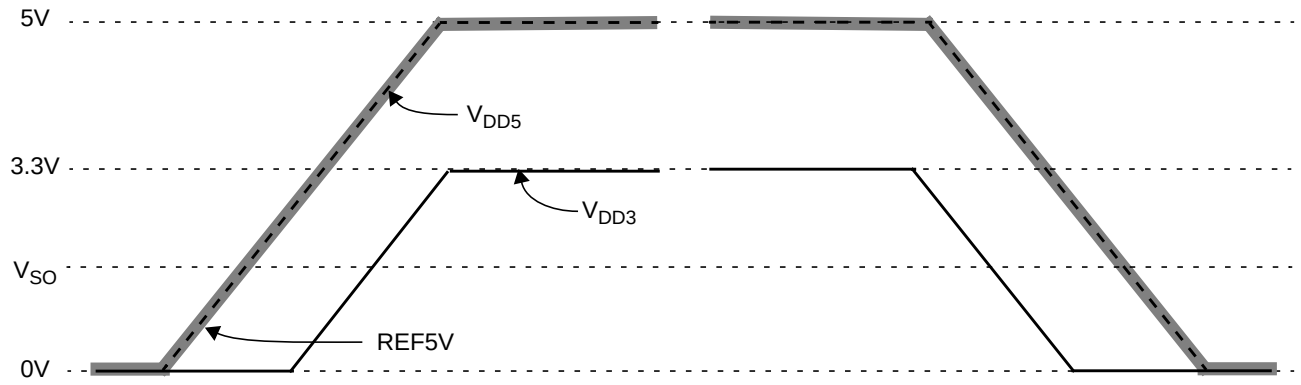
- If $V_A > V_B$, then $V_{DD3} > V_{DD5}$; the switch is **closed**, and the output voltage $V_{REF5V} = V_{DD3}$.
- If $V_A < V_B$, then $V_{DD3} < V_{DD5}$; the switch is **open**, and the output voltage $V_{REF5V} = V_{DD5}$, through the external 1 KΩ resistor, is connected to the V_{DD5} power supply.

The internal circuit is powered from the V_{DD3} supply. For $V_{DD3} < V_{SO}$, switch “S” is **open**; therefore, the V_{REF5V} output tracks only the V_{DD5} supply. Figure 22 shows REF5 output in four cases of V_{DD3} and V_{DD5} ramp up and ramp down.

a. V_{DD3} Ramps Up Before and Ramps Down After V_{DD5}



b. V_{DD3} Ramps Up After and Ramps Down Before V_{DD5}



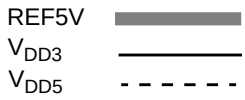


Figure 22. REF5 as a Function of V_{DD3} and V_{DD5}

Table 44 defines the DC characteristics of the REF5 output, relative to the V_{DD3} supply. For the AC characteristics, see *Highest Active Main and Standby Supply Reference* on page 170.

Table 44. REF5V DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{SO}	Switch Open, V_{DD3} Voltage Range	$0 < V_{DD5} < 5.5V$	0	1.5[1]	V
V_{TRK}	Output Voltage Tracking of V_{DD3} Voltage[1,]	$1.5V < V_{DD3}$, $V_{DD5} < V_{DD3} + 150$ mV	− 150	+ 150	mV

1. Not tested. Guaranteed by characterization.

9.0 Glue Functions (Continued)

9.2.2 Highest Active Standby Supply Reference

This function generates the REF5V_STBY analog output signal (see specification in Section 13.2.10 on page 155). When the Standby power supply is turned on or off, the REF5V_STBY signal tracks either the V_{SB3} or V_{SB5} power supplies, whichever has a higher voltage.

The circuit that generates the REF5V_STBY output is composed of two parts:

- One part tracks the V_{SB3} supply voltage and is implemented in the PC87373 device.
- One part tracks the V_{SB5} supply voltage and is implemented by an external resistor connected to the V_{SB5} power supply.

Figure 23 shows a simplified diagram of the circuit that generates the REF5V_STBY analog output signal

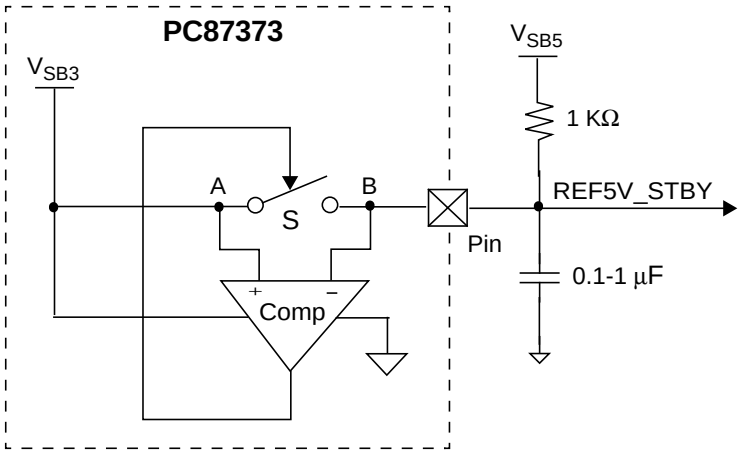


Figure 23. REF5_STBY Generation (Simplified Diagram)

The voltage levels at both sides of switch “S” are measured by the comparator (“Comp”), which controls the state of the switch as follows:

- If $V_A > V_B$, then $V_{SB3} > V_{SB5}$; the switch is **closed** and the output voltage $V_{REF5V\_STBY} = V_{SB3}$
- If $V_A < V_B$, then $V_{SB3} < V_{SB5}$; the switch is **open** and the output voltage $V_{REF5V\_STBY} = V_{SB5}$, through the external 1 KΩ resistor, is connected to the V_{SB5} power supply

The internal circuit is powered from the V_{SB3} supply. For $V_{SB3} < V_{SO}$, switch “S” is **open**; therefore, the V_{REF5V_STBY} output tracks only the V_{SB5} supply. Figure 24 shows the behavior of the REF5V_STBY output in four cases of V_{SB3} and V_{SB5} ramp up and ramp down.

9.0 Glue Functions (Continued)

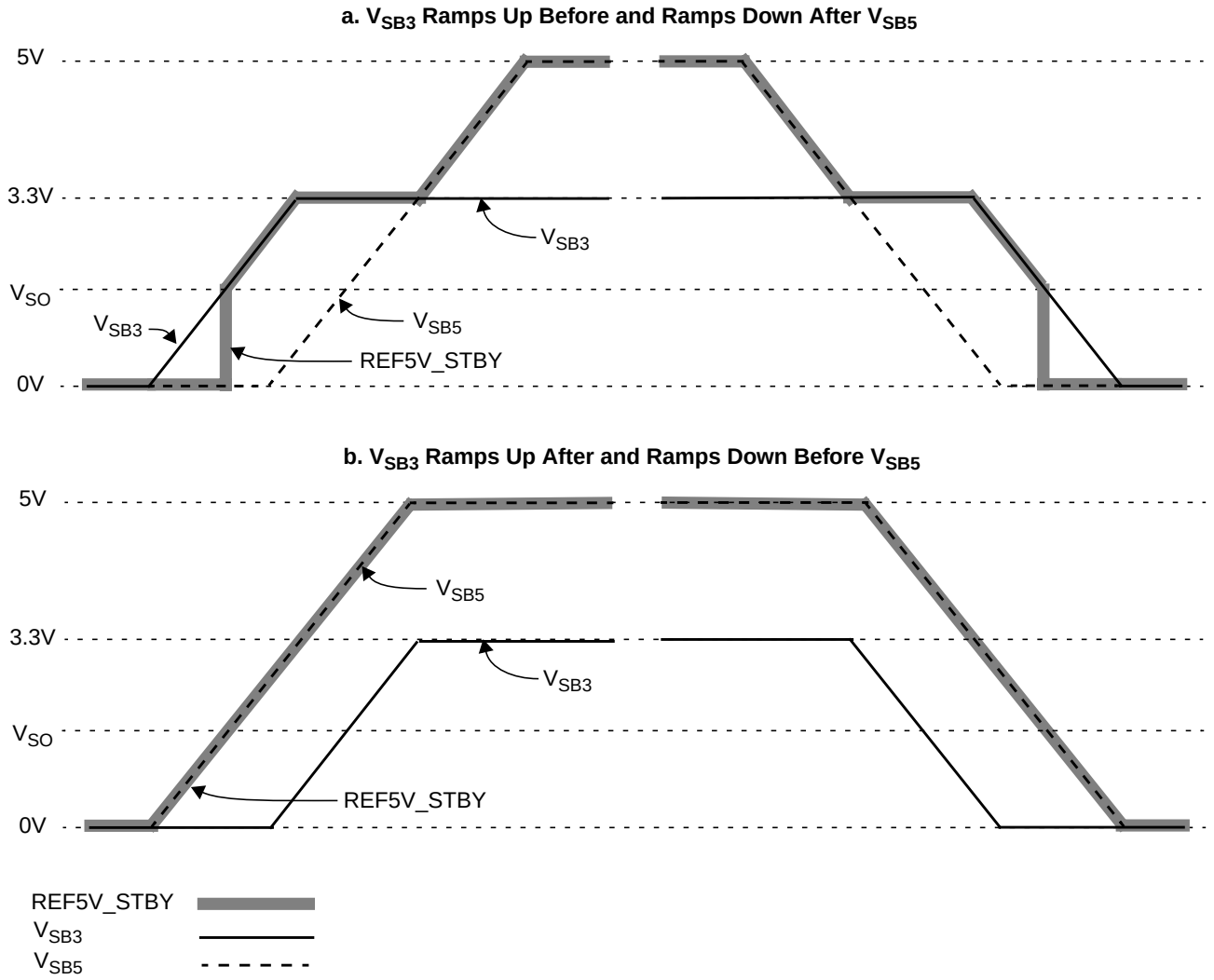


Figure 24. REF5_STBY as a Function of V_{SB3} and V_{SB5}

Table 44 defines the DC characteristics of the REF5_STBY output relative to the V_{SB3} supply. For the AC characteristics, see *Highest Active Main and Standby Supply Reference* on page 170.

Table 45. REF5V_STBY DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{SO}	Switch Open, V_{SB3} Voltage Range	$0 < V_{SB5} < 5.5V$	0	1.5[1]	V
V_{TRK}	Output Voltage Tracking of V_{SB3} Voltage[1,]	$1.5V < V_{SB3}$, $V_{SB5} < V_{SB3} + 150$ mV	− 150	+ 150	mV

1. Not tested. Guaranteed by characterization.

9.0 Glue Functions (Continued)

9.2.3 Resume Reset

This function generates the $\overline{\text{RSMRST}}$ signal by sensing the voltage level at the V_{SB5} analog input (see specification in Section 13.2.6 on page 154). The $\overline{\text{RSMRST}}$ signal serves both as a Power-Up reset and as a "Brown-Out" reset for the system resume power well (powered by the V_{SB3} or V_{SB5} supplies).

The Resume Reset circuit compares the voltage at the V_{SB5} input with a threshold value (V_{TRIP}). When the V_{SB3} supply voltage is active, the circuit generates the $\overline{\text{RSMRST}}$ active low output signal, as follows:

- When V_{SB5} rises above V_{TRIP}, the $\overline{\text{RSMRST}}$ signal switches from low to high after a t_{RD} delay.
- When V_{SB5} falls below V_{TRIP}, the $\overline{\text{RSMRST}}$ signal switches from high to low after a t_{FD5} delay.
- When a glitch shorter than t_{GA} (the time V_{SB5} is below V_{TRIP}) occurs at the V_{SB5} input, the $\overline{\text{RSMRST}}$ signal is not guaranteed to react (remains high).

The Resume Reset circuit is powered by the V_{SB3} supply. When the V_{SB5} supply voltage is active, the circuit compares the V_{SB3} power supply voltage with the threshold value (V_{SB3ON} or V_{SB3OFF}); see Section 13.1.5 on page 152. As a result, the $\overline{\text{RSMRST}}$ active low output signal is generated, as follows:

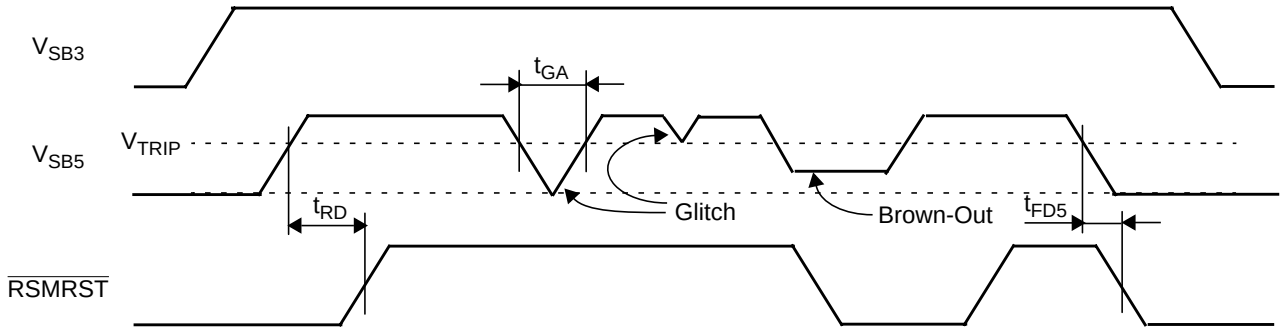
- When V_{SB3} rises above V_{SB3ON}, the $\overline{\text{RSMRST}}$ signal switches from low to high after a t_{RD} delay.
- When V_{SB3} falls below V_{SB3OFF}, the $\overline{\text{RSMRST}}$ signal switches from high to low after a t_{FD3} delay.
- When a glitch shorter than t_{GA} (the time V_{SB3} is below V_{SB3OFF}) occurs at the V_{SB3} input, the $\overline{\text{RSMRST}}$ signal is not guaranteed to react (remains high).

When the V_{SB3} power supply is off, the $\overline{\text{RSMRST}}$ output is at low level (active) having an internal impedance of Z_{OFF}.

The delays in $\overline{\text{RSMRST}}$ switching, generated by the Resume Reset circuit, are independent of the toggling of any of the clock domains of the PC87373 device (32 KHz, 48 MHz or LPC).

Figure 25 shows the behavior of the $\overline{\text{RSMRST}}$ output at V_{SB3} and V_{SB5} switching.

a. V_{SB5} Switching, V_{SB3} Steady



b. V_{SB3} Switching, V_{SB5} Steady

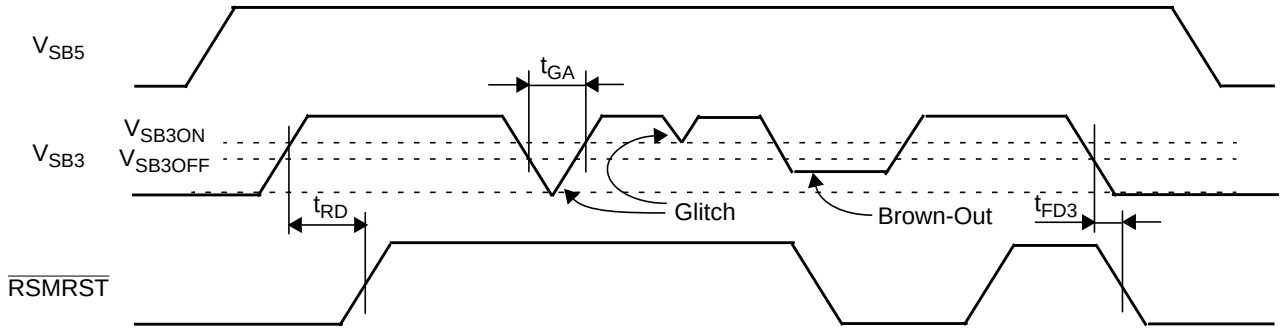


Figure 25. $\overline{\text{RSMRST}}$ at V_{SB5} and V_{SB3} Switching

9.0 Glue Functions (Continued)

Table 46 defines the DC characteristics of the Resume Reset circuit. For the AC characteristics, see *Resume Reset* on page 170.

Table 46. Resume Reset Circuit DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{TRIP}	V_{SB5} Threshold Level	V_{SB3} = 3.3V ±10%	4.05	4.5	V
Z_{OFF}	Output Impedance at V_{SB3} Off[1]	V_{SB3} = 0V, V_{SB5} = 5V ±10%	TBD	TBD	KΩ

1. Not tested. Guaranteed by characterization.

9.2.4 Main Power Good

This function generates the PWRGD_3V signal, indicating that the Main power supply voltage is valid and the reset button on the front panel is not pressed. The PWRGD_3V signal indicates to system components that their input power supplies are valid.

The $\overline{\text{FPRST}}$ input is debounced for at least t_{DB} before entering the Main Power Good circuit, to ensure that the signal is stable. The debouncer adds a t_{DB} delay to the PWRGD_3V output change in output caused by the $\overline{\text{FPRST}}$ input. The debouncer timing is based on the 32 KHz clock domain, which therefore must be valid to enable the correct operation of the Power Good function.

The PWRGD_3V is the AND function of the PWRGD_PS and $\overline{\text{FPRST}}$ inputs. Figure 26 shows a simplified diagram of the circuit that generates the PWRGD_3V signal.

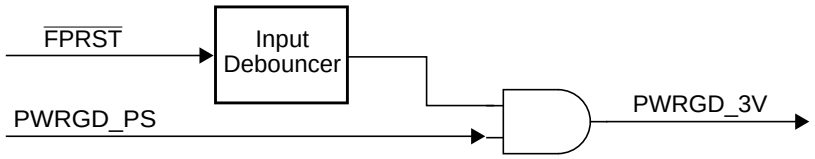


Figure 26. PWRGD_3V Generation (Simplified Diagram)

For the AC characteristics, see *Main Power Good* on page 171.

9.2.5 Rambus SCK Clock Gate Control

This function generates the SCK_BJT_GATE signal, which controls an external circuit that gates the SCK clock to the Rambus socket.

The SCK clock to the Rambus socket is disabled by an active high SCK_BJT_GATE signal, generated when either the Main power supply voltage is not valid **or** the reset button on the front panel is pressed (PWRGD_3V = low).

Figure 27 shows a simplified diagram of the circuit that generates the SCK_BJT_GATE signal.

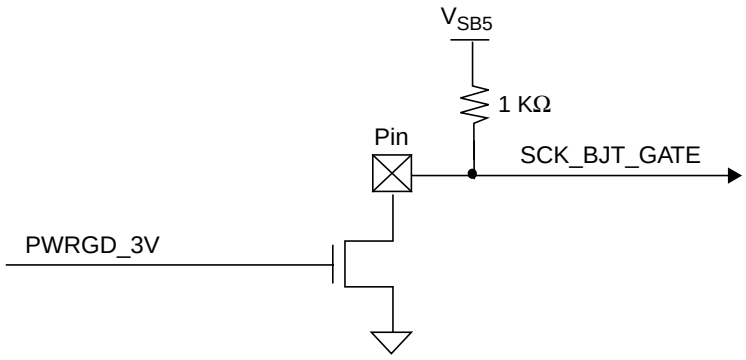


Figure 27. SCK_BJT_GATE Generation (Simplified Diagram)

For the AC characteristics, see *CNR Downstream Codec Dynamic Control* on page 172.

9.0 Glue Functions (Continued)

9.2.6 Power Distribution Control

This function generates the $\overline{\text{BKFD\_CUT}}$ and the LATCHED_BF_CUT power distribution control signals.

An active low $\overline{\text{BKFD\_CUT}}$ signal is generated when the Main power supply voltage is valid (PWRGD_PS = high) **and** the system is **not** in one of the S3 to S5 sleep states ($\overline{\text{SLP\_S3}}$ = high).

The LATCHED_BF_CUT signal is generated from $\overline{\text{BKFD\_CUT}}$ and $\overline{\text{SLP\_S5}}$ as follows:

- Rising edge of $\overline{\text{BKFD\_CUT}}$ while the system is **not** in S5 sleep state ($\overline{\text{SLP\_S5}}$ = high) sets LATCHED_BF_CUT to high.
- Falling edge of $\overline{\text{BKFD\_CUT}}$ while the system is **not** in S5 sleep state ($\overline{\text{SLP\_S5}}$ = high) resets LATCHED_BF_CUT to low.
- When the system is in S5 sleep state ($\overline{\text{SLP\_S5}}$ = low), LATCHED_BF_CUT is reset to low.

Figure 28 shows a simplified diagram of the circuit that generates the $\overline{\text{BKFD\_CUT}}$ and the LATCHED_BF_CUT signals.

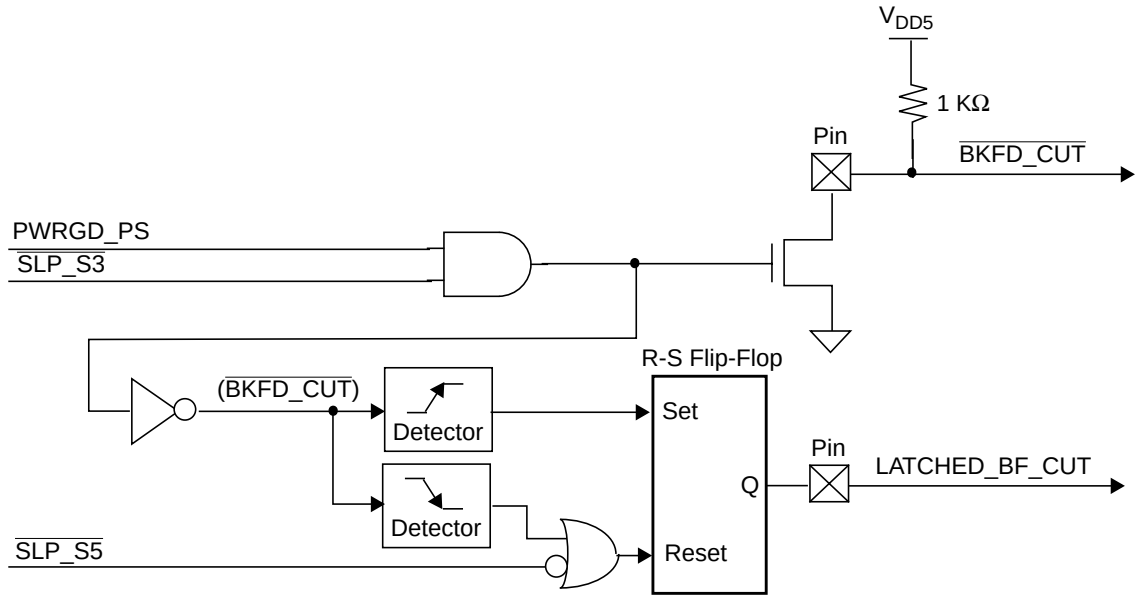


Figure 28. $\overline{\text{BKFD\_CUT}}$ and LATCHED_BF_CUT Generation (Simplified Diagram)

For the AC characteristics, see *Power Distribution Control* on page 171.

9.2.7 Main Power Supply Control

This function generates the $\overline{\text{PS\_ON}}$ signal, which turns the Main power supply on and off.

The Main power supply is turned on by an active low $\overline{\text{PS\_ON}}$ signal, generated when the processor is currently inserted in its socket ($\overline{\text{CPU\_PRESENT}}$ = low) **and** the system is **not** in one of the S3 to S5 sleep states ($\overline{\text{SLP\_S3}}$ = high).

Figure 29 shows a simplified diagram of the circuit that generates the $\overline{\text{PS\_ON}}$ signal.

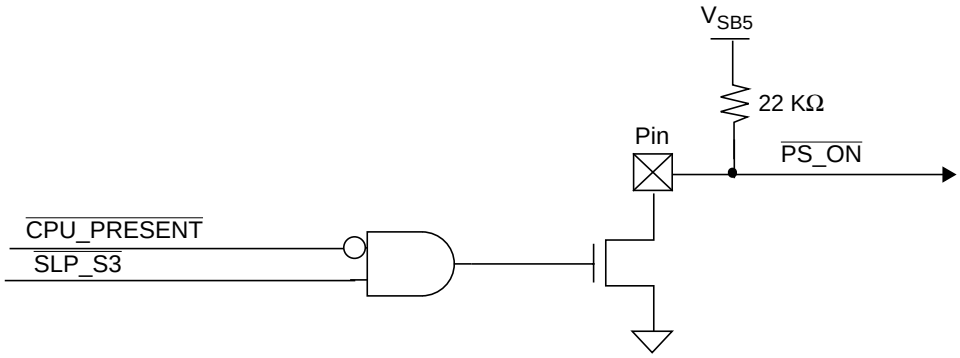


Figure 29. $\overline{\text{PS\_ON}}$ Generation (Simplified Diagram)

For the AC characteristics, see *Main Power Supply Control* on page 172.

9.0 Glue Functions (Continued)

9.2.8 CNR Downstream Codec Dynamic Control

This function generates the $\overline{\text{CDC\_DWN\_RST}}$ signal, which enables the audio CNR board.

An active low codec reset signal ($\overline{\text{CDC\_DWN\_RST}}$) is generated either when an active (low) $\overline{\text{AUD\_LINK\_RST}}$ is received **or** when CNR Downstream Codec is disabled ($\overline{\text{CDC\_DWN\_ENAB}}$ = high).

The level of the $\overline{\text{CDC\_DWN\_ENAB}}$ system configuration signal is controlled as follows:

- Externally, by connecting a pull-down resistor between the $\overline{\text{CDC\_DWN\_ENAB}}$ pin and GND (in this case, the output buffer of GPIO14 must be disabled; see Section 3.14.4 on page 64)
- Internally, by enabling the output buffer of GPIO14 and by writing the required level for $\overline{\text{CDC\_DWN\_ENAB}}$ to bit 4 of GPDO1 (or GPDIO1) register; see Section 5.4.3 on page 78 (in this case, it is not necessary to remove the pull-down resistor if it is connected between the $\overline{\text{CDC\_DWN\_ENAB}}$ pin and GND).

Figure 30 shows a simplified diagram of the circuit that generates the $\overline{\text{CDC\_DWN\_RST}}$ signal.

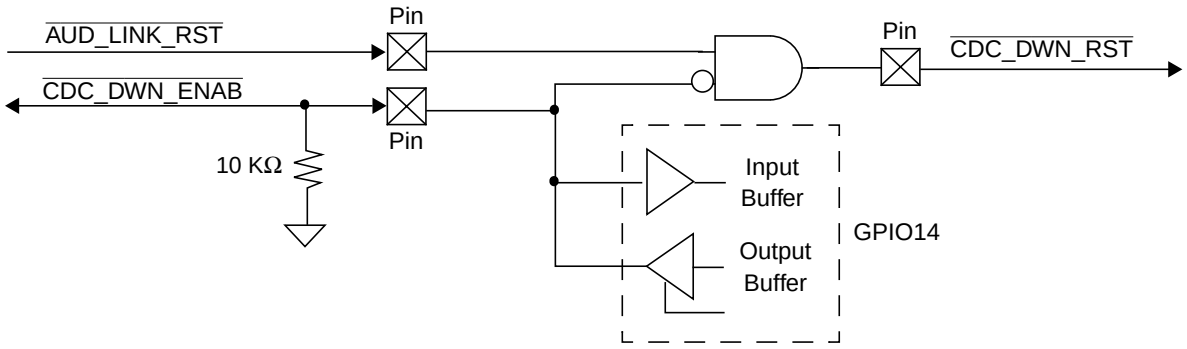


Figure 30. $\overline{\text{CDC\_DWN\_RST}}$ Generation (Simplified Diagram)

For the AC characteristics, see *CNR Downstream Codec Dynamic Control* on page 172.

9.2.9 Hard-Disk LED Indicator Control

This function generates the $\overline{\text{HD\_LED}}$ signal, which controls the Hard Drive, red LED indicator.

The Hard Drive LED is turned on by an active low $\overline{\text{HD\_LED}}$ signal, generated when at least one of the $\overline{\text{PRIMARY\_HD}}$ **or** $\overline{\text{SECONDARY\_HD}}$ **or** $\overline{\text{SCSI}}$ pins is active (low).

Figure 31 shows a simplified diagram of the circuit that generates the $\overline{\text{HD\_LED}}$ signal.

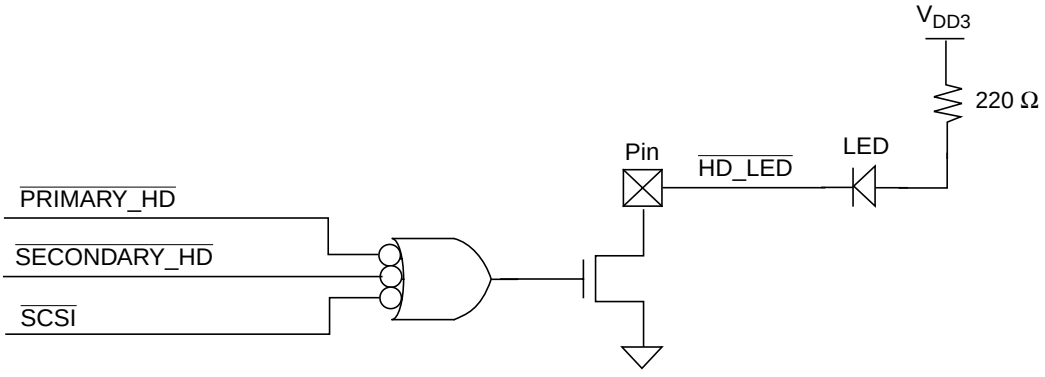


Figure 31. $\overline{\text{HD\_LED}}$ Generation (Simplified Diagram)

9.2.10 SMBus Voltage Translation

This function performs "passive" level translation between the V_{DD3}-powered 3V_DDCSCL and 3V_DDCSDA signals and the V_{DD5}-powered 5V_DDCSCL and 5V_DDCSDA signals, respectively, for interfacing the Data Display Channel.

The signals connected to the 3V_DDCSCL, 3V_DDCSDA, 5V_DDCSCL and 5V_DDCSDA pins are compatible with Intel's SMBus (*Specification Rev 1.1, Dec. 11, 1998*) two-wire synchronous serial interface specifications.

9.0 Glue Functions (Continued)

The 3V_DDCSCL and 5V_DDCSCL pins are connected through a switch. This switch is controlled by a Level Translation Control circuit, according to the voltage levels at the 3V_DDCSCL and 5V_DDCSCL pins (for the DC characteristics, see Section 13.2.11 on page 156):

- For $V_{IN} < V_{ISC}$ at **either** pin, the switch is closed; therefore, both pins (3V_DDCSCL, and 5V_DDCSCL) are held at low level.
- For $V_{IN} > V_{ISO}$ at **both** pins, the switch is open; therefore, each pin is pulled up to high level by the external resistor connected to V_{DD3} (for the 3V_DDCSCL pin) and to V_{DD5} (for the 5V_DDCSCL pin).

In addition, when the V_{DD3} power is off, the switch is open, regardless of the voltage levels at the 3V_DDCSCL and 5V_DDCSCL pins.

The 3V_DDCSDA and 5V_DDCSDA pins are connected through a similar level translation circuit and behave like 3V_DDCSCL and 5V_DDCSCL.

Figure 32 shows a simplified diagram of the circuit that performs SMBus voltage translation.

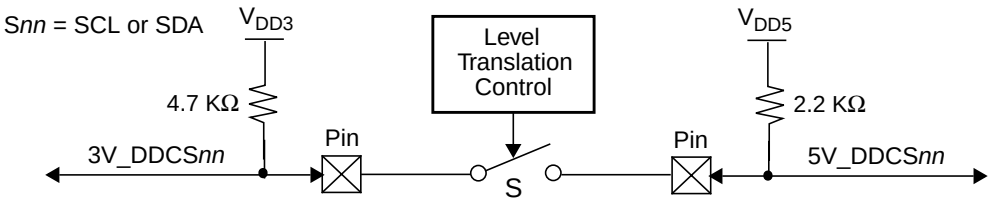


Figure 32. SMBus Voltage Translation (Simplified Diagram)

For the AC characteristics, see *SMBus Voltage Translation and Isolation Timing* on page 172.

9.2.11 SMBus Isolation

When the Main power is off, this function performs “passive” bus isolation between the SMB1_SCL, SMB1_SDA signals and the SMB2_SCL, SMB2_SDA signals respectively. The bus isolation enables the operation of the serial bus section connected to Standby power, if the other serial bus is connected to the Main power and the Main power is off.

The signals connected to the SMB1_SCL, SMB1_SDA, SMB2_SCL and SMB2_SDA pins are compatible Intel's SMBus (*Specification Rev 1.1, Dec. 11, 1998*) two-wire synchronous serial interface specifications.

The SMB1_SCL and SMB2_SCL pins are connected through a switch. This switch is controlled by the voltage levels at the SMB1_SCL and SMB2_SCL pins (for the DC characteristics, see Section 13.2.11 on page 156):

- For $V_{IN} < V_{ISC}$ at **either** pin, the switch is closed; therefore, both pins (SMB1_SCL, and SMB2_SCL) are held at low level.
- For $V_{IN} > V_{ISO}$ at **both** pins, the switch is open; therefore, each pin is pulled up to high level by the external resistor connected to V_{SUP1} (for the SMB1_SCL pin) and to V_{SUP2} (for the SMB2_SCL pin).

In addition, when the Main power supply voltage is not valid (PWRGD_PS = low), the switch is forced open and the unpowered SMB*x*_SCL signal is disconnected from the powered SMB*x*_SCL signal (*x* is either 1 or 2). This isolation between the two signals prevents the loading of the powered SMB*x*_SCL signal by the unpowered SMB*x*_SCL signal.

The SMB1_SDA and SMB2_SDA pins are connected through a similar level isolation circuit and behave like SMB1_SCL and SMB2_SCL.

Figure 33 shows a simplified diagram of the circuit that performs SMBus isolation.

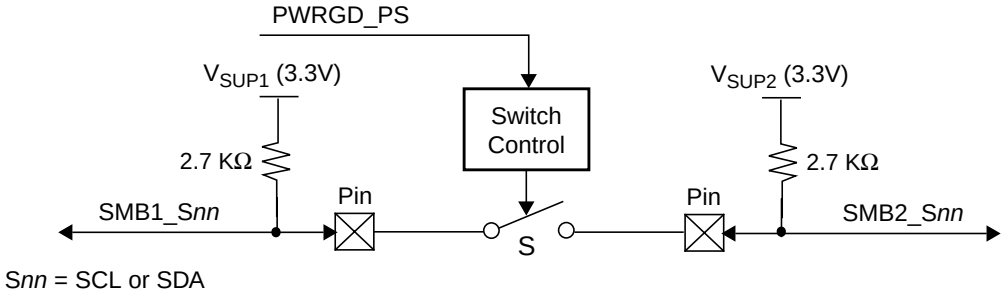


Figure 33. SMBus Isolation (Simplified Diagram)

For the AC characteristics, see *SMBus Voltage Translation and Isolation Timing* on page 172.

10.0 Game Port (GMP)

10.1 OVERVIEW

This chapter describes a generic Game Port. For the implementation used in this device, see Section 3.16.1 on page 70.

The Game Port monitors the interface of up to two game devices and provides data that can be used to determine the status of these game devices at any specific moment.

A game device is an instrument used for inputting commands to a PC, usually to control a game executed on that PC. The game device inputs these commands passively, by indicating several status parameters that can be captured by the system via the Game Port. A joystick is a commonly used game device.

The status of a game device includes the following parameters:

- Button status (pressed/released) of up to two buttons per game device
- Horizontal (X-axis) position indicated by the game device
- Vertical (Y-axis) position indicated by the game device

Figure 34 shows the basic system configuration of the Game Port.

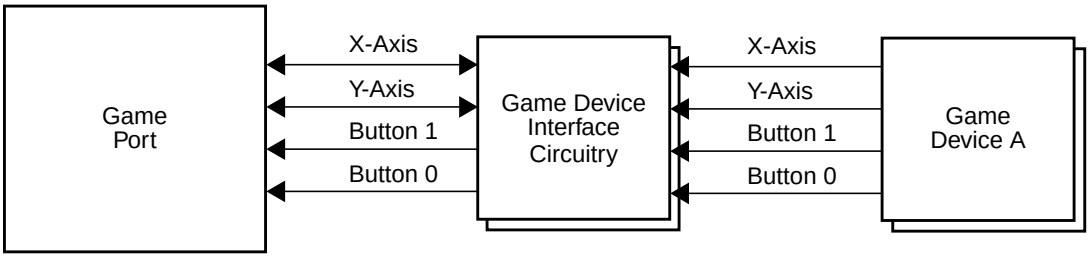


Figure 34. Game Port System Configuration

10.2 FUNCTIONAL DESCRIPTION

10.2.1 Game Device Axis Position Indication

A typical game device has the following interface pins:

- X-axis position indicator
- Y-axis position indicator
- One or two button status indicator(s)

The X and Y axis indicators are fed into the Game Port via pins JOYnX and JOYnY, respectively, where ‘n’ indicates the game device number. The status indicators of buttons 0 and 1 are fed into the Game Port via JOYnBTN0,1, respectively.

The X and Y axis position indication mechanism of each game device includes external components, as shown in Figure 35. Such a mechanism is implemented for each axis line of each game device.

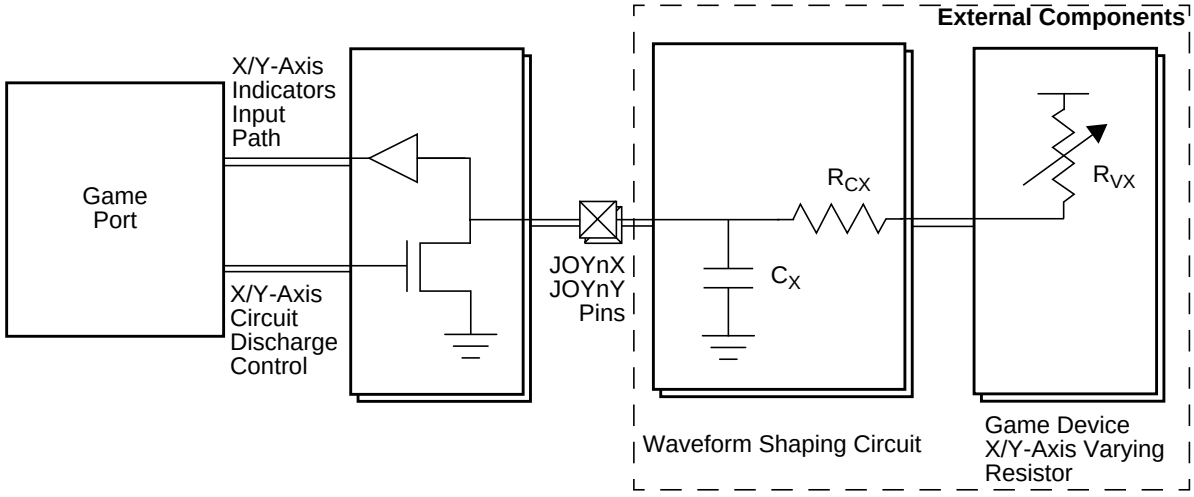


Figure 35. Game Device Axis Position Indication Mechanism

10.0 Game Port (GMP) (Continued)

The varying resistors R_{VX} and R_{VY} are typically implemented in the game device. Their resistance values are determined directly by the horizontal and vertical positions, respectively, indicated by the game device. The waveform shaping circuits are typically implemented outside the game device using constant resistors ($R_{CX/Y}$) and constant capacitors ($C_{X/Y}$). Together with $R_{VX/Y}$, these components implement two R-C structures, the varying parameters of which are used to determine the exact position, at any specific moment, indicated by the game device.

When the Game Port is enabled but not in the process of reading a game device position, it drives the JOYnX,Y pins low. In this state, the capacitors $C_{X/Y}$ are completely discharged.

10.2.2 Capturing the Position

The process of capturing the position indicated by the game device is initiated by a command written to the Game Port to release the JOYnX,Y lines, thus allowing the capacitors $C_{X/Y}$ to be charged. This command is given by performing a write access to the Game Port Status Register (GMPST; see Section 10.3.2). Once the JOYnX,Y pins are released, $R_{CX/Y}$ and $R_{VX/Y}$ start charging $C_{X/Y}$, and the voltage level of the JOYnX,Y pins increases until it reaches V_{IH}. This process is shown in Figure 36.

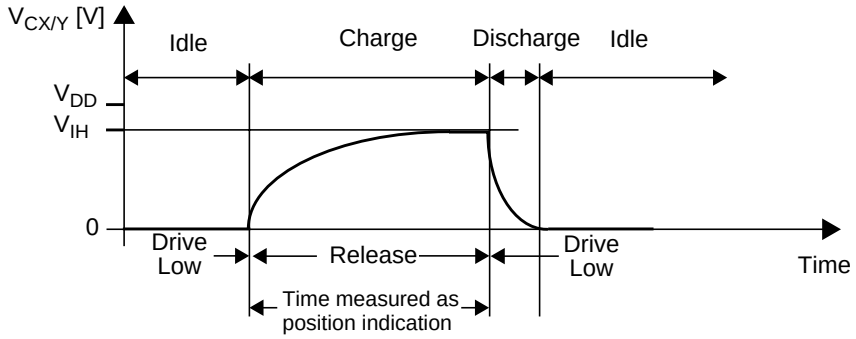


Figure 36. Position Reading Process Waveform (not to scale)

The vertical and horizontal positions indicated by the game device are determined by measuring the time it takes for the voltage level on the JOYnX,Y pins to reach the level of logic 1. Since the charging time is determined by the resistance values of $R_{VX/Y}$, measuring this time actually indicates the resistance values of $R_{VX/Y}$, and therefore also reflects the position indicated by the game device.

Once an axis pin is sensed as logic 1, the axis circuit discharge control is activated to discharge $C_{X/Y}$. This causes the corresponding axis pin to be driven low for approximately 1.5 µs. After that, this axis line is held low until another position reading process is initiated.

During the charge time and the 1.5 µs discharge time that follows, the corresponding axis line does not respond to any status reading process initiation. This prevents software from disturbing the position reading process and makes the position reading processes of all axis lines independent of each other.

10.2.3 Button Status Indication

The button status indication mechanism is shown in Figure 37. Although this figure shows an active-low button (R_{BU0}>>R_{BD0}), the polarity of the button can be either high or low, assuming that the Game Port software is aware of the button's polarity.

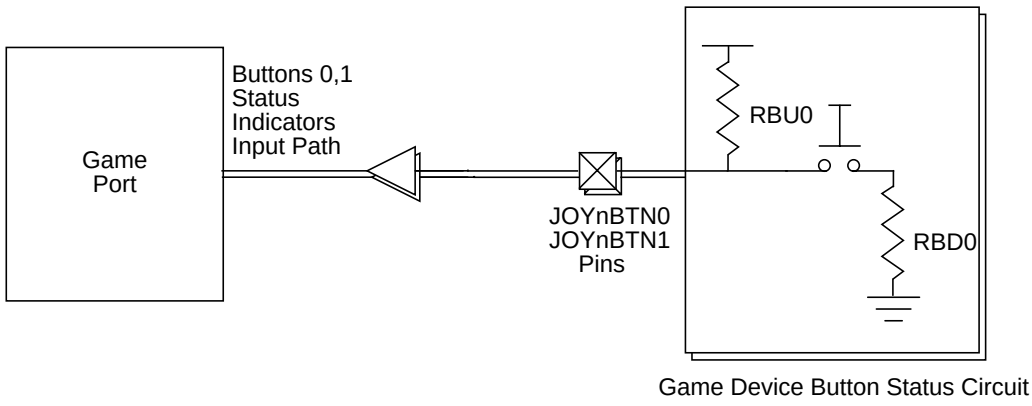


Figure 37. Game Device Button Status Indication Mechanism

10.0 Game Port (GMP) (Continued)

A simple push-button mechanism is typically used to implement the game device buttons. The status of each button is sensed by the Game Port via the JOYnBTN0,1 pins as either high or low, and reflected by the GMPST register. It is the responsibility of the software to determine the actual status of the buttons according to their polarity, which depends on the specific implementation of the system and the game device.

10.2.4 Game Port Operation

The Game Port monitors the game device position and button status indicators by polling their status at a specific moment via the Game Port Status register (GMPST, see Section 10.3.2).

The process of reading the position status of the game device(s) is initiated by performing a write access to the GMPST register. This write access causes the Game Port to release the JOYnX,Y pins. When a JOYnX,Y pin is released, the corresponding bit in the GMPST register is set to 1. To capture the position indicated by the game device, the software should poll the GMPST register and measure the time it takes for the JOYnX,Y to go high. This measurement should be performed by measuring the time during which an axis bit is 1.

Reading the status of the buttons of the game device is done by polling the GMPST register and looking for changes in the bits reflecting the status of the JOYnBTN0,1 pins.

Optional debouncers for the button status pins can be enabled by setting the DBNC_EN bit of the Game Port Configuration register to 1. The Game Port Configuration register is located at Index F0h in the Game Port's logical device configuration space (see Section 3.16.2 on page 70). These debouncers can be used to ensure that the status of a button pin is reflected by the associated GMPST bit only after that pin has been stable for at least 16 ms. If the debouncers are not enabled (default), it is the responsibility of the software to implement the debounce for the button status pins, if necessary.

10.0 Game Port (GMP) (Continued)

10.3 GAME PORT REGISTERS

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from register (write to the same address is to a different register).
- W = Write (see above).
- RO = Read Only.
- WO = Write Only. Reading from the bit returns 0.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

10.3.1 Game Port Register Map

The following table lists the Game Port registers. For the Game Port register bitmap, see Section 10.4 on page 129. The Game Port registers are V_{DD3} powered.

Table 47. Game Port Register Map

Offset	Mnemonic	Register Name	Type	Power Well
00h	GMPST	Game Port Status	RO	V_{DD3}

10.3.2 Game Port Status Register (GMPST)

Reading this register returns the status and the state of Device A and B button and Axis pins, as defined in the table below. Writing to the offset of this register initiates a game device position reading process by forcing a low pulse to be driven on the axis pins.

Power Well: V_{DD3}

Location: Offset 00h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Device B Button 1 Pin Status**	**Device B Button 0 Pin Status**	**Device A Button 1 Pin Status**	**Device A Button 0 Pin Status**	**Device B Y-Axis Pin Status**	**Device B X-Axis Pin Status**	**Device A Y-Axis Pin Status**	**Device A X-Axis Pin Status**
Reset	X	X	X	X	X	X	X	X

Bit	Type	Description
7	RO	**Device B Button 1 Pin Status.** This bit directly reflects the status of Device B Button 1 input pin. 0: Low 1: High
6	RO	**Device B Button 0 Pin Status.** This bit directly reflects the status of Device B Button 0 input pin. 0: Low 1: High
5	RO	**Device A Button 1 Pin Status.** This bit directly reflects the status of Device A Button 1 input pin. 0: Low 1: High
4	RO	**Device A Button 0 Pin Status.** This bit directly reflects the status of Device A Button 0 input pin. 0: Low 1: High
3	RO	**Device B Y-Axis Pin Status.** This bit reflects the state of Device B Y-axis input pin. 0: JOYBY pin is driven low 1: JOYBY pin is released for charging

10.0 Game Port (GMP) (Continued)

Bit	Type	Description
2	RO	**Device B X-Axis Pin Status.** This bit reflects the state of Device B X-axis input pin. 0: JOYBX pin is driven low 1: JOYBX pin is released for charging
1	RO	**Device A Y-Axis Pin Status.** This bit reflects the state of Device A Y-axis input pin. 0: JOYAY pin is driven low 1: JOYAY pin is released for charging
0	RO	**Device A X-Axis Pin Status.** This bit reflects the status of Device A X-axis input pin. 0: JOYAX pin is driven low 1: JOYAX pin is released for charging

10.4 GAME PORT REGISTER BITMAP

Table 48. Game Port Register Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	GMPST	Device B Button 1 Pin Status	Device B Button 0 Pin Status	Device A Button 1 Pin Status	Device A Button 0 Pin Status	Device B Y-Axis Pin Status	Device B X-Axis Pin Status	Device A Y-Axis Pin Status	Device A X-Axis Pin Status

11.0 Musical Instrument Digital Interface (MIDI) Port

11.1 OVERVIEW

This chapter describes a generic MIDI Port. For the implementation used in this device, see Section 3.17.1 on page 71.

The MIDI Port is an asynchronous receiver/transmitter that uses a two-wire, bidirectional, relatively slow communication channel to transmit and receive data bytes to or from MIDI-compliant devices, according to a predefined communication protocol. The MIDI Port is compatible with MPU-401 UART mode.

The MIDI was originally defined to establish a standard interface between computers and digital musical instruments such as synthesizers, and has become the de facto standard for this purpose. However, the MIDI is also commonly used for other purposes, such as communicating with advanced game devices.

The MIDI Port serves as a communication pipe between software and a MIDI device. The software and the MIDI device must interpret the data they exchange and act accordingly.

The MIDI Port supports the following two feature types:

- Legacy (MPU-401)
- Enhanced

Legacy. These include all features supported by MPU-401 UART mode. They can all be operated via the Legacy I/O address space of two bytes, traditionally allocated for the MIDI Port.

Enhanced. These features extend the capabilities of the MIDI Port. They can only be operated if the MIDI is allocated with an address space of at least three bytes.

The basic system configuration of the MIDI Port consists of the port itself, a single pull-up resistor for the MDRX pin, and a MIDI compliant device. This system configuration is shown in Figure 38. The purpose of the pull-up resistor is to make sure that the MIDI Port senses an inactive (high) MIDI receive signal in the absence of a MIDI device.

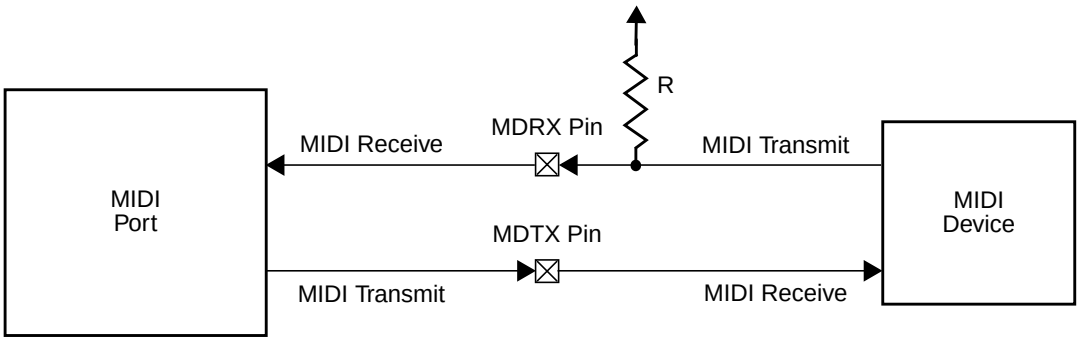


Figure 38. MIDI System Configuration

11.2 FUNCTIONAL DESCRIPTION

The MIDI Port consists of five major functional blocks:

- Internal Bus Interface Unit
- Port Control and Status Registers
- Data Buffers and FIFOs
- MIDI Communication Engine
- MIDI Signals Routing Control Logic

See Figure 39 for a block diagram of the MIDI Port.

11.0 Musical Instrument Digital Interface (MIDI) Port (Continued)

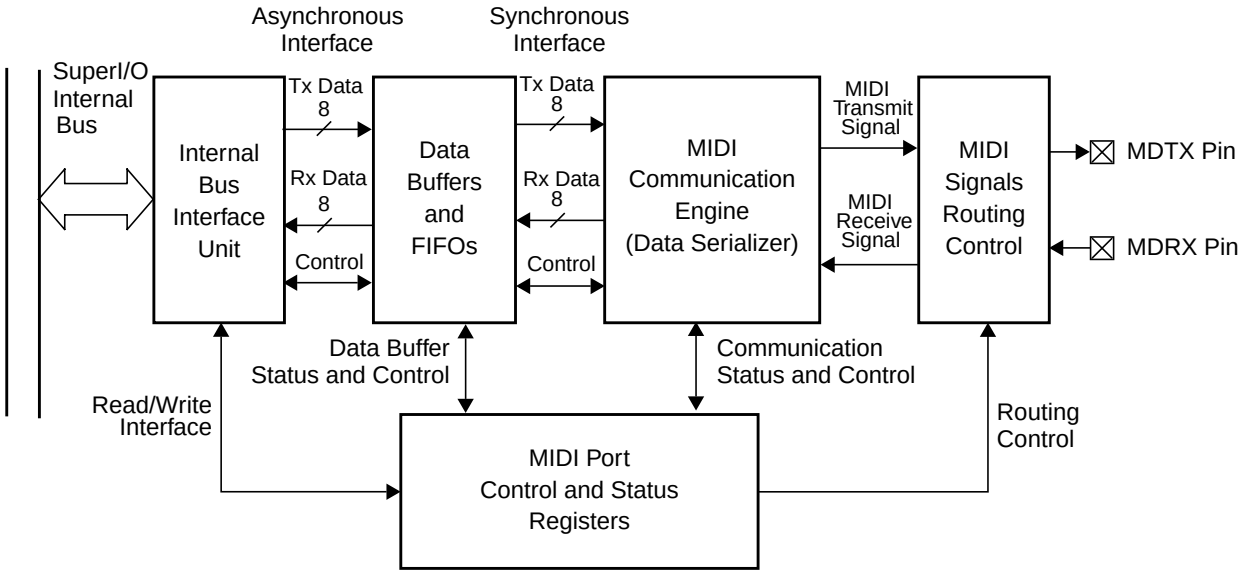


Figure 39. MIDI Port Block Diagram

11.2.1 Internal Bus Interface Unit

The Internal Bus Interface Unit handles all read and write transactions between the host and the registers of the MIDI Port. It also controls the MIDI Port interrupt request logic (see Section 11.2.8).

11.2.2 Port Control and Status Registers

A Control register (MCNTL; see Section 11.3.6 on page 138) and a Status register (MSTAT; see Section 11.3.4 on page 137) allow the user to control the operation of the MIDI, and provide status information regarding its various functional units. A Command register (MCOM; see Section 11.3.5 on page 138) allows the user to control the operation mode of the MIDI Port by serving as a port via which the host can issue commands to the MIDI. A MIDI Port command is defined as a write access to the MIDI Command register. The meaning of each command is determined by the data byte written during this write access.

11.2.3 Data Buffers and FIFOs

The Data Buffers and FIFOs function as a mechanism for synchronizing between the Internal Bus Interface Unit and the MIDI Communication Engine. This synchronization allows each of these units to handle its own tasks without having to pause to send/receive data to/from the other unit. Synchronization also bridges the gap in the data transfer rate between these two units. Data transfer rate matching is done when the FIFOs of the MIDI Port are enabled. It allows the MIDI Port to interface a bus at a relatively high data transfer rate while maintaining communication with a MIDI device over a communication channel that supports a relatively low data transfer rate.

11.2.4 MIDI Communication Engine

The MIDI Communication Engine handles the serializing of outgoing data and the de-serializing of incoming data transferred between the MIDI Port and the MIDI device. During Transmit (serial data transfer from the MIDI Port to the MIDI device), the Communication Engine receives data bytes from the output data buffer or FIFO, serializes them into a stream of data bits, and transmits them as a sequence of high and low pulses over the MDTX pin according to the MIDI communication protocol. During Receive (serial data transfer from the MIDI device to the MIDI Port), the Communication Engine receives a sequence of high and low pulses via the MDRX pin, converts them into a stream of data bits and de-serializes them into data bytes that it sends to the input data buffer or FIFO.

Both Transmit and Receive are performed at a fixed serial data rate of 31.25 Kbits per second. The serial data format is also fixed, and consists of 1 Start bit, 8 Data bits and 1 Stop bit. See the waveform illustrating a MIDI byte transfer in Figure 40.

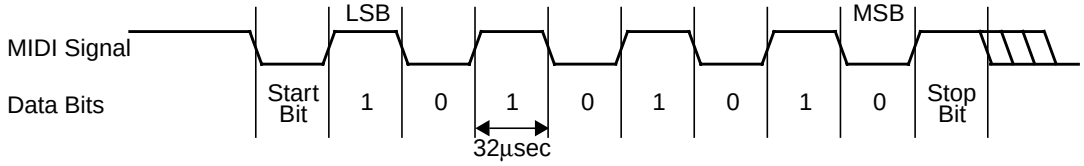


Figure 40. MIDI Byte Transfer Waveform

11.0 Musical Instrument Digital Interface (MIDI) Port (Continued)

11.2.5 MIDI Signals Routing Control Logic

The MIDI Signals Routing Control Logic controls the various routing options available for the MIDI transmit and receive signals. It is controlled by the MIDI Control register (MCNTL; see Section 11.3.6 on page 138). These routing options are not part of the Legacy definition of the MIDI Port.

11.2.6 Operation Modes

The MIDI Port can be operated in one of the following modes:

- Pass-Thru (Non-UART) Mode (default)
- UART Mode

Pass-Thru (Non-UART) Mode

After a hardware reset, the MIDI Port is in Pass-Thru mode.

In this mode, transmission is disabled by default, and all writes to the MIDI Data Out register (MDO; see Section 11.3.3 on page 136) are ignored. Transmission in this mode may be enabled by setting bit 4 of the MIDI Control register (MCNTL; see Section 11.3.6 on page 138).

Receive in Pass-Thru mode is enabled, and a 16-byte Receive FIFO is available. Reading the MIDI Data In register (MDI; see Section 11.3.2 on page 136) in this mode returns the oldest data stored in the Receive FIFO. If serial data is received while the Receive FIFO is full with data that has not yet been read, the last received data is lost, thus maintaining the data that was previously stored in the Receive Buffer.

When in Pass-Thru mode, the MIDI Port responds to host commands as follows:

- 3Fh puts the MIDI Port in UART mode. Also, in response to this command, the MIDI Port puts an acknowledge byte of FEh in the Receive buffer.
- A0h-A7h or ABh causes the MIDI Port to put an acknowledge byte of FEh followed by a data byte of 00h in the Receive buffer.
- ACh causes the MIDI Port to put an acknowledge byte of FEh, followed by a data byte of 15h, in the Receive buffer.
- ADh causes the MIDI Port to put an acknowledge byte of FEh, followed by a data byte of 01h, in the Receive buffer.
- AFh causes the MIDI Port to put an acknowledge byte of FEh, followed by a data byte of 64h, in the Receive buffer.
- FFh resets the MIDI Port to its initial state, including all the bits of the MSTAT register. In response, the MIDI Port puts an acknowledge of FEh in the Receive buffer. This command is usually referred to as the MIDI Reset Command.
- The MIDI Port responds to all other commands by putting an acknowledge byte of FEh in the Receive buffer.

Putting the acknowledge byte of FEh in the Receive buffer is equivalent to receiving a data byte. Therefore, once an acknowledge byte is put in the Receive buffer, it causes the Receive Buffer Empty status flag (see Section 11.3.4 on page 137) to be cleared, which may also cause a MIDI Port interrupt request to be issued.

When the Receive FIFO is disabled, switching from Pass-Thru mode to UART mode causes data stored in the Receive buffer to be lost. After switching to UART mode, the MIDI Port is blocked for receiving until the acknowledge byte is read from the Receive buffer.

If a command is issued to the MIDI Port while the MIDI Communication Engine is in the middle of a byte transfer (the Start bit has been transmitted or received), the execution of the command and the response are postponed until the current byte transfer is completed.

After each MIDI Port operation in Pass-Thru mode, the MIDI Status register (MSTAT; see Section 11.3.4 on page 137) is updated accordingly.

UART Mode

Entering UART mode is done by software, by giving the MIDI Port command of 3Fh. Once in UART mode, both Transmit and Receive are enabled. In addition, the two 16-byte Receive and Transmit FIFOs are automatically enabled.

In UART mode, data written to the MDO register is placed in the Transmit FIFO, from which it is taken by the MIDI Communication Engine and transmitted via the MDTX pin to the MIDI device. Likewise, whenever the Transmit FIFO is not empty, the next byte is taken out by the Communication Engine and transmitted via the MDTX pin to the MIDI device.

Whenever serial data is received by the Communication Engine via the MDRX pin, it is de-serialized and put in the Receive FIFO. Reading the MDI register returns the next byte in the Receive FIFO. The MDI register should not be read while the Receive FIFO is empty. If serial data is received while the Receive FIFO is full, this data is lost and not stored in the Receive FIFO, thus keeping the data that was previously stored in the Receive FIFO.

11.0 Musical Instrument Digital Interface (MIDI) Port (Continued)

When in UART mode, the MIDI Port responds to commands given by the host as follows:

- A command of FFh returns the MIDI Port to Pass-Thru mode, and resets it to its initial state.
- All other commands, issued while the MIDI Port is in UART mode, are ignored.

When switching from UART mode to Pass-Thru mode, any data previously stored in the Receive FIFO is lost, unless the FIFO is enabled for Pass-Thru mode.

As in Pass-Thru mode, if a command is issued to the MIDI Port while the MIDI Communication Engine is in the middle of a byte transfer, the execution of the command and the response are postponed until the current byte transfer is completed.

The MIDI commands supported by the MIDI Port and their respective responses are listed in Table 49.

After each MIDI Port operation in UART mode, the MSTAT register is updated accordingly.

Table 49. MIDI Commands Supported by the MIDI Port

Command	MIDI Port Response	
	Pass-Thru Mode	UART Mode
3Fh	Enter UART mode FEh (Acknowledge)	Ignored
A0h-A7h, ABh	FEh (Acknowledge) 00h	Ignored
ACh	FEh (Acknowledge) 15h	Ignored
ADh	FEh (Acknowledge) 01h	Ignored
AFh	FEh (Acknowledge) 64h	Ignored
FFh	MIDI Port Reset FEh (Acknowledge)	Enter Pass-Thru Mode MIDI Port Reset
Others	FEh (Acknowledge)	Ignored

11.2.7 MIDI Port Status Flags

The status of the various functional units of the MIDI Port is reflected by the MSTAT register. This register is functional in both Pass-Thru and UART modes. Some of the status indications provided by the MSTAT register are not included in the Legacy definition of the MIDI Port. These indications can be ignored if they are not required by the software.

The following status flags are included in the Legacy definition of the MIDI Port:

- Receive Buffer Empty
- Transmit Buffer Full

The Receive Buffer Empty flag is reflected by bit 7 of the MSTAT register. The Transmit Buffer Full flag is reflected by bit 6 of the MSTAT register. When operating in UART mode, these bits reflect the status of the Receive and Transmit FIFOs.

The Receive Buffer Empty status flag is cleared to 0 also when an acknowledge byte is put by the MIDI Port itself following a MIDI command.

The values of these bits are set by the MIDI Port hardware and are not affected by reading the MSTAT register.

The following status indications are provided by the MIDI Port, although they are not included in the Legacy definition of the MIDI Port:

- Receive FIFO Full
- Transmit FIFO Empty
- Receive Overrun Error
- MIDI Port Operation Mode

11.0 Musical Instrument Digital Interface (MIDI) Port (Continued)

The Receive FIFO Full and Transmit FIFO Empty status flags are reflected by MSTAT register bits 5 and 2, respectively. These bits are updated only when the MIDI Port operates in UART mode or when in Pass-Thru mode with the Receive FIFO enabled. Otherwise, these bits are constantly cleared. The values of these bits are set by the MIDI Port hardware and are not affected by reading the MSTAT register.

The Receive Overrun Error flag indicates that serial data was received by the MIDI Communication Engine while the Receive Buffer of FIFO was full. This flag is reflected by bit 3 of the MSTAT register. It is updated in both Pass-Thru and UART modes. When a Receive Overrun Event occurs, the data in the Receive Buffer/FIFO is kept and all incoming data is lost. Incoming data will keep getting lost until there is room in the Receive Buffer/FIFO to accept it. The Receive Overrun Error status flag is cleared when the MSTAT register is read.

The MIDI Port Operation Mode flag indicates whether the MIDI Port is currently operating in Pass-Thru or UART mode. This status flag is reflected by bit 4 of the MSTAT register. It can be used by software to keep track of the currently selected MIDI Port operation mode.

11.2.8 MIDI Port Interrupts

The MIDI Port supports interrupt assertion in both Pass-Thru and UART modes in response to one or both of the following events:

- Receive Data Ready
- Transmit Buffer Empty

The Receive Data Ready event refers to the case in which there is data to be read in the Receive Buffer/FIFO. An interrupt request is asserted by the MIDI Port to indicate a Receive Data Ready event in one of the following cases:

- The MIDI Port is in Pass-Thru mode and the Receive Buffer contains a data or acknowledge byte that has not been read yet. In this case, the interrupt request is de-asserted once the Receive buffer is read.
- The MIDI Port is either in UART mode and the Receive FIFO contains eight or more data bytes that have not been read yet, or it is in Pass-Thru mode with the Receive FIFO enabled. In this case, the interrupt request is de-asserted once the Receive FIFO level drops below eight bytes.
- The MIDI Port is in UART mode, the Receive FIFO contains less than eight data bytes which have not been read yet, and no data was received by the Communication Engine, the MIDI Port is in Pass-Thru mode with the Receive FIFO enabled, or a read occurs from the Receive FIFO during a timeout period of approximately 1.28 msec (the time it takes to transfer 4 bytes over the MIDI communication channel). In this case, the interrupt request is de-asserted when either new data is received by the Communication Engine or data is read from the Receive FIFO.

The Transmit Buffer Empty event refers to the case in which the Transmit Buffer/FIFO of the MIDI Port can still accept data to transmit. An interrupt request is asserted by the MIDI Port to indicate a Transmit Buffer Empty event in one of the following cases:

- The MIDI Port is in Pass-Thru mode and the Transmit Buffer is empty. In this case, the interrupt request is de-asserted once a byte is written to the Transmit Buffer.
- The MIDI Port is in UART mode and the Transmit FIFO is empty. In this case, the interrupt request is de-asserted once the Transmit FIFO is filled with at least three bytes.

After a Hardware reset, interrupts are asserted by the MIDI Port only in response to a Receive Data Ready event. Interrupt assertion in response to Transmit Buffer Empty events can be enabled by writing 1 to bit 1 of the MCNTL register. Interrupt assertion in response to Receive Data Ready events can be disabled by writing 0 to bit 3 of the MCNTL register.

11.2.9 Enhanced MIDI Port Features

The MIDI Port supports the following modes/operations, which are not part of the Legacy definition of the MIDI Port:

- Transmit in Pass-Thru
- Loopback mode
- MIDI Thru
- MDTX pin masking

Transmit in Pass-Thru. When the MIDI Port is operated in Pass-Thru mode, transmit is disabled by default. To enable it, write 1 to bit 4 of the MCNTL register.

Loopback Mode. The MIDI serial data transmit signal is routed internally to the MIDI Serial Data Receive signal. This causes all the data transmitted by the MIDI Port to also be received. Loopback mode can be used as a mode for testing the MIDI Port or its software. To enable it, write 1 to bit 7 of the MCNTL register.

11.0 Musical Instrument Digital Interface (MIDI) Port (Continued)

MIDI Thru. The MIDI serial data receive signal is routed internally to the MIDI Serial Data Transmit signal. This causes any incoming stream of pulses received via the MDRX pin to be driven immediately on the MDTX pin. This feature allows the MIDI Port to be connected as a link in a chain of several MIDI devices. In parallel to routing the MIDI Receive signal to the MIDI Transmit signals, the incoming serial data is also received by the MIDI Port itself. To enable it, write 1 to bit 6 of the MCNTL register.

MDTX Pin Masking. MDTX pin masking forces this pin to remain at a high level. This causes all transmit processes to occur without physically driving the serial data via the MDTX pin. Writing 1 to bit 2 of the MCNTL register enables MDTX pin masking.

The last three features are handled by the MIDI Signals Routing Control Logic, which is illustrated in Figure 41.

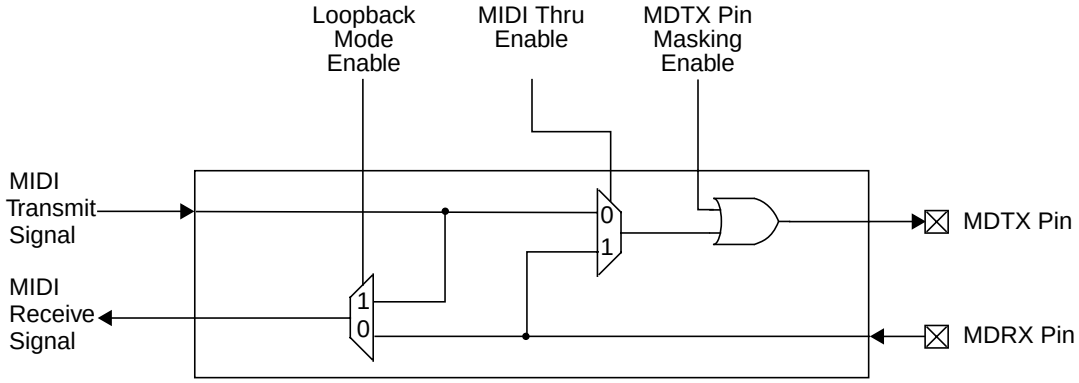


Figure 41. MIDI Signals Routing Control Logic

11.0 Musical Instrument Digital Interface (MIDI) Port (Continued)

11.3 MIDI PORT REGISTERS

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from register (write to the same address is to a different register).
- W = Write (see above).
- RO = Read Only.
- WO = Write Only. Reading from the bit returns 0.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

11.3.1 MIDI Port Register Map

The following table lists the MIDI Port registers. For the MIDI Port register bitmap, see Section 11.4 on page 139. The MIDI Port registers are V_{DD3} powered.

Table 50. MIDI Port Register Map

Offset	Mnemonic	Register Name	Type	Power Well	Section
00h	MDI	MIDI Data In	R	V_{DD3}	11.3.2
00h	MDO	MIDI Data Out	W	V_{DD3}	11.3.3
01h	MSTAT	MIDI Status	R	V_{DD3}	11.3.4
01h	MCOM	MIDI Command	W	V_{DD3}	11.3.5
02h	MCNTL	MIDI Control	R/W	V_{DD3}	11.3.6
03h	Reserved				

11.3.2 MIDI Data In Register (MDI)

This read register is used for reading data received by the MIDI Port and for reading status information returned by the MIDI Port in response to a previously issued command. When the FIFOs of the MIDI Port are enabled, reading from this offset returns the next byte taken out of the Receive FIFO.

Power Well: V_{DD3}

Location: Offset 00h

Type: R

Bit	7	6	5	4	3	2	1	0
Name	**Data In**							
Reset	X	X	X	X	X	X	X	X

11.3.3 MIDI Data Out Register (MDO)

This write register is used for writing data to be transmitted by the MIDI Port. When the FIFOs of the MIDI Port are enabled, writing to this offset puts the data byte into the Transmit FIFO.

Power Well: V_{DD3}

Location: Offset 00h

Type: W

Bit	7	6	5	4	3	2	1	0
Name	**Data Out**							
Reset	X	X	X	X	X	X	X	X

11.0 Musical Instrument Digital Interface (MIDI) Port (Continued)

11.3.4 MIDI Status Register (MSTAT)

This read register provides status information regarding the functional blocks of the MIDI Port.

Power Well: V_{DD3}

Location: Offset 01h

Type: R

Bit	7	6	5	4	3	2	1	0
Name	**Rx Buffer Empty**	**Tx Buffer Full**	**Rx FIFO Full**	**MIDI Port Operation Mode**	**Rx Overrun Error**	**Tx FIFO Not Empty**	**Reserved**	
Reset	1	0	0	0	0	0	0	0

Bit	Description
7	**Rx Buffer Empty.** When set to 1, this bit indicates that either the Receive buffer (in Pass-Thru mode) or the FIFO (in UART mode) is empty. When set to 0, it indicates that the Receive buffer or FIFO contains data that can be read via the MDI register. 0: Not empty 1: Empty (default)
6	**Tx Buffer Full.** When set to 1, this bit indicates that the Transmit Buffer or FIFO cannot accept any more data. When set to 0, it indicates that the Transmit Buffer or FIFO can accept more data written to the MDO register. 0: Not full (default) 1: Full
5	**Rx FIFO Full.** When set to 1, this bit indicates that the Receive FIFO cannot accept any more received data bytes. When set to 0, it indicates that the Receive FIFO can accept more received data bytes. This bit is forced to 0 when the FIFOs are disabled. 0: Not full or disabled (default) 1: Full
4	**MIDI Port Operation Mode.** When set to 1, this bit indicates that the MIDI Port is currently operating in UART mode. When set to 0, it indicates that the MIDI Port is currently operating in Pass-Thru (non-UART) mode. 0: Pass-Thru mode (default) 1: UART mode
3	**Rx Overrun Error.** This bit is cleared to 0 when the MSTAT register is read. An overrun error is defined as the state in which one or more data bytes were received by the MIDI Port while the Receive Buffer, or FIFO, was full. 0: No overrun error (default) 1: Overrun error
2	**Tx FIFO Not Empty.** This bit is forced to 0 when the FIFOs are disabled. 0: Empty or disabled (default) 1: Not empty
1-0	**Reserved.**

11.0 Musical Instrument Digital Interface (MIDI) Port (Continued)

11.3.5 MIDI Command Register (MCOM)

This write register is a port via which commands are issued by the host to the MIDI Port.

Power Well: V_{DD3}

Location: Offset 01h

Type: W

Bit	7	6	5	4	3	2	1	0
Name	**Command Byte**							
Reset	X	X	X	X	X	X	X	X

11.3.6 MIDI Control Register (MCNTL)

This register controls enhanced MIDI functions.

Power Well: V_{DD3}

Location: Offset 02h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Loopback Mode Enable**	**MIDI Thru Enable**	**Reserved**	**Pass-Thru Transmit Enable**	**Rx Data Ready Interrupt Enable**	**MDTX Pin Masking Enable**	**Tx Buffer Empty Interrupt Enable**	**Rx FIFO Enable for Pass-Thru Mode**
Reset	0	0	0	0	1	0	0	1
Required			0					

Bit	Type	Description
7	R/W	**Loopback Mode Enable.** When this bit is enabled, the MIDI Receive signal is internally connected to the MIDI Transmit signal. 0: Disabled (default) 1: Enabled
6	R/W	**MIDI Thru Enable.** When this bit is enabled, the MDRX pin is internally connected to the MDTX pin, which then reflects the MIDI Receive signal. When this bit is disabled, the MDTX pin is driven with data coming from the MIDI Port transmit engine. 0: Disabled (default) 1: Enabled
5	-	**Reserved.** Must be 0.
4	R/W	**Pass-Thru Transmit Enable.** When this bit is enabled, data is transmitted in Pass-Thru (non-UART) mode. 0: Disabled (default) 1: Enabled
3	R/W	**Rx Data Ready Interrupt Enable.** When this bit is enabled, an interrupt request is asserted in response to a Receive Data Ready event. 0: Disabled 1: Enabled (default)
2	R/W	**MDTX Pin Masking Enable.** When this bit is enabled, the MDTX pin is constantly driven high by the MIDI Port. When disabled, MDTX serves as the MIDI Port transmit line. 0: Disabled (default) 1: Enabled
1	R/W	**Tx Buffer Empty Interrupt Enable.** When this bit is enabled, an interrupt request is asserted in response to a Transmit Buffer Empty event. 0: Disabled (default) 1: Enabled

11.0 Musical Instrument Digital Interface (MIDI) Port (Continued)

Bit	Type	Description
0	R/W	**Rx FIFO Enable for Pass-Thru Mode.** When this bit is enabled, the Receive FIFO is enabled in Pass-Thru mode. This bit is ignored in UART mode. 0: Disabled 1: Enabled (default)

11.4 MIDI PORT BITMAP

Table 51. MIDI Port Bitmap

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	MDI	Data In							
00h	MDO	Data Out							
01h	MSTAT	Rx Buffer Empty	Tx Buffer Full	Rx Buffer Full	MIDI Port Operation Mode	Rx Overrun Error	Tx FIFO Empty	Reserved	
01h	MCOM	Command Byte							
02h	MCNTL	Loopback Mode Enable	MIDI Thru Enable	Reserved	Pass-Thru Transmit Enable	Rx Data Ready Interrupt Enable	MDTX Pin Masking Enable	Tx Buffer Empty Interrupt Enable	Rx FIFO Enable for Pass-Thru Mode

12.0 Legacy Functional Blocks

This chapter briefly describes the following blocks, which provide legacy device functions:

- Floppy Disk Controller (FDC)
- Parallel Port (PP)
- Serial Port1 and 2 (SP1 and SP2)
- Keyboard and Mouse Controller (KBC)

For details on the general implementation of each legacy block, see the *SuperI/O Legacy Functional Blocks* datasheet.

The register maps in this chapter use the following abbreviations for Type:

- R/W = Read/Write.
- R = Read from register (write to the same address is to a different register).
- W = Write (see above).
- RO = Read Only.
- WO = Write Only. Reading from the bit returns 0.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

12.1 FLOPPY DISK CONTROLLER (FDC)

12.1.1 General Description

The generic FDC is a standard FDC with a digital data separator; it is software compatible with the µDP8473 and N82077. The PC87373 FDC supports 14 of the 17 standard FDC signals described in the generic Floppy Disk Controller (FDC) chapter, including:

- FDC supportS FM and MFM modes. To select either mode, set bit 6 of the first command byte when writing to/reading from a diskette, where:
  - — 0 = FM mode
  - — 1 = MFM mode
- A logic 1 is returned during LPC I/O read cycles by all register bits, reflecting the state of floating (TRI-STATE) FDC pins.

Exceptions to standard FDC are:

- Automatic media sense using MSEN0 and MSEN1 signals is not supported.
- DRATE1 is not supported.
- $\overline{DR1}$ is not supported.
- $\overline{MTR1}$ is not supported.

Table 52 lists the FDC functional block registers. All registers are V_{DD3} powered.

Table 52. FDC Register Map

Offset[1]	Mnemonic	Register Name	Type
00h	SRA	Status A	RO
01h	SRB	Status B	RO
02h	DOR	Digital Output	R/W
03h	TDR	Tape Drive	R/W
04h	MSR	Main Status	R
	DSR	Data Rate Select	W
05h	FIFO	Data (FIFO)	R/W

12.0 Legacy Functional Blocks (Continued)

Table 52. FDC Register Map

Offset[1]	Mnemonic	Register Name	Type
06h		N/A	X
07h	DIR	Digital Input	R
	CCR	Configuration Control	W

1. From the 8-byte aligned FDC base address.

12.1.2 FDC Bitmap Summary

The FDC supports two system operation modes: PC-AT mode and PS/2 mode. Unless specifically indicated otherwise, all fields in all registers are valid in both operation modes.

Table 53. FDC Bitmap Summary

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	SRA[1]	IRQ Pending	Reserved	Step	$\overline{\text{TRK0}}$	Head Select	$\overline{\text{INDEX}}$	$\overline{\text{WP}}$	Head Direction
01h	SRB[1]	Reserved		Drive Select 0 Status	$\overline{\text{WDATA}}$	$\overline{\text{RDATA}}$	$\overline{\text{WGATE}}$	$\overline{\text{MTR1}}$	$\overline{\text{MTR0}}$
02h	DOR	Reserved		Motor Enable 1	Motor Enable 0	DMAEN	Reset Controller	Drive Select	
03h	TDR	Reserved						Tape Drive Select 1,0	
	TDR[2]	Reserved (must be 1111)				Logical Drive Exchange		Tape Drive Select 1,0	
04h	MSR	RQM	Data I/O Direction	Non-DMA Execution	Command in Progress	Reserved		Drive 1 Busy	Drive 0 Busy
	DSR	Software Reset	Low Power	Reserved	Precompensation Delay Select			Data Transfer Rate Select	
05h	FIFO	Data Bits							
07h	DIR[3]	$\overline{\text{DSKCHG}}$	Reserved						
	DIR[1]	$\overline{\text{DSKCHG}}$	Reserved				DRATE 1,0 Status		High Density
07h	CCR	Reserved						DRATE1,0	

1. Applicable only in PS/2 Mode.
2. Applicable only in Enhanced TDR Mode.
3. Applicable only in PC-AT Compatible Mode.

12.0 Legacy Functional Blocks (Continued)

12.2 PARALLEL PORT

12.2.1 General Description

The Parallel Port supports all IEEE1284 standard communication modes:

- Compatibility (known also as Standard or SPP)
- Bi-directional (known also as PS/2)
- FIFO
- EPP (known also as Mode 4)
- ECP (with an optional Extended ECP mode)

12.2.2 Parallel Port Register Map

The Parallel Port includes two groups of runtime registers, as follows:

- A group of 21 registers at first level offset, sharing 14 entries. Three of these registers (at offsets 403h, 404h and 405h) are used only in Extended ECP mode.
- A group of four registers, used only in Extended ECP mode, accessed by a second level offset.

EPP and second level offset registers are available only when the base address is 8-byte aligned.

The desired mode is selected by the ECR runtime register (offset 402h). The selected mode determines which runtime registers and which address bits are used for the base address. See Tables 54 and 55 for a listing of all registers, their offset addresses and the associated modes. All registers are V_{DD3} powered.

Table 54. Parallel Port Registers at First Level Offset

Offset	Mnemonic	Mode(s)	Register Name	Type
00h	DATAR	0,1	Data	R/W
	AFIFO	3	ECP FIFO (Address)	W
	DTR	4	Data (for EPP)	R/W
01h	DSR	All, except 4	Status	RO
	STR	4	Status (for EPP)	RO
02h	DCR	All, except 4	Control	R/W
	CTR	4	Control (for EPP)	R/W
03h	ADDR	4	EPP Address	R/W
04h	DATA0	4	EPP Data Port 0	R/W
05h	DATA1	4	EPP Data Port 1	R/W
06h	DATA2	4	EPP Data Port 2	R/W
07h	DATA3	4	EPP Data Port 3	R/W
400h	CFIFO DFIFO TFIFO CNFGA	2 3 6 7	PP Data FIFO ECP Data FIFO Test FIFO Configuration A	W R/W R/W RO
401h	CNFGB	7	Configuration B	RO
402h	ECR	All	Extended Control	R/W
403h	EIR[1]	0,1,2,3	Extended Index	R/W
404h	EDR[1]	0,1,2,3	Extended Data	R/W
405h	EAR[1]	0,1,2,3	Extended Auxiliary Status	R/W

1. These registers are extended to the standard IEEE1284 registers. They are only accessible when enabled by bit 4 of the Parallel Port Configuration register (see Section 3.9.3 on page 53).

12.0 Legacy Functional Blocks (Continued)

Table 55. Parallel Port Registers at Second Level Offset

Offset	Mnemonic	Register Name	Type
00h	Control0	Extended Control 0	R/W
02h	Control2	Extended Control 1	R/W
04h	Control4	Extended Control 4	R/W
05h	PP Confg0	Configuration 0	R/W

12.2.3 Parallel Port Bitmap Summary

The Parallel Port functional block bitmaps are grouped according to first and second level offsets.

Table 56. Parallel Port Bitmap Summary for First Level Offset

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
000h	DATAR	Data Bits							
	AFIFO	Address Bits							
001h	DSR	Printer Status	$\overline{\text{ACK}}$ Status	PE Status	SLCT Status	$\overline{\text{ERR}}$ Status	Reserved		EPP Time-Out Status
002h	DCR	Reserved		Direction Control	Interrupt Enable	PP Input Control	Printer Initialization Control	Automatic Line Feed Control	Data Strobe Control
003h	ADDR	EPP Device or Register Selection Address Bits							
004h	DATA0	EPP Device or R/W Data							
005h	DATA1	EPP Device or R/W Data							
006h	DATA2	EPP Device or R/W Data							
007h	DATA3	EPP Device or R/W Data							
400h	CFIFO	Data Bits							
400h	DFIFO	Data Bits							
400h	TFIFO	Data Bits							
400h	CNFGA	Reserved				Bit 7 of PP Confg0	Reserved		
401h	CNFGB	Reserved	Interrupt Request Value	Interrupt Select			Reserved	DMA Channel Select	
402h	ECR	ECP Mode Control			ECP Interrupt Mask	ECP DMA Enable	ECP Interrupt Service	FIFO Full	FIFO Empty
403h	EIR	Reserved					Second Level Offset		
404h	EDR	Data Bits							
405h	EAR	FIFO Tag	Reserved						

12.0 Legacy Functional Blocks (Continued)

Table 57. Parallel Port Bitmap Summary for Second Level Offset

Register		Bits							
Second Level Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	Control0	Reserved		DCR Register Live	Freeze Bit	Reserved			EPP Time-Out Interrupt Mask
02h	Control2	SPP Compatibility	Channel Address Enable	Reserved	Revision 1.7 or 1.9 Select	Reserved			
04h	Control4	Reserved	PP DMA Request Inactive Time			Reserved	PP DMA Request Active Time		
05h	PP Confg0	Bit 3 of CNFGA	Demand DMA Enable	ECP IRQ Channel Number			PE Internal Pull-Up or Pull-Down	ECP DMA Channel Number	

12.0 Legacy Functional Blocks (Continued)

12.3 UART FUNCTIONALITY (SERIAL PORT 1 AND SERIAL PORT 2)

12.3.1 General Description

The Serial Port (SP) provides UART functionality. The generic SP supports serial data communication with a remote peripheral device or modem, using a wired interface. The functional block can function as a standard NS16450 or NS16550A or as an Extended UART.

12.3.2 UART Register Bank Overview

Four register banks, each containing eight registers, control UART operation. All registers use the same 8-byte address space to indicate offsets 00h through 07h. The Bank Select Register (BSR) selects the active bank and is common to all banks (see Figure 42).

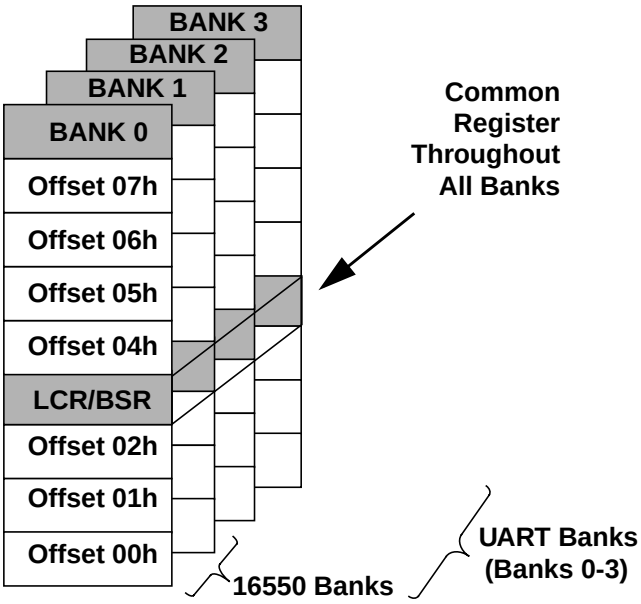


Figure 42. UART Register Bank Architecture

12.3.3 SP1 and SP2 Register Maps

All registers are V_{DD3} powered.

Table 58. Bank 0 Register Map

Offset	Mnemonic	Register Name	Type
00h	RXD	Receiver Data Port	RO
00h	TXD	Transmitter Data Port	W
01h	IER	Interrupt Enable	R/W
02h	EIR	Event Identification (Read Cycles)	RO
	FCR	FIFO Control (Write Cycles)	W
03h	LCR[1]	Line Control	R/W
	BSR[1]	Bank Select	
04h	MCR	Modem/Mode Control	R/W
05h	LSR	Link Status	RO
06h	MSR	Modem Status	RO
07h	SPR/ASCR	Scratchpad/Auxiliary Status and Control	R/W

1. When bit 7 of this register is set to 1, bits 6–0 of BSR select the bank.

12.0 Legacy Functional Blocks (Continued)

Table 59. Bank Selection Encoding

BSR Bits								Bank Selected	Functionality
7	6	5	4	3	2	1	0		
0	x	x	x	x	x	x	x	0	UART (Serial Port 1 and Serial Port 2)
1	0	x	x	x	x	x	x	1	
1	1	x	x	x	x	1	x	1	
1	1	x	x	x	x	x	1	1	
1	1	1	0	0	0	0	0	2	
1	1	1	0	0	1	0	0	3	

Table 60. Bank 1 Register Map

Offset	Mnemonic	Register Name	Type
00h	LBGD(L)	Legacy Baud Generator Divisor Port (Low Byte)	R/W
01h	LBGD(H)	Legacy Baud Generator Divisor Port (High Byte)	R/W
02h	Reserved		
03h	LCR/BSR	Line Control/Bank Select	R/W
04h-07h	Reserved		

Table 61. Bank 2 Register Map

Offset	Mnemonic	Register Name	Type
00h	BGD(L)	Baud Generator Divisor Port (Low Byte)	R/W
01h	BGD(H)	Baud Generator Divisor Port (High Byte)	R/W
02h	EXCR1	Extended Control1	R/W
03h	LCR/BSR	Line Control/Bank Select	R/W
04h	EXCR2	Extended Control2	R/W
05h	Reserved		
06h	TXFLV	TX_FIFO Level	R/W
07h	RXFLV	RX_FIFO Level	R/W

Table 62. Bank 3 Register Map

Offset	Mnemonic	Register Name	Type
00h	MRID	Module Revision ID	RO
01h	SH_LCR	Shadow of LCR (Read Only)	RO
02h	SH_FCR	Shadow of FIFO Control (Read Only)	RO
03h	LCR/BSR	Line Control/Bank Select	R/W
04h-07h	Reserved		

12.0 Legacy Functional Blocks (Continued)

12.3.4 SP1 and SP2 Bitmap Summary

Table 63. Bank 0 Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	RXD	Receiver Data Bits							
	TXD	Transmitter Data Bits							
01h	IER[1]	Reserved				MS_IE	LS_IE	TXLDL_IE	RXHDL_IE
	IER[2]	Reserved		TXEMP_IE	Reserved	MS_IE	LS_IE	TXLDL_IE	RXHDL_IE
02h	EIR[1]	FEN1	FEN0	Reserved		RXFT	IPR1	IPR0	IPF
	EIR[2]	Reserved		TXEMP_EV	Reserved	MS_EV	LS_EV or TXHLT_EV	TXLDL_EV	RXHDL_EV
	FCR	RXFTH1	RXFTH0	TXFTH1	TXFTH0	Reserved	TXSR	RXSR	FIFO_EN
03h	LCR[3]	BKSE	SBRK	STKP	EPS	PEN	$\overline{STB}$	WLS1	WLS0
	BSR[3]	BKSE	Bank Select						
04h	MCR[1]	Reserved			LOOP	ISEN or DCDLP	RILP	RTS	$\overline{DTR}$
	MCR[2]	Reserved				TX_DFR	Reserved	RTS	$\overline{DTR}$
05h	LSR	ER_INF	TXEMP	TXRDY	BRK	FE	PE	OE	RXDA
06h	MSR	DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS
07h	SPR[1]	Scratch Data							
	ASCR[2]	Reserved							RXF_TOUT

1. Non-Extended Mode.
2. Extended Mode.
3. When bit 7 of this register is set to 1, bits 6-0 of BSR select the bank, as shown in Table 59 on page 146.

12.0 Legacy Functional Blocks (Continued)

Table 64. Bank 1 Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	LBGD(L)	Legacy Baud Generator Divisor (Least Significant Bits)							
01h	LBGD(H)	Legacy Baud Generator Divisor (Most Significant Bits)							
02h	Reserved								
03h	LCR/BSR	Same as Bank 0							
04h-07h	Reserved								

Table 65. Bank 2 Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	BGD(L)	Baud Generator Divisor Low (Least Significant Bits)							
01h	BGD(H)	Baud Generator Divisor High (Most Significant Bits)							
02h	EXCR1	BTEST	Reserved	ETDLBK	LOOP	Reserved			EXT_SL
03h	LCR/BSR	Same as Bank 0							
04h	EXCR2	LOCK	Reserved	PRESL1	PRESL0	Reserved			
05h	Reserved								
06h	TXFLV	Reserved			TFL4	TFL3	TFL2	TFL1	TFL0
07h	RXFLV	Reserved			RFL4	RFL3	RFL2	RFL1	RFL0

Table 66. Bank 3 Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	MRID	Module ID (MID 7-4)				Revision ID (RID 3-0)			
01h	SH_LCR	BKSE	SBRK	STKP	EPS	PEN	$\overline{\text{STB}}$	WLS1	WLS0
02h	SH_FCR	RXFTH1	RXFTH0	TXFHT1	TXFTH0	Reserved	TXSR	RXSR	FIFO_EN
03h	LCR/BSR	Same as Bank 0							
04h-07h	Reserved								

12.0 Legacy Functional Blocks (Continued)

12.4 KEYBOARD AND MOUSE CONTROLLER (KBC)

12.4.1 General Description

The KBC is implemented physically as a single hardware module and houses two separate logical devices: a mouse controller (Logical Device 5) and a keyboard controller (Logical Device 6). The KBC is functionally equivalent to the industry standard 8042AH keyboard controller. The 8042AH datasheet can be used as a detailed technical reference for the KBC.

The hardware KBC module is integrated to provide the following pin functions: $\overline{\text{KBRST}}$ (P20), GA20 (P21), KBDAT, KBCLK, MDAT and MCLK. $\overline{\text{KBRST}}$ and GA20 are implemented as bi-directional open-drain pins with internal active pull-up. The keyboard and mouse interfaces are implemented as bi-directional open-drain pins. Their internal connections are shown in Figure 43.

Ports P10-P17 and P22-P27 of the KBC core are not available on dedicated pins; neither are T0 and T1. P10, P11, P22, P23, P26, P27, T0 and T1 are used to implement the keyboard and mouse interface.

The KBC executes a program fetched from an on-chip 2 Kbyte ROM. The code programed in this ROM is user-customizable. The KBC has two interrupt request signals: one for the keyboard and one for the mouse. The interrupt requests are implemented using ports P24 and P25 of the KBC core. The interrupt requests are controlled exclusively by the KBC firmware, except for the IRQ type and number, which are set by configuration registers (see Section 3.2.3 on page 36).

The interrupt requests are implemented as bi-directional signals. When an I/O port is read, all unused bits return the value latched in the output registers of the ports.

For KBC firmware that implements interrupt-on-OBF schemes, the following is the recommended implementation:

1. Put the data in DBBOUT.
2. Set the appropriate port bit to issue an interrupt request.

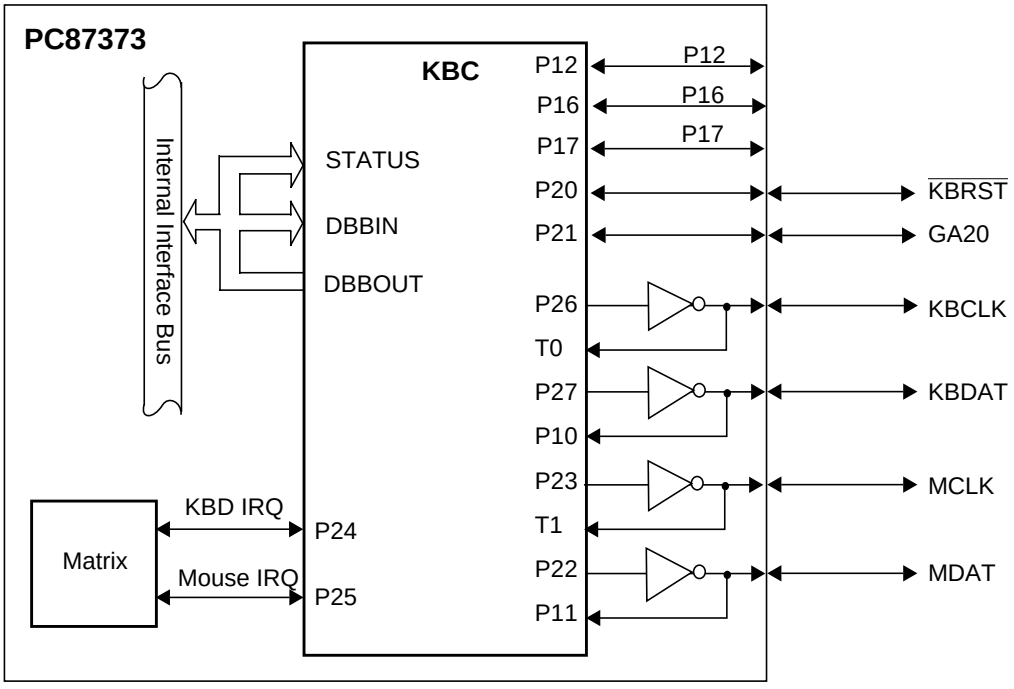


Figure 43. Keyboard and Mouse Interfaces

12.0 Legacy Functional Blocks (Continued)

12.4.2 KBC Register Map

All registers are V_{DD3} powered.

Table 67. KBC Register Map

Offset	Mnemonic	Register Name	Type
00h	DBBOUT	Read KBC Data	R
	DBBIN	Write KBC Data	W
04h	STATUS	Read Status	R
	DBBIN	Write KBC Command	W

12.4.3 KBC Bitmap Summary

Table 68. KBC Bitmap Summary

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	DBBOUT	KBC Data Bits (For Read cycles)							
	DBBIN	KBC Data Bits (For Write cycles)							
04h	STATUS	General-Purpose Flags				F1	F0	IBF	OBF
	DBBIN	KBC Command Bits (For Write cycles)							

13.0 Device Characteristics

13.1 GENERAL DC ELECTRICAL CHARACTERISTICS

13.1.1 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD3}	Main 3V Supply Voltage	3.0	3.3	3.6	V
V_{SB3}	Standby 3V Supply Voltage	3.0	3.3	3.6	V
V_{BAT}	Battery Backup Supply Voltage	2.4	3.0	3.6	V
T_A	Operating Temperature	0		+70	°C

13.1.2 Absolute Maximum Ratings

Absolute maximum ratings are values beyond which damage to the device may occur. Unless otherwise specified, all voltages are relative to ground (V_{SS}).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{SUP}	Supply Voltage[1]		–0.5	+4.1	V
V_I	Input Voltage	All other pins	–0.5	5.5	V
		PCI_CLK, LAD3-0, $\overline{\text{LFRAME}}$, $\overline{\text{PCI\_RESET}}$, SERIRQ, $\overline{\text{LPCPD}}$	–0.5	V_{DD3} + 0.5	V
V_O	Output Voltage	All other pins	–0.5	5.5	V
		LAD3-0, $\overline{\text{LDRQ}}$, SERIRQ	–0.5	V_{DD3} + 0.5	V
T_{STG}	Storage Temperature		–65	+165	°C
P_D	Power Dissipation			1	W
T_L	Lead Temperature Soldering (10 s)			+260	°C
	ESD Tolerance	C_{ZAP} = 100 pF R_{ZAP} = 1.5 KΩ[2]	2000		V

1. V_{SUP} is V_{DD3}, V_{SB3}.
2. Value based on test complying with RAI-5-048-RA human body model ESD testing.

13.1.3 Capacitance

Symbol	Parameter	Conditions	Min[2]	Typ[1]	Max[2]	Unit
C_{IN}	Input Pin Capacitance			4	5	pF
C_{INC}	LPC Clock Input Capacitance	PCI_CLK	5	8	12	pF
C_{PCI}	LPC Pin Capacitance	LAD3-0, $\overline{\text{LFRAME}}$, $\overline{\text{PCI\_RESET}}$, SERIRQ, $\overline{\text{LPCPD}}$, $\overline{\text{LDRQ}}$		8	10	pF
C_{IO}	I/O Pin Capacitance			8	10	pF
C_O	Output Pin Capacitance			6	8	pF

1. T_A = 25°C; f = 1 MHz.
2. Not tested. Guaranteed by characterization.

13.0 Device Characteristics (Continued)

13.1.4 Power Consumption under Recommended Operating Conditions

Symbol	Parameter	Conditions[1]	Typ	Max[2]	Unit
I_{DD3}	V_{DD3} Average Supply Current	V_{IL} = 0.5V, V_{IH} = 2.4V, No Load	TBD	TBD	mA
I_{DD3LP}	V_{DD3} Quiescent Supply Current in Low Power Mode[3]	V_{IL} = V_{SS}, V_{IH} = V_{DD3}, No Load	0.5	0.8	mA
I_{SB3}	V_{SB3} Average Supply Current	V_{IL} = 0.5V, V_{IH} = 2.4V, No Load	TBD	TBD	mA
I_{SB3LP}	V_{SB3} Quiescent Supply Current in Low Power Mode[3]	V_{IL} = V_{SS}, V_{IH} = V_{SB3}, No Load	TBD	TBD	mA
I_{BAT}	V_{BAT} Battery Supply Current	V_{DD3}, V_{SB3} = 0V, V_{BAT} = 3V	TBD	TBD	µA

1. All parameters specified for 0°C ≤ T_A ≤ 70°C; V_{DD3} and V_{SB3} = 3.3V ±10% unless otherwise specified.
2. Not tested. Guaranteed by characterization.
3. All the modules disabled; no LPC bus activity.

13.1.5 Voltage Thresholds

Symbol	Parameter[1]	Min[2]	Typ	Max[2]	Unit
V_{DD3ON}	V_{DD3} Detected as Power-on	2.3	2.6	2.9	V
V_{DD3OFF}	V_{DD3} Detected as Power-off	2.2	2.5	2.8	V
V_{DD3HY}	V_{DD3} Hysteresis (V_{DD3ON} − V_{DD3OFF})	0.1			V
V_{SB3ON}	V_{SB3} Detected as Power-on	2.3	2.6	2.9	V
V_{SB3OFF}	V_{SB3} Detected as Power-off	2.2	2.5	2.8	V
V_{SB3HY}	V_{SB3} Hysteresis (V_{SB3ON} − V_{SB3OFF})	0.1			V
V_{BATLOW}	V_{BAT} Detected as “Low”	1.8		2.3	V

1. All parameters specified for 0°C ≤ T_A ≤ 70°C.
2. Not tested. Guaranteed by characterization.

13.0 Device Characteristics (Continued)

13.2 DC CHARACTERISTICS OF PINS, BY I/O BUFFER TYPES

The following tables summarize the DC characteristics of all device pins described in Section 1.2 on page 14. The characteristics describe the general I/O buffer types defined in Table 1 on page 14. For exceptions, refer to Section 13.2.12 on page 156. The DC characteristics of the LPC interface meet the *PCI Local Bus Specification (Rev 2.2 December 18, 1998)* for 3.3V DC signaling.

13.2.1 Input, Game Port Compatible with Schmitt Trigger

Symbol: IN_{GP}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		0.75 V_{SUP}[1]	5.5[2]	V
V_{IL}	Input Low Voltage		–0.5[2]	0.3 V_{SUP}[1]	V
V_{HY}	Input Hysteresis		300[3]		mV
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{SUP}$		±1[4]	µA

1. V_{SUP} is V_{DD}, V_{SB} or V_{PP} according to the input power well.
2. Not tested. Guaranteed by design.
3. Not tested. Guaranteed by characterization.
4. Maximum 20 µA for all pins together. Not tested. Guaranteed by characterization.

13.2.2 Input, TTL Compatible

Symbol: IN_{T}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	5.5[1]	V
V_{IL}	Input Low Voltage		–0.5[1]	0.8	V
I_{IL}[2]	Input Leakage Current	$0 < V_{IN} < V_{SUP}$[3]		±1[4]	µA

1. Not tested. Guaranteed by design.
2. Input leakage current includes the output leakage of the bi-directional buffers with TRI-STATE outputs.
3. V_{SUP} is V_{DD3} or V_{SB3} according to the input power well.
4. Maximum 20 µA for all pins together (for exceptions, refer to Section 13.2.12 on page 156). Not tested. Guaranteed by characterization.

13.2.3 Input, TTL Compatible, with Schmitt Trigger

Symbol: IN_{TS}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	5.5[1]	V
V_{IL}	Input Low Voltage		–0.5[1]	0.8	V
V_{HY}	Input Hysteresis		250[2]		mV
I_{IL}[3]	Input Leakage Current	$0 < V_{IN} < V_{SUP}$[4]		±1[5]	µA

1. Not tested. Guaranteed by design.
2. Not tested. Guaranteed by characterization.
3. Input leakage current includes the output leakage of the bi-directional buffers with TRI-STATE outputs.
4. V_{SUP} is V_{DD3} or V_{SB3} according to the input power well.
5. Maximum 20 µA for all pins together (for exceptions, refer to Section 13.2.12 on page 156.). Not tested. Guaranteed by characterization.

13.0 Device Characteristics (Continued)

13.2.4 Input, TTL Compatible, with 400 mV Schmitt Trigger

Symbol: IN_{TS4}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	5.5[1]	V
V_{IL}	Input Low Voltage		–0.5[1]	0.8	V
V_{HY}	Input Hysteresis		400[2]		mV
I_{IL}[3]	Input Leakage Current	$0 < V_{IN} < V_{SUP}$[4]		±1[5]	µA

1. Not tested. Guaranteed by design.
2. Not tested. Guaranteed by characterization.
3. Input leakage current includes the output leakage of the bi-directional buffers with TRI-STATE outputs.
4. V_{SUP} is V_{DD3} or V_{SB3} according to the input power well.
5. Maximum 20 µA for all pins together (for exceptions, refer to Section 13.2.12 on page 156.). Not tested. Guaranteed by characterization.

13.2.5 Input, PCI 3.3V Compatible

Symbol: IN_{PCI}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		0.5 V_{DD}	V_{DD} + 0.5[1]	V
V_{IL}	Input Low Voltage		–0.5[1]	0.3 V_{DD}	V
I_{IL}[2]	Input Leakage Current	$0 < V_{IN} < V_{DD3}$		±1[3]	µA

1. Not tested. Guaranteed by design.
2. Input leakage current includes the output leakage of the bi-directional buffers with TRI-STATE outputs.
3. Maximum 20 µA for all pins together (for exceptions, refer to Section 13.2.12 on page 156.). Not tested. Guaranteed by characterization.

13.2.6 Analog Input

Symbol: AI

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IR}	Input Voltage Range		0	5.5[1]	V
I_{IL}	Input Leakage Current	$V_{IN} = V_{IR}$		300[2]	µA

1. Not tested. Guaranteed by characterization.
2. This buffer type is excluded from the pins for which the total pins leakage of the device is maximum 20 µA. Not tested. Guaranteed by characterization.

13.0 Device Characteristics (Continued)

13.2.7 Output, TTL/CMOS Compatible, Push-Pull Buffer

Symbol: $O_{p/n}$

Output, TTL/CMOS Compatible, rail-to-rail push-pull buffer that is capable of sourcing *p* mA and sinking *n* mA

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –*p* mA	2.4		V
		I_{OH} = –50 µA	V_{SUP} – 0.2[1]		V
V_{OL}	Output Low Voltage	I_{OL} = *n* mA		0.4	V
		I_{OL} = 50 µA		0.2	V

1. V_{SUP} is V_{DD3} or V_{SB3} according to the output power well.

13.2.8 Output, TTL/CMOS Compatible, Open-Drain Buffer

Symbol: OD_n

Output, TTL/CMOS-compatible open-drain output buffer capable of sinking *n* mA. Output from these signals is open-drain and is never forced high.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output Low Voltage	I_{OL} = *n* mA		0.4	V
		I_{OL} = 50 µA		0.2	V

13.2.9 Output, PCI 3.3V Compatible

Symbol: O_{PCI}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{out} = –500 µA	0.9 V_{DD3}		V
V_{OL}	Output Low Voltage	I_{out} = 1500 µA		0.1 V_{DD3}	V

13.2.10 Analog Output

Symbol: AO

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OR}	Output Voltage Range		0	5.5[1]	V
V_{OD}	Output Drive Voltage	I_{out} = –3.6 mA	V_{SUP}[2] – 150 mV		
I_{OL}	Output Leakage Current	V_{OUT} = V_{OR}, V_{SUP} < V_{OUT}		20[3]	µA

1. Not tested. Guaranteed by characterization.
2. V_{SUP} is V_{DD3} or V_{SB3} according to the pin power well.
3. This buffer type is excluded from the pins for which the total pins leakage of the device is maximum 10 µA. Not tested. Guaranteed by characterization.

13.0 Device Characteristics (Continued)

13.2.11 Input/Output Switch, SMBus Compatible

Symbol: SW_{SM}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRP}	Pin-to-Pin Voltage Drop	I_{SW} = ±3 mA, Switch Closed		150[1]	mV
V_{ISC}	Input Voltage for Switch Closed	I_{SW} = ±3 mA	1.5[1]		V
V_{ISO}	Input Voltage for Switch Open	I_{SW} = ±20 µA		V_{SUP}[2,3]	V
I_{IL}	Input Leakage Current	$V_{ISO} < V_{IN} < 5.5V$		±20[1]	µA

1. Not tested. Guaranteed by characterization.
2. V_{SUP} is V_{DD3} or V_{SB3} according to the pin power well.
3. Not tested. Guaranteed by design.

13.2.12 Exceptions

1. All pins are 5V tolerant except for the pins with PCI (IN_{PCI}, O_{PCI}) buffer types.
2. All pins are back-drive protected except for the output pins with PCI (O_{PCI}) buffer types.
3. The following pins are excluded from the requirement of total pins leakage maximum 10 µA: V_{SB5}, REF5V, REF5V_STBY, 3V_DDCSCL, 5V_DDCSCL, 3V_DDCSDA, 5V_DDCSDA, SMB1_SCL, SMB1_SDA, SMB2_SCL, SMB2_SDA.
4. The following pins have an internal static pull-up resistor (when enabled) and therefore may have leakage current from V_{SUP} (when V_{IN} = 0): $\overline{\text{LPCPD}}$, $\overline{\text{ACK}}$, $\overline{\text{AFD\_DSTRB}}$, $\overline{\text{ERR}}$, $\overline{\text{INIT}}$, PE, $\overline{\text{SLIN\_ASTRB}}$, $\overline{\text{STB\_WRITE}}$, $\overline{\text{KBRST}}$, GA20, $\overline{\text{SIOPME}}$, JYABT0-1, JYBBT0-1, MDRX, GPIOE00-07, GPIOE10-13, PWRGD_PS, $\overline{\text{CPU\_PRESENT}}$, $\overline{\text{FPRST}}$, $\overline{\text{PRIMARY\_HD}}$, $\overline{\text{SECONDARY\_HD}}$, $\overline{\text{SCSI}}$.
5. The following pins have an internal static pull-down resistor (when enabled) and therefore may have leakage current to V_{SS} (when $V_{IN} = V_{SUP}$): BUSY_$\overline{\text{WAIT}}$, PE and SLCT.
6. The following strap pins have an internal static pull-up resistor enabled during Power-Up reset and therefore may have leakage current to V_{SUP} (when V_{IN} = 0): $\overline{\text{BADDR}}$, $\overline{\text{TRIS}}$, $\overline{\text{TEST}}$.
7. When V_{DD3} = 0V, the following pins present a DC load to V_{SS} of 30 KΩ minimum (not tested, guaranteed by design) for a pin voltage of 0V to 3.6V: $\overline{\text{CTS1}}$, $\overline{\text{CTS2}}$, $\overline{\text{DCD1}}$, $\overline{\text{DCD2}}$, $\overline{\text{DSR1}}$, $\overline{\text{DSR2}}$, $\overline{\text{DTR\_BOUT1}}$, $\overline{\text{DTR\_BOUT2}}$, $\overline{\text{RI1}}$, $\overline{\text{RI2}}$, $\overline{\text{RTS1}}$, $\overline{\text{RTS2}}$, SIN1, SIN2, SOUT1, SOUT2.
8. Output from SLCT, BUSY_$\overline{\text{WAIT}}$ (and PE if bit 2 of PP Confg0 register is 0) is open-drain in all SPP modes except in SPP-Compatible mode when the setup mode is ECP-based FIFO and bit 4 of the Control2 parallel port register is 1. Otherwise, output from these signals is level 2. External 4.7 KΩ pull-up resistors should be used.
9. Output from $\overline{\text{ACK}}$, $\overline{\text{ERR}}$ (and PE if bit 2 of PP Confg0 register is set to 1) is open-drain in all SPP modes except in SPP-Compatible mode when the setup mode is ECP-based FIFO and bit 4 of the Control2 parallel port register is set to 1. Otherwise, output from these signals is level 2. External 4.7 KΩ pull-up resistors should be used.
10. Output from $\overline{\text{STB}}$, $\overline{\text{AFD}}$, $\overline{\text{INIT}}$ and $\overline{\text{SLIN}}$ is open-drain in all SPP modes, except in SPP-Compatible mode when the setup mode is ECP-based (FIFO). Otherwise, output from these signals is level 2. External 4.7 KΩ pull-up resistors should be used.
11. I_{OH} is valid for a GPIO pin only when it is not configured as open-drain.
12. In XOR Tree mode, the buffer type of the input pins participating in the XOR Tree (see Section 2.4.2 on page 33) is IN_T (Input, TTL compatible), regardless of the buffer type of these pins in normal device operation mode (see Section 1.4 on page 16)

13.2.13 Terminology

Back-Drive Protection. A pin that is back-drive protected does not sink current into the supply when an input voltage higher than the supply, but below the pin's maximum input voltage, is applied to the pin. This is true even when the supply is inactive. Note that active pull-up resistors and active output buffers are typically not back-drive protected.

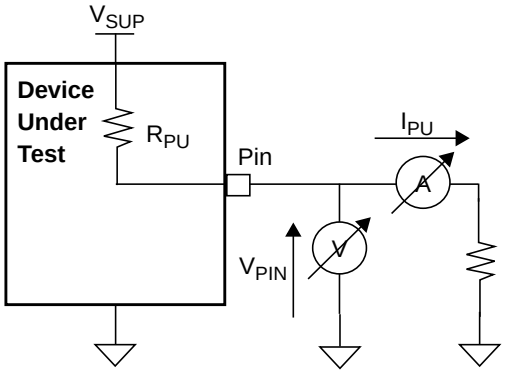
5-Volt Tolerance. An input signal that is 5V tolerant can operate with input voltage of up to 5V even though the supply to the device is only 3.3V. The actual maximum input voltage allowed to be supplied to the pin is indicated by the maximum high voltage allowed for the input buffer. Note that some pins have multiple buffers, not all of which are 5V tolerant. In such cases, there is a note that indicates at what conditions a 5V input may be applied to the pin; if there is no note, the low maximum voltage among the buffers is the maximum voltage allowed for the pin.

13.0 Device Characteristics (Continued)

13.3 INTERNAL RESISTORS

DC Test Conditions

Pull-Up Resistor Test Circuit



Pull-Down Resistor Test Circuit

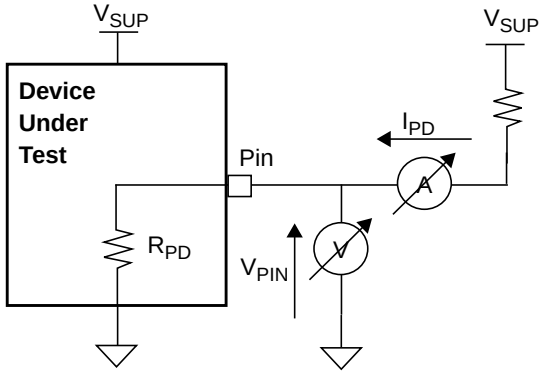


Figure 44. Internal Resistor Test Conditions, T_A = 0°C to 70°C, V_{SUP} = 3.3V

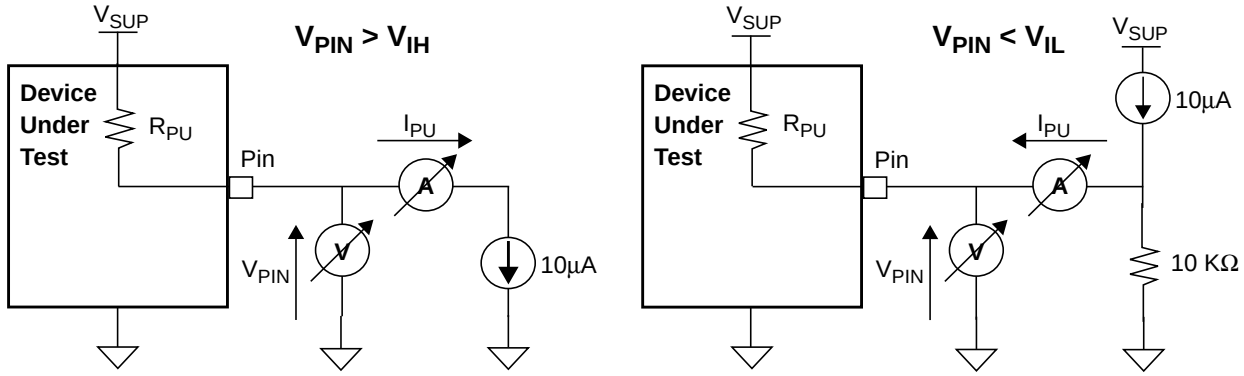


Figure 45. Internal Pull-Down Resistor for Straps, T_A = 0°C to 70°C, V_{SUP} = 3.3V

Notes for Figures 44 and 45:

1. V_{SUP} is V_{DD3} or V_{SB3} according to the pin power well.
1. The equivalent resistance of the pull-up resistor is calculated by $R_{PU} = (V_{SUP} - V_{PIN}) / I_{PU}$.
2. The equivalent resistance of the pull-down resistor is calculated by $R_{PD} = V_{PIN} / I_{PD}$.

13.3.1 Pull-Up Resistor

Symbol: PU_{nn}

Symbol	Parameter	Conditions[1]	Min[2]	Typical	Max[2]	Unit
R_{PU}	Pull-up equivalent resistance	V_{PIN} = 0V	*nn* – 30%	*nn*	*nn* + 30%	KΩ
		V_{PIN} = 0.8 V_{SUP}[3]			*nn* – 38%	KΩ
		V_{PIN} = 0.17 V_{SUP}[3]	*nn* – 35%			KΩ

1. TA = 0°C to 70°C, V_{SUP} = 3.3V.
2. Not tested. Guaranteed by characterization.
3. For strap pins only.

13.3.2 Pull-Down Resistor

Symbol: PD_{nn}

Symbol	Parameter	Conditions[1]	Min[2]	Typical	Max[2]	Unit
R_{PD}	Pull-down equivalent resistance	V_{PIN} = V_{SUP}	*nn* – 30%	*nn*	*nn* + 30%	KΩ

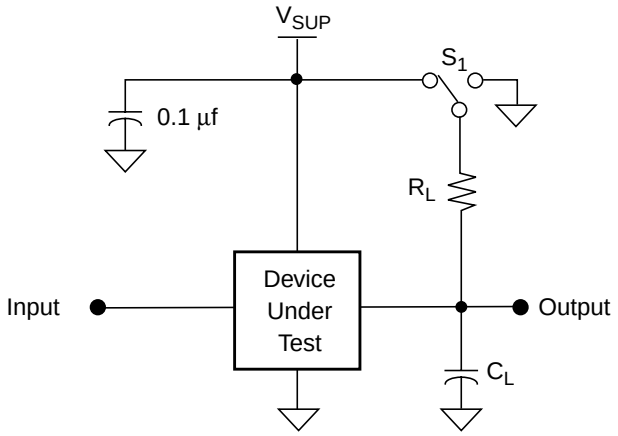
1. TA = 0°C to 70°C, V_{SUP} = 3.3V.
2. Not tested. Guaranteed by characterization.

13.0 Device Characteristics (Continued)

13.4 AC ELECTRICAL CHARACTERISTICS

13.4.1 AC Test Conditions

Load Circuit



AC Testing Input, Output Waveform

(unless otherwise specified)

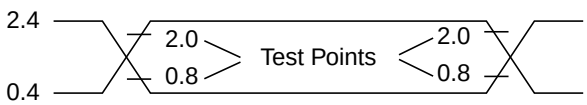


Figure 46. AC Test Conditions, T_A = 0°C to 70°C, V_{SUP} = 3.3V ±10%

Notes:

1. V_{SUP} is either V_{DD3} or V_{SB3}, according to the pin power well.
2. C_L = 50 pF for all output pins except the following pin groups:
   – C_L = 100 pF for Serial Port 1 and 2 pins (see Section 1.4.2 on page 17), Parallel Port pins (see Section 1.4.3) and Floppy Disk Controller pins (see Section 1.4.4)
   – C_L = 40 pF for $\overline{\text{IDE\_RSTDRV}}$ pin
   – C_L = 400 pF for SMBus pins (see *SMBus Voltage Translation and Isolation Timing* on page 172)

   These values include both jig and oscilloscope capacitance.
3. S_1 = Open – for push-pull output pins.
   S_1 = V_{SUP} – for high-impedance to active low and active low to high impedance transition measurements
   S_1 = GND – for high-impedance to active high and active high to high impedance transition measurements
   R_L = 1.0 KΩ– for all the pins
4. For the FDC open-drain interface pins, S_1 = V_{DD3} and R_L = 150Ω.

13.0 Device Characteristics (Continued)

13.4.2 Reset Timing

V_{SB} Power-Up Reset

Symbol	Figure	Description	Reference Conditions		Min[1]	Max[1]
t_{IRST}	47	Internal Power-Up Reset Time	V_{SB3} power-up to end of internal reset	Ended by 32 KHz Clock Domain		$t_{32KW} + t_{32KVAL}$[2] + 17 * t_{CP}
	48			Ended by $\overline{\text{PCI\_RESET}}$		t_{LRST}
t_{LRST}	48	$\overline{\text{PCI\_RESET}}$ active time	V_{SB3} power-up to end of $\overline{\text{PCI\_RESET}}$		10 ms	

1. Not tested. Guaranteed by design.
2. $t_{32KW} + t_{32KVAL}$ from V_{SB3} power-up to 32 KHz domain toggling; see *Low-Frequency Clock Timing on page 162*.

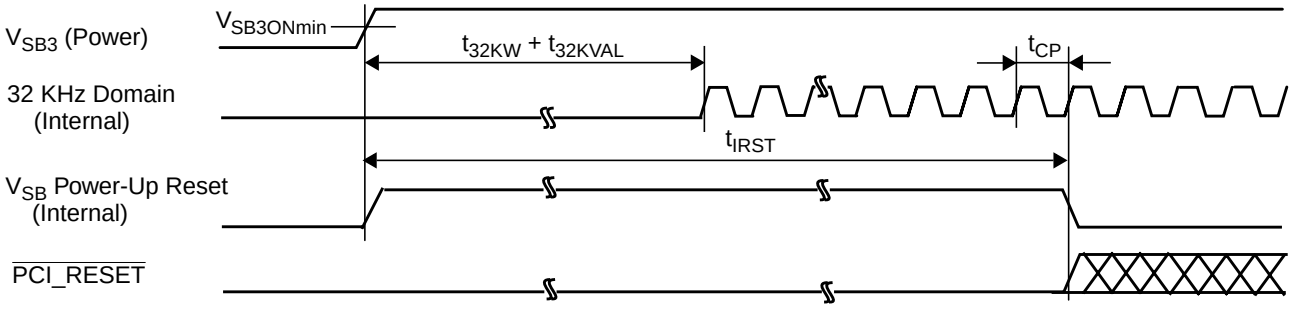


Figure 47. Internal V_{SB} Power-Up Reset - Ended by 32 KHz Clock

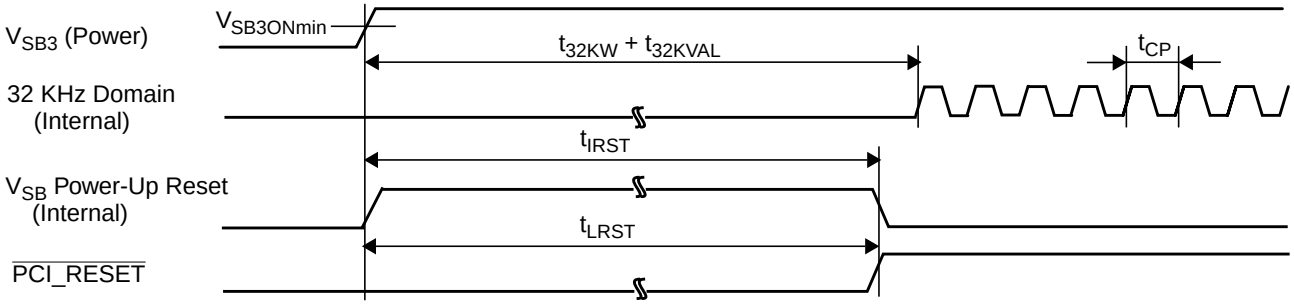


Figure 48. Internal V_{SB} Power-Up Reset - Ended by $\overline{\text{PCI\_RESET}}$

13.0 Device Characteristics (Continued)

V_{DD} Power-Up Reset

Symbol	Figure	Description	Reference Conditions	Min[1]	Max[1]
t_{IRST}	49	Internal Power-Up reset time	V_{DD3} power-up to end of internal reset		t_{LRST}
t_{LRST}	49	$\overline{PCI\_RESET}$ active time	V_{DD3} power-up to end of $\overline{PCI\_RESET}$	10 ms	
t_{IPLV}	49	Internal strap pull-up resistor, valid time[2]	Before end of internal reset	t_{IRST}	
t_{EPLV}	49	External strap pull-down resistor, valid time	Before end of internal reset	t_{IRST}	

1. Not tested. Guaranteed by design.
2. Active only during V_{DD3} Power-Up reset.

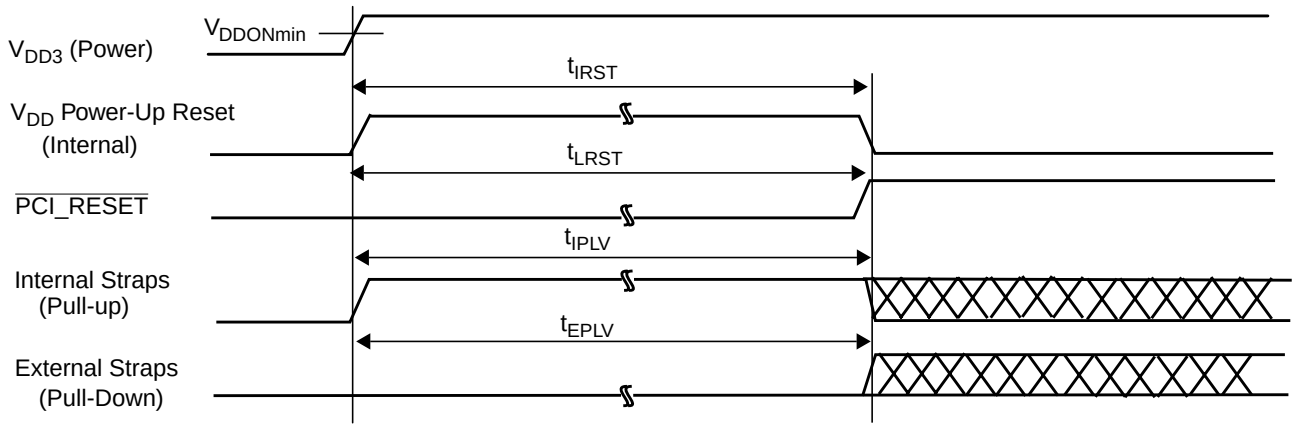


Figure 49. Internal V_{DD} Power-Up Reset

Hardware Reset

Symbol	Figure	Description	Reference Conditions	Min	Max
t_{WRST}	50	$\overline{PCI\_RESET}$ pulse width		100 ns	

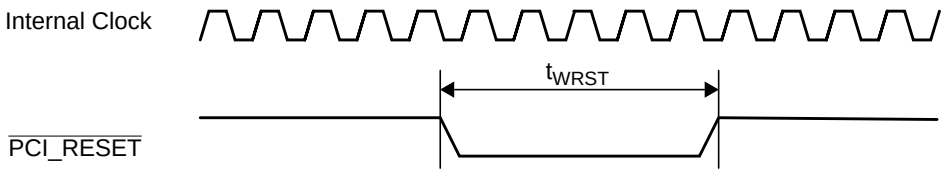


Figure 50. Hardware Reset

13.0 Device Characteristics (Continued)

13.4.3 Clock Timing

High-Frequency Clock Timing

Symbol	Figure	Clock Input Parameters	Reference Conditions	CLOCKI14			Units
				Min	Typ	Max	
t_{CH}	51	Clock High Pulse Width[1]		29.5			ns
t_{CL}	51	Clock Low Pulse Width[1]		29.5			ns
t_{CP}	51	Clock Period[1] (50%-50%)		69.14	69.84	70.54	ns
F_{CK}	–	Clock Frequency		F_{CKTYP} – 1%	14.31818	F_{CKTYP} + 1%	MHz
t_{CR}	51	Clock Rise Time[1] (20%-80%)				5[2]	ns
t_{CF}	51	Clock Fall Time[1] (80%-20%)				5[2]	ns
t_{14MW}	52	Clock Wake-Up Time	V_{DD3} stable to clock start toggling	System dependent			
t_{14MVAL}	52	Clock Valid Time[1]	Clock start toggling to clock valid	System dependent			

1. Not tested. Guaranteed by design.
2. Recommended value

Sym.	Fig.	Internal Clock Parameter	Reference Conditions	INT48M			Units
				Min	Typ	Max	
t_{CP}	51	Clock Period[1] (50%-50%)			20.83		ns
F_{CK}	–	Clock Frequency			48		MHz
t_{48MD}	52	Clock Wake-Up Time[1]	After Clock Generator enabled			500	µs

1. Not tested. Guaranteed by characterization.

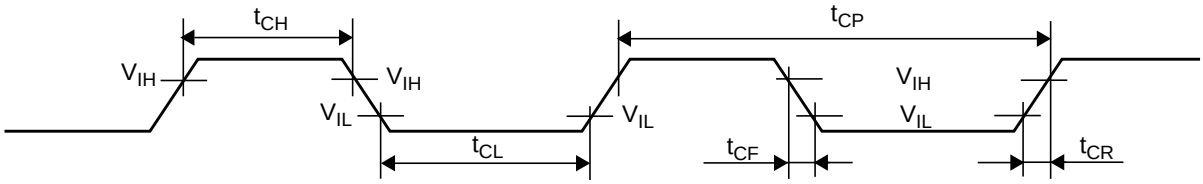


Figure 51. High-Frequency Clock Waveform Timing

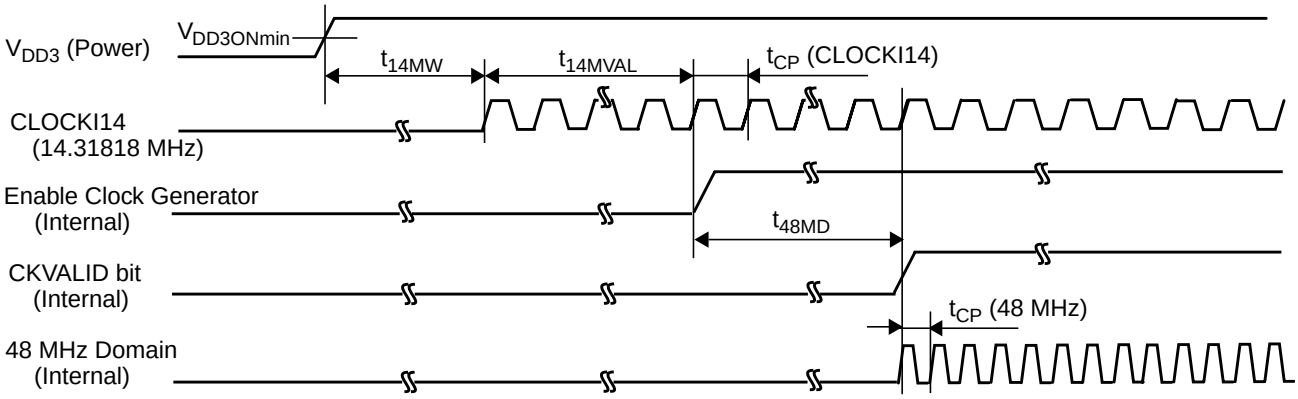


Figure 52. CLOCKI14 and Internal 48 MHz Domain Timing

13.0 Device Characteristics (Continued)

Low-Frequency Clock Timing

Symbol	Figure	Clock Input Parameters	Reference Conditions	CLOCKI32			Units
				Min	Typ	Max	
t_{CP}	53	Clock Period[1] (50%-50%)		30.4871	30.517578	30.5481	µs
F_{CK}	–	Clock Frequency		F_{32TYP} – 0.1%	32.768 (F_{32TYP})	F_{32TYP} + 0.1%	KHz
t_{32KW}	53	Clock wake-up time	V_{SB3} stable to clock start toggling	System dependent[2]			
t_{32KVAL}	53	Clock valid time[1]	Clock start toggling to clock valid			256 * t_{CP}	

1. Not tested. Guaranteed by design.
2. If t_{32KW} of the CLOCKI32 input is lower than 0.5 ms, use the 0.5 ms value in calculations involving the total wake-up time of the low-frequency clock (t_{32KW} + t_{32KVAL}).

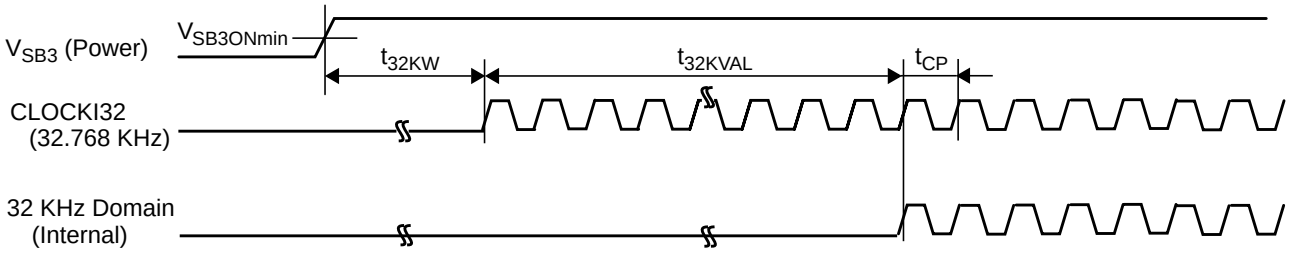


Figure 53. CLOCKI32 Timing

13.0 Device Characteristics (Continued)

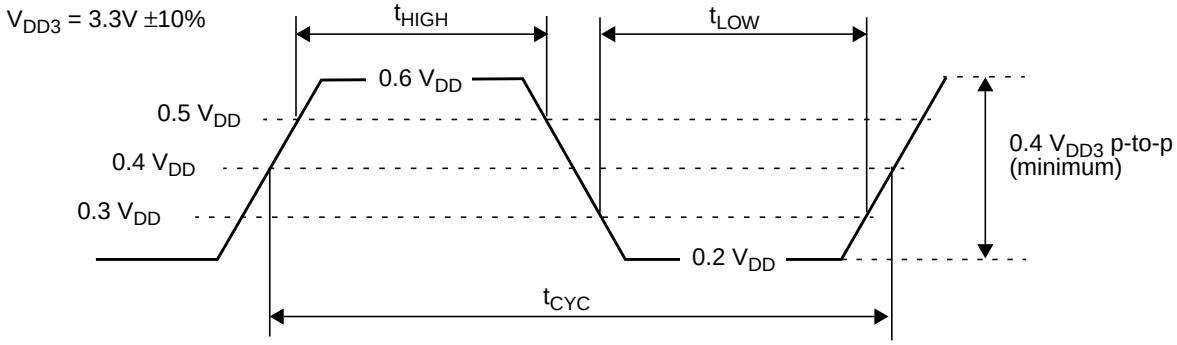
13.4.4 LPC Interface Timing

The AC characteristics of the LPC interface meet the PCI Local Bus Specification *(Rev 2.2 December 18, 1998)* for 3.3V DC signaling.

PCI_CLK and $\overline{\text{PCI\_RESET}}$

Symbol	Parameter	Min	Max	Units
t_{CYC}[1]	PCI_CLK Cycle Time	30		ns
t_{HIGH}	PCI_CLK High Time[2]	11		ns
t_{LOW}	PCI_CLK Low Time[2]	11		ns
–	PCI_CLK Slew Rate[2,3]	1	4	V/ns
–	$\overline{\text{PCI\_RESET}}$ Slew Rate[2,4]	50		mV/ns

1. The PCI may have any clock frequency between nominal DC and 33 MHz. Device operational parameters at frequencies under 16 MHz are guaranteed by design rather than by testing. The clock frequency may be changed at any time during the operation of the system as long as the clock edges remain “clean” (monotonic) and the minimum cycle high and low times are not violated. The clock may only be stopped in a low state.
2. Not tested. Guaranteed by characterization.
3. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock wavering (0.2 * V_{DD3} to 0.6 * V_{DD3}) as shown below.
4. The minimum $\overline{\text{PCI\_RESET}}$ slew rate applies only to the rising (de-assertion) edge of the reset signal and ensures that system noise cannot make an otherwise monotonic signal appear to bounce in the switching range.



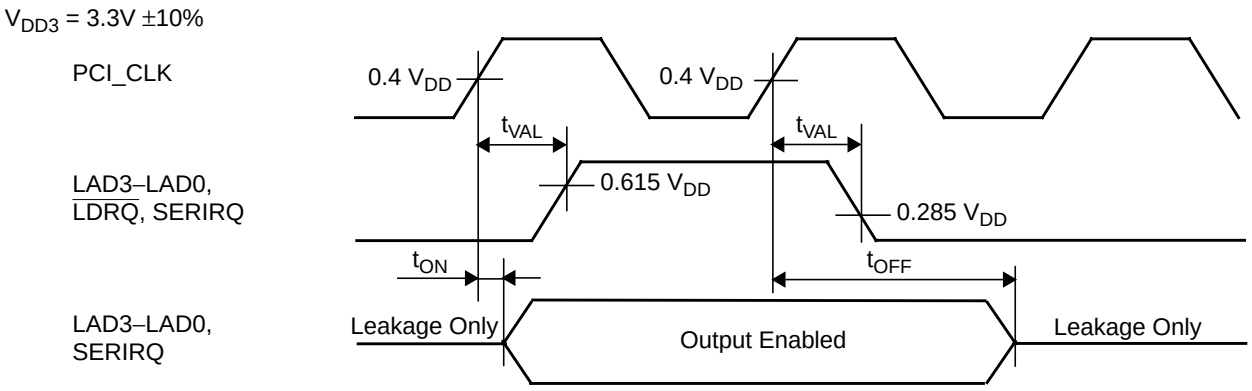
13.0 Device Characteristics (Continued)

LPC Signals

Symbol	Figure	Description	Reference Conditions	Min	Max	Unit
t_{VAL}	Outputs	Output Valid Delay	After RE of CLK		11	ns
t_{ON}	Outputs	Float to Active Delay	After RE of CLK	2		ns
t_{OFF}	Outputs	Active to Float Delay	After RE of CLK		28	ns
t_{SU}	Inputs	Input Setup Time	Before RE of CLK	7		ns
t_{HL}	Inputs	Input Hold Time	After RE of CLK	0		ns
t_{PDR}	Reset Outputs	Rise Propagation Delay	From RE of $\overline{\text{PCI\_RESET}}$ to RE of $\overline{\text{PCIRST\_OUT}}$, $\overline{\text{PCIRST\_OUT2}}$		30	ns
t_R	Reset Outputs	Rise Time	$\overline{\text{PCIRST\_OUT}}$, $\overline{\text{PCIRST\_OUT2}}$		50	ns
t_{PDF}	Reset Outputs	Fall Propagation Delay	From FE of $\overline{\text{PCI\_RESET}}$ to FE of $\overline{\text{IDE\_RSTDRV}}$		20	ns
t_F	Reset Outputs	Fall Time	$\overline{\text{IDE\_RSTDRV}}$		15	ns

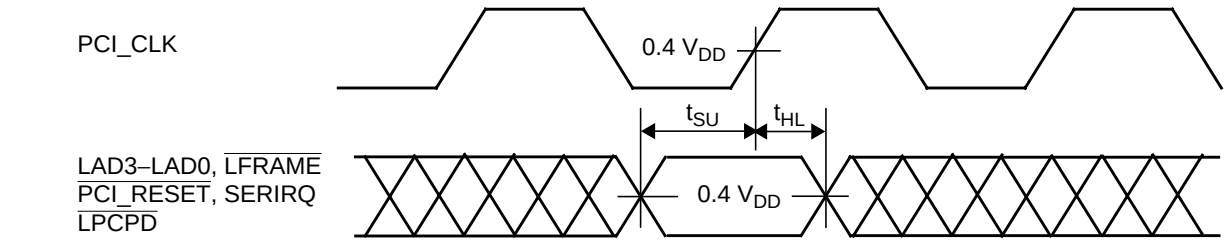
Outputs

V_{DD3} = 3.3V ±10%

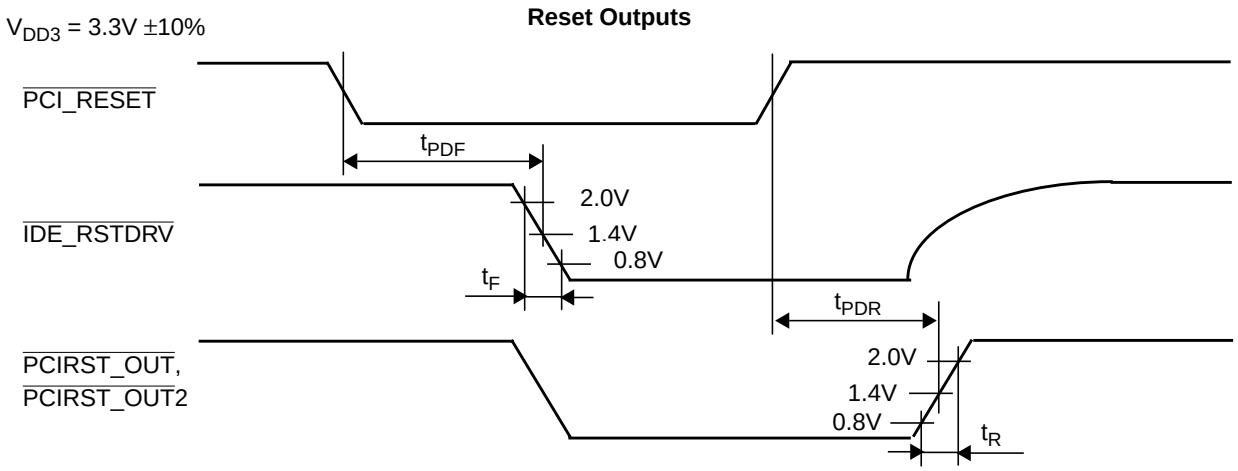


Inputs

V_{DD3} = 3.3V ±10%



13.0 Device Characteristics (Continued)

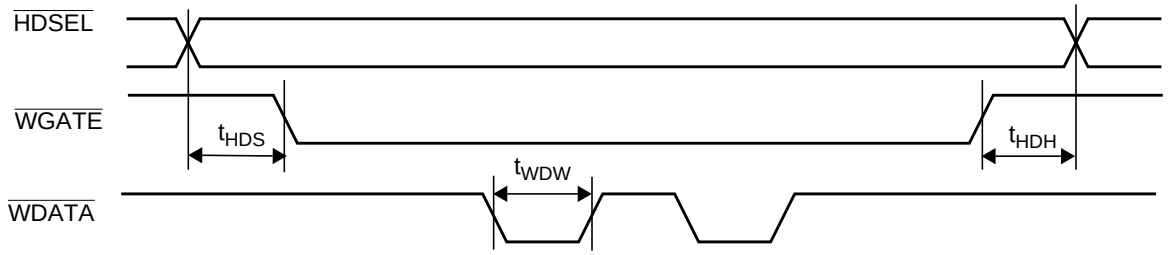


13.4.5 FDC Timing

FDC Write Data Timing

Symbol	Parameter	Min	Max	Unit
t_{HDH}	HDSEL Hold from WGATE Inactive[1]	100		µs
t_{HDS}	HDSEL Setup to WGATE Active[1]	100		µs
t_{WDW}	Write Data Pulse Width[1]	See t_{DRP}, t_{ICP} and t_{WDW} values in table below		

1. Not tested. Guaranteed by design.



t_{DRP} t_{ICP} t_{WDW} Values

Data Rate	t_{DRP}	t_{ICP}	t_{ICP} Nominal	t_{WDW}	t_{WDW} Minimum	Unit
1 Mbps	1000	6 x t_{CP}[1]	125	2 x t_{ICP}	250	ns
500 Kbps	2000	6 x t_{CP}[1]	125	2 x t_{ICP}	250	ns
300 Kbps	3333	10 x t_{CP}[1]	208	2 x t_{ICP}	375	ns
250 Kbps	4000	12 x t_{CP}[1]	250	2 x t_{ICP}	500	ns

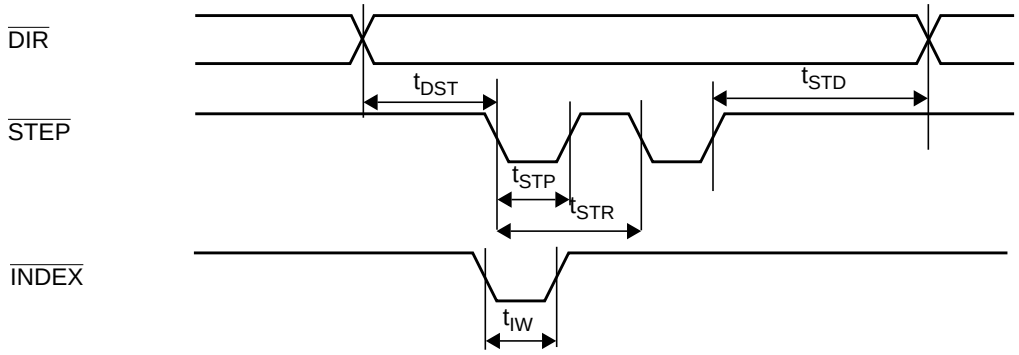
1. t_{CP} is the clock period defined for CLOCKI in *Clock Timing on page 161*.

13.0 Device Characteristics (Continued)

FDC Drive Control Timing

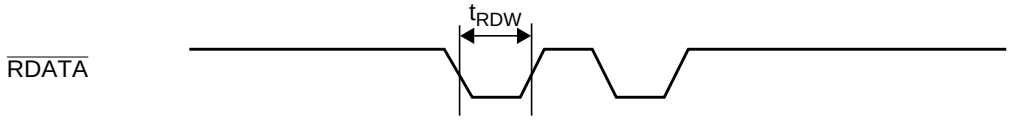
Symbol	Parameter	Min	Max	Unit
t_{DST}	$\overline{DIR}$ Setup to $\overline{STEP}$ Active[1]	6		µs
t_{IW}	Index Pulse Width	100		ns
t_{STD}	$\overline{DIR}$ Hold from $\overline{STEP}$ Inactive	t_{STR}		ms
t_{STP}	$\overline{STEP}$ Active High Pulse Width[1]	8		µs
t_{STR}	$\overline{STEP}$ Rate Time[1]	0.5		ms

1. Not tested. Guaranteed by design.



FDC Read Data Timing

Symbol	Parameter	Min	Max	Unit
t_{RDW}	Read Data Pulse Width	50		ns

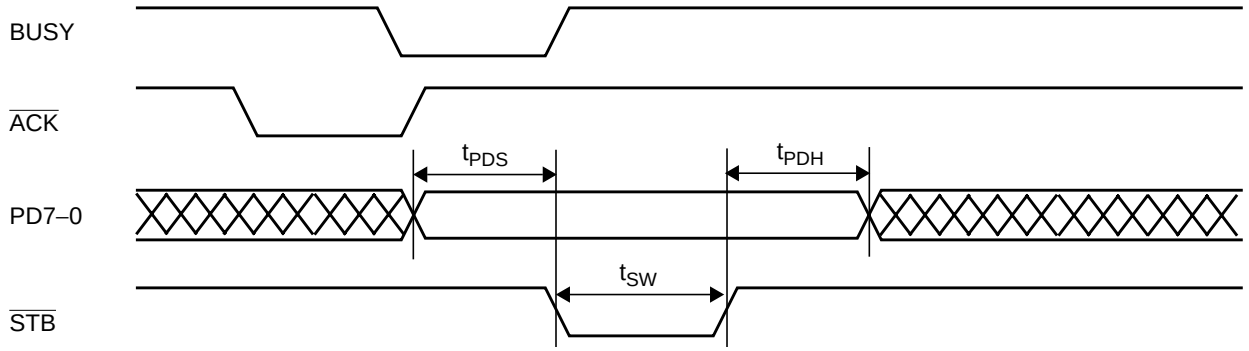


13.0 Device Characteristics (Continued)

13.4.6 Parallel Port Timing

Standard Parallel Port Timing

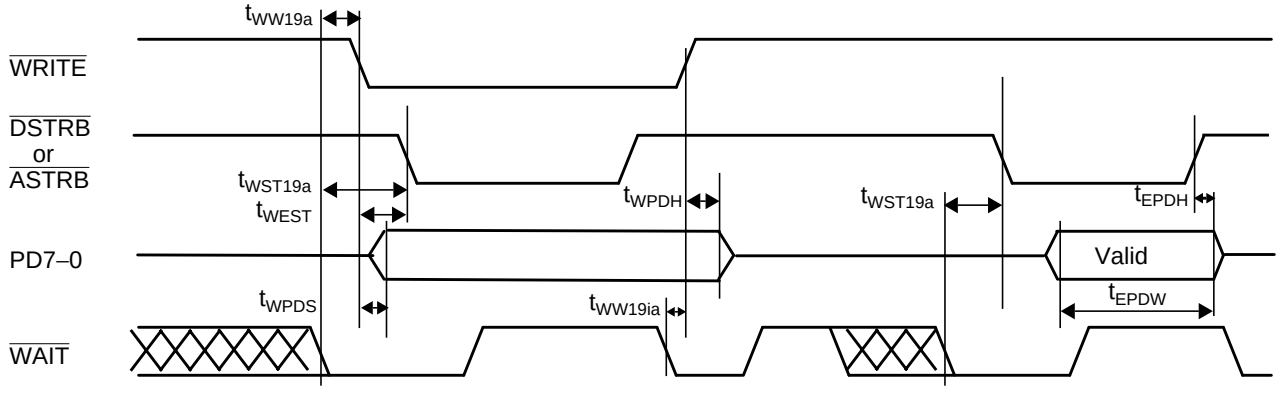
Symbol	Parameter	Conditions	Min	Max	Unit
t_{PDH}	Port Data Hold	SPP Mode 0 and Mode 1, ECP Mode 0 and Mode1: system dependent; ECP Mode 2: device dependent.	750		ns
t_{PDS}	Port Data Setup	SPP Mode 0 and Mode 1, ECP Mode 0 and Mode1: system dependent; ECP Mode 2: device dependent.	750		ns
t_{SW}	Strobe Width	SPP Mode 0 and Mode 1, ECP Mode 0 and Mode1: system dependent; ECP Mode 2: device dependent.	750		ns



Enhanced Parallel Port Timing

Symbol	Parameter	Min	Max	EPP 1.7[1]	EPP 1.9[1]	Unit
t_{WW19a}	$\overline{WRITE}$ Active from $\overline{WAIT}$ Low		45		✔	ns
t_{WW19ia}	$\overline{WRITE}$ Inactive from $\overline{WAIT}$ Low		45		✔	ns
t_{WST19a}	$\overline{DSTRB}$ or $\overline{ASTRB}$ Active from $\overline{WAIT}$ Low		65		✔	ns
t_{WEST}	$\overline{DSTRB}$ or $\overline{ASTRB}$ Active after $\overline{WRITE}$ Active	10		✔	✔	ns
t_{WPDH}	PD7–0 Hold after $\overline{WRITE}$ Inactive	0		✔	✔	ns
t_{WPDS}	PD7–0 Valid after $\overline{WRITE}$ Active		15	✔	✔	ns
t_{EPDW}	PD7–0 Valid Width	80		✔	✔	ns
t_{EPDH}	PD7–0 Hold after $\overline{DSTRB}$ or $\overline{ASTRB}$ Inactive	0		✔	✔	ns

1. Also in ECP Mode 4



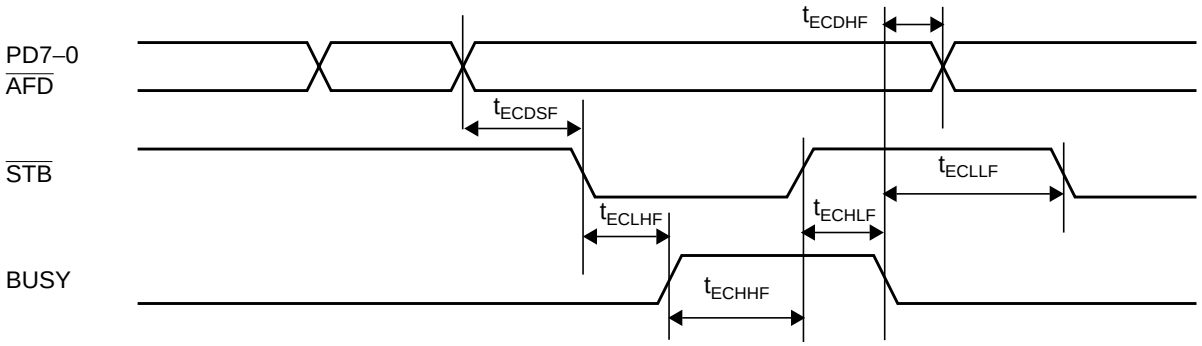
13.0 Device Characteristics (Continued)

Extended Capabilities Port (ECP) Timing

Forward Mode

Symbol	Parameter	Min	Max	Unit
t_{ECDSF}	Data Setup before $\overline{STB}$ Active	0		ns
t_{ECDHF}	Data Hold after BUSY Inactive	0		ns
t_{ECLHF}	BUSY Active after $\overline{STB}$ Active	75		ns
t_{ECHHF}	$\overline{STB}$ Inactive after BUSY Active[1]	0	1	s
t_{ECHLF}	BUSY Inactive after $\overline{STB}$ Active[1]	0	35	ms
t_{ECLLF}	$\overline{STB}$ Active after BUSY Inactive	0		ns

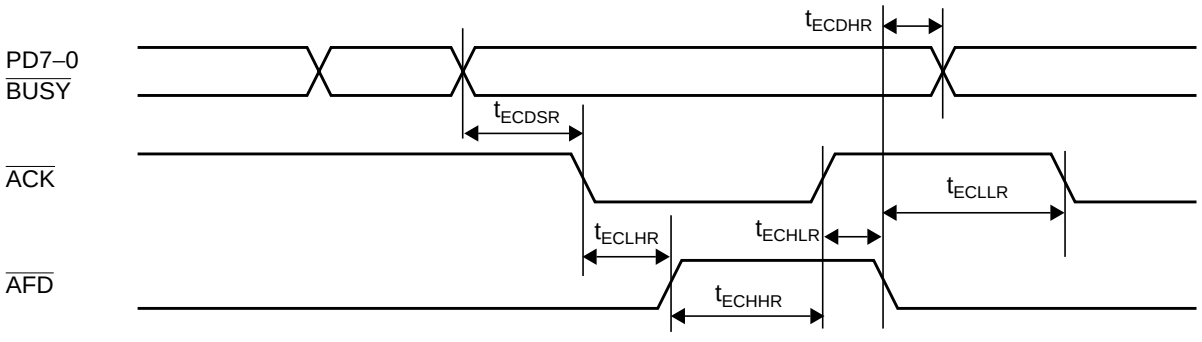
1. Not tested. Guaranteed by design.



Reverse Mode

Symbol	Parameter	Min	Max	Unit
t_{ECDSR}	Data Setup before $\overline{ACK}$ Active	0		ns
t_{ECDHR}	Data Hold after $\overline{AFD}$ Active	0		ns
t_{ECLHR}	$\overline{AFD}$ Inactive after $\overline{ACK}$ Active	75		ns
t_{ECHHR}	$\overline{ACK}$ Inactive after $\overline{AFD}$ Inactive[1]	0	35	ms
t_{ECHLR}	$\overline{AFD}$ Active after $\overline{ACK}$ Inactive[1]	0	1	s
t_{ECLLR}	$\overline{ACK}$ Active after $\overline{AFD}$ Active	0		ns

1. Not tested. Guaranteed by design.



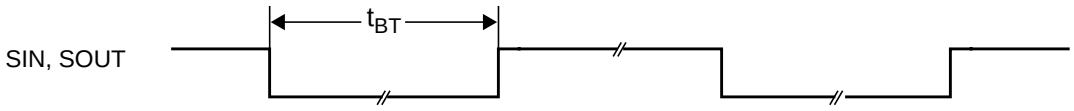
13.0 Device Characteristics (Continued)

13.4.7 Serial Ports 1 and 2 Timing

Serial Port Data Timing

Symbol	Parameter	Conditions	Min	Max	Unit
t_{BT}	Single Bit Time in Serial Port[1]	Transmitter	t_{BTN} – 25[2]	t_{BTN} + 25[2]	ns
		Receiver	t_{BTN} – 2%[2]	t_{BTN} + 2%[2]	ns

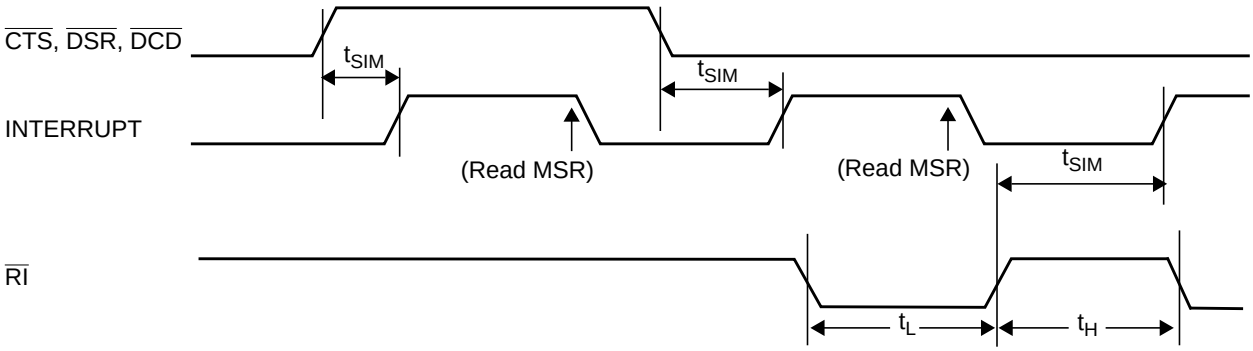
1. Not tested. Guaranteed by design.
2. t_{BTN} is the nominal bit time in the Serial Port; it is determined by the setting of the Baud Generator Divisor registers.



Modem Control Timing

Symbol	Parameter	Min	Max	Unit
t_L	$\overline{RI1,2}$ Low Time[1,2]	10		ns
t_H	$\overline{RI1,2}$ High Time[1,2]	10		ns
t_{SIM}	Delay to Set IRQ from Modem Input		40	ns

1. Not tested. Guaranteed by characterization.
2. The value also applies to $\overline{RI1,2}$ wake-up detection in the SWC module



13.0 Device Characteristics (Continued)

13.4.8 Glue Function Timing

Highest Active Main and Standby Supply Reference

Symbol	Figure	Description	Reference Conditions	Min	Max
Main					
t_{PD}	54	V_{DD3} to REF5V Propagation Delay[1]	V_{DD5} = 0; V_{DD3} slew rate > 10 V/ms		1 ms
Standby					
t_{PD}	54	V_{SB3} to REF5V_STBY Propagation Delay[1]	V_{SB5} = 0; V_{SB3} slew rate > 10 V/ms		1 ms

1. Not tested. Guaranteed by design.

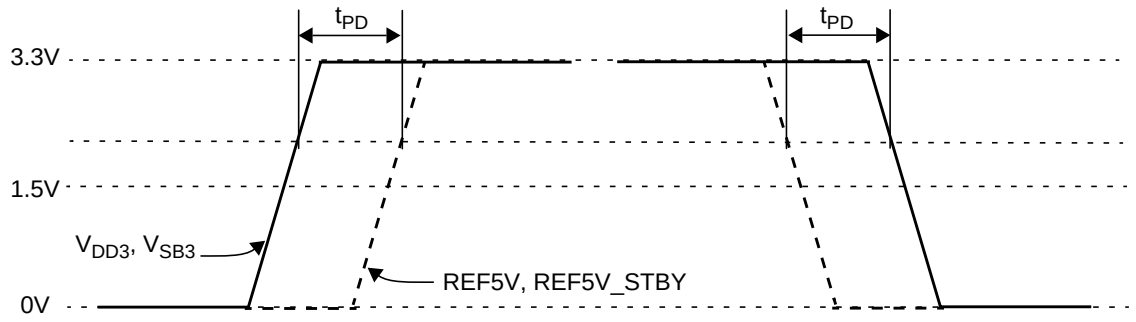


Figure 54. REF5V and REF5V_STBY (AC Characteristics)

Resume Reset

Symbol	Figure	Description	Reference Conditions	Min	Max	Units
t_{RD}	55	Rising Supply Delay[1] (typ. 32 ms)	$V_{SB5} > V_{TRIP}$ or $V_{SB3} > V_{SB3ON}$	10	100	ms
t_{FD5}	55	Falling V_{SB5} Supply Delay[1]	$V_{SB5} < V_{TRIP}$ and $V_{SB3} > V_{SB3ON}$		100	ns
t_{GA}	55	V_{SB5} and V_{SB3} Glitch Allowance[1]	$V_{SB5} < V_{TRIP}$ or $V_{SB3} < V_{SB3ON}$		100	ns
t_{FD3}	55	Falling V_{SB3} Supply Delay[1]	$V_{SB3} < V_{SB3ON}$ and $V_{SB5} > V_{TRIP}$		TBD	ns
t_R	55	Rise Time[2]	$V_{SB3} > V_{SB3ON}$		100	ns
t_F	55	Fall Time[2]	$V_{SB3} > V_{SB3ON}$		100	ns

1. Not tested. Guaranteed by characterization.
2. Not tested. Guaranteed by design.

13.0 Device Characteristics (Continued)

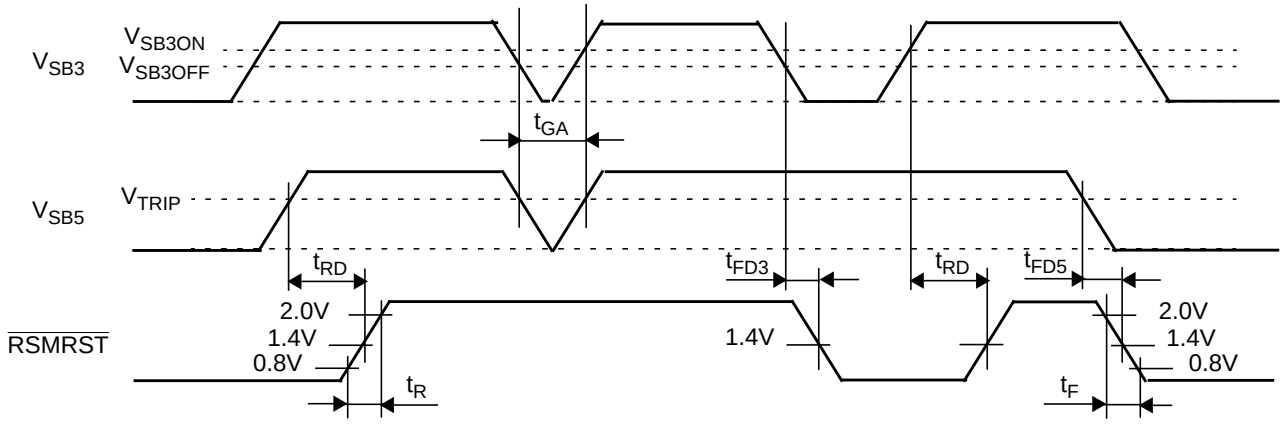


Figure 55. $\overline{RSMRST}$ (AC Characteristics)

Main Power Good

Symbol	Figure	Description	Reference Conditions	Min	Max	Units
t_{DB}	–	Debouncing time[1]	After RE or FE of $\overline{FPRST}$	768 * t_{CP}[2]	832 * t_{CP}	
t_{PDF}	–	$\overline{FPRST}$ Propagation Delay[1]	After RE or FE of $\overline{FPRST}$	768 * t_{CP}	832 * t_{CP}	
t_{PDP}	–	PWRGD_PS Propagation Delay[1]	After RE or FE of PWRGD_PS		1	µs
t_R	–	Rise Time[1]	0.8V to 2.0V		50	ns
t_F	–	Fall Time[1]	2.0V to 0.8V		50	ns

1. Not tested. Guaranteed by design.
2. t_{CP} is the cycle time of the 32 KHz clock domain (see *Low-Frequency Clock Timing on page 162*)

Rambus SCK Clock Gate Control

Symbol	Figure	Description	Reference Conditions	Min	Max	Units
t_{PF}	–	Fall Propagation Delay[1]	PWRGD_3V to FE of SCK_BJT_GATE		50	ns
t_F	–	Fall Time	0.8V to 2.0V		15	ns

1. Not tested. Guaranteed by characterization.

Power Distribution Control

Symbol	Figure	Description	Reference Conditions	Min	Max	Units
t_{PB}	–	$\overline{BKFD\_CUT}$ Propagation Delay[1]	PWRGD_PS or $\overline{SLP\_S3}$ to $\overline{BKFD\_CUT}$		1	µs
t_{TB}	–	$\overline{BKFD\_CUT}$ Transition Time[1]	0.8V to 2.0V		50	ns
t_{PL}	56	LATCHED_BF_CUT Propagation Delay[1]	$\overline{BKFD\_CUT}$ or $\overline{SLP\_S5}$ to LATCHED_BF_CUT		1	µs
t_{TL}	56	LATCHED_BF_CUT Transition Time[1]	0.8V to 2.0V		50	ns

1. Not tested. Guaranteed by design.

13.0 Device Characteristics (Continued)

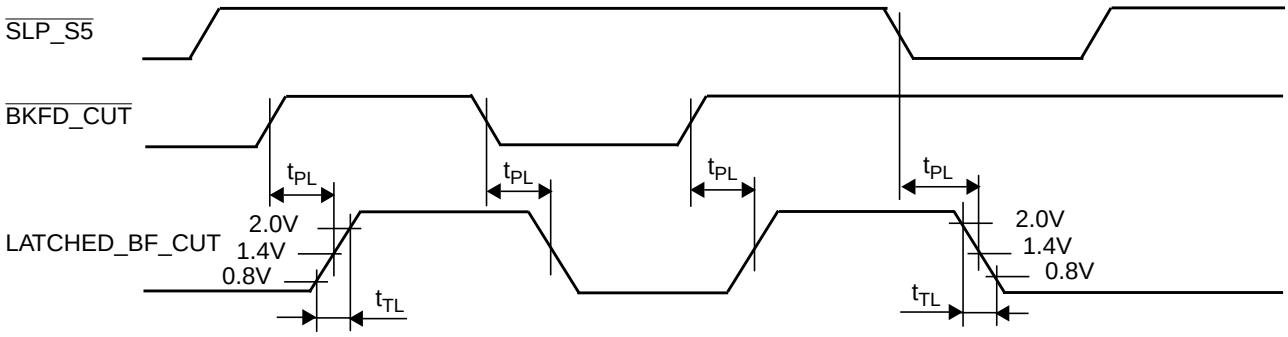


Figure 56. BKFD_CUT and LATCHED_BF_CUT (AC Characteristics)

Main Power Supply Control

Symbol	Figure	Description	Reference Conditions	Min	Max	Units
t_{PR}	–	Rise Propagation Delay[1]	CPU_PRESENT or SLP_S3 to RE of PS_ON		1	µs
t_{PF}	–	Fall Propagation Delay[1]	CPU_PRESENT or SLP_S3 to FE of PS_ON		1	µs
t_R	–	Rise Time[1]	0.8V to 2.0V		50	ns
t_F	–	Fall Time[1]	0.8V to 2.0V		50	ns

1. Not tested. Guaranteed by design.

CNR Downstream Codec Dynamic Control

Symbol	Figure	Description	Reference Conditions	Min	Max	Units
t_{PD}	–	Propagation Delay[1]	AUD_LINK_RST to CDC_DWN_RST		30	ns
t_{TR}	–	Transition Time[1]	0.8V to 2.0V		15	ns

1. Not tested. Guaranteed by characterization.

SMBus Voltage Translation and Isolation Timing

Symbol	Figure	Description	Type of Requirement[1]	Min	Max	Unit
t_{SMBR}	–	Rise Time (all signals)	Input		1000[2,3]	ns
t_{SMBF}	–	Fall Time (all signals)	Input		250[3]	ns
			Output		300[2,4]	ns
t_{SMBD}	–	Propagation Delay (each signal pair, in both directions)	Output		500[2,4]	ns

1. An “Input” type is a value the PC87373 device expects from the system; an “Output” type is a value the PC87373 device provides to the system.
2. Test conditions: R_L = 1 KΩ to V_{DD3} = 3.3V, or R_L = 1.5 KΩ to V_{DD5} = 5V and C_L = 400 pF to GND.
3. Not tested. Guaranteed by design.
4. Not tested. Guaranteed by characterization.

13.0 Device Characteristics (Continued)

13.4.9 SWC Timing

Wake-Up Inputs at V_{SB3} Power Switching

Symbol	Figure	Description	Reference Conditions	Min	Max
t_{EWIV}	57	External Wake-Up Inputs Valid[1]	At V_{SB3} power on, after the 32 KHz Domain is toggling	24576 * t_{CP}[2]	32768 * t_{CP}

1. Not tested. Guaranteed by characterization.
2. t_{CP} is the cycle time of the 32 KHz clock domain (see *Low-Frequency Clock Timing on page 162*)

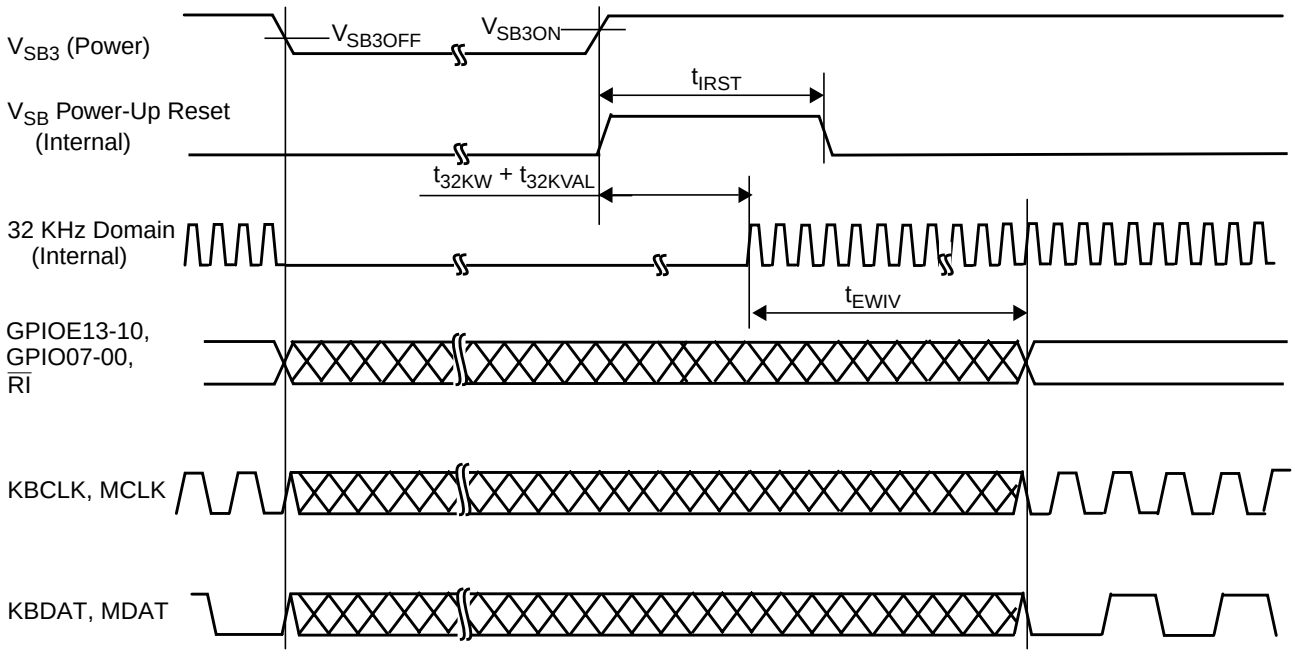


Figure 57. Inputs at V_{SB3} Power Switching

Wake-Up Inputs at V_{DD3} Power Switching

Symbol	Figure	Description	Reference Conditions	Min	Max
t_{EWIV}	58	External Wake-Up Inputs Valid[1]	After V_{DD3} power on[2]	24576 * t_{CP}[3]	32768 * t_{CP}

1. Not tested. Guaranteed by characterization.
2. The 32 KHz clock domain is assumed to be toggling at V_{DD3} power stable.
3. t_{CP} is the cycle time of the 32 KHz clock domain (see *Low-Frequency Clock Timing on page 162*)

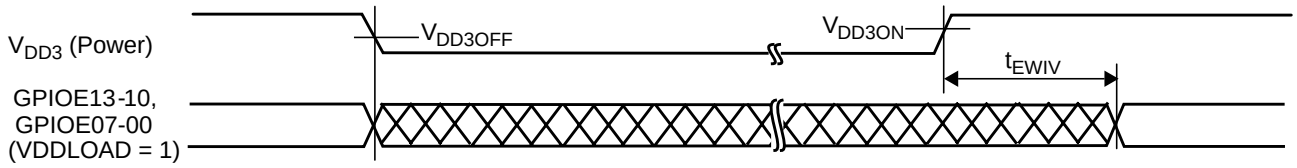
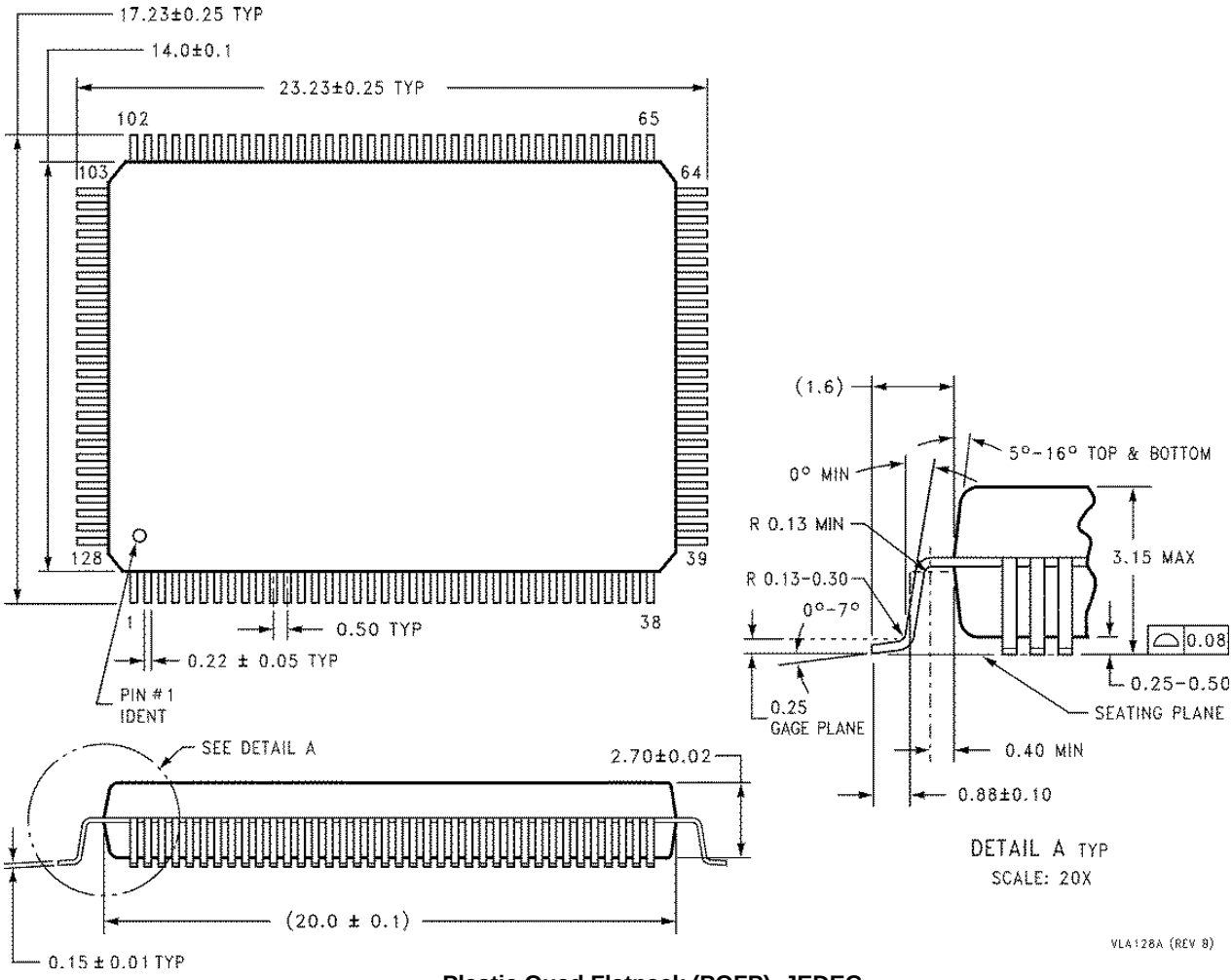


Figure 58. Wake-Up Inputs at V_{DD3} Power Switching

Physical Dimensions

All dimensions are in millimeters



Plastic Quad Flatpack (PQFP), JEDEC
Order Number PC87373-xxx/VLA
NS Package Number VLA128A

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