DATA SHEET

PCA9512

Level shifting hot swappable I^{2}C and SMBus buffer

Product data sheet

2004 Oct 05

Philips
Semiconductors

PHILIPS

Level shifting hot swappable I²C and SMBus buffer PCA9512

DESCRIPTION

The PCA9512 is a hot swappable I²C and SMBus buffer that allows I/O card insertion into a live backplane without corruption of the data and clock buses and includes two dedicated supply voltage pins to provide level shifting between 3.3 V and 5 V systems while maintaining the best noise margin for each voltage level. Either pin may be powered with supply voltages ranging from 2.7 V to 5.5 V with no constraints on which supply voltage is higher. Control circuitry prevents the backplane from being connected to the card until a stop bit or bus idle occurs on the backplane without bus contention on the card. When the connection is made, the PCA9512 provides bi-directional buffering, keeping the backplane and card capacitances isolated.

The dynamic offset design of the PCA9510/11/12/13/14 I/O drivers allow them to be connected to another PCA9510/11/12/13/14 device in series or in parallel and to the A side of the PCA9517. The PCA9510/11/12/13/14 can **not** connect to the static offset I/Os used on the PCA9515/15A/16/16A/17 B side and PCA9518.

FEATURES

- Bi-directional buffer for SDA and SCL lines increases fanout and prevents SDA and SCL corruption during live board insertion and removal from multi-point backplane systems
- Compatible with I²C standard mode, I²C fast mode, and SMBus standards
- ΔV/Δt rise time accelerators on all SDA and SCL lines with ability to disable ΔV/Δt rise time accelerators through the ACC pin for lightly loaded systems
- 5 V to 3.3 V level translation with optimum noise margin
- High-impedance SDA, SCL pins for V_{CC} or V_{CC2} = 0 V
- 1 V precharge on all SDA and SCL lines
- Supports clock stretching and multiple master arbitration/synchronization
- Operating power supply voltage range: 2.7 V to 5.5 V
- 5.5 V tolerant I/Os
- 0 kHz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8, TSSOP8 (MSOP8)

APPLICATION

- cPCI, VME, AdvancedTCA cards and other multi-point backplane cards that are required to be inserted or removed from an operating system.

PIN CONFIGURATION

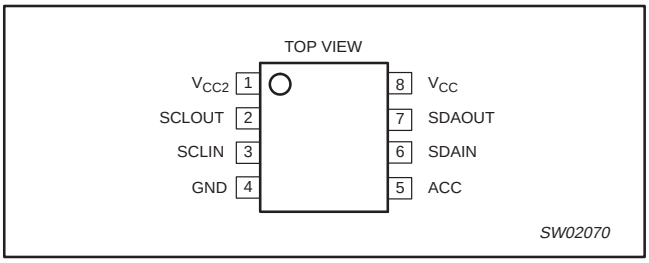


Figure 1. Pin configuration.

PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	V_{CC2}	Supply voltage for devices on the card I²C-buses. Connect pull-up resistors from SDAOUT and SCLOUT to this pin.
2	SCLOUT	Serial clock output to and from the SCL bus on the card.
3	SCLIN	Serial clock input to and from the SCL bus on the backplane.
4	GND	Ground. Connect this pin to a ground plane for best results.
5	ACC	CMOS threshold digital input pin that enables and disables the rise-time accelerators on all four SDA and SCL pins. ACC enables all accelerators when set to V_{CC2}, and turns them off when set to GND.
6	SDAIN	Serial data input to and from the SDA bus on the backplane/long distance bus.
7	SDAOUT	Serial data output to and from the SDA bus on the card.
8	V_{CC}	Power supply. From the backplane, connect pull-up resistors from SDAIN and SCLIN to this pin.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
8-pin plastic SO	–40 °C to +85 °C	PCA9512D	PCA9512	SOT96-1
8-pin plastic TSSOP (MSOP)	–40 °C to +85 °C	PCA9512DP	9512	SOT505-1

Standard packing quantities and other packaging data are available at www.standardproducts.philips.com/packaging.

TYPICAL APPLICATION

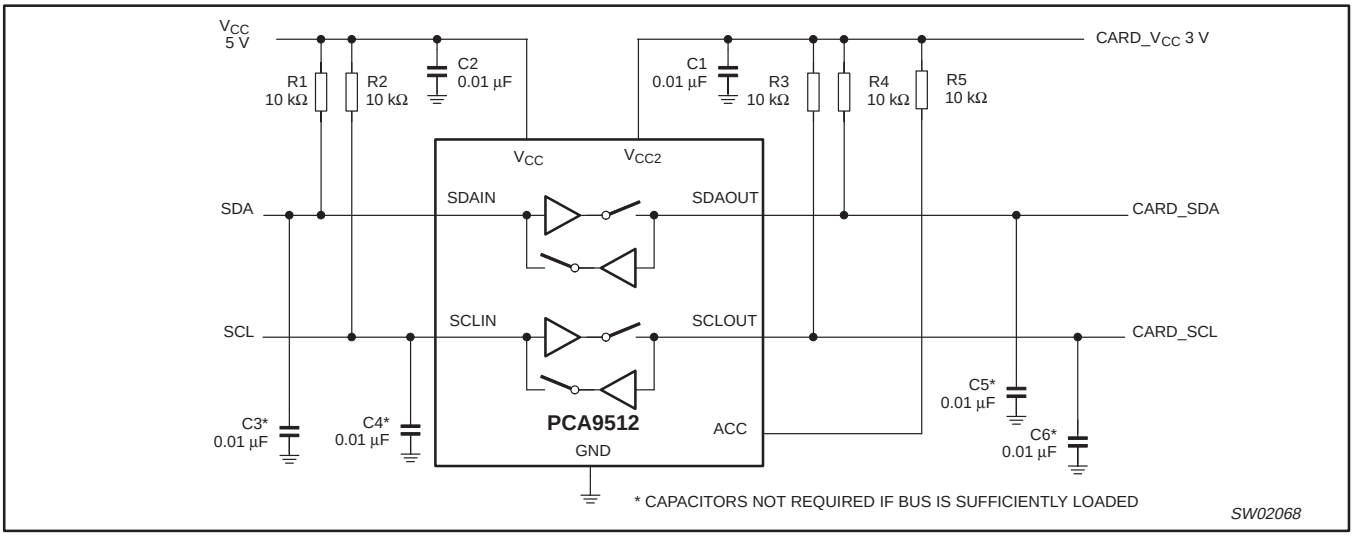


Figure 2. Typical application

BLOCK DIAGRAM

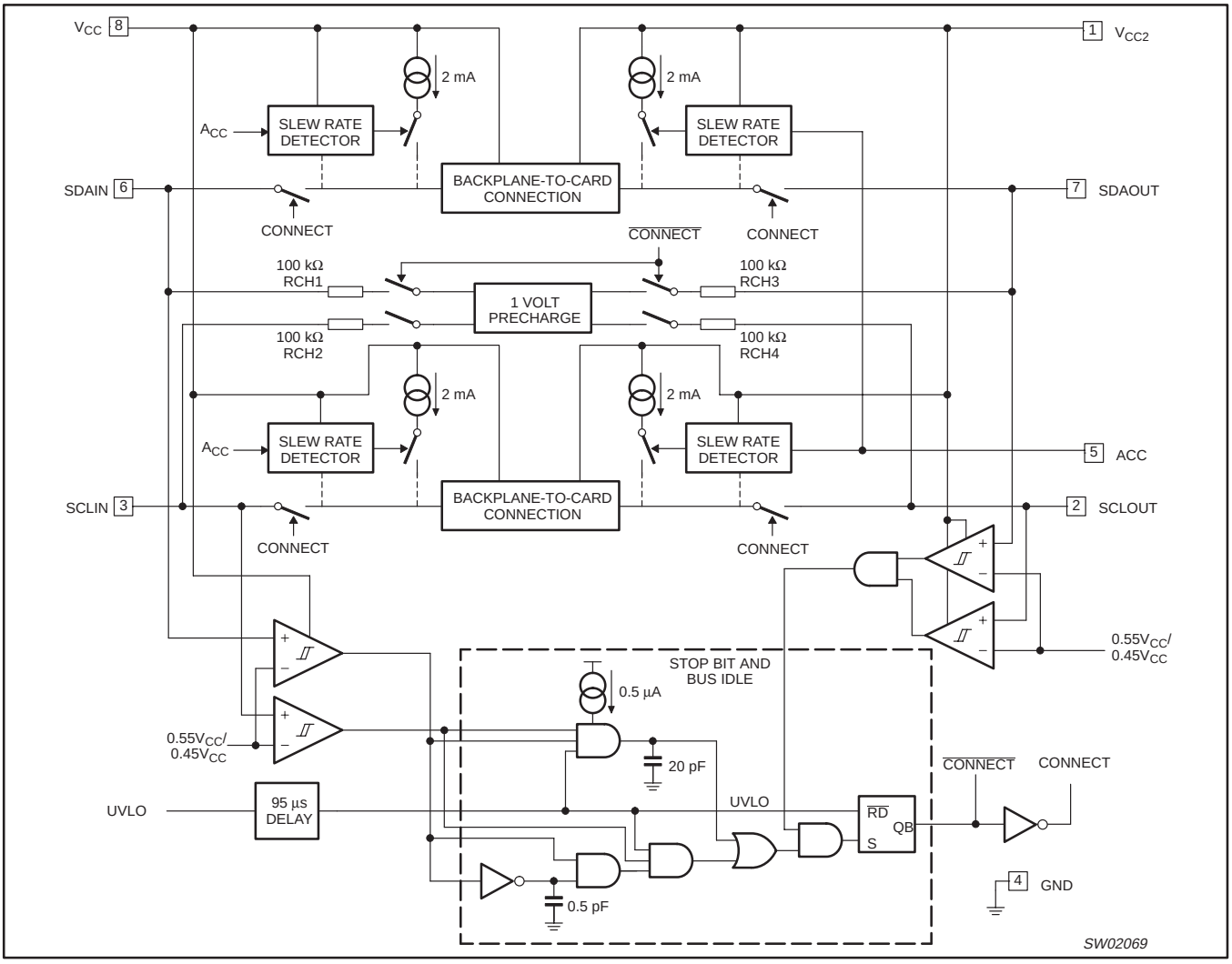


Figure 3. Block diagram.

FEATURE SELECTION CHART

FEATURES	PCA9510	PCA9511	PCA9512	PCA9513	PCA9514
Idle detect	Yes	Yes	Yes	Yes	Yes
High impedance SDA, SCL pins for V_{CC} = 0 V	Yes	Yes	Yes	Yes	Yes
Rise time accelerator circuitry on all SDA and SCL lines	—	Yes	Yes	Yes	Yes
Rise time accelerator circuitry hardware disable pin for lightly loaded systems	—	—	Yes	—	—
Rise time accelerator threshold 0.8 V vs 0.6 V improves noise margin	—	—	—	Yes	Yes
Ready open drain output	Yes	Yes	—	Yes	Yes
Two V_{CC} pins to support 5 V to 3.3 V level translation with improved noise margins	—	—	Yes	—	—
1 V precharge on all SDA and SCL lines	IN only	Yes	Yes	—	—
92 μA current source on SCLIN and SDAIN for PICMG applications	—	—	—	Yes	—

OPERATION

Start-up

When the PCA9512 is powered up either V_{CC} or V_{CC2} may rise first and either may be more positive or they may can be equal, however the PCA9512 will not leave the under voltage lock out/initialization state until both V_{CC} and V_{CC2} have gone above 2.5 V. If either V_{CC} or V_{CC2} drops below 2.0 V it will return to the under voltage lock out/initialization state. In the under voltage lock out state the connection circuitry is disabled, the rise time accelerators are disabled, and the precharge circuitry is also disabled. After both V_{CC} and V_{CC2} are valid, independent of which is higher, the PCA9512 enters the initialization state, during this state the 1 V precharge circuitry is activated and pulls up the SDA and SCL pins to 1 V through individual 100 kΩ nominal resistors. At the end of the initialization state the “Stop Bit And Bus Idle” detect circuit is enabled. When all the SDA and SCL pins have been HIGH for the bus idle time or when all pins are HIGH and a stop condition is seen on the SDAIN and SCLIN pins, the connect circuitry is activated, connecting SDAIN to SDAOUT and SCLIN to SCLOUT. The 1 V precharge circuitry is disabled when the connection is made, unless the ACC pin is LOW, the rise time accelerators are enabled at this time also.

Connection Circuitry

Once the connection circuitry is activated, the behavior of SDAIN and SDAOUT as well as SCLIN and SCLOUT become identical with each acting as a bidirectional buffer that isolated the input bus capacitance from the output bus capacitance while communicating the logic levels. If $V_{CC} \neq V_{CC2}$, then a level shifting function is also performed between input and output. A LOW forced on either SDAIN or SDAOUT will cause the other pin to be driven LOW by the PCA9512. The same is also true for the SCL pins. Noise between $0.7V_{CC}$ and V_{CC} on the SDAIN and SCLIN pins and $0.7V_{CC2}$ and V_{CC2} on the SDAOUT and SCLOUT pins is generally ignored because a falling edge is only recognized when it falls below the $0.7V_{CC}$ for SDAIN and SCLIN (or $0.7V_{CC2}$ for SDAOUT and SCLOUT pins) with a slew rate of at least 1.25 V/μs. When a falling edge is seen on one pin the other pin in the pair turns on a pull down driver that is reference to a small voltage above the falling pin. The driver will pull the pin down at a slow rate determined by the driver and the load. The first falling pin may have a fast or slow slew rate, if it is faster than the pull down slew rate then the initial pull down rate will continue until it is LOW. If the first falling pin has a slow slew rate then the second pin will be pulled down at its initial slew rate only until it is just above the first pin voltage then they will both continue down at the slew rate of the first. Once both sides are LOW they will remain LOW until all the external drivers have stopped driving LOWs. If both sides are being driven LOW to the same or nearly the same value by external drivers, which is the case for clock stretching and is typically the case for acknowledge, and one side external driver stops driving, that pin will rise and rise above the nominal offset voltage until the internal driver catches up and pulls it back down to the offset voltage. This bounce is worst for low capacitances and low resistances, and may become excessive. When the last external driver stops driving a LOW, that pin will bounce up and settle out just above the other pin as both rise together with a slew rate determined by the internal slew rate control and the RC time constant. As long as the slew rate is at least 1.25 V/μs, when the pin voltage exceed 0.6 V the rise time accelerator circuits are turned on and the pull down driver is turned off. If the ACC pin is LOW the rise time accelerator circuits will be disabled but the pull down driver will still turn off.

Maximum number of devices in series

Each buffer adds about 0.065 V dynamic level offset at 25 °C with the offset larger at higher temperatures. Maximum offset (V_{OS}) is 0.150 V. The LOW level at the signal origination end (master) is dependent upon the load and the only specification point is the I²C-bus specification of 3 mA will produce V_{OL} < 0.4 V, although if lightly loaded the V_{OL} may be ~0.1 V. Assuming V_{OL} = 0.1 V and V_{OS} = 0.1 V, the level after four buffers would be 0.5 V, which is only about 0.1 V below the threshold of the rising edge accelerator (about 0.6 V). With great care a system with four buffers may work, but as the V_{OL} moves up from 0.1 V, noise or bounces on the line will result in firing the rising edge accelerator thus introducing false clock edges. Generally it is recommended to limit the number of buffers in series to two.

The PCA9510 (rise time accelerator is permanently disabled) and the PCA9512 (rise time accelerator can be turned off) are a little different with the rise time accelerator turned off because the rise time accelerator will not pull the node up, but the same logic that turns on the accelerator turns the pull-down off. If the V_{IL} is above ~0.6 V and a rising edge is detected, the pull-down will turn off and will not turn back on until a falling edge is detected; so if the noise is small enough it may be possible to use more than two PCA9510 or PCA9512 parts in series but is not recommended.

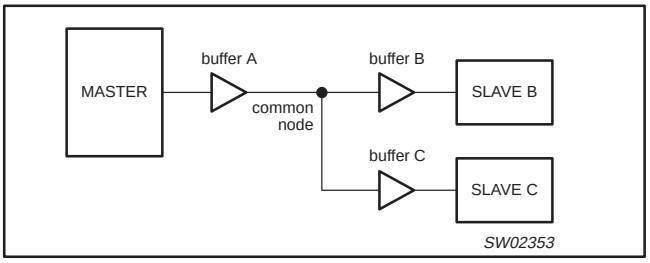


Figure 4.

Consider a system with three buffers connected to a common node and communication between the Master and Slave B that are connected at either end of Buffer A and Buffer B in series as shown in Figure 4. Consider if the V_{OL} at the input of Buffer A is 0.3 V and the V_{OL} of Slave B (when acknowledging) is 0.4 V with the direction changing from Master to Slave B and then from Slave B to Master. Before the direction change you would observe V_{IL} at the input of Buffer A of 0.3 V and its output, the common node, is ~0.4 V. The output of Buffer B and Buffer C would be ~0.5 V, but Slave B is driving 0.4 V, so the voltage at Slave B is 0.4 V. The output of Buffer C is ~0.5 V. When the Master pull-down turns off, the input of Buffer A rises and so does its output, the common node, because it is the only part driving the node. The common node will rise to 0.5 V before Buffer B's output turns on, if the pull-up is strong the node will bounce. If the bounce goes above the threshold for the rising edge accelerator ~0.6 V the accelerators on both Buffer A and Buffer C will fire contending with the output of Buffer B. The node on the input of Buffer A will go HIGH as will the input node of Buffer C. After the common node voltage is stable for a while the rising edge accelerators will turn off and the common node will return to ~0.5 V because the Buffer B is still on. The voltage at both the Master and Slave C nodes would then fall to ~0.6 V until Slave B turned off. This would not cause a failure on the data line as long as the return to 0.5 V on the common node (~0.6 V at the Master and Slave C) occurred before the data setup time. If this were the SCL line, the parts on Buffer A and Buffer C would see a false clock rather than a stretched clock, which would cause a system error.

Propagation Delays

The delay for a rising edge is determined by the combined pull-up current from the bus resistors and the PCA9512 and the effective capacitance on the lines. If the pull-up currents are the same, any difference in capacitance between the two sides. The t_{PLH} may be negative if the output capacitance is less than the input capacitance and would be positive if the output capacitance is larger than the input capacitance, when the currents are the same.

The t_{PHL} can never be negative because the output does not start to fall until the input is below $0.7V_{CC}$ (or $0.7V_{CC2}$ for SDAOUT and SCLOUT) and the output pull down turn on has a nonzero delay, and the output has a limited maximum slew rate and even it the input slew rate is slow enough that the output catches up it will still lag the falling voltage of the input by the offset voltage, The maximum t_{PHL} occurs when the input is driven LOW with zero delay and the output is still limited by its turn on delay and the falling edge slew rate, The output falling edge slew rate (which is a function of temperature, V_{CC} or V_{CC2}, and process) as well as load current and load capacitance.

Rise Time Accelerators

During positive bus transitions a 2 mA current source is switched on to quickly slew the SDA and SCL lines HIGH once the input level of 0.6 V is exceeded. The rising edge rate should be at least 1.25 V/µs to guarantee turn on of the accelerators.

ACC Boost Current Enable

Users having lightly loaded systems may wish to disable the rise-time accelerators. Driving this pin to ground turns off the rise-time accelerators on all four SDA and SCL pins. Driving this pin to the V_{CC2} voltage enables normal operation of the rise-time accelerators.

Resistor Pull-up Value Selection

The system pull-up resistors must be strong enough to provide a positive slew rate of 1.25 V/µs on the SDA and SCL pins, in order to activate the boost pull-up currents during rising edges. Choose maximum resistor value using the formula:

$$R \leq (V_{CC(MIN)} - 0.6)\ (800{,}000)/C$$

where R is the pull-up resistor value in ohms, $V_{CC(MIN)}$ is the minimum V_{CC} voltage and C is the equivalent bus capacitance in picofarads (pF).

In addition, regardless of the bus capacitance, always choose $R \leq 16\ k\Omega$ for $V_{CC} = 5.5$ V maximum, $R \leq 24\ k\Omega$ for $V_{CC} = 3.6$ V maximum. The start-up circuitry requires logic HIGH voltages on SDAOUT and SCLOUT to connect the backplane to the card, and these pull-up values are needed to overcome the precharge voltage. See the curves in Figures 5 and 6 for guidance in resistor pull-up selection.

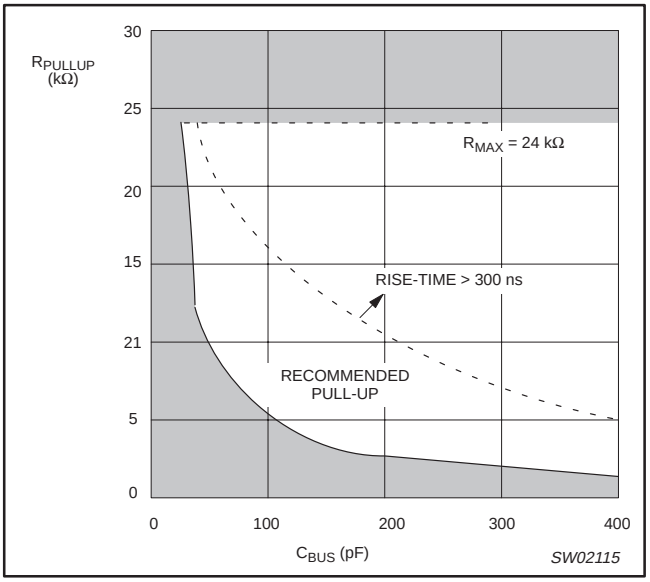


Figure 5. Bus requirements for 3.3 V systems

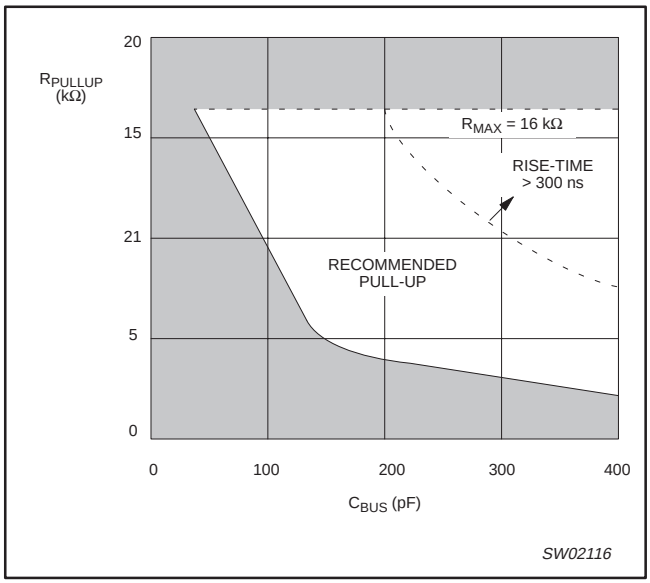


Figure 6. Bus requirements for 5 V systems

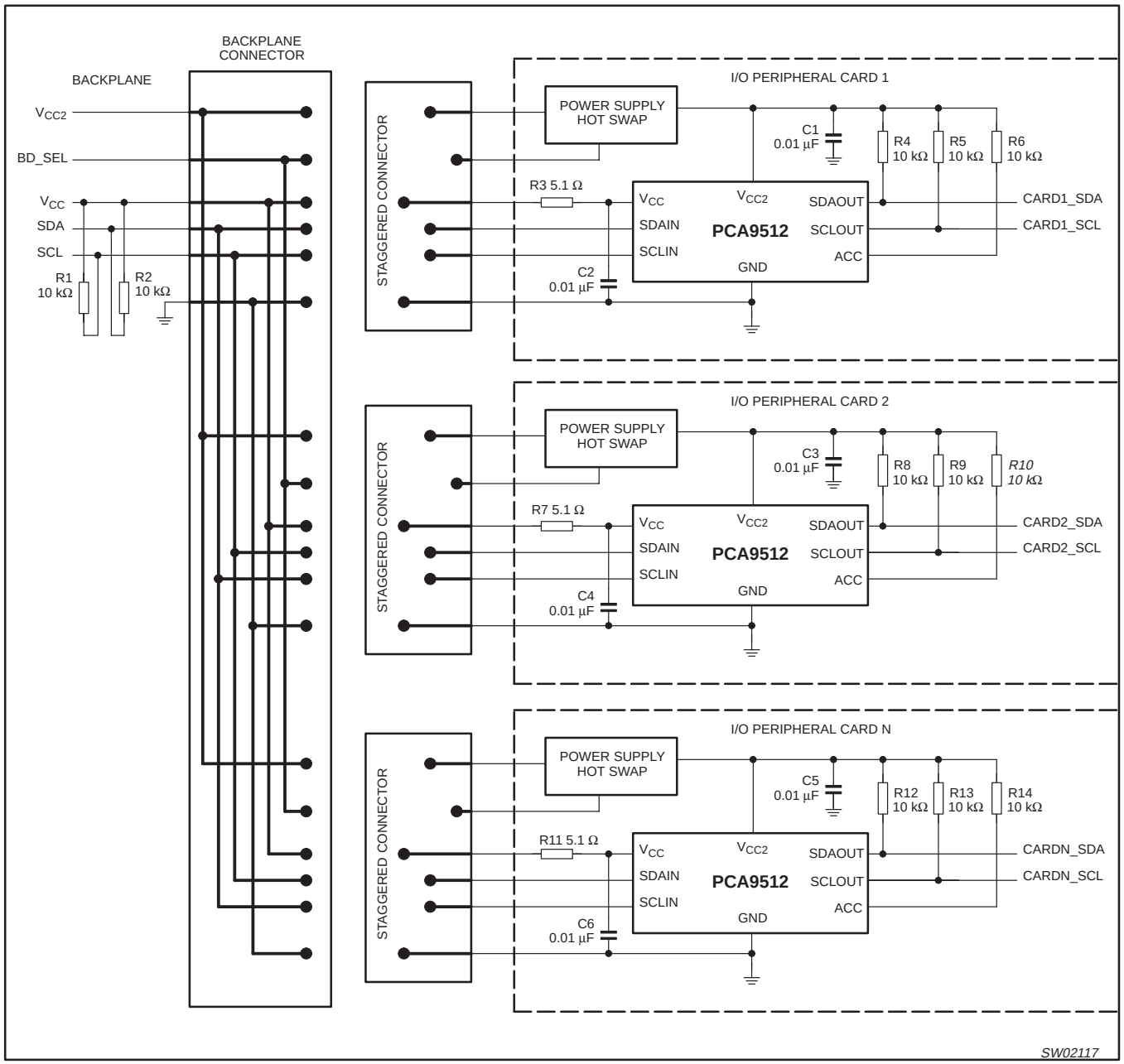
Minimum SDA and SCL Capacitance Requirements

The device connection circuitry requires a minimum capacitance loading on the SDA and SCL pins in order to function properly. The value of this capacitance is a function of V_{CC} and the bus pull-up resistance. Estimate the bus capacitance on both the backplane and the card data and clock buses, and refer to Figures 5 and 6 to choose appropriate pull-up resistor values. Note from the figures that 5 V systems should have at least 47 pF capacitance on their buses and 3.3 V systems should have at least 22 pF capacitance for proper operation of the PCA9512. Although the device has been designed to be marginally stable with smaller capacitance loads, for applications with less capacitance, provisions need to be made to add a capacitor to ground to ensure these minimum capacitance conditions if oscillations are noticed during initial signal integrity verification.

Hot Swapping and Capacitance Buffering Application

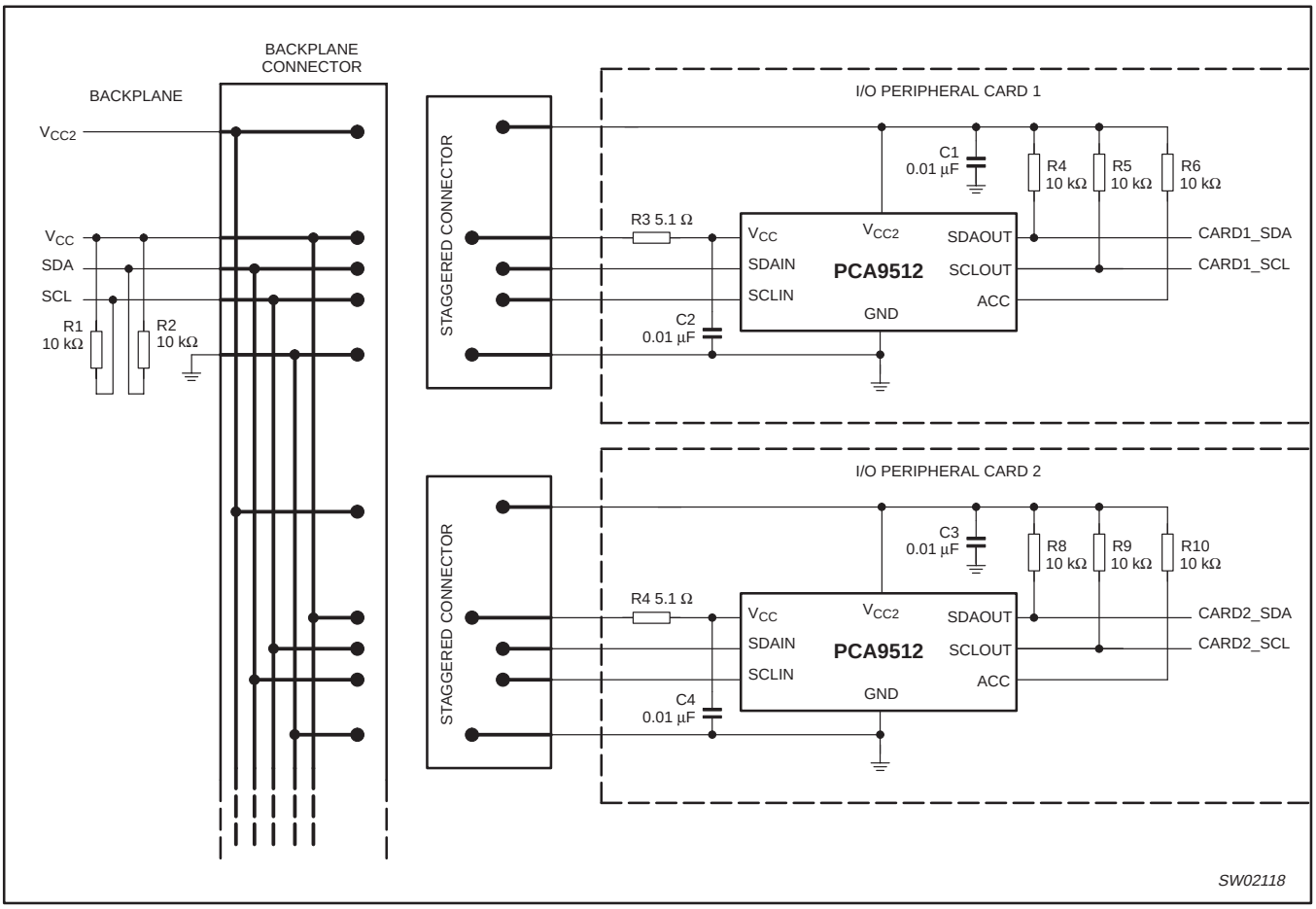
Figures 7 through 9 illustrate the usage of the PCA9512 in applications that take advantage of both its hot swapping and capacitance buffering features. In all of these applications, note that if the I/O cards were plugged directly into the backplane, all of the backplane and card capacitances would add directly together, making rise- and fall-time requirements difficult to meet. Placing a PCA9512 on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O card, the PCA9512 drives the capacitance of everything on the card and the backplane must drive only the the capacitance of the bus buffer, which is less than 10 pF, the connector, trace, and all additional cards on the backplane.

See Application Note *AN10160, Hot Swap Bus Buffer* for more information on applications and technical assistance.



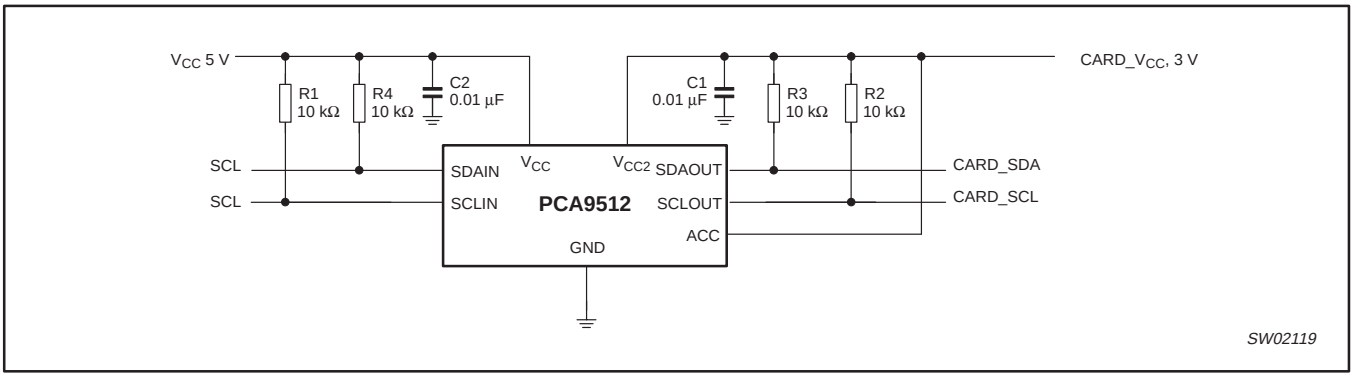
NOTE: Application assumes bus capacitance within “proper operation” region of Figures 5 and 6.

Figure 7. Hot swapping multiple I/O cards into a backplane using the PCA9512 in a CompactPCI, VME, and AdvancedTCA system



NOTE: Application assumes bus capacitance within “proper operation” region of Figures 5 and 6.

Figure 8. Hot swapping multiple I/O cards into a backplane using the PCA9512 with a custom connector



NOTE: Application assumes bus capacitance within “proper operation” region of Figures 5 and 6.

Figure 9. 5 V to 3.3 V level translator and bus buffer

ABSOLUTE MAXIMUM RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
Voltages with respect to pin GND.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN.	MAX.	
V_{CC}	Supply voltage range V_{CC}	–0.5	+7	V
V_{CC2}	Supply voltage range V_{CC2}	–0.5	+7	V
V_n	SDAIN, SCLIN, SDAOUT, SCLOUT, ACC	–0.5	+7	V
I_I	Maximum current for inputs	–	± 20	mA
I_{IO}	Maximum current for I/O pins	–	± 50	mA
T_{opr}	Operating temperature range	–40	+85	°C
T_{stg}	Storage temperature range	–65	+125	°C
T_{sld}	Lead soldering temperature (10 sec max)	—	+300	°C
$T_{j(max)}$	Maximum junction temperature	—	+125	°C

NOTE:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{CC} = 2.7 V to 5.5 V; T_{amb} = –40 °C to +85 °C unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power supply						
V_{CC}	Supply voltage	Note 1.	2.7	—	5.5	V
V_{CC2}	Card side supply voltage	Note 1.	2.7	—	5.5	V
I_{VCCI}	V_{CC} supply current	V_{CC} = 5.5 V; V_{SDAIN} = V_{SCLIN} = 0 V	—	1.2	3.6	mA
I_{VCC2}	V_{CC} supply current	V_{CC} = 5.5 V; V_{SDAOUT} = V_{SCLOUT} = 0 V	—	1.1	2.4	mA
Start-up circuitry						
V_{PRE}	Precharge voltage	SDA, SCL floating; Note 1.	0.8	1.1	1.2	V
t_{EN}	Enable time on power-up	Note 6.	—	180	—	µs
t_{IDLE}	Bus idle time	Notes 1 and 7.	50	140	250	µs
Rise time accelerators						
$I_{PULLUPAC}$	Transient boosted pull-up current	Positive transition on SDA, SCL, ACC = 0.7 V × V_{CC2}; V_{CC} = 2.7 V; Slew rate = 1.25 V/µs; Note 2.	1	2	—	mA
V_{ACCDIS}	Accelerator disable threshold		0.3 × V_{CC2}	0.5 × V_{CC2}	—	V
V_{ACCEN}	Accelerator enable threshold		—	0.5 × V_{CC2}	0.7 × V_{CC2}	V
I_{VACC}	A_{CC} input current		–1	± 0.1	1	µA
t_{PDOFF}	A_{CC} delay, on/off		—	5	—	ns
Input–output connection						
V_{OS}	Input–output offset voltage	10 kΩ to V_{CC} on SDA, SCL; V_{CC} = 3.3 V, V_{CC2} = 3.3 V; V_{IN} = 0.2 V; Note 1; Note 3.	0	70	150	mV
f_{SCL_SDA}	operating frequency	Guaranteed by design, not subject to test	0	—	400	kHz
C_{IN}	Digital input capacitance	Guaranteed by design, not subject to test	—	—	10	pF
V_{OL}	LOW-level output voltage	Input = 0 V. SDA, SCL pins; I_{SINK} = 3 mA; V_{CC} = 2.7 V; V_{CC2} = 2.7 V; Note 1.	0	—	0.4	V
I_{LI}	Input leakage current	SDA, SCL pins = V_{CC} = 5.5 V; V_{CC2} = 5.5 V	–1	—	5	µA
Timing characteristics						
f_{I2C}	I²C operating frequency	Note 4	0	—	400	kHz
t_{BUF}	Bus free time between stop and start condition	Note 4	1.3	—	—	µs
$t_{HD;STA}$	Hold time after (repeated) start condition	Note 4	0.6	—	—	µs
$t_{SU;STA}$	Repeated start condition setup time	Note 4	0.6	—	—	µs
$t_{SU;STO}$	Stop condition setup time	Note 4	0.6	—	—	µs
$t_{HD;DAT}$	Data hold time	Note 4	300	—	—	ns
$t_{SU;DAT}$	Data setup time	Note 4	100	—	—	ns
t_{LOW}	Clock LOW period	Note 4	1.3	—	—	µs
t_{HIGH}	Clock HIGH period	Note 4	0.6	—	—	µs
t_f	Clock, data fall time	Notes 4 and 5	20 + 0.1 × C_B	—	300	ns
t_r	Clock, data rise time	Notes 4 and 5	20 + 0.1 × C_B	—	300	ns

NOTES:
1. This specification applies over the full operating temperature range.
2. $I_{PULLUPAC}$ varies with temperature and V_{CC} voltage, as shown in the Typical Performance Characteristics section.

3. The connection circuitry always regulates its output to a higher voltage than its input. The magnitude of this offset voltage as a function of the pull-up resistor and V_{CC} voltage is shown in the Typical Performance Characteristics section.
4. Guaranteed by design, not production tested.
5. C_B = total capacitance of one bus line in pF.
6. Enable time is from power-up of V_{CC} and $V_{CC2} \geq 2.7$ V to when idle or stop time begins.
7. Idle time is from when SDAx and SCLx are HIGH after enable time has been met.

TYPICAL PERFORMANCE CHARACTERISTICS

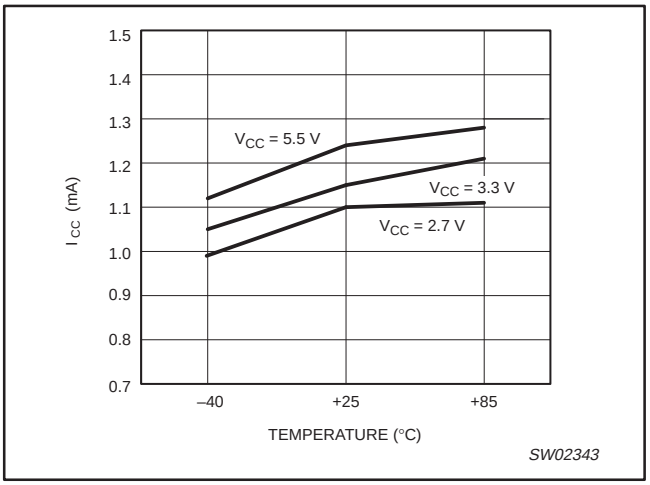


Figure 10. I_{CC} versus Temperature (Note 1)

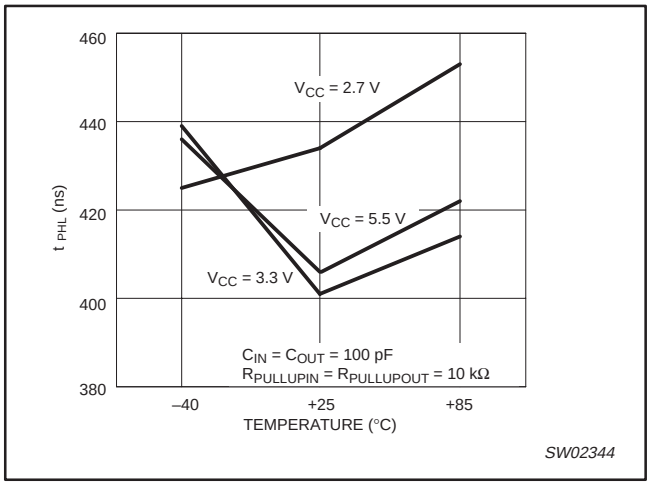


Figure 12. Input–output t_{PHL} versus Temperature

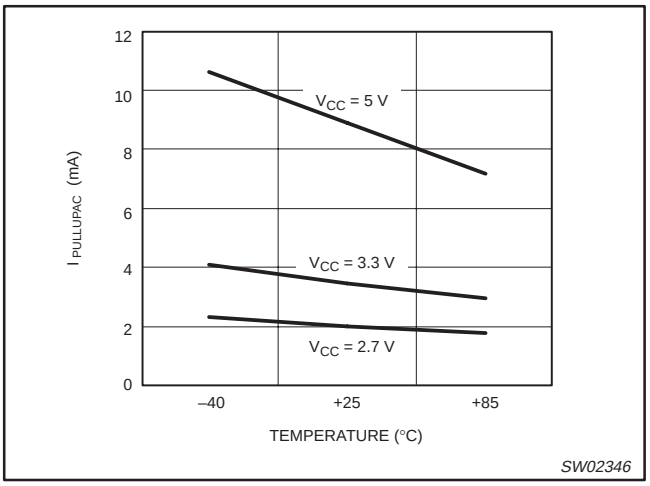


Figure 11. $I_{PULLUPAC}$ versus Temperature

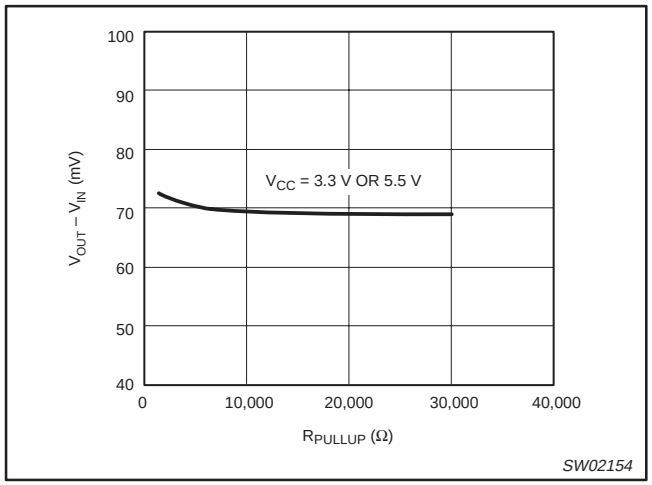
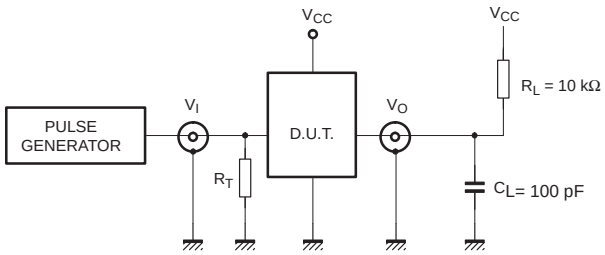


Figure 13. Connection circuitry $V_{OUT} - V_{IN}$

NOTE:
1. I_{CC2} (Pin 1) typical current averages 0.1 mA less than I_{CC} on Pin 8.

TEST CIRCUIT



DEFINITIONS

R_L = Load resistor.

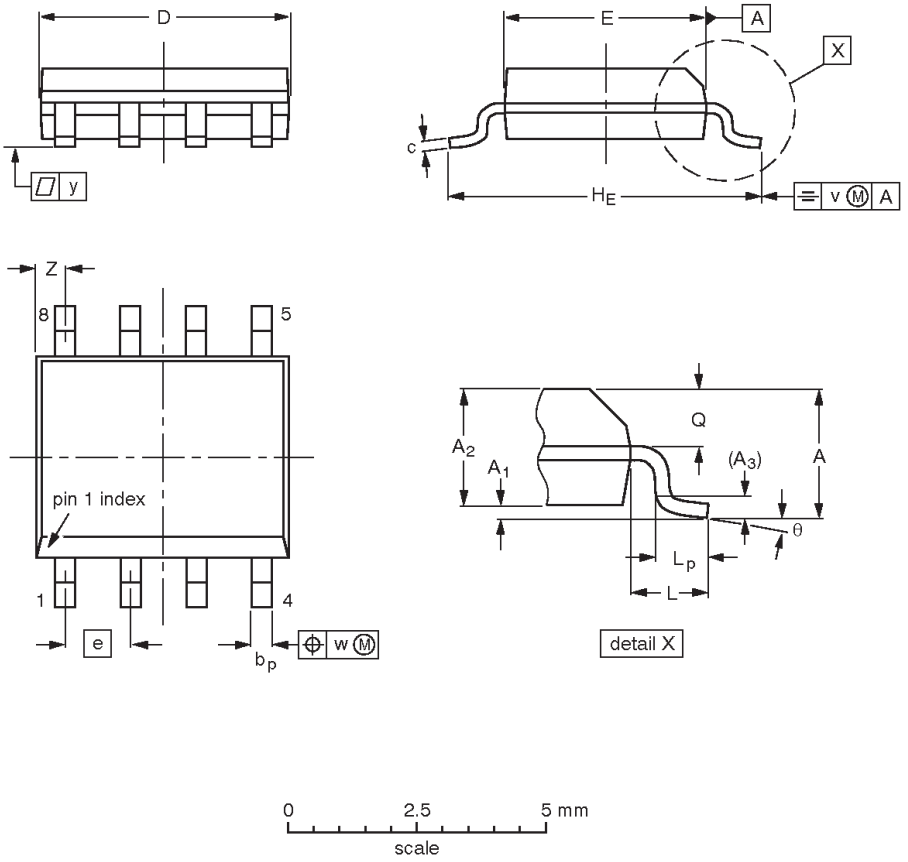
C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to the output impedance Z_O of the pulse generators.

SW02345

Figure 14. Test circuitry for switching times

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

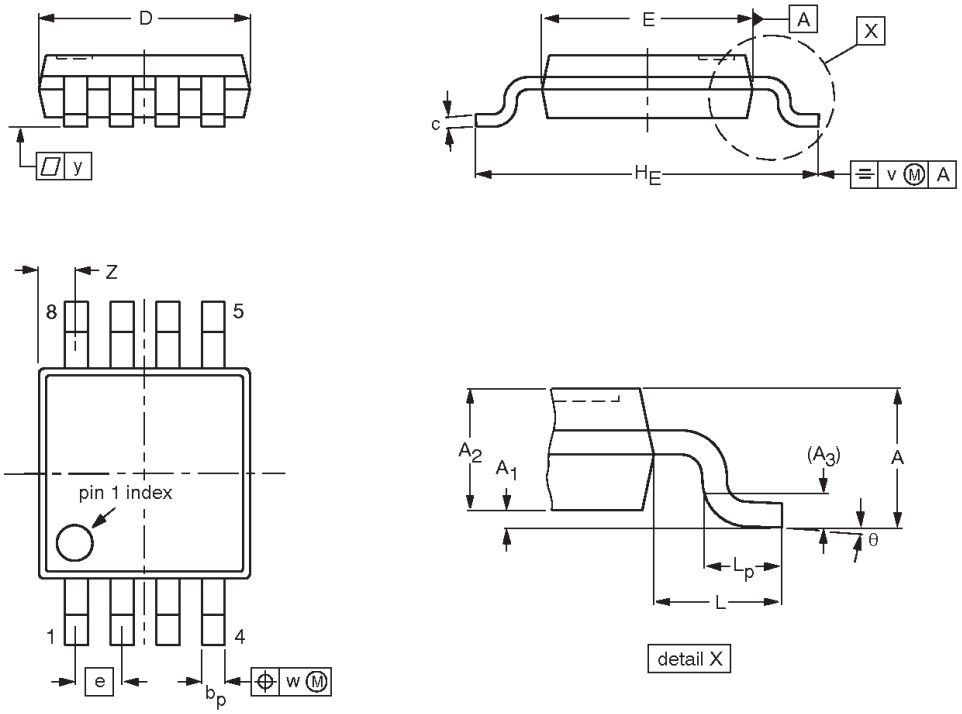
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

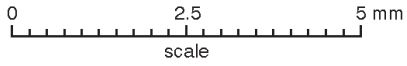
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

REVISION HISTORY

Rev	Date	Description
_1	20041005	**Product data sheet (9397 750 14005).**

Level shifting hot swappable I²C and SMBus buffer PCA9512

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 10-04

Document number: 9397 750 14005

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