CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCB8573 is a low threshold, monolithic CMOS circuit that functions as a real time clock/calendar in the Inter IC (I^2C) bus-orientated microcomputer systems. The device includes an addressable time counter and an addressable alarm register, both for minutes, hours, days and months. Three special control/status flags, COMF, POWF and NODA, are also available. Information is transferred serially via a two line bidirectional bus (I^2C). To transfer data a second supply voltage must be present. Back-up for the clock during supply interruptions is provided by a 1,2 V nickel cadium battery. The time base is generated from a 32,768 kHz crystal-controlled oscillator.

Features

- Serial input/output bus (I^2C) interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32,768 kHz)

QUICK REFERENCE DATA

purple binder, tab 5

Supply voltage range (logic)	$V_{DD}-V_{SS1}$	1,1 to 2,6	V
Supply voltage range (level shifter)	$V_{DD}-V_{SS2}$	2,5 to 6,0	V
Crystal oscillator frequency	f_{osc}	typ. 32 768	Hz

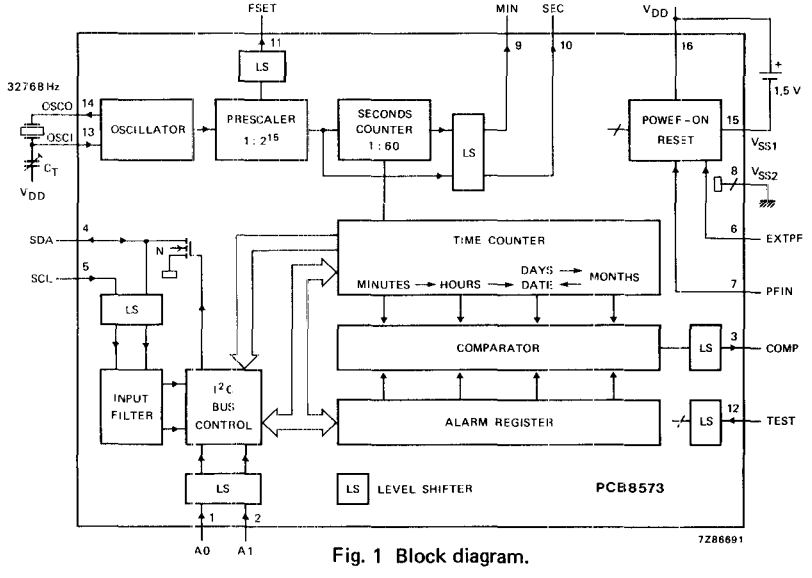


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

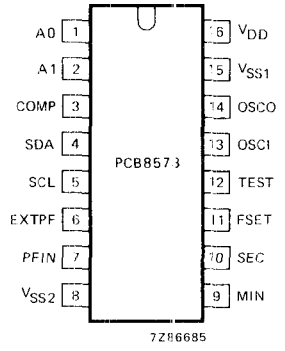


Fig. 2 Pinning diagram.

PINNING

1	A0	level shifter input
2	A1	level shifter input
3	COMP	comparator output
4	SDA	serial data line* (I²C bus)
5	SCL	serial clock line (I²C bus)
6	EXTPF	external power fail flag input
7	PFIN	internal power fail flag input
8	V_{SS2}	negative supply 2
9	MIN	one pulse per minute output
10	SEC	one pulse per second output
11	FSET	oscillator set output
12	TEST	test input; must be connected to V_{SS2} when not in use
13	OSCI	oscillator input
14	OSCO	oscillator input/output
15	V_{SS1}	negative supply 1
16	V_{DD}	common positive supply

FUNCTIONAL DESCRIPTION

The following is a functional description of the PCB8573.

Oscillator

The PCB8573 has an intergrated crystal-controlled oscillator which provides the timebase for the prescaler. The frequency is determined by a single 32,768 kHz crystal connected between OSCI and OSCO. A trimmer (C_T) is connected between OSCI and V_{DD}.

Prescaler and time counter

The prescaler provides a 128 Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC, MIN respectively, and are also readable via the I²C bus. The mark-to-space ratio of both signals is 1 : 1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH to LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected once every four years. Cycle lengths are shown in Table 1.

* Output open drain n-channel.

Table 1 Cycle length of the time counter

unit	number of bits	counting cycle	carry for following unit	content of month counter
minutes	7	00 to 59	59 → 00	
hours	6	00 to 23	23 → 00	
days	6	01 to 28	28 → 01	2 (see note)
			or 29 → 01	
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	5	01 to 12	12 → 01	

Note: Day counter may be set to 29 by a write transmission with EXECUTE ADDRESS.

Alarm register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I^2C bus.

Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal the flag COMP will be set 4 ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I^2C bus. A clear instruction may be transmitted immediately after the flag is set and will be executed. The effect of both COMP and POWF being set is dependent upon the master software. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I^2C bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I^2C bus.

Power on/power fail detection

If the voltage $V_{DD}-V_{SS1}$ falls below a certain value the operation of the clock becomes undefined. Thus a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTE ADDRESS has been received. The flag POWF can be set by an internally generated power fail level-discriminator signal, for application with $V_{DD}-V_{SS1} > V_{TH1}$, or by an externally generated power fail signal, for application with $V_{DD}-V_{SS1} < V_{TH1}$. The external signal must be applied to the input PFIN. The input stage operates with signals of any slow rise and fall times. Internal or externally controlled POWF can be selected by input EXTPF as shown in Table 2.

FUNCTIONAL DESCRIPTION (continued)

Table 2 Power fail selection

EXTPF	PFIN	function
0	0	power fail is sensed internal
0	1	test mode
1	0	power fail is sensed external
1	1	no power fail sensed

0 : connected to V_{SS} (LOW)
1 : connected to V_{DD} (HIGH)

The external power fail control operates by absence of the $V_{DD}-V_{SS2}$ supply. Therefore the input levels applied to PFIN and EXTPF must be within the range of $V_{DD}-V_{SS1}$. A LOW level at PFIN indicates a power fail. POWF is readable via the I^2C bus. A power on reset for the I^2C bus control is generated on-chip, when the supply voltage $V_{DD}-V_{SS2}$ is 1,5 V $<$ ($V_{DD}-V_{SS1}$) $<$ 2,5 V.

Interface level shifters

The level shifters adjust the 5 V operating voltage ($V_{DD}-V_{SS2}$) of the microcomputer to the internal $\geqslant$ 1,1 V supply voltage ($V_{DD}-V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD}-V_{SS2}$ supply voltage. If the voltage $V_{DD}-V_{SS2}$ is absent ($V_{SS2} = V_{DD}$) the output signal of the level shifter is HIGH because V_{DD} is the common mode of the $V_{DD}-V_{SS2}$ and the $V_{DD}-V_{SS1}$ supply. Because the level shifters invert the input signal, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages, for applications the source capability on these outputs is cut off when the supply voltage V $V_{DD}-V_{SS2} = 0$.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for two-way, 2 line-communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer (see Fig. 3)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line ate this time will be interpreted as control signals.

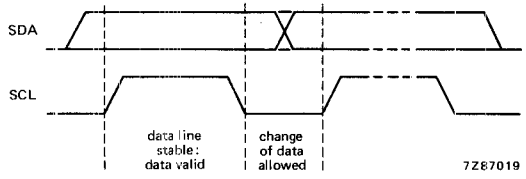


Fig. 3 Bit transfer.

Start and stop conditions (see Fig. 4)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

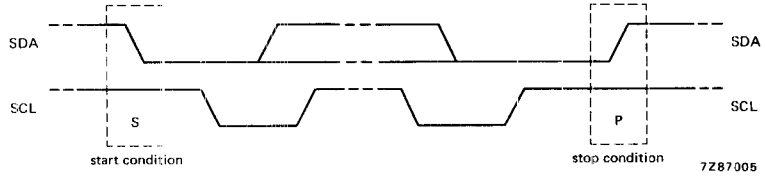


Fig. 4 Definition of start and stop conditions.

System configuration (see Fig. 5)

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

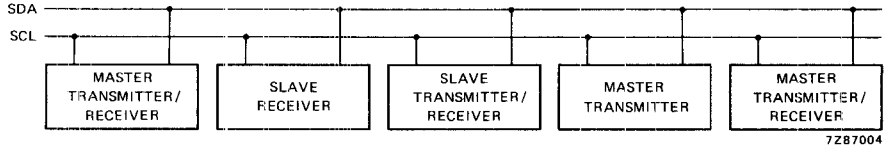


Fig. 5 System configuration.

CHARACTERISTICS OF THE I²C bus (continued)

Acknowledge (see Fig. 6)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition. (See Fig. 13 and Fig. 14.)

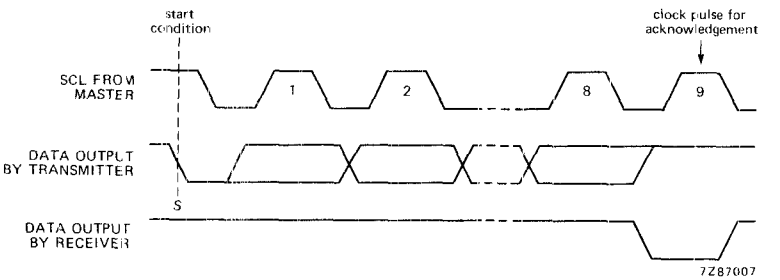


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCB8573 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

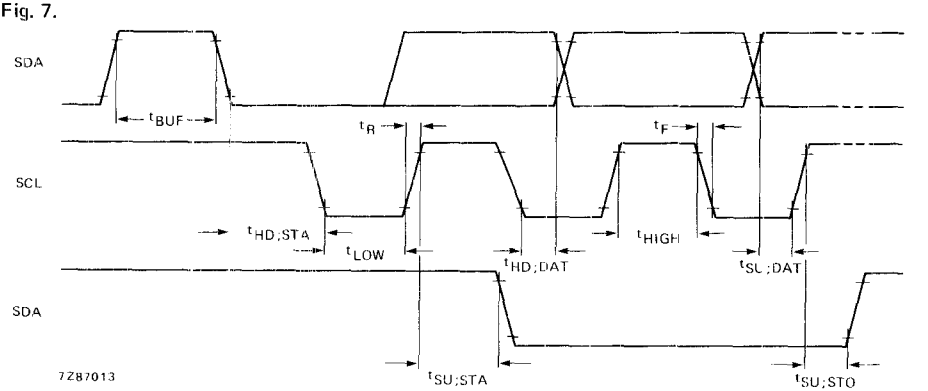


Fig. 7 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values referred to V_{IH} and V_{IL} levels.

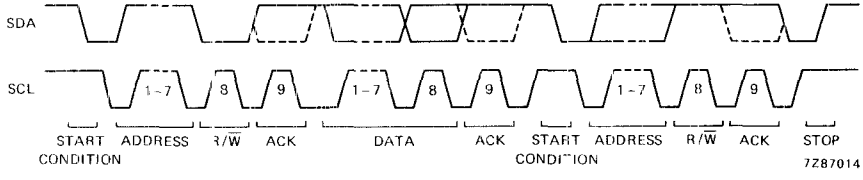


Fig. 8 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

CHARACTERISTICS OF THE I²C BUS (continued)

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 9.

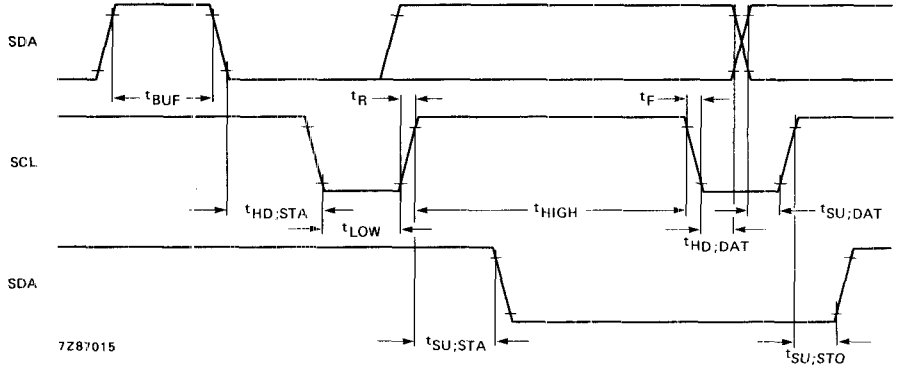


Fig. 9 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	130 μs ± 25 μs
t_{HIGH}	390 μs ± 25 μs
$t_{SU;STA}$	130 μs ± 25 μs*
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	130 μs ± 25 μs

Note

All the values referred to V_{IH} and V_{IL} levels, for definitions see high-speed mode.

* Only valid for repeated start code.

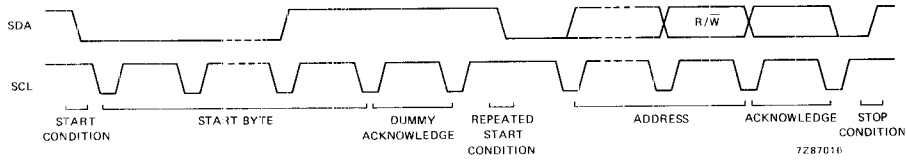


Fig. 10 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

DEVELOPMENT SAMPLE DATA

ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock calendar slave address is shown in Fig. 11.

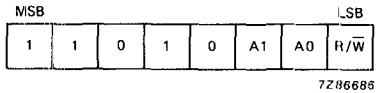


Fig. 11 Slave address.

The subaddress bits A0 and A1 correspond to the two hardware address pins A0 and A1 which allows the device 1 of 4 different addresses.

Clock/calendar READ/WRITE cycles

The I²C bus configuration for different clock/calendar READ and WRITE cycles is shown in Fig. 12 and Fig. 13.

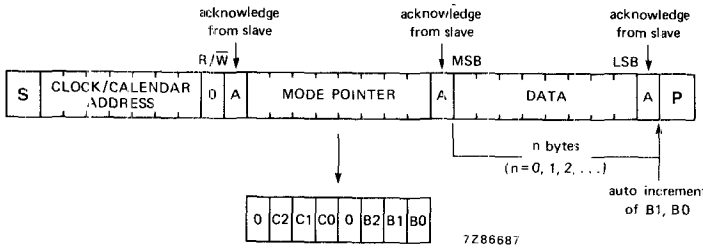


Fig. 12 Master transmitter transmits to clock/calendar slave receiver.

This mode is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-WORD which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nibble is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

Table 3 CONTROL-nibble

	C2	C1	C0	function
0	0	0	0	execute address
0	0	0	1	read control/status flags
0	0	1	0	reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	time adjust, with carry for minute counter (see note)
0	1	0	0	reset NODA flag
0	1	0	1	set NODA flag
0	1	1	0	reset COMP flag

Note

If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. −30 s. From the count 30 there is a carry which adjusts the time by max. + 30 s.

Table 4 ADDRESS-nibble

	B2	B1	B0	addressed to:
0	0	0	0	time counter hours
0	0	0	1	time counter minutes
0	0	1	0	time counter days
0	0	1	1	time counter months
0	1	0	0	alarm register hours
0	1	0	1	alarm register minutes
0	1	1	0	alarm register days
0	1	1	1	alarm register months

DEVELOPMENT SAMPLE DATA

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

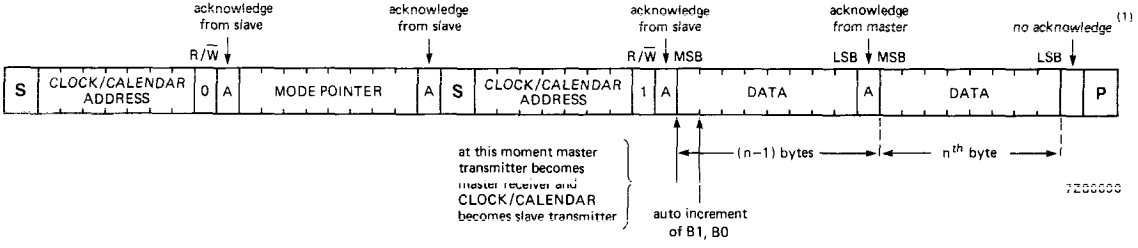
Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register respectively.

Table 5 Placement of BCD digits in the DATA byte

MSB				DATA			LSB	
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to:
X	X	D	D	D	D	D	D	hours
X	D	D	D	D	D	D	D	minutes
X	X	D	D	D	D	D	D	days
X	X	X	D	D	D	D	D	months

Where "X" is the don't care bit and "D" is the data bit.

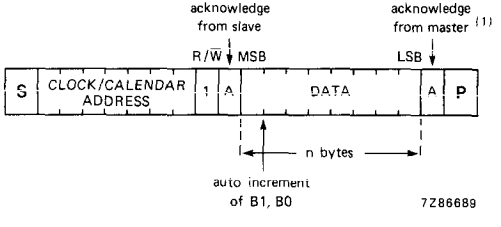
Acknowledgement response of the clock calendar as the slave receiver is shown in Table 6.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 13 Master transmitter reads clock/calendar after setting mode pointer.

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 14 Master reads clock/calendar immediately after first bite.

The status of the MODE-POINTER-WORD concerning the CONTROL-nibble remains unchanged until a write to MODE POINTER condition occurs.

ADDRESSING (continued)

Table 6 Slave receiver acknowledgement

mode pointer								acknowledge on byte		
								address	mode pointer	data
	C2	C1	C0		B2	B1	B0			
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

Where "X" is the don't care bit.

Table 7 Organization of the BCD digits in the DATA byte

MSB DATA LSB								
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to
0	0	D	D	D	D	D	D	hours
0	D	D	D	D	D	D	D	minutes
0	0	D	D	D	D	D	D	days
0	0	0	D	D	D	D	D	months
0	0	0	*	**	NODA	COMP	POWF	control/status flags

Where: "D" is the data bit.
* = minutes.
** = seconds.

DEVELOPMENT SAMPLE DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges	V_{DD}–V_{SS1}		−0,3 to + 8 V
	V_{DD}–V_{SS2}		−0,3 to + 8 V
Voltage on pins 4 and 5		V_{SS2}	−0,8 to V_{DD} + 0,8 V*
Voltage on pins 6, 7, 13 and 14		V_{SS1}	−0,6 to V_{DD} + 0,6 V
Voltage on any other pin		V_{SS2}	−0,6 to V_{DD} + 0,6 V
Input current	I_I	max.	100 μA
Output current	I_O	max.	10 mA
Power dissipation per output	P_O	max.	100 mW
Total power dissipation per package	P_{tot}	max.	200 mW
Operating ambient temperature range	T_{amb}		0 to + 70 °C
Storage temperature range	T_{stg}		−55 to + 125 °C

* Impedance min. 500 Ω.

CHARACTERISTICS

V_{SS2} = 0 V; T_{amb} = 0 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage level shifter	$V_{DD}-V_{SS2}$	2,5	5	6,0	V
Supply voltage logic	$V_{DD}-V_{SS1}$	1,1	–	2,6	V
Supply current V_{SS1} at $V_{DD}-V_{SS1}$ = 1,5 V	$-I_{SS1}$	–	–	10	μA
Supply current V_{SS2} at $V_{DD}-V_{SS2}$ = 5 V (I_O = 0 mA on all outputs)	$-I_{SS2}$	–	–	50	μA
Inputs					
Inputs SCL, SDA, A0, A1, TEST					
Input leakage current at $V_{DD}-V_{SS2}$ = 6 V; T_{amb} = 25 °C					
V_I = 6 V	I_I	–	–	1	μA
V_I = 0 V	$-I_I$	–	–	1	μA
Inputs SCL, SDA, A0, A1, TEST (level shifter inputs) at $V_{DD}-V_{SS2}$ = 2,5 to 6 V					
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	–	V
Input voltage LOW	V_{IL}	–	–	0,3 x V_{DD}	V
Inputs EXTPF, PFIN at $V_{DD}-V_{SS1}$ = 1,1 to 2,6 V					
Input voltage HIGH	V_{IH}	0,7 x $V_{DD}-V_{SS1}$		–	V
Input voltage LOW	V_{IL}	–	–	0,3 x $V_{DD}-V_{SS1}$	V
Input leakage current at $V_{DD}-V_{SS1}$ = 2,6 V; T_{amb} = 25 °C					
$V_I = V_{DD}$	I_I	–	–	0,1	μA
$V_I = V_{SS1}$	$-I_I$	–	–	0,1	μA

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Outputs					
Outputs SEC, MIN, COMP, FSET (*normal buffer outputs*)					
Output voltage HIGH					
at $V_{DD}-V_{SS2}$ = 2,5 V $-I_O$ = 0,1 mA	V_{OH}	$V_{DD}-0,4$	–	–	V
at $V_{DD}-V_{SS2}$ = 4 to 6 V $-I_O$ = 0,5 mA	V_{OH}	$V_{DD}-0,4$	–	–	V
Output voltage LOW					
at $V_{DD}-V_{SS2}$ = 2,5 V I_O = 0,3 mA	V_{OL}	–	–	0,4	V
at $V_{DD}-V_{SS2}$ = 4 to 6 V I_O = 1,6 mA	V_{OL}	–	–	0,4	V
Output SDA (N-channel open drain)					
Output "ON": I_O = 3 mA at $V_{DD}-V_{SS2}$ = 2,5 to 6 V	V_{OL}	–	–	0,4	V
Output "OFF" (leakage current)					
V_O = 6 V; T_{amb} = 25 °C at $V_{DD}-V_{SS2}$ = 6 V	I_O	–	–	1	μA
Internal threshold voltage					
Power failure detection	V_{TH1}	1	1,2	1,4	V
Power "ON" reset at $V_{SCL} = V_{SDA} = V_{DD}$	V_{TH2}	1,5	2,0	2,5	V
Rise and fall times of input signals					
Input EXTPF at $V_{DD}-V_{SS1}$ = 1,1 to 2,6 V	t_r, t_f	–	–	1	μs
Input PFIN at $V_{DD}-V_{SS1}$ = 1,1 to 2,6 V (10% to 90% ($V_{DD}-V_{SS1}$))	t_r, t_f	–	–	∞	μs
Input signals except EXTPF and PFIN at $V_{DD}-V_{SS2}$ = 2,5 to 6 V between V_{IL} and V_{IH} levels					
rise time	t_r	–	–	1	μs
fall time	t_f	–	–	0,3	μs

parameter	symbol	min.	typ.	max.	unit
Frequency at SCL					
at $V_{DD}-V_{SS2}$ = 4 to 6 V					
Pulse width LOW (see Figs 7 and 9)	t_{LOW}	4,7	–	–	μs
Pulse width HIGH (see Figs 7 and 9)	t_{HIGH}	4	–	–	μs
Noise suppression time constant at SCL and SDA output	T_I	0,25	1	2,5	μs
Input capacitance (SCL, SDA)	C_I	–	–	7	pF
Oscillator					
Integrated oscillator capacitance	C_{out}	–	40	–	pF
Oscillator feedback resistance	R_f	–	3	–	MΩ
Oscillator stability for: $\Delta(V_{DD}-V_{SS1})$ = 100 mV at $V_{DD}-V_{SS1}$ = 1,55 V; T_{amb} = 25 °C	f/f_{osc}	–	2×10^{-6}	–	–
Quartz crystal parameters					
Frequency = 32,768 kHz					
Series resistance	R_S	–	–	40	kΩ
Parallel capacitance	C_L	–	9	–	pF
Trimmer capacitance	C_T	–	5,25	–	pF

DEVELOPMENT SAMPLE DATA

APPLICATION INFORMATION

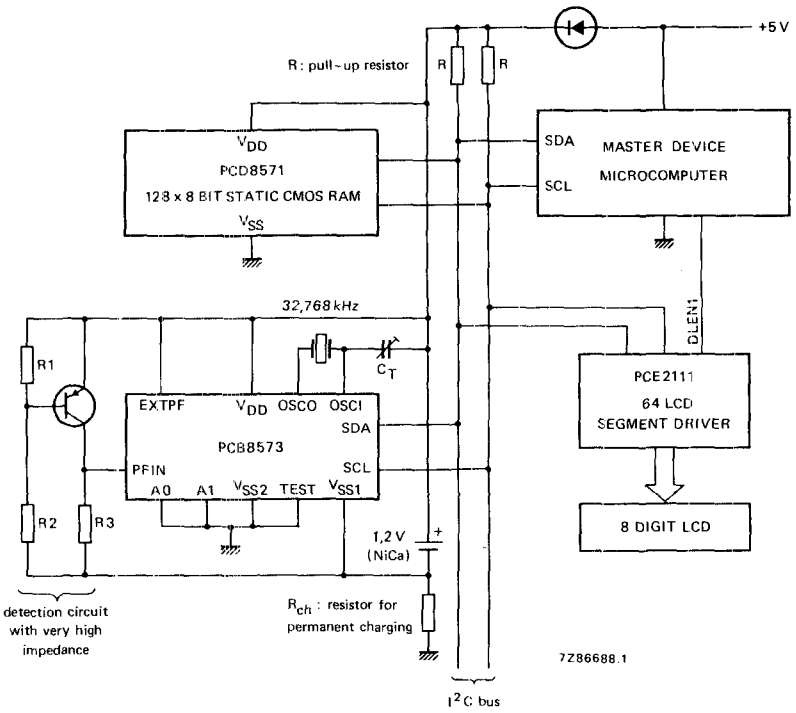
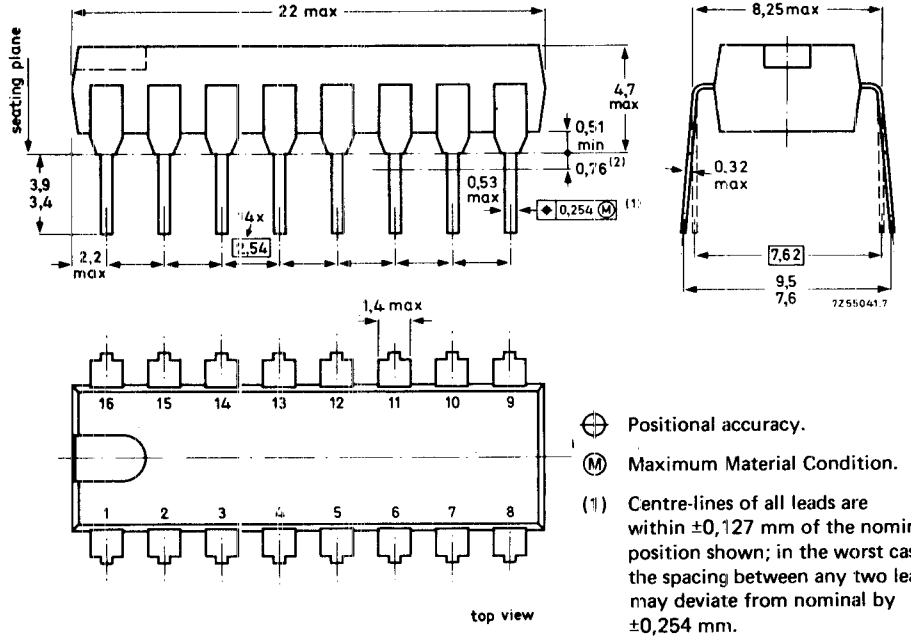


Fig. 15 Application example of the PCB8573 clock/calendar.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

DEVELOPMENT SAMPLE DATA

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.