PCD3311/12
DTMF/Modem/Musical Tone Generators

Product Specification

Linear Products

DESCRIPTION

The PCD3311 and PCD3312 are single-chip silicon gate CMOS integrated circuits. They are intended to provide dual-tone multi-frequency (DTMF) combinations required for tone dialing systems in telephone sets which contain a microcontroller for the control functions.

The various audio output frequencies are generated from an on-chip 3.58MHz quartz crystal-controlled oscillator.

The devices can interface directly to all standard microcontrollers by accepting a binary-coded parallel input or serial data input (I^2C bus).

With their on-chip voltage reference the PCD3311 and PCD3312 provide constant output amplitudes which are independent of the operating supply voltage and ambient temperature.

An on-chip filtering system assures a very low total harmonic distortion in accordance with the CEPT CS203 recommendations.

In addition to the standard DTMF frequencies, the devices provide 12 MODEM frequencies (300 to 1200 bits per second) used in simplex MODEM applications and two octaves of musical scale in steps of semitones.

FEATURES

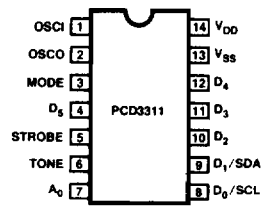
- **Stabilized output voltage level**
- **Low output distortion with on-chip filtering (CEPT CS203 compatible)**
- **Latched inputs for data bus applications**
- **I^2C bus compatible**
- **Mode select input (selection of parallel or serial data input)**
- **MODEM and melody tone generators**

APPLICATION

- **Microcontrolled telephone sets**

PIN CONFIGURATIONS

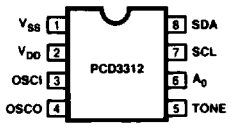
N Package



TOP VIEW

CD12720S

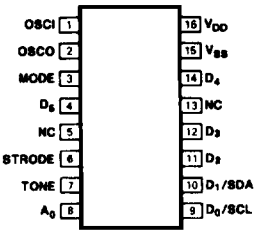
D, N Packages



TOP VIEW

CD12730S

D Package



CD15330S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP (SOT-27k, M, T)	−25°C to +70°C	PCD3311PN
16-Pin Plastic SO (SO-16L; SOT-162A)	−25°C to +70°C	PCD3311TD
8-Pin Plastic DIP (SOT-97A)	−25°C to +70°C	PCD3312PN
8-Pin Plastic SO (SO-8L; SOT-176)	−25°C to +70°C	PCD3312TD

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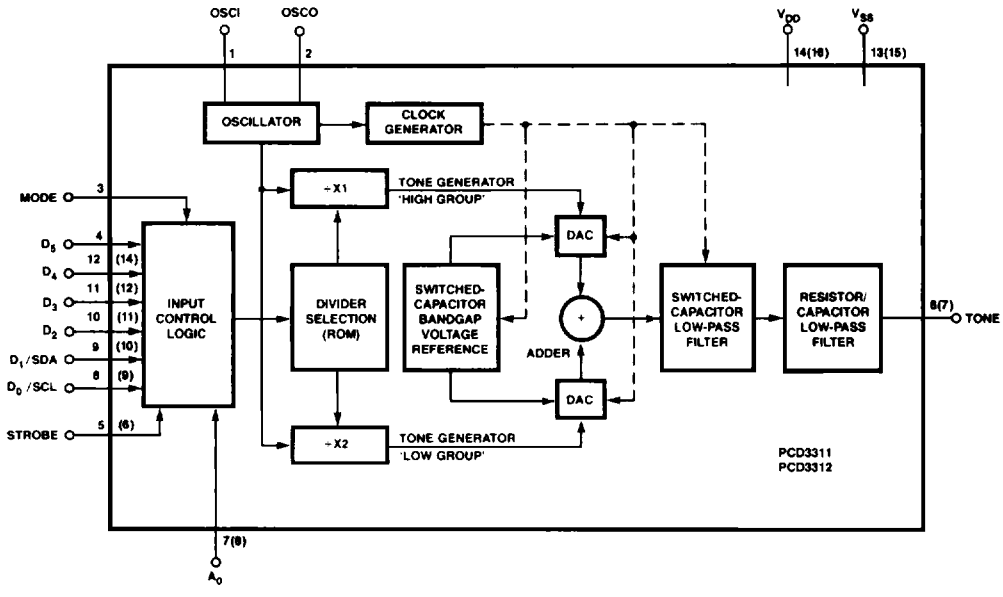
BLOCK DIAGRAM



NOTE:
The pin numbers in parentheses refer to the PCD3311TD; Pins 5 and 13 are NC.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{DD}	Supply voltage range	−0.8	+8.0	V
V_I	Input voltage range (any input)	−0.8	V_{DD} + 0.8	V
$\pm I_I$	DC input current (any input)		10	mA
$\pm I_O$	DC output current (any output)		10	mA
$\pm I_{DD}$; $\pm I_{SS}$	Supply current		50	mA
P_O	Power dissipation per output		50	mW
P_{TOT}	Total power dissipation per package		300	mW
T_A	Operating ambient temperature range	−25	+70	°C
T_{STG}	Storage temperature range	−65	+150	°C

DC AND AC ELECTRICAL CHARACTERISTICS V_{DD} = 2.5 to 6V; V_{SS} = 0V; crystal parameters: f_{OSC} = 3.579 545MHz, R_{SMAX} = 50Ω; T_A = −25°C to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{DD}	Operating supply voltage	2.5		6.0	V
	Operating supply current[1] oscillator ON; V_{DD} = 3V				
I_{DD}	no output tone		50	100	μA
I_{DD}	single output tone		0.5	1.0	mA
I_{DD}	dual output tone		0.6	1.2	mA
	Static standby current[1]				
I_{DDO}	oscillator OFF			3	μA
Inputs/outputs (SDA)					
	D_0 to D_5; MODE; STROBE				
V_{IL}	Input voltage LOW	0		$0.3 \times V_{DD}$	V
V_{IH}	Input voltage HIGH	$0.7 \times V_{DD}$		V_{DD}	V
	D_2 to D_5; MODE; STROBE; A_0				
$-I_{IL}$	Pull-down input current, $V_I = V_{DD}$	30	150	300	nA
	SCL (D_0); SDA (D_1)				
I_{OL}	Output current LOW (SDA), V_{OL} = 0.4V	3			mA
f_{SCL}	Clock frequency (see Figure 7)			100	kHz
C_I	Input capacitance; $V_I = V_{SS}$			7	pF
t_I	Allowable input spike pulse width			100	ns
TONE output (See Figure 11)					
	DTMF output voltage levels (RMS values)				
$V_{HG(RMS)}$	HIGH group	158	192	205	mV
$V_{LG(RMS)}$	LOW group	125	150	160	mV
V_{DC}	DC voltage level		½ V_{DD}		V
ΔV_G	Pre-emphasis of group	1.85	2.10	2.35	dB
	Total harmonic distortion, T_A = 25°C				
THD	dual tone[2]		−25		dB
THD	modem tone[3]		−29		dB
$\|Z_O\|$	Output impedance		0.1	0.5	kΩ
OSCI input					
$V_{OSC(P-P)}$	Maximum allowable amplitude at OSCI			$V_{DD} - V_{SS}$	V
Timing (V_{DD} = 3V)					
$t_{OSC(ON)}$	Oscillator start-up time		3		ms
$t_{TONE(ON)}$	TONE start-up time[4]		0.5		ms
t_{STR}	STROBE pulse width[5]	400			ns
t_{DS}	Data setup time[5]	150			ns
t_{DH}	Data hold time[5]	100			ns

NOTES:
1. Crystal is connected between OSCI and OSCO; D_0/SCL and D_1/SDA via a resistance of 5.6kΩ to V_{DD}; all other pins left open.
2. Related to the level of the LOW group frequency component (CEPT CS203).
3. Related to the level of the fundamental frequency.
4. Oscillator must be running.
5. Values are referenced to the 10% and 90% levels of the relevant pulse amplitudes, with a total voltage swing from V_{SS} to V_{DD}.

FUNCTIONAL DESCRIPTION

Clock/Oscillator (OSCI and OSCO)

The timebase for the PCD3311 and PCD3312 is a crystal-controlled oscillator with a 3.58MHz quartz crystal connected between OSCI and OSCO. Alternatively, the OSCI input can be driven from an external clock.

Mode Select (MODE)

This input selects the data input mode. When connected to V_{DD}, data can be received in the parallel mode (only for the PCD3311), or, when connected to V_{SS} or left open, data can be received via the serial I^2C bus (for both PCD3311 and PCD3312).

Parallel mode can only be obtained for the PCD3311 by setting MODE input HIGH.

Data Inputs (D_0, D_1, D_2, D_3, D_4 and D_5)

Inputs D_0 and D_1 have no internal pull-down or pull-up resistors and must not be left open in any application. Inputs D_2 to D_5 have internal pull-down. D_5 and D_4 are used to select between DTMF dual, DTMF single, MODEM and melody tones (see Table 1). D_3 to D_0 select the combination of the tones for DTMF or single-tone itself.

Strobe Input (STROBE, only for the PCD3311)

This input (with internal pull-down) allows the loading of parallel data into D_0 to D_5 when MODE is HIGH.

The data inputs must be stable preceding the positive-going edge of the strobe pulse (active HIGH). Input data are loaded at the negative-going edge of the strobe pulse and then the corresponding tone (or standby mode) is provided at the TONE output. The output remains unchanged until the negative-going edge of the next STROBE pulse (for new data) is received.

Serial mode can only be obtained for the PCD3311 by setting MODE input LOW.

Table 1. D_5 and D_4 in Accordance With the Selected Application

D_5	D_4	APPLICATION
0	0	DTMF single tones; standby; melody tones
0	1	DTMF dual tones (all 16 combinations)
1	0	MODEM tones; standby; melody tones
1	1	Melody tones

NOTES:
1 = H = HIGH voltage level
0 = L = LOW voltage level

Serial Clock and Data Inputs (SCL and SDA)

SCL and SDA are combined with D_0 and D_1, respectively. For the PCD3311, the selection of SCL and SDA is controlled by the MODE input. SCL and SDA are serial clock and data lines according to the I^2C bus specification (see CHARACTERISTICS OF THE I^2C BUS). Both inputs must be pulled-up externally to V_{DD}.

Address Input (A_0)

A_0 is the slave address input and it identifies the device when up to two PCD3311 or PCD3312 devices are connected to the same I^2C bus. In any case, A_0 must be connected to V_{DD} or V_{SS}.

I^2C Bus Data Configuration (see Figure 2)

The PCD3311 and PCD3312 are always slave receivers in the I^2C bus configuration (R/$\overline{W}$ bit = 0).

The slave address consists of 7 bits in the serial mode for the PCD3311 as well as for the PCD3312, where the least significant bit is selectable by hardware on input A_0 and the other more significant bits are internally fixed. In the serial mode the same input codes are used as in the parallel mode (see Tables 2, 3, 4, and 5). D_6 and D_7 are don't care (X) bits.

Tone Output (TONE)

The single and the dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an active RC low-pass filter. Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 3 shows the frequency tolerance of the output tones for DTMF signalling; Tables 4 and 5 for the modem and melody tones.

Power-On Reset

In order to avoid undefined states of the devices when the power is switched ON, an internal reset circuit sets them to the standby mode (oscillator OFF).

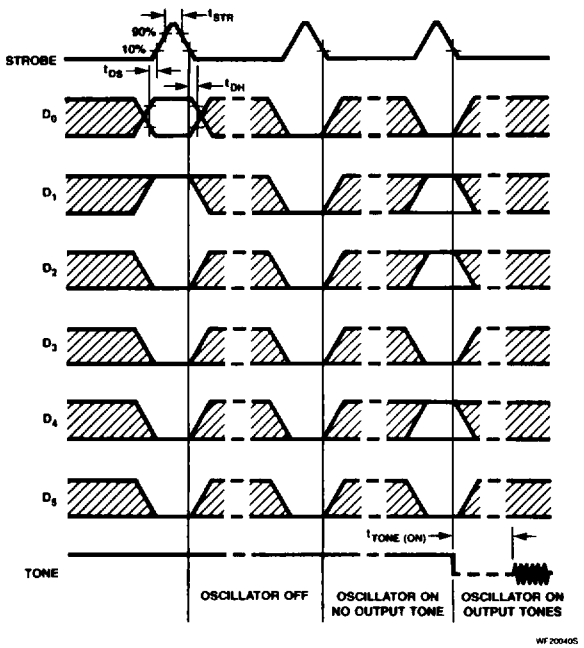


Figure 1. Timing Diagram Showing Control Possibilities of the Oscillator and the TONE Output (e.g., 770Hz + 1477Hz) in the Parallel Mode (MODE = HIGH)

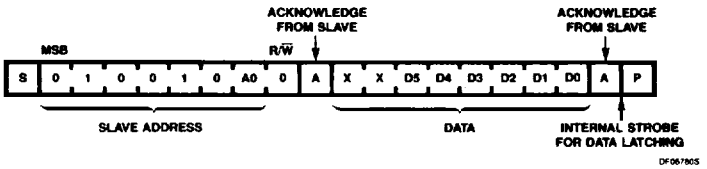


Figure 2. I^2C Bus Data Format

Table 2. Input Data for Control (No Output Tone; TONE at V_{DD})

D_5	D_4	D_3	D_2	D_1	D_0	HEX	OSCILLATOR
X	0	0	0	0	0	00/20	ON
X	0	0	0	0	1	01/21	OFF
X	0	0	0	1	0	02/22	OFF
X	0	0	0	1	1	03/23	OFF

NOTES:
1 = H = HIGH voltage level
0 = L = LOW voltage level
X = don't care

Table 3. Input Data for DTMF

D_5	D_4	D_3	D_2	D_1	D_0	HEX	SYMBOL	STANDARD FREQUENCY (Hz)	TONE OUTPUT FREQ. (Hz)[1]	FREQUENCY DEVIATION	
										%	Hz
0	0	1	0	0	0	08		697	697.90	+0.13	+0.90
0	0	1	0	0	1	09		770	770.46	+0.06	+0.46
0	0	1	0	1	0	0A		852	850.45	−0.18	−1.55
0	0	1	0	1	1	0B		941	943.23	+0.24	+2.23
0	0	1	1	0	0	0C		1209	1206.45	−0.21	−2.55
0	0	1	1	0	1	0D		1336	1341.66	+0.42	+5.66
0	0	1	1	1	0	0E		1477	1482.21	+0.35	+5.21
0	0	1	1	1	1	0F		1633	1638.24	+0.32	+5.24
0	1	0	0	0	0	10	0	941 + 1336			
0	1	0	0	0	1	11	1	697 + 1209			
0	1	0	0	1	0	12	2	697 + 1336			
0	1	0	0	1	1	13	3	697 + 1477			
0	1	0	1	0	0	14	4	770 + 1209			
0	1	0	1	0	1	15	5	770 + 1336			
0	1	0	1	1	0	16	6	770 + 1477			
0	1	0	1	1	1	17	7	852 + 1209			
0	1	1	0	0	0	18	8	852 + 1336			
0	1	1	0	0	1	19	9	852 + 1477			
0	1	1	0	1	0	1A	A	697 + 1633			
0	1	1	0	1	1	1B	B	770 + 1633			
0	1	1	1	0	0	1C	C	852 + 1633			
0	1	1	1	0	1	1D	D	941 + 1633			
0	1	1	1	1	0	1E	*	941 + 1209			
0	1	1	1	1	1	1F	#	941 + 1477			

Table 4. Input Data for MODEM Frequencies

D_5	D_4	D_3	D_2	D_1	D_0	HEX	STANDARD FREQUENCY (Hz)	TONE OUTPUT FREQ. (Hz)[1]	FREQUENCY DEVIATION		REMARKS
									%	Hz	
1	0	0	1	0	0	24	1300	1296.94	−0.24	−3.06	V.23
1	0	0	1	0	1	25	2100	2103.14	+0.15	+3.14	
1	0	0	1	1	0	26	1200	1197.17	−0.24	−2.83	Bell 202
1	0	0	1	1	1	27	2200	2192.01	−0.36	−7.99	
1	0	1	0	0	0	28	980	978.82	−0.12	−1.18	V.21
1	0	1	0	0	1	29	1180	1179.03	−0.08	−0.97	
1	0	1	0	1	0	2A	1070	1073.33	+0.31	+3.33	Bell 103
1	0	1	0	1	1	2B	1270	1265.30	−0.37	−4.70	
1	0	1	1	0	0	2C	1650	1655.66	+0.34	+5.66	V.21
1	0	1	1	0	1	2D	1850	1852.77	+0.15	+2.77	
1	0	1	1	1	0	2E	2025	2021.20	−0.19	−3.80	Bell 103
1	0	1	1	1	1	2F	2225	2223.32	−0.08	−1.68	

NOTES:
1. Tone output frequency when using a 3.579 545MHz crystal
1 = H = HIGH voltage level
0 = L = LOW voltage level

Table 5. Input Data for Melody Tones

D_5	D_4	D_3	D_2	D_1	D_0	HEX	NOTE	STANDARD FREQUENCY (Hz)[1]	TONE OUTPUT FREQUENCY (Hz)[2]
1	1	0	0	0	0	30	D#5	622.3	622.5
1	1	0	0	0	1	31	E5	659.3	659.5
1	1	0	0	1	0	32	F5	698.5	697.9
1	1	0	0	1	1	33	F#5	740.0	741.1
1	1	0	1	0	0	34	G5	784.0	782.1
1	1	0	1	0	1	35	G#5	830.6	832.3
1	1	0	1	1	0	36	A5	880.0	879.3
1	1	0	1	1	1	37	A#5	932.3	931.9
1	1	1	0	0	0	38	B5	987.8	985.0
1	1	1	0	0	1	39	C6	1046.5	1044.5
1	1	1	0	1	0	3A	C#6	1108.7	1111.7
1	0	1	0	0	1	29	D6	1174.7	1179.0
1	1	1	0	1	1	3B	D#6	1244.5	1245.1
1	1	1	1	0	0	3C	E6	1318.5	1318.9
1	1	1	1	0	1	3D	F6	1396.9	1402.1
0	0	1	1	1	0	0E	F#6	1480.0	1482.2
1	1	1	1	1	0	3E	G6	1568.0	1572.0
1	0	1	1	0	0	2C	G#6	1661.2	1655.7
1	1	1	1	1	1	3F	A6	1760.0	1768.5
0	0	0	1	0	0	04	A#6	1864.7	1875.1
0	0	0	1	0	1	05	B6	1975.5	1970.0
1	0	0	1	0	1	25	C7	2093.0	2103.1
1	0	1	1	1	1	2F	C#7	2217.5	2223.3
0	0	0	1	1	0	06	D7	2349.3	2358.1
0	0	0	1	1	1	07	D#7	2489.0	2470.4

NOTES:
1. Standard scale based on A4 = 440Hz.
2. Tone output frequency when using a 3.579 545MHz crystal.
   1 = H = HIGH voltage level
   0 = L = LOW voltage level

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CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time will be interpreted as control signals.

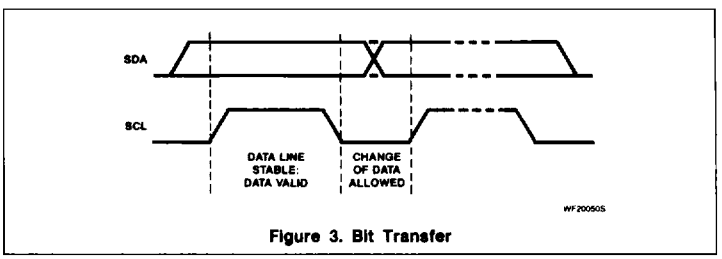


Figure 3. Bit Transfer

Start and Stop Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

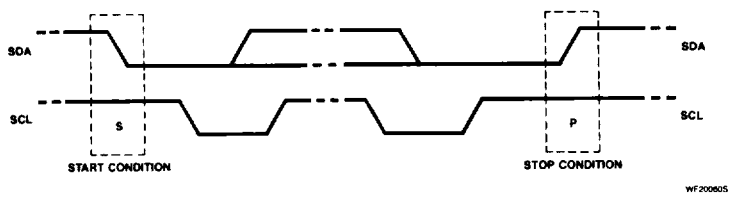


Figure 4. Definition of Start and Stop Conditions

System Configuration

A device generating a message is a "transmitter"; a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse; so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, setup and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate to stop condition.

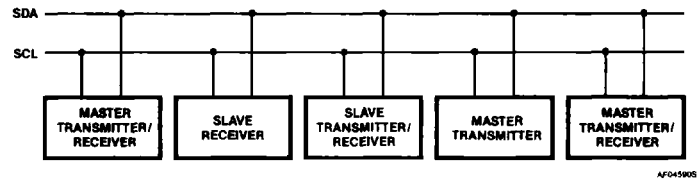


Figure 5. System Configuration

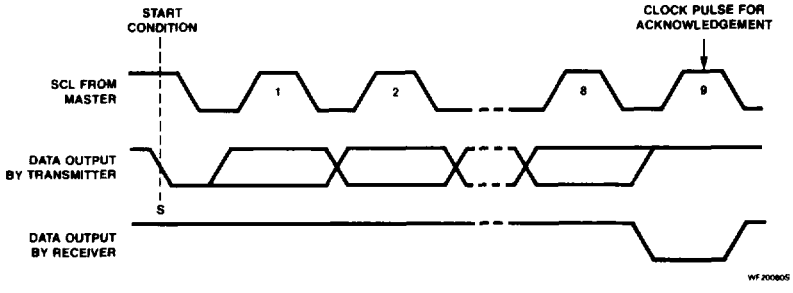
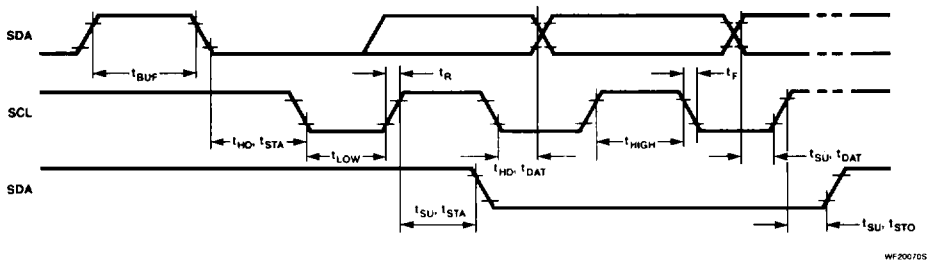


Figure 6. Acknowledgment on the I^2C Bus

Timing Specifications

Masters generate a bus clock with a maximum frequency of 100kHz. Detailed timing is shown in Figure 7.

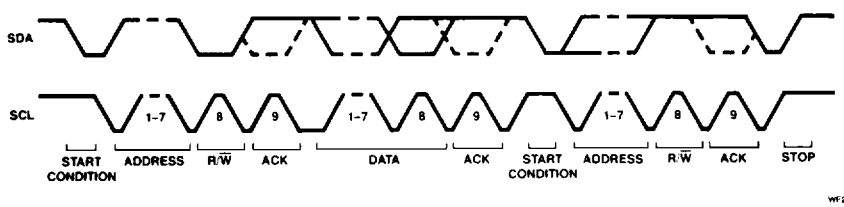


Where:

t_{BUF}	$t \geq t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
t_{HD}; t_{STA}	$t \geq t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4.7μs	Clock LOW period
$t_{HIGHmin}$	4μs	Clock HIGH period
t_{SU}; t_{STA}	$t \geq t_{LOWmin}$	Start condition setup time, only valid for repeated start code
t_{HD}; t_{DAT}	$t \geq 0\mu s$	Data hold time
t_{SU}; t_{DAT}	$t \geq 250ns$	Data setup time
t_R	$t \leq 1\mu s$	Rise time of both the SDA and SCL line
t_F	$t \leq 300ns$	Fall time of both the SDA and SCL line
t_{SU};t_{STO}	$t \geq t_{LOWmin}$	Stop condition setup time

NOTE:
All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

Figure 7. Timing



Where:

Clock t_{LOWmin}	4.7μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgment of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Maximum number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Figure 8. Complete Data Transfer

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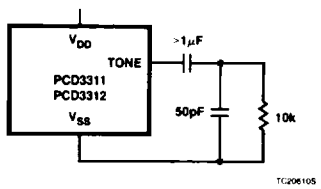

Figure 9. TONE Output Test Circuit

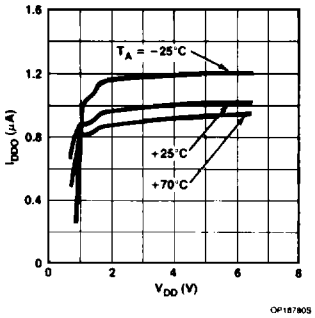

Figure 10. Standby Supply Current as a Function of Supply Voltage; Oscillator OFF

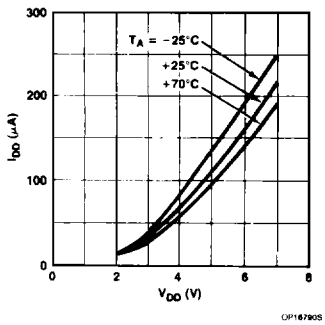

Figure 11. Operating Supply Current as a Function of Supply Voltage; Oscillator ON; No Output at TONE

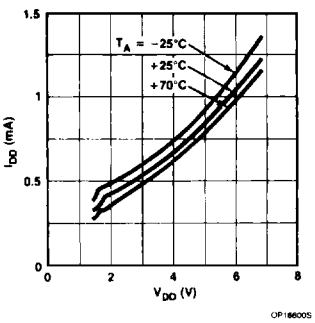

Figure 12. Operating Supply Current as a Function of Supply Voltage; Oscillator ON; Dual-Tone at TONE

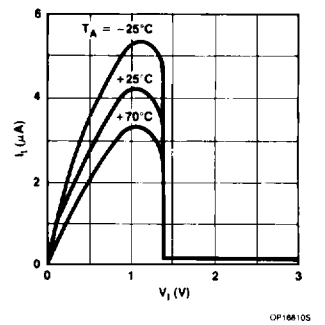

Figure 13. Pull-Down Input Current as a Function of Input Voltage; V_{DD} = 3V

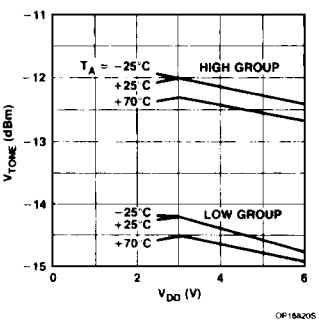

Figure 14. DTMF Output Voltage Levels as a Function of Operating Supply Voltage; R_L = 1MΩ

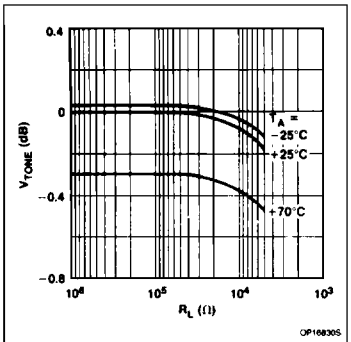

Figure 15. Dual-Tone Output Voltage Level as a Function of Output Load Resistance

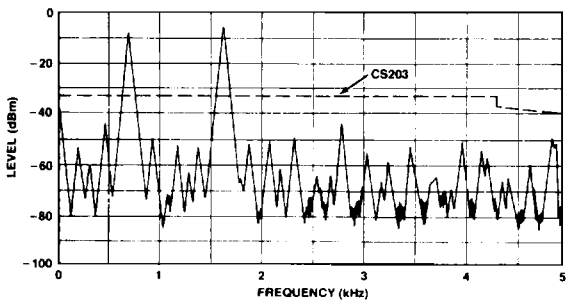

Figure 16. Typical Frequency Spectrum of a Dual-Tone Signal After Flat-Band Amplification of 6dB

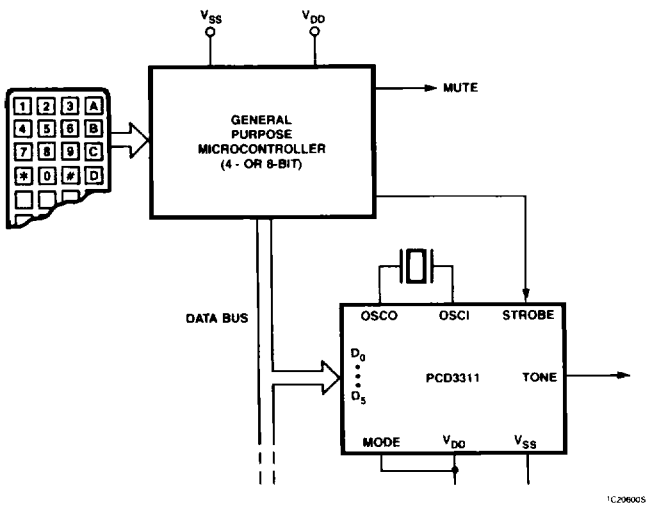

Figure 17. PCD3311 Driven by a Microcontroller with Parallel Data Bus

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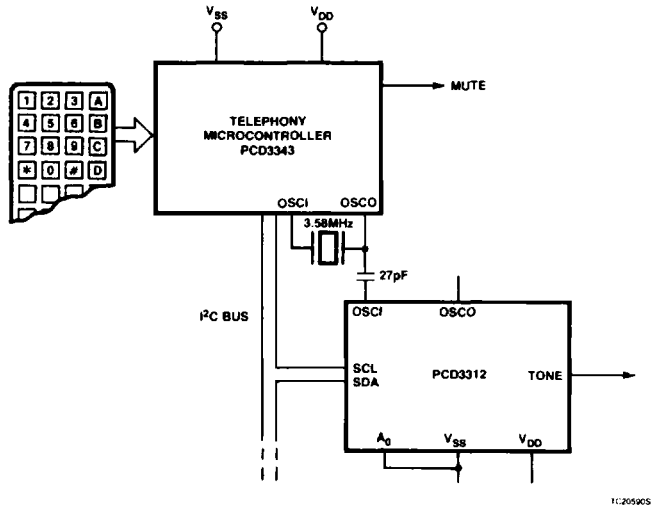

NOTE:
The PCD3343 is a single-chip 8-bit microcontroller with 3k ROM/224 RAM bytes.
The same application is possible with the PCD3311 with MODE = V_{SS}.

Figure 18. PCD3312 Driven by Telephony Microcontroller PCD3343 with Serial I/O (I^2C Bus)