

## Pulse dialler circuits with redial

## PCD332XC family

### GENERAL DESCRIPTION

The PCD332XC family comprises seven CMOS pulse dialler circuits with redial. Each circuit converts 3 x 4 matrix keyboard entries into correctly-timed line current interruptions. For redial, the last-dialled number (up to 23 digits) is stored in an on-chip RAM. A RAM overflow is handled by inhibiting the redial but manual dialling of more than 23 digits still can be made. The circuits include a delayed reset for line power breaks to ensure correct operation.

Most ICs of the family regenerate an access pause during redial. Insertion of the access pause during the original entry is either automatic or via the '\*' key. Termination of the regenerated access pause during redial is via the '#' key, after a built-in delay or controlled by an external tone recognizer. Other differences between the circuits are selections of pulse dialling frequency, mark/space ratio, regenerated access pause duration, mute, hold/access pause output control and oscillator frequency.

### Features

- Operating supply voltage range: 2.0 to 6.0 V
- Static supply voltage (with redial memory data retention): down to 1.5 V
- Low operating supply current: typ. 60  $\mu$ A
- Low static standby supply current: typ. 0.65  $\mu$ A
- On-chip RAM capacity: 23 keyboard entries (digits and access pauses)
- Redial inhibited after memory overflow
- Manual dialling can continue beyond 23 keyboard entries (excess entries are stored at lower RAM addresses)
- (Re)dialling procedure is not affected by line interruptions shorter than the reset delay time (if the supply voltage does not fall below the static standby voltage)
- Line interruptions longer than the reset delay time are regarded as on-hook situations
- Hold facility for lengthening the inter-digit period
- On-chip oscillator for 3.58 MHz crystal (type for ceramic resonator is also available)
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard
- Pull-up or pull-down circuits at all inputs except CE
- Electrostatic discharge protection at all inputs
- High input noise immunity
- Test mode in which the dialling frequency is increased.

### Note:

the PCD3320C, PCD3322C, PCD3324C and PCD3325C are not to be used for new design-ins

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The PCD332XC family of ICs comprises the following types:

- PCD3320C dialler with several mute signals
- PCD3321C dialler with two automatic access pauses
- PCD3322C variant of PCD3320C
- PCD3324C dialler with one automatic access pause
- PCD3325C dialler with manual access pause control
- PCD3326C variant of PCD3321C
- PCD3327C variant of PCD3325C for ceramic resonator with automatic reset of access pause

functional survey	PCD . . .						
	3320C	3321C	3322C	3324C	3325C	3326C	3327C
Number of pins	18	18	18	18	18	18	18
Dialling frequency 10 Hz selectable with F01, F02 16, 20 Hz	●	●	●	●	●	●	●
Mark/space ratio 3 : 2 selectable with M/S 2 : 1	●	●	●	●	●	●	●
Access pauses repeated during redial		●		●	●	●	●
Manual insertion of access pauses		●		●	●	●	●
Automatic access pause insertion 1 max 2 max				●		●	
Access pause duration 32 x T <sub>DP</sub> selectable with APD 64 x T <sub>DP</sub> not automatically terminated		●		●		●	●
M1, inverted mute output	●		●				
M2, strobe output			●				
M3, AND function of mute (M1) and inverted dialling pulse (DP) outputs	●						
HOLD, dialling-interrupt input	●		●				
APO + HOLD, internally connected		●		●	●	●	●

T<sub>DP</sub> = dialling pulse period

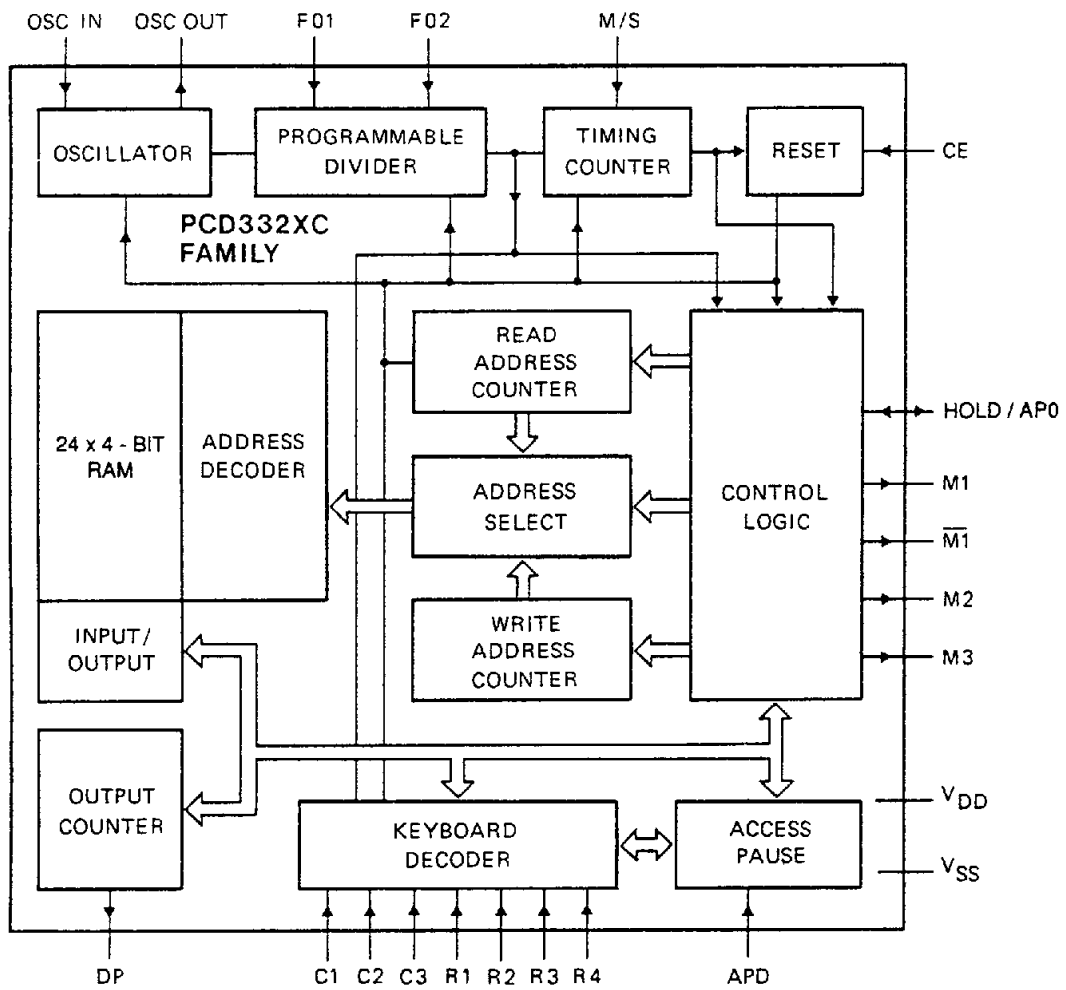
\* PCD3327C for ceramic resonator

Features common to all PCD332XC family

- OSC IN } on-chip oscillator input and
- OSC OUT } output
- C1 to C3, column keyboard inputs with on-chip pull-up
- R1 to R4, row keyboard outputs with on-chip pull-down
- CE, chip enable input
- DP, dialling pulse output to external line-switching transistor or relay
- M1, mute output

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Fig.1 Block diagram.

PACKAGE OUTLINES

- PCD3320CP
  - PCD3321CP
  - PCD3322CP
  - PCD3324CP
  - PCD3325CP
  - PCD3326CP
  - PCD3327CP
  - PCD3320CD
  - PCD3321CD
  - PCD3321CT
  - PCD3322CT
  - PCD3327CT
  - PCD3327U: uncased chip in tray.
- 18-lead DIL; plastic (SOT102G).
- 18-lead DIL; ceramic (SOT133B).
- 20-lead mini-pack; plastic (SOT163A).

## Pulse dialler circuits with redial

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## PINNING

pin	purpose	PCD ...						
		3320C	3321C	3322C	3324C	3325C	3326C	3327C
<b>Supplies</b>								
VDD	positive supply	•	•	•	•	•	•	•
VSS	negative supply	•	•	•	•	•	•	•
<b>Inputs</b>								
M/S	controls mark/space ratio of the line pulses		•		•	•		•
F01	define the dialling pulse frequency	•	•	•	•	•	•	•
F02			•		•	•	•	
CE	Chip enable: used to initialize the system, to select between operating and static standby mode and to handle line power breaks	•	•	•	•	•	•	•
C1	keyboard column inputs with on-chip pull-up	•	•	•	•	•	•	•
C2								
C3								
ADP	Access Pause Duration: selects the maximum duration of an access pause if no external APR appears						•	
R1	keyboard row outputs with on-chip pull-down	•	•	•	•	•	•	•
R2								
R3								
R4								
HOLD	interrupts dialling after completion of the current digit or immediately during an inter-digit pause	•		•				
<b>Outputs</b>								
DP	Dialling Pulse: drive of the external switching transistor or relay	•	•	•	•	•	•	•
M1	Muting: normally used for muting during the dialling sequence	•	•	•	•	•	•	•

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pin	purpose	PCD . . .						
		3320C	3321C	3322C	3324C	3325C	3326C	3327C
M2	strobe; HIGH during pulsing of each digit, LOW during an inter-digit pause			•				
M3	AND-function with $\overline{DP}$ and M1 as inputs; for direct drive of a switching transistor for dialling pulses and muting	•						
<b>Oscil- lator</b>								
OSC IN	input and output of the on-chip oscillator	•	•	•	•	•	•	•
OSC OUT		•	•	•	•	•	•	•
<b>Input/ outputs</b>								
HOLD/ APO	The HOLD and APO features are connected together at this pin, normally an output pin but can be forced as an input		•		•	•	•	•

Pulse dialler circuits with redial

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PINNING (continued)

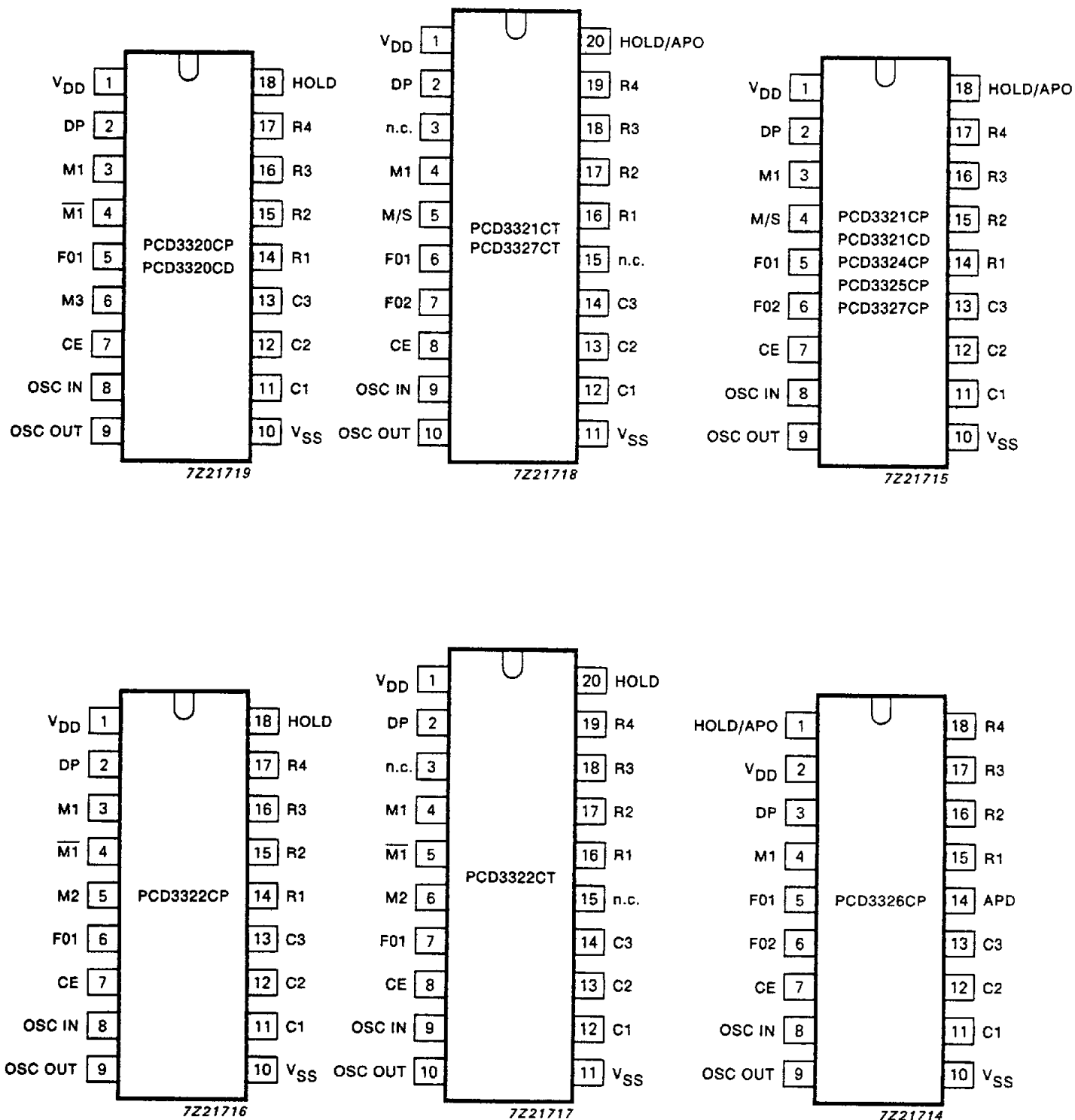


Fig.2 Pinning diagrams.

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**Pulse dialler circuits with redial****PCD332XC family**

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**FUNCTIONAL DESCRIPTION****Clock oscillator (OSC IN, OSC OUT)**

The time base for the circuit is a crystal-controlled on-chip oscillator which is completed by the connection of a crystal between the OSC IN and OSC OUT pins (a ceramic resonator may be used with the PCD3327C). Alternatively, the OSC IN pin can be driven by an external clock signal.

**Clock divider (F01, F02)**

The oscillator is followed by a frequency divider, the division ratio of which can be set externally (F01, F02) to provide one of four chip system clocks, i.e. three 'normal' clock frequencies and one higher frequency for testing.

Other frequencies can also be obtained by driving OSC IN, as previously stated.

**Chip enable (CE)**

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped at reset, excepting the WRITE ADDRESS COUNTER (WAC). The keyboard input is prohibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time  $t_{rD}$  (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the  $t_{rD}$  period. The system is then in the static standby mode. Short CE pulses of  $< t_{rD}$  will not affect the operation of the circuit and reset pulses are not produced.

**Debouncing keyboard entries (C1 to C3; R1 to R4)**

The column keyboard inputs to the integrated circuits ( $C_n$ ) and the row keyboard outputs ( $R_n$ ) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig.3, or to a double contact keyboard with a common left open contact (see Fig.4).

An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input. Any other input combinations are not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig.5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for five or six clock pulse periods (entry period  $t_e$ ). The next keyboard entry will not be accepted until the previously closed contact has been left open for four or five clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the leading edge of the first clock pulse after the entry.

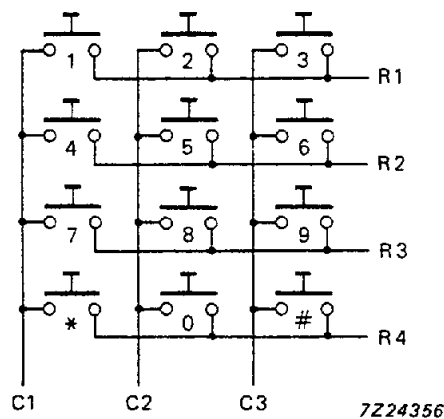
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## Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 codes are written into the RAM, memory overflow results and the access keycodes replace the data in the lower-numbered locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time  $t_e$ , the corresponding keycode is written into the first RAM location and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly-timed dialling pulses at output DP. If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset (see 'Access Pause System'). During redial, no keyboard entry will be accepted and stored in the RAM. But, when all numbers stored in the RAM have been pulsed out, new keyboard entries will be accepted and stored in the RAM position after the last digit code of the original entry and converted into correctly-timed dialling pulses.



- \* Access pause set.
- # Redial or access pause reset.

Fig.3 Single contact keyboard.

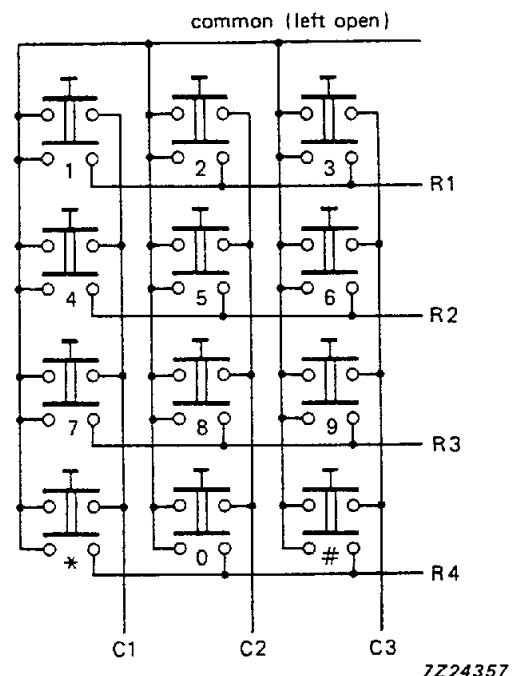
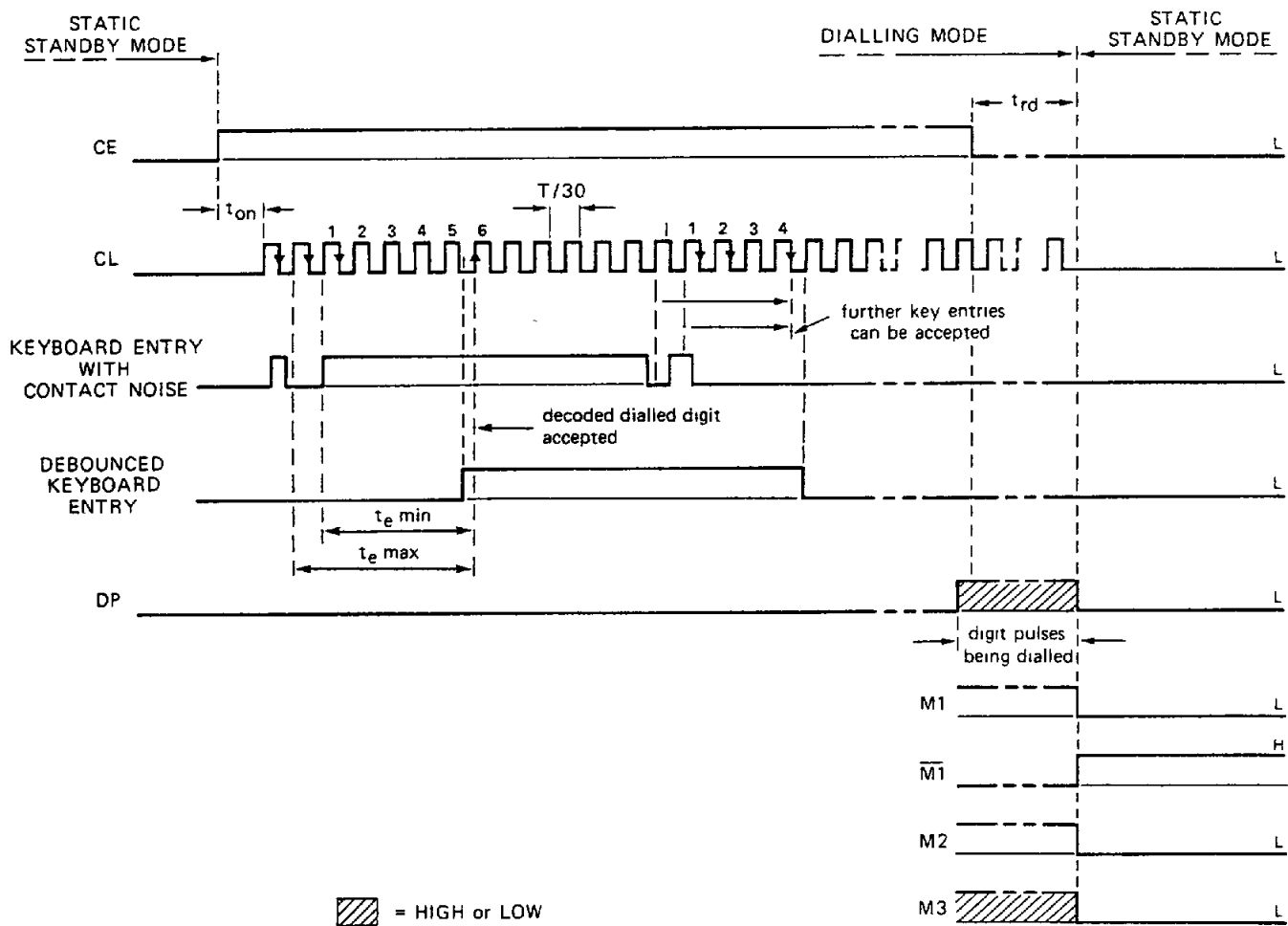


Fig.4 Double contact keyboard.



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Fig.5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

**Dialling sequence**

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig.6.

Then, approximately 4 ms ( $t_{on}$ ) after CE goes HIGH, the clock pulse generator starts and ten clock pulse periods later a prepulse with a duration of ten clock pulse periods ( $t_d$ ) appears at outputs M1 and M3. This prepulse ensures that if a polarized muting relay with two stable positions is used it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period  $t_e$  commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (see Fig.7).

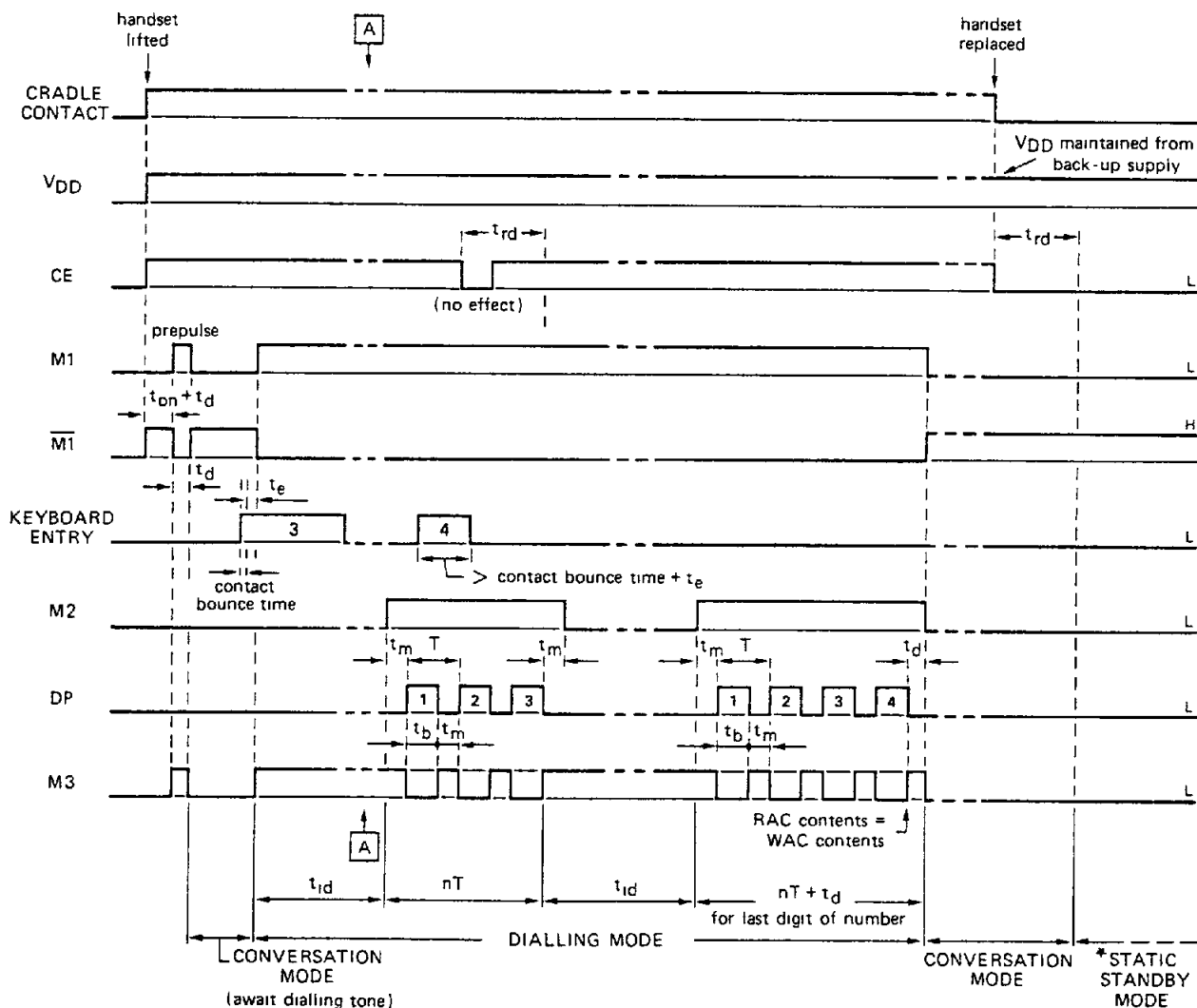
When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to  $V_{DD}$  and CE becomes HIGH. Approximately 4 ms ( $t_{on}$ ) after CE goes high, the clock pulse generator starts and data entry period  $t_e$  commences. After period  $t_e$ , M1 goes HIGH and the pushbutton can be released. The supply to  $V_{DD}$  and CE is then maintained via the

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## Dialling sequence (continued)

Referring to Fig.6, when the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause ( $t_{id}$ ) ensues. M2 then goes HIGH, the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at outputs DP and M3. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time ( $t_{rd} = 1.6$  dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although  $V_{DD}$  is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to  $V_{DD}$ ). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains  $V_{DD}$  above the level  $V_{DD0} = 1.5$  V, which is detected by the power-on reset circuit.



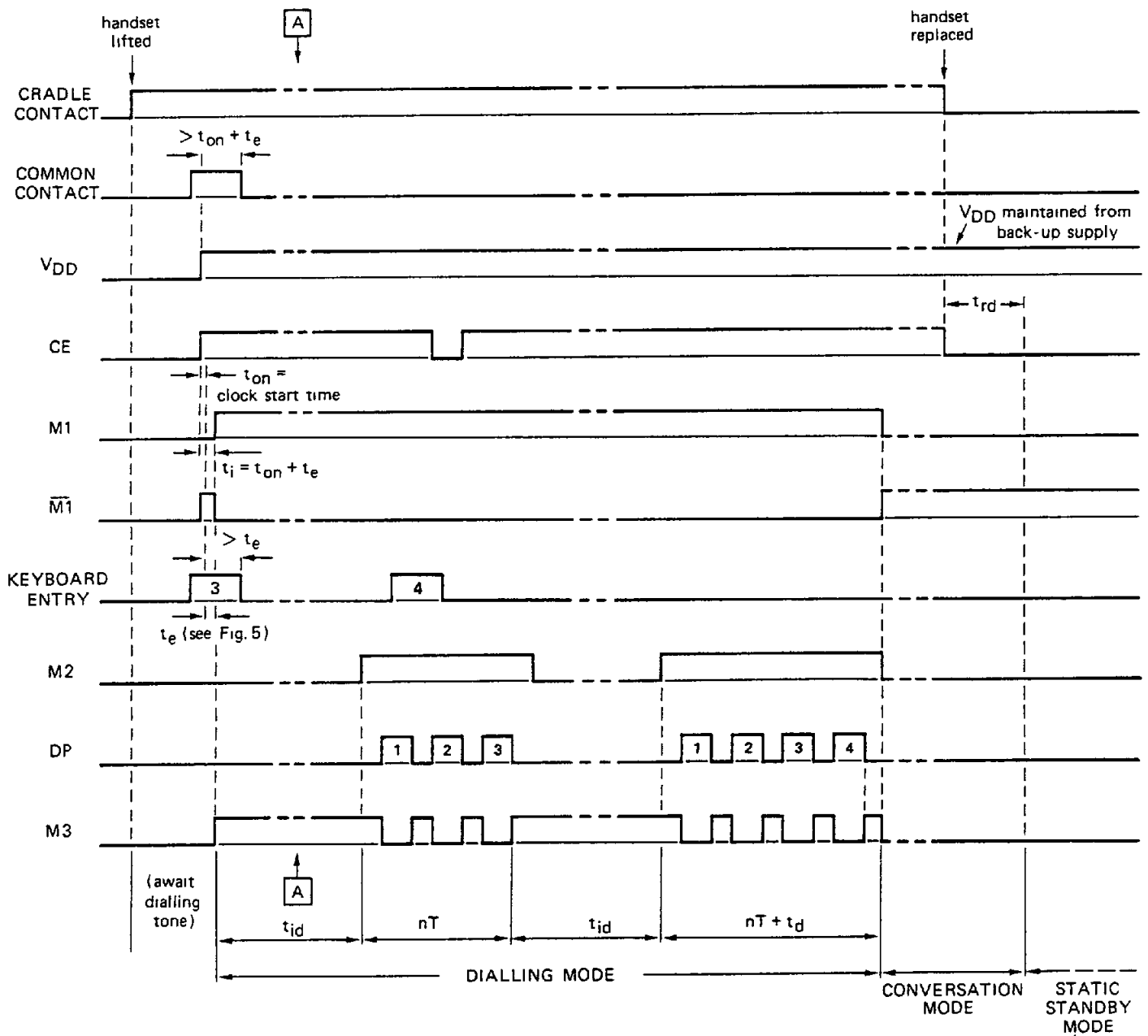
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\* Oscillator off; all registers reset; keyboard input inhibited; number stored in RAM until  $V_{DD} < 1.5$  V.

Fig 6. Timing diagram of dialling sequence with  $V_{DD}$  and CE HIGH before keyboard entry (a) supply

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Fig.7 Timing diagram for initiating the dialling mode with  $V_{DD}$  and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig.6 for pulse timings after point A.

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**Hold function (HOLD)**

As shown in Fig.8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD input is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM to be converted into dialling pulses on M3 and DP until the HOLD input is set LOW again and an inter-digit pause has elapsed.

HOLD can be controlled by the Access Pause Output (see section "Access pause system").

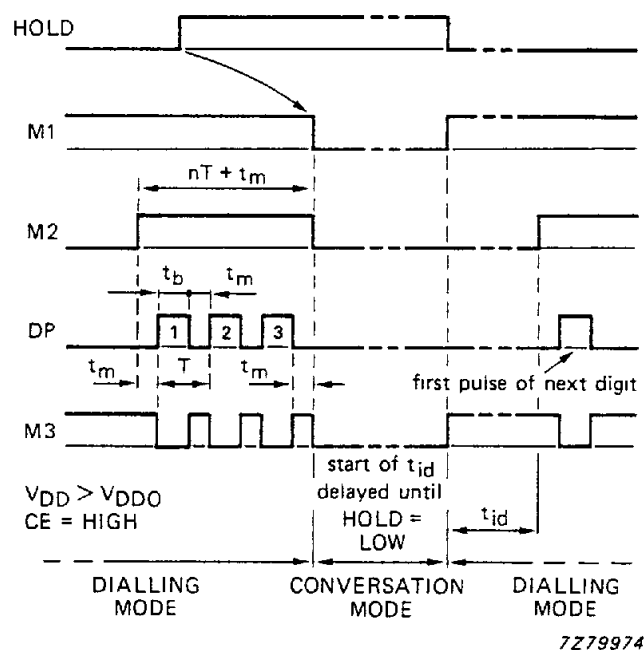


Fig.8 Timing diagram showing the effect of activating the HOLD input during the transmission of dialling pulses.

**Access pause system (HOLD/APO)**

The PCD3320C and PCD3322C only have the HOLD input and therefore these devices cannot reproduce the access pauses during redial (the access pause system is disabled). In all the other devices the HOLD input is internally connected to the APO output. This pin (HOLD/APO) can be used as an output, or forced as an input (e.g. by an external tone recognizer). Access pauses can be stored at appropriate positions in the RAM during the original entry of a number. As soon as the access pause code is read from the RAM, the access pause output (HOLD/APO) goes HIGH and dialling is interrupted.

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## Storing access pauses during dialling

Access pauses can be stored by one or both of the following ways:

- Manually by pressing the access pause key (\*). The number of access pauses that can be stored in this way is limited only by the capacity of the RAM (digits + access pauses  $\leq 23$ ).
- In some ICs of the family an access pause is stored automatically in the RAM (see Fig.9) during the original entry after all the digits so far entered have been transmitted (when M1 goes LOW, see Fig.6). The maximum number of access pause codes that can be entered in this manner is either one or two, depending on the type of IC.

Note: that when access pauses are manually inserted into ICs with automatic insertion of access pauses, the circuit automatically adds an access pause code after the number. This increases the RAM digit-count by one and reduces the maximum number of digits to 22 (including actual access pauses). The same would happen if the maximum number of access pauses for automatic entry is not reached before the end of the number.

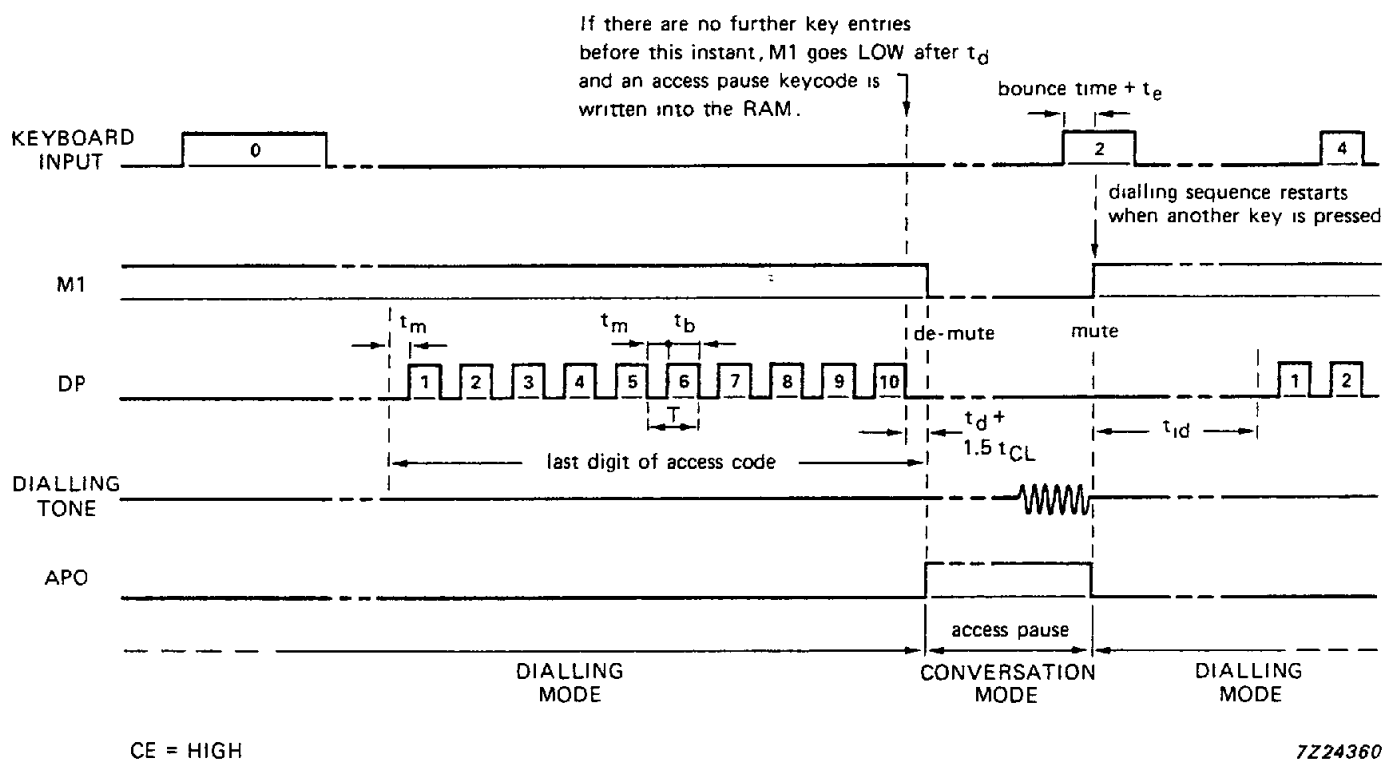


Fig.9 Dialling sequence showing how an access pause code is automatically stored in the RAM for possible redialling if no further key entries are made until all of the previously entered digits have been transmitted. The dialling sequence continues when another key is pressed.

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Terminating access pauses during redial (APD)

If APO is connected to HOLD, there are three ways of terminating access pauses during redial (see Fig.10):

- Manually by pressing the redial key before  $t_{ap}$  expires.
- Automatically if the built-in time  $t_{ap}$  expires; APO, and also HOLD, then go LOW so that the next digit will be dialled. With the Access Pause Delay (APD) select input,  $t_{ap}$  can be set to one of two values. With ICs that do not terminate access pauses in this way,  $t_{ap}$  is virtually infinity.
- By forcing HOLD/APO LOW (e.g. with an external tone recognizer).

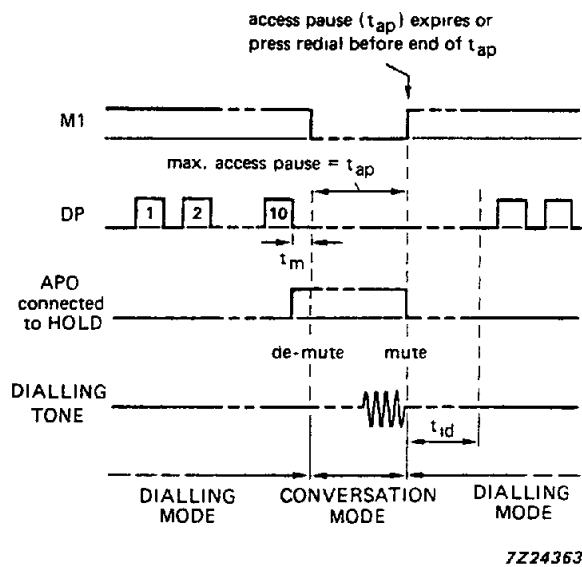
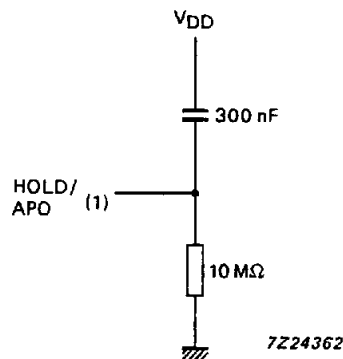


Fig.10 Timing diagram showing access pause reset.

For types with automatic reset of the access pause it is possible to lengthen the access pulse duration with external components (see Fig.11).



(1)  $\Delta t_{ap} \approx 2 \text{ s.}$

Fig. 11 External circuit required to lengthen the access pulse duration for ICs with automatic reset of the access pause

## Pulse dialler circuits with redial

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## FAMILY RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		$V_{DD}$	-0.5	8.0	V
Voltage on any pin		$V_I$	$V_{SS}-0.3$	$V_{DD}+0.3$	V
Operating ambient temperature range		$T_{amb}$	-25	+70	°C
Storage temperature range		$T_{stg}$	-55	+125	°C

## FAMILY CHARACTERISTICS

 $V_{DD} = 3\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ; crystal parameters  $f_{osc} = 3.58\text{ MHz}$  and  $R_{Smax} = 100\ \Omega$  (note 3); $T_{amb} = 25\text{ °C}$ ; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage	$T_{amb} = -25\text{ to }+70\text{ °C}$	$V_{DD}$	2.0	3.0	6.0	V
Standby supply voltage (note 1)	$T_{amb} = -25\text{ to }+70\text{ °C}$	$V_{DDO}$	1.5	—	6.0	V
Operating supply current	$CE = V_{DD}$ ; notes 2 and 3	$I_{DD}$	—	60	120	$\mu\text{A}$
	$V_{DD} = 6\text{ V}$ ; $CE = V_{DD}$ ; notes 2 and 3	$I_{DD}$	—	200	400	$\mu\text{A}$
Standby supply current	$CE = V_{SS}$ ; note 2	$I_{DDO}$	—	0.65	2.0	$\mu\text{A}$
	$V_{DD} = 1.8\text{ V}$ ; $T_{amb} = -25\text{ to }+70\text{ °C}$	$I_{DDO}$	—	—	2	$\mu\text{A}$
Input voltage LOW	$1.8\text{ V} \leq V_{DD} \leq 6\text{ V}$	$V_{IL}$	—	—	$0.3 \times V_{DD}$	V
Input voltage HIGH	$1.8\text{ V} \leq V_{DD} \leq 6\text{ V}$	$V_{IH}$	$0.7 \times V_{DD}$	—	—	V
CE input leakage current LOW	$CE = V_{SS}$	$-I_{IL}$	—	—	50	nA
HIGH	$CE = V_{DD}$	$I_{IH}$	—	—	50	nA
M/S pull-up input current	$V_I = V_{SS}$	$-I_{IL}$	30	100	300	nA
F01, F02, HOLD/APO APD pull-down input current	$V_I = V_{DD}$	$I_{IH}$	30	100	300	nA
<b>Matrix keyboard operation</b>						
Keyboard current	$C_n$ connected to $R_n$ ; $CE = \text{HIGH}$	$I_K$	—	30	—	$\mu\text{A}$
Keyboard 'ON' resistance	contact 'ON'; note 4	$R_{KON}$	—	—	2	k $\Omega$
Keyboard 'OFF' resistance	contact 'OFF';					

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## FAMILY CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
<b>Matrix keyboard operation (continued)</b>						
Outputs R <sub>1</sub> to R <sub>4</sub> sink current		$I_O$	–	3	–	mA
source current		$-I_O$	–	40	–	$\mu$ A
Outputs M1, $\overline{M1}$ , M2, M3, DP sink current	$V_{OL} = 0.5$ V	$I_{OL}$	0.7	2.0	4.0	mA
source current	$V_{OH} = 2.5$ V	$-I_{OH}$	0.65	1.8	3.6	mA
Outputs HOLD/APO source current	$V_{OH} = 2.5$ V	$-I_{OH}$	0.7	2.0	4.0	mA

## Notes to family characteristics

1.  $V_{DDO} = 1.5$  V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between OSC IN and OSC OUT pins < 3 pF.
4. Guarantees correct keyboard operation.

## FAMILY TIMING DATA

$V_{DD} = 3$  V;  $V_{SS} = 0$  V;  $f_{osc} = 3.58$  MHz

parameter	conditions	symbol	min.	typ.	max.	unit
Clock start-up time	CE: from $V_{SS}$ to $V_{DD}$ note 1	$t_{on}$	–	4	–	ms

## Note to family timing data

1. Stray capacitance between OSC IN and OSC OUT < 3 pF.



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FAMILY CURVES

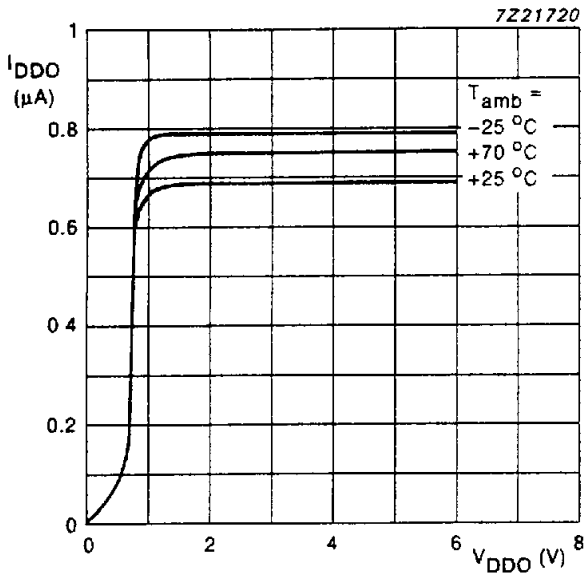


Fig.12 Standby supply current as a function of standby supply voltage.

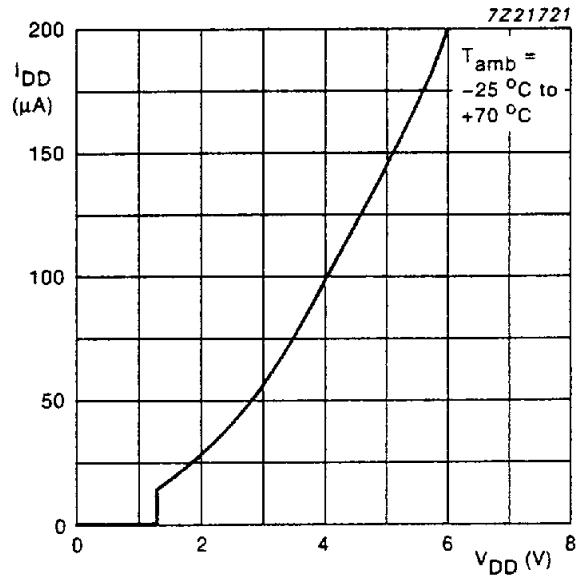


Fig.13 Operating supply as a function of operating supply voltage.

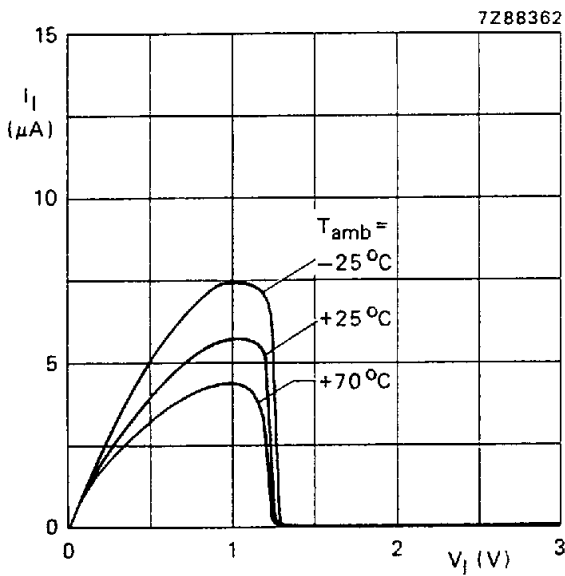


Fig.14 Pull-down input current as a function of input voltage;  $V_{DD} = 3 V$ .

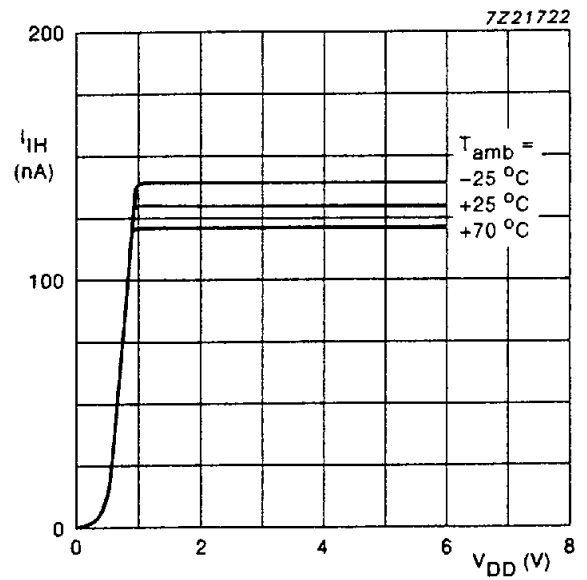


Fig.15 Pull-down input current as a function of supply voltage,  $V_I = V_{DD}$ .

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## FAMILY CURVES (continued)

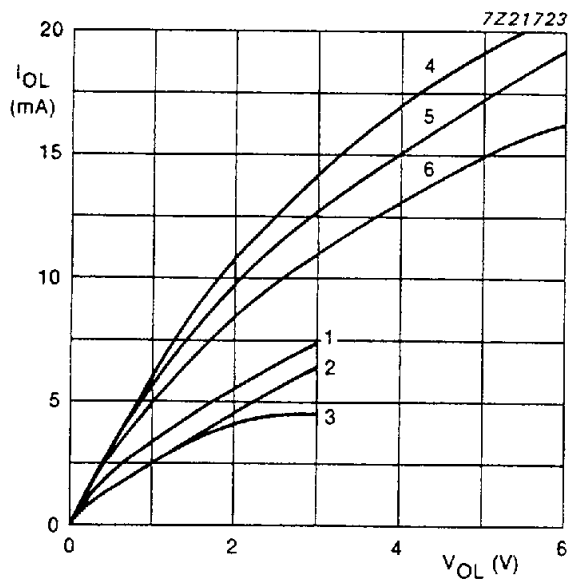


Fig. 16 Output (N-channel) sink characteristics for M1, M1, M2, M3 and DP.

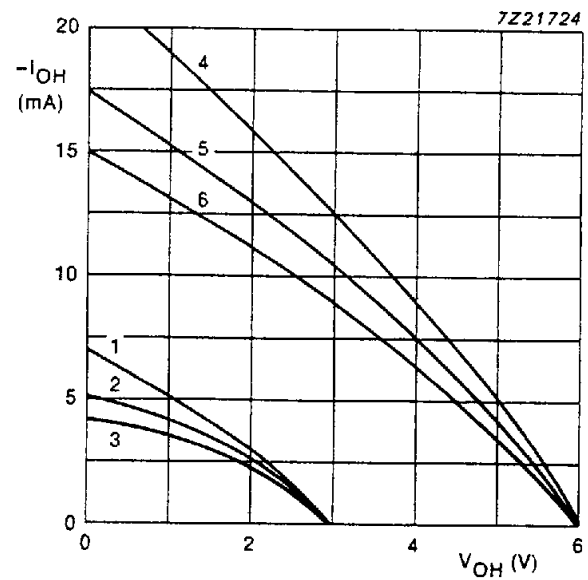


Fig. 17 Output (P-channel) source characteristics for M1, M1, M2, M3 and DP.

## Key to Figs 16 and 17

$T_{amb}$	$V_{DD} = 3\text{ V}$	$V_{DD} = 6\text{ V}$
$-25\text{ }^{\circ}\text{C}$	curve 1	curve 4
$+25\text{ }^{\circ}\text{C}$	curve 2	curve 5
$+70\text{ }^{\circ}\text{C}$	curve 3	curve 6

## Pulse dialler circuits with redial

## PCD332XC family

## CHARACTERISTICS PER TYPE

## PCD3320C specification

Inputs that are not available are defined internally as follows:

F02 = APD = LOW and M/S = HIGH

Outputs not available are M2 and APO.

Features additional to the common family specification are:

$\overline{M1}$	inverted mute output
M3	AND-function of mute (M1) and inverted dialling pulse (DP) outputs
HOLD	input that interrupts dialling

Redial of the last entered number is possible up to 23 digits; access pauses are not generated. Mark/space ratio is 3:2.

Using the F01 input it is possible to select either normal mode (F01 = LOW) or test mode (F01 = HIGH). In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.

## PCD3320C timing data

$V_{DD} = 2.0$  to  $6$  V;  $V_{SS} = 0$  V;  $f_{osc} = 3.58$  MHz

parameter	conditions	symbol	F01 = LOW (dialling)	unit
Dialling pulse frequency	note 1	$f_{DP}$	10.13	Hz
Dialling pulse period; $1/f_{DP}$	see Fig. 6 and 7	$T_{DP}$	98.7	ms
Clock pulse frequency; $30 \times f_{DP}$		$f_{CLK}$	303.9	Hz
Break time; $3/5 \times T_{DP}$	see Fig. 6	$t_b$	59.2	ms
Make time; $2/5 \times T_{DP}$	see Fig. 6	$t_m$	39.5	ms
Inter-digit pause; $8 \times T_{DP}$	see Figs 6 and 7	$t_{id}$	790	ms
Reset delay time; $1.6 \times T_{DP}$	see Figs 5, 6 and 7	$t_{rd}$	158	ms
Prepulse duration; $1/3 \times T_{DP}$	see Figs 6 and 7	$t_d$	33	ms
Debounce time; min. $5/30 \times T_{DP}$	see Fig. 5	$t_{e \text{ min}}$	16.45	ms
max. $6/30 \times T_{DP}$	see Fig. 5	$t_{e \text{ max}}$	19.74	ms
Initial data entry time (typ.); $t_{on} + t_e$		$t_i$	22	ms

## Note to the PCD3320C timing data

[www.DataSheet4U.com](http://www.DataSheet4U.com)

## Pulse dialler circuits with redial

## PCD332XC family

## CHARACTERISTICS PER TYPE (continued)

## PCD3321C specification

The PCD3321C is pin-compatible with the DF320 and MT4320 types. It includes additional features that make it ideal for Private Automatic Branch Exchange (PABX) systems. Two access pauses can be stored automatically during the original entry of a number, or several made via the keyboard. The circuit regenerates access pauses during redial. A regenerated access pause can be terminated during redial either automatically after a built-in delay, via the keyboard or with an external dial tone recognizer.

Inputs that are not available are defined internally as follows:

APD = LOW

Outputs not available are  $\overline{M1}$ , M2 and M3.

Features additional to the common family specification are:

F01 + F02 inputs giving selection between one of the three dialling speeds or the test speed. In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.

HOLD/APO input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected)

M/S input for M/S ratio selection to 3:2 or 2:1

## PCD3321C timing data

$V_{DD} = 2.0$  to  $6$  V;  $V_{SS} = 0$  V;  $f_{osc} = 3.579545$  MHz

parameter	conditions	symbol	FO1:	LOW	HIGH	LOW	unit
			FO2:	LOW	HIGH	HIGH	
Dialling pulse frequency; $1/T_{DP}$	note 1	$f_{DP}$		10.13	15.54	19.42	Hz
Dialling pulse period; $1/f_{DP}$		$T_{DP}$		98.7	64.4	51.5	ms
Clock pulse frequency; $30 \times f_{DP}$		$f_{CL}$		303.9	466.1	582.6	Hz
Break time; $3/5 \times T_{DP}$	M/S = HIGH or n.c.; notes 2 and 3	$t_b$		59.2	38.6	30.9	ms
Make time; $2/5 \times T_{DP}$	M/S = HIGH or n.c.; notes 2 and 3	$t_m$		39.5	25.8	20.6	ms
Break time; $2/3 \times T_{DP}$	M/S = LOW note 4	$t_b$		65.8	42.9	34.3	ms
Make time; $1/3 \times T_{DP}$	M/S = LOW note 4	$t_m$		32.9	21.5	17.2	ms
Inter-digit pause; $8 \times T_{DP}$		$t_{id}$		790	515	412	ms
Reset delay time; $1.6 \times T_{DP}$		$t_{rd}$		158	103	82.4	ms
Access pause time;							

## Pulse dialler circuits with radial

## PCD332XC family

parameter	conditions	symbol	FO1:	LOW	HIGH	LOW	unit
			FO2:	LOW	HIGH	HIGH	
Prepulse duration; $1/3 \times T_{DP}$		$t_d$		33.0	21.5	17.2	ms
Debounce time; min. $5/30 \times T_{DP}$ max. $6/30 \times T_{DP}$		$t_e$ min		16.45	10.70	8.58	ms
		$t_e$ max		19.74	12.88	10.30	ms
Initial data time (typ.); $t_{on} + t_e$		$t_i$		22.0	16.0	13.5	ms

## Notes to the PCD3321C timing data

- $f_{DP}$  is 10 Hz when a 3.5328 MHz crystal is used.
- In the n.c. (not connected) condition, the input is drawn to the HIGH state by internal pull-up current.
- Mark/space ratio = 3:2.
- Mark/space ratio = 2:1.

## Pulse dialler circuits with redial

## PCD332XC family

## CHARACTERISTICS PER TYPE (continued)

## PCD3322C specification

Inputs that are not available are defined internally as follows:

F02 = APD = LOW and M/S = HIGH

Outputs not available are M3 and APO.

Features additional to the common family specification are:

$\overline{M1}$  inverted mute output

M2 strobe; HIGH during pulsing of a digit, LOW during an inter-digit pause

HOLD input that interrupts dialling

Redial of the last entered number is possible up to 23 digits; access pauses are not generated. Mark/space ratio is 3:2.

Using the F01 input it is possible to select either normal mode (F01 = LOW) or test mode (F01 = HIGH). In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.

## PCD3322C timing data

$V_{DD} = 2.0$  to  $6$  V;  $V_{SS} = 0$  V;  $f_{osc} = 3.58$  MHz

parameter	conditions	symbol	F01 = LOW (dialling)	unit
Dialling pulse frequency	note 1	$f_{DP}$	10.13	Hz
Dialling pulse period; $1/f_{DP}$	see Figs 6 and 7	$T_{DP}$	98.7	ms
Clock pulse frequency; $30 \times f_{DP}$		$f_{CLK}$	303.9	Hz
Break time; $3/5 \times T_{DP}$	see Fig.6	$t_b$	59.2	ms
Make time; $2/5 \times T_{DP}$	see Fig. 6	$t_m$	39.5	ms
Inter-digit pause; $8 \times T_{DP}$	see Figs 6 and 7	$t_{id}$	790	ms
Reset delay time; $1.6 \times T_{DP}$	see Figs 5,6 and 7	$t_{rd}$	158	ms
Prepulse duration; $1/3 \times T_{DP}$	see Figs 6 and 7	$t_d$	33	ms
Debounce time; min. $5/30 \times T_{DP}$	see Fig. 5	$t_{e \text{ min}}$	16.45	ms
max. $6/30 \times T_{DP}$	see Fig. 5	$t_{e \text{ max}}$	19.74	ms
Initial data entry time (typ.); $t_{on} + t_e$		$t_i$	22	ms

## Note to the PCD3322C timing data

1.  $f_{DP}$  is 10 Hz when a 3.5328 MHz crystal is used.

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**Pulse dialler circuits with redial****PCD332XC family**

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**PCD3324C specification**

The PCD3324C is pin-compatible with the DF320 and MT4320 types. It includes additional features that make it ideal for PABX systems. One access pause can be stored automatically during the original entry of a number, or several made via the keyboard. The circuit regenerates access pauses during redial. A regenerated access pause can be terminated during redial either automatically after a built-in delay, via the keyboard or with an external dial tone recognizer.

Inputs that are not available are internally defined as follows:

APD = LOW

Outputs not available are  $\overline{M1}$ , M2 and M3.

Features additional to the common family specification are:

- F01 + F02      inputs giving selection between one of the three dialling speeds or the test speed. In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.
- HOLD/APO      input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected)
- M/S             input for M/S ratio selection to 3:2 or 2:1.

## Pulse dialler circuits with radial

## PCD332XC family

## CHARACTERISTICS PER TYPE (continued)

## PCD3324C timing data

 $V_{DD} = 2.0$  to  $6$  V;  $V_{SS} = 0$  V;  $f_{OSC} = 3.579545$  MHz

parameter	conditions	symbol	FO1:	LOW	HIGH	LOW	unit
			FO2:	LOW	HIGH	HIGH	
Dialling pulse frequency $1/T_{DP}$	note 1	$f_{DP}$		10.13	15.54	19.42	Hz
Dialling pulse period: $1/f_{DP}$		$T_{DP}$		98.7	64.4	51.5	ms
Clock pulse frequency; $30 \times f_{DP}$		$f_{CLK}$		303.9	466.1	582.6	Hz
Break time; $3/5 \times T_{DP}$	M/S = HIGH or n.c.; notes 2 and 3	$t_b$		59.2	38.6	30.9	ms
Make time; $2/5 \times T_{DP}$	M/S = HIGH or n.c.; notes 2 and 3	$t_m$		39.5	25.8	20.6	ms
Break time; $2/3 \times T_{DP}$	M/S = LOW note 4	$t_b$		65.8	42.9	34.3	ms
Make time; $1/3 \times T_{DP}$	M/S = LOW note 4	$t_m$		32.9	21.5	17.2	ms
Inter-digit pause; $8 \times T_{DP}$		$t_{id}$		790	515	412	ms
Reset delay time ; $1.6 \times T_{DP}$		$t_{rd}$		158	103	82.4	ms
Access pause time; $32 T_{DP} \cdot t_m \cdot 1/f_{CL}$		$t_{ap}$		3.12	2.03	1.63	s
Prepulse duration; $1/3 \times T_{DP}$		$t_d$		33.0	21.5	17.2	ms
Debounce time; min. $5/30 \times T_{DP}$		$t_{e \text{ min}}$		16.45	10.70	8.58	ms
max. $6/30 \times T_{DP}$		$t_{e \text{ max}}$		19.74	12.88	10.30	ms
Initial data entry time (typ.) $t_{on} + t_e$		$t_i$		22.0	16.0	13.5	ms

## Notes to the PCD3324C timing data

- $f_{DP}$  is 10 Hz when a 3.5328 MHz crystal is used.
- In the n.c. (not connected) condition, the input is drawn to the HIGH state by the internal pull-up current.
- Mark/space ratio = 3:2.



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**Pulse dialler circuits with redial****PCD332XC family**

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**PCD3325C specification**

The PCD3325C is pin-compatible with the DF320 and MT4320 types. It includes additional features that make it ideal for PABX systems. Access pauses can be stored via the keyboard during the original entry of a number (there is no automatic storage of access pauses). The circuit regenerates access pauses during redial. A regenerated access pause can be terminated during redial either via the keyboard or with an external dial tone recognizer.

Inputs that are not available are defined internally as follows:

APD = LOW

Outputs not available are  $\overline{M1}$ , M2 and M3.

Features additional to the common family specification are:

- F01 + F02      inputs giving selection between one of the three dialling speeds or the test speed. In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.
- HOLD/APO      input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected).
- M/S              input for M/S ratio selection to 3:2 or 2:1.

## Pulse dialler circuits with radial

## PCD332XC family

## CHARACTERISTICS PER TYPE (continued)

## PCD3325C timing data

 $V_{DD} = 2.0$  to  $6$  V;  $V_{SS} = 0$  V;  $f_{osc} = 3.579545$  MHz

parameter	conditions	symbol	FO1:	LOW	HIGH	LOW	unit
			FO2:	LOW	HIGH	HIGH	
Dialling pulse frequency; $1/T_{DP}$	note 1	$f_{DP}$		10.13	15.54	19.42	Hz
Dialling pulse period; $1/f_{DP}$		$T_{DP}$		98.7	64.4	51.5	ms
Clock pulse frequency; $30 \times f_{DP}$		$f_{CLK}$		303.9	466.1	582.6	Hz
Break time; $3/5 \times T_{DP}$	M/S = HIGH or n.c.; notes 2 and 3	$t_b$		59.2	38.6	30.9	ms
Make time; $2/5 \times T_{DP}$	M/S = HIGH or n.c.; notes 2 and 3	$t_m$		39.5	25.8	20.6	ms
Break time; $2/3 \times T_{DP}$	M/S = LOW note 4	$t_b$		65.8	42.9	34.3	ms
Make time; $1/3 \times T_{DP}$	M/S = LOW note 4	$t_m$		32.9	21.5	17.2	ms
Inter-digit pause; $8 \times T_{DP}$		$t_{id}$		790	515	412	ms
Reset delay time; $1.6 \times T_{DP}$		$t_{rd}$		158	103	82.4	ms
Prepulse duration; $1/3 \times T_{DP}$		$t_d$		33.0	21.5	17.2	ms
Debounce time min. $5/30 \times T_{DP}$		$t_{e \text{ min}}$		16.45	10.70	8.58	ms
max. $6/30 \times T_{DP}$		$t_{e \text{ max}}$		19.74	12.88	10.30	ms
Initial data entry time (typ.); $t_{on} + t_e$		$t_i$		22.0	16.0	13.5	ms

## Notes to the PCD3325C timing data

- $f_{DP}$  is 10 Hz when a 3.5328 MHz crystal is used.
- In the n.c. (not connected) condition, the input is drawn to the HIGH state by the internal pull-up current.
- Mark/space ratio = 3:2.
- Mark/space ratio = 2:1.

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**Pulse dialler circuits with redial****PCD332XC family**

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**PCD3326C specification**

The PCD3326C includes many additional features that make it ideal for PABX systems. Two access pauses can be stored automatically during the original entry of a number, or several stored via the keyboard. The circuit regenerates access pauses during redial. A regenerated access pause can be terminated during redial either automatically after a built-in delay, via the keyboard or with an external dial tone recognizer.

Inputs that are not available are internally defined as follows:

M/S = HIGH

Outputs not available are  $\overline{M1}$ , M2 and M3.

Features additional to the common family specification are:

- F01 + F02    inputs giving selection between one of the three dialling speeds or the test speed. In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.
- HOLD/APO    input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected)
- APD          input for selecting access pause duration.

## Pulse dialler circuits with radial

## PCD332XC family

## CHARACTERISTICS PER TYPE (continued)

## PCD3326C timing data

 $V_{DD} = 2.0$  to  $6$  V;  $V_{SS} = 0$  V;  $f_{osc} = 3.579545$  MHz

parameter	conditions	symbol	FO1:	LOW	HIGH	LOW	unit
			FO2:	LOW	HIGH	HIGH	
Dialling pulse frequency; $1/T_{DP}$	note 1	$f_{DP}$		10.13	15.54	19.42	Hz
Dialling pulse period; $1/f_{DP}$		$T_{DP}$		98.7	64.4	51.5	ms
Clock pulse frequency; $30 \times f_{DP}$		$f_{CLK}$		303.9	466.1	582.6	Hz
Break time; $3/5 \times T_{DP}$	note 2	$t_b$		59.2	38.6	30.9	ms
Make time; $2/5 \times T_{DP}$	note 2	$t_m$		39.5	25.8	20.6	ms
Inter-digit pause; $8 \times T_{DP}$		$t_{id}$		790	515	412	ms
Reset delay time; $1.6 \times T_{DP}$		$t_{rd}$		158	103	82.4	ms
Access pause time $32 \times T_{DP} - t_m - 1/f_{CL}$	APD = LOW; or n.c.; note 3	$t_{ap}$		3.12	2.03	1.63	s
$64 \times T_{DP} - t_m - 1/f_{CL}$	APD = HIGH	$t_{ap}$		6.28	4.09	3.28	s
Prepulse duration; $1/3 \times T_{DP}$		$t_d$		33.0	21.5	17.2	ms
Debounce time, min. $5/30 \times T_{DP}$		$t_{e \text{ min}}$		16.45	10.70	8.58	ms
max. $6/30 \times T_{DP}$		$t_{e \text{ max}}$		19.74	12.88	10.33	ms
Initial data entry time (typ.); $t_{on} + t_e$		$t_i$		22.0	16.0	13.5	ms

## Notes to the PCD3326C timing data

- $f_{DP}$  is 10 Hz when a 3.5328 MHz crystal is used.
- Mark/space ratio = 3:2.
- In the n.c. (not connected) condition, the input is drawn to the LOW state by the internal pull-down current.

## Pulse dialler circuits with redial

## PCD332XC family

## PCD3327C specification

The PCD3327C contains an oscillator with sufficient gain to provide oscillation when using an inexpensive 455 kHz ceramic resonator. Two additional capacitors are required as shown in Fig.18. Alternatively, the OSC IN pin may be driven from an external 455 kHz clock signal.

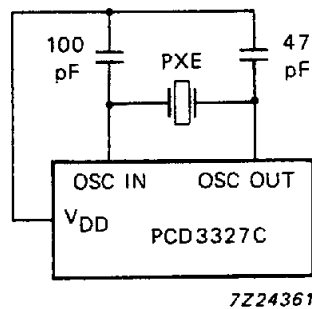


Fig.18 PCF3327 oscillator circuit.

This IC is pin-compatible with the DF320 and MT4320 types and includes additional features that make it ideal for PABX systems. The circuit allows several access pauses to be stored via the keyboard and regenerates the access pauses during redial. A regenerated access pause can be terminated during redial either automatically after a built-in delay, via the keyboard or with an external dial tone recognizer.

Inputs that are not available are internally defined as follows:

APD = LOW

Outputs not available are  $\overline{M1}$ , M2 and M3.

Features additional to the common family specification are:

F01 + F02 inputs giving selection between one of the three dialling speeds or the test speed. In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.

HOLD/APO input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected).

M/S input for M/S ratio selection to 3:2 or 2:1.

## Pulse dialler circuits with radial

## PCD332XC family

## CHARACTERISTICS PER TYPE (continued)

## PCD3327C timing data

 $V_{DD} = 2.0$  to  $6$  V;  $V_{SS} = 0$  V;  $f_{osc} = 455$  kHz

parameter	conditions	symbol	FO1:	LOW	HIGH	LOW	unit
			FO2:	LOW	HIGH	HIGH	
Dialling pulse frequency; $1/T_{DP}$	note 1	$f_{DP}$		10.3	15.8	19.7	Hz
Dialling pulse period; $1/f_{DP}$		$T_{DP}$		97	63	51	ms
Clock pulse frequency; $30 \times f_{DP}$		$f_{CLK}$		309	474	592	Hz
Break time; $3/5 \times T_{DP}$	M/S = HIGH or n.c.; notes 2 and 3	$t_b$		58	38	30	ms
Make time; $2/5 \times T_{DP}$	M/S = HIGH or n.c.; notes 2 and 3	$t_m$		39	25	20	ms
Break time; $2/3 \times T_{DP}$	M/S = LOW note 4	$t_b$		65	42	34	ms
Make time; $1/3 \times T_{DP}$	M/S = LOW note 4	$t_m$		32	21	17	ms
Inter-digit pause; $8 \times T_{DP}$		$t_{id}$		776	506	405	ms
Reset delay time; $1.6 \times T_{DP}$		$t_{rd}$		155	101	81	ms
Access pause time; $32 \times T_{DP} - t_m - 1/f_{CL}$		$t_{ap}$		3.12	2.03	1.63	s
Prepulse duration; $1/3 \times T_{DP}$		$t_d$		32	21	17	ms
Debounce time; min. $5/30 \times T_{DP}$		$t_{e \text{ min}}$		16.18	10.54	8.45	ms
max. $6/30 \times T_{DP}$		$t_{e \text{ max}}$		19.41	12.66	10.13	ms
Initial data entry time (typ.); $t_{on} + t_e$		$t_j$		22.0	16.0	13.5	ms

## Notes to the PCD3327C timing data

- $f_{DP}$  is 10 Hz when a 441.6 PXE ceramic resonator is used.
- In the n.c. (not connected) condition, the input is drawn to the HIGH state by the internal pull-up current.