DATA SHEET

PCD3745A
8-bit microcontroller with 4.5 kbytes OTP memory and 32 kHz real-time clock

Product specification
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Philips
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PHILIPS

CONTENTS

1 FEATURES

- 8-bit CPU, RAM and I/O
- 4.5 kbytes OTP memory; 224 bytes RAM
- 32 kHz adjustable crystal oscillator for real-time clock
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 16 quasi-bidirectional I/O port lines
- 8-bit programmable Timer/event counter 1
- Two 16-bit counters with count inputs pins
- 2 single-level vectored interrupts:
  - external; peripheral Counters 1 and 2; RTC alarm
  - 8-bit programmable Timer/event counter 1
- Two test inputs, one of which also serves as the external interrupt input
- Stop and Idle modes for power saving
- Logic supply: 1.8 to 6 V
- CPU clock frequency: 1 to 16 MHz
- Operating temperature: –25 to +70 °C
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

The PCD3745A is a microcontroller oriented towards communication and metering applications. It has 4.5 kbytes of One Time Programmable (OTP) memory, 224 bytes RAM and 16 I/O lines.

The PCD3745A also incorporates a low power Real-Time Clock (RTC) and two low power 16-bit counters. The RTC runs using a 32 kHz crystal oscillator and is register adjustable. The RTC and the counters are able to operate in all microcontroller modes. The instruction set is based on that of the MAB8048 and is software compatible with the PCD33xxA family.

This data sheet details the specific properties of the PCD3745A. The shared characteristics of the PCD33xxA family of microcontrollers are described in the *"Data Handbook IC14; Section PCD33xxA Family"*, which should be read in conjunction with this publication.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3745AP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCD3745AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCD3745AH	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

4 BLOCK DIAGRAM

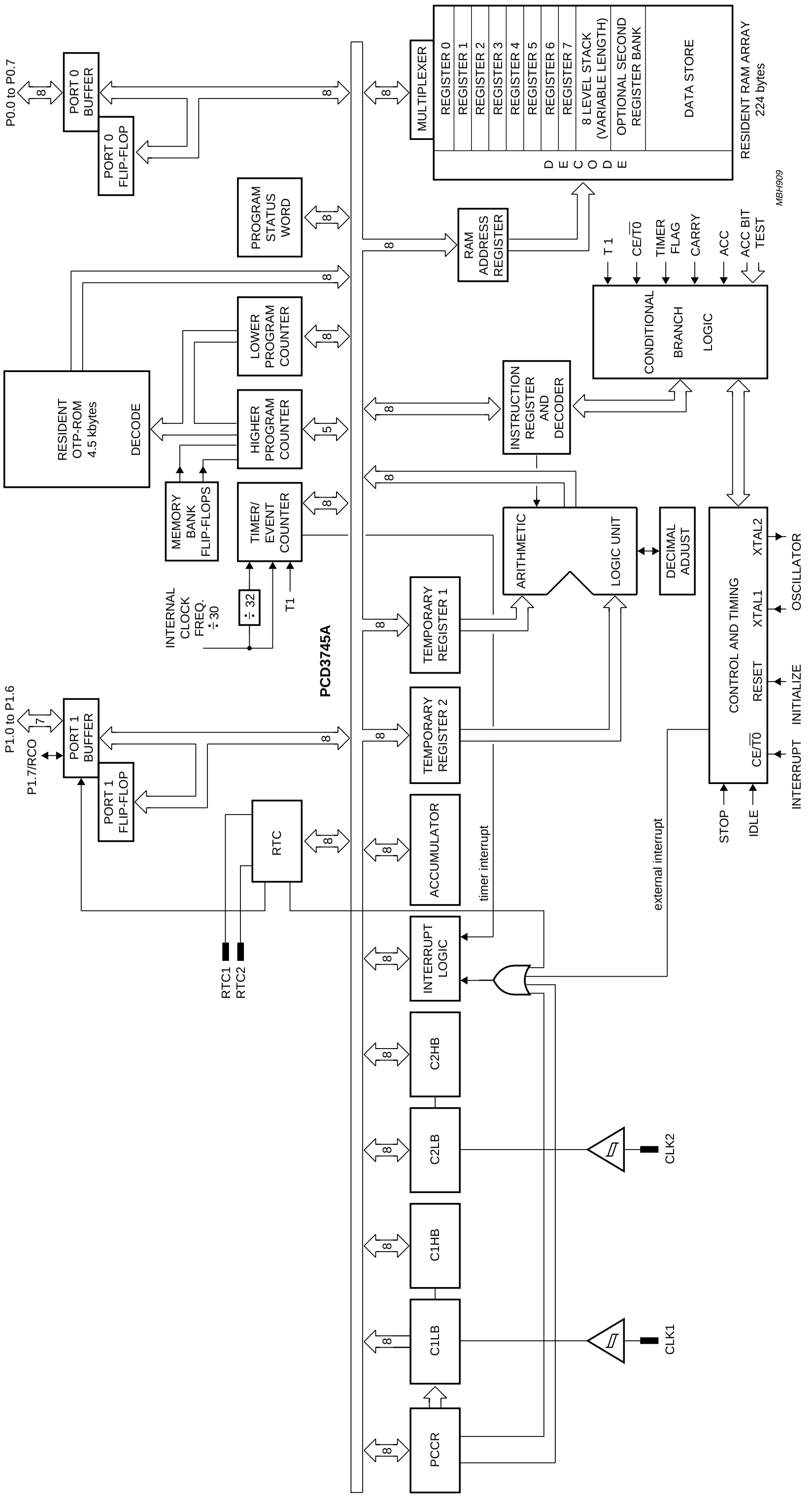


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

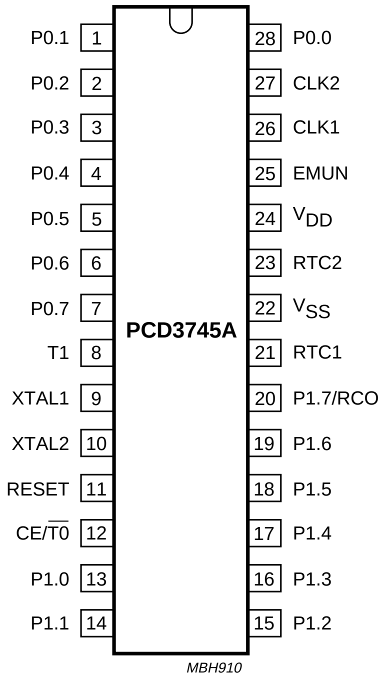


Fig.2 Pin configuration (SOT117-1 and SOT136-1).

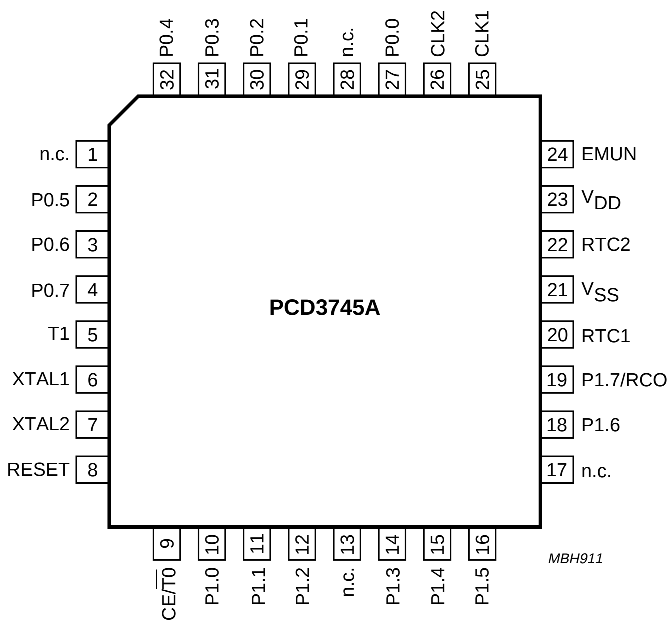


Fig.3 Pin configuration (SOT358-1).

5.2 Pin description

Table 1 SOT117-1 and SOT136-1 packages

SYMBOL	PIN	DESCRIPTION
P0.0 to P0.7	28, 1 to 7	Port 0: 8 quasi-bidirectional I/O lines
T1	8	Test 1 or count input of 8-bit Timer/event counter 1
XTAL1	9	crystal oscillator or external clock input
XTAL2	10	crystal oscillator output
RESET	11	reset input
CE/$\overline{T0}$	12	chip enable or Test 0
P1.0 to P1.6	13 to 19	Port 1: 7 quasi-bidirectional I/O lines
P1.7/RCO	20	Port 1: 1 quasi-bidirectional I/O line/Real Clock Output 16 kHz
RTC1	21	RTC 32 kHz oscillator input
V_{SS}	22	ground
RTC2	23	RTC 32 kHz oscillator output
V_{DD}	24	positive supply voltage
EMUN	25	emulation pin, must be connected to V_{DD} for normal mode operation.
CLK1	26	count input of 16-bit peripheral Counter 1
CLK2	27	count input of 16-bit peripheral Counter 2

Table 2 SOT358-1 package

SYMBOL	PIN	DESCRIPTION
n.c.	1, 13, 17, 28	not connected
T1	5	Test 1 or count input of 8-bit Timer/event counter 1
XTAL1	6	crystal oscillator or external clock input
XTAL2	7	crystal oscillator output
RESET	8	reset input
CE/$\overline{T0}$	9	chip enable or Test 0
P1.0 to P1.6	10 to 12, 14 to 16, 18	Port 1: 7 quasi-bidirectional I/O lines
P1.7/RCO	19	Port 1: 1 quasi-bidirectional I/O line/Real Clock Output 16 kHz
RTC1	20	RTC 32 kHz oscillator input
V_{SS}	21	ground
RTC2	22	RTC 32 kHz oscillator output
V_{DD}	23	positive supply voltage
EMUN	24	emulation pin, must be connected to V_{DD} for normal mode operation.
CLK1	25	count input of 16-bit peripheral Counter 1
CLK2	26	count input of 16-bit peripheral Counter 2
P0.0 to P0.7	27, 29 to 32, 2 to 4	Port 0: 8 quasi-bidirectional I/O lines

6 REAL-TIME CLOCK (RTC)

The RTC consists of a 32 kHz crystal oscillator, a 32 kHz to 1 second, 1.5 second and 1 minute divider chain, an 8-bit Frequency Adjustment Register (FAR) and the Clock Control Register (CLCR). The complete real-time clock section is independent of the microcontroller status, even in Idle or Stop mode.

6.1 Oscillator

The internal 32 kHz oscillator requires an external 32.768 kHz quartz crystal (a positive deviation up to +259 ppm is allowed by using frequency adjustment) and an external feedback resistor (4.7 MΩ) connected between the RTC1 and RTC2 pins. The oscillator is controlled by the RUN bit in the Clock Control Register.

6.2 Divider chain

The divider chain operates with the 32 kHz oscillator output and divides this signal down to produce three different clocks with periods of 1 second, 1.5 second and 1 minute. Depending on the state of the ITS and SITS bits in the Clock Control Register, the falling edge of the 1 second, 1.5 second or 1 minute clock is used to set the Clock Interrupt Flag (CIF) in the Clock Control Register. Since the clock interrupt is used to let the microcontroller leave the Stop mode, it is wire ORed with the external interrupt (CE/$\overline{\text{T0}}$) and has the same functionality, e.g. it must be enabled in the Clock Control Register (ECI = 1) and by execution of EN I. The clock interrupt will then be treated as an external interrupt

Additionally, the divider chain generates a 16 kHz clock (RCO) that can be routed through port line P1.7/RCO, controlled by the ERCO bit in the Clock Control Register.

6.3 Frequency adjustment

Frequency adjustment is used to extend the interrupt time by defining the number of 16 kHz clocks in the Frequency Adjustment Register that will be counted twice within the first 1 second or 1.5 second period after a minute interrupt. The DIV512 is reset if its contents is equal to FAR, this will extend the time of the next interrupt. This is done within the first 1 second or 1.5 seconds of every minute. If the second interrupt is used (ITS = 1 and SITS = 0), every 60th interval may be up to 15.3 ms longer than the others as a result of the frequency adjustment. If the 1.5 second interrupt is used (ITS = 1 and SITS = 1), the prolongation will affect every 40th interval. The adjusted Minute Interrupt Time (MIT) shows now a maximum deviation of 0.5 ppm.

The frequency adjustment value of the real-time clock section is defined by the decimal value of the contents of the 8-bit Frequency Adjustment Register. It can be read or written. The significance of the individual bits is illustrated by the following equation:

$$\text{Minute Interrupt Time (MIT)} = 60 \times 2^{\frac{14}{\text{FRCO}}} + \frac{\text{FAR}}{2^{14}}$$

Table 7 shows the recommended correction factor FAR for all allowed real-time clock frequencies (FRCO).

The value of CLCR and FAR at reset is 00H.

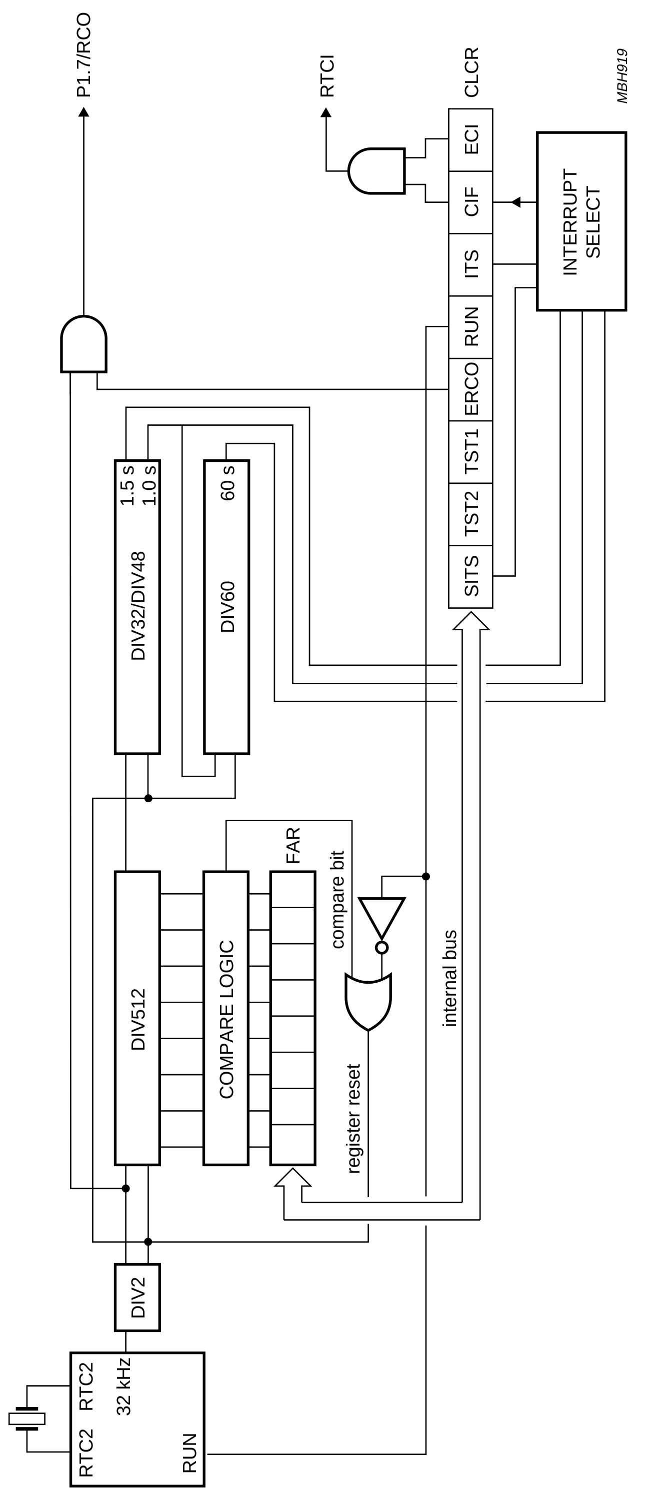


Fig.4 RTC block diagram.

6.4 Clock Control Register (CLCR)

Table 3 Clock Control Register (address 20H)

7	6	5	4	3	2	1	0
SITS	TST2	TST1	ERCO	RUN	ITS	CIF	ECI

Table 4 Description of CLCR bits

BIT	SYMBOL	DESCRIPTION
7	SITS	**Second Interrupt Time Select.** If SITS = 1 and ITS = 1, then the interrupt time is 1.5 seconds.
6	TST2	**Test 2 input.** This is a test bit and must be fixed at zero by user software.
5	TST1	**Test 1 input.** This is a test bit and must be fixed at zero by user software.
4	ERCO	**Enable 16 kHz Clock Output.** If ERCO = 0, then P1.7/RCO is a port line. If ERCO = 1, then P1.7/RCO is a 16 kHz clock output. The port instructions for P1.7/RCO are not inhibited and therefore the state of both the port line and flip-flop may be read in and the port flip-flop may be written to by port instructions.
3	RUN	**Clock Run/Stop.** If RUN = 0, then the 32 kHz oscillator is stopped and the divider chain is reset. If RUN = 1, then the 32 kHz oscillator and the divider chain are running.
2	ITS	**Interrupt Time Select.** If ITS = 1 and SITS = 0, then the interrupt time is one second. If ITS = 0 and SITS = X, then the interrupt time is one minute.
1	CIF	**Clock Interrupt Flag.** Set by hardware, if RTC divider chain overflows (every second, 1.5 second or minute depending on ITS) or by software. Reset: by software.
0	ECI	**Enable Clock Interrupt.** If ECI = 0, the RTC interrupt is disabled. If ECI = 1, the RTC interrupt is enabled.

6.5 Frequency Adjustment Register (FAR)

Table 5 Frequency Adjustment Register (address 21H)

7	6	5	4	3	2	1	0
FAR7	FAR6	FAR5	FAR4	FAR3	FAR2	FAR1	FAR0

Table 6 Description of FAR bits

BIT	SYMBOL	DESCRIPTION
7	FAR7	The state of these 8-bits determine the frequency adjustment value for the real-time clock section; see Table 7.
6	FAR6	
5	FAR5	
4	FAR4	
3	FAR3	
2	FAR2	
1	FAR1	
0	FAR0	

Table 7 Selection of FRCO

FAR (HEX)	FRCO
00	16384.000
01	16384.018
02	16384.033
03	16384.051
04	16384.066
05	16384.084
06	16384.100
07	16384.117
08	16384.135
09	16384.150
0A	16384.168
0B	16384.184
0C	16384.201
0D	16384.217
0E	16384.234
0F	16384.250
10	16384.268
11	16384.283
12	16384.301
13	16384.316
14	16384.334
15	16384.350
16	16384.367
17	16384.385
18	16384.400
19	16384.418
1A	16384.434
1B	16384.451
1C	16384.467
1D	16384.484
1E	16384.500
1F	16384.518
20	16384.533
21	16384.551

FAR (HEX)	FRCO
22	16384.566
23	16384.584
24	16384.600
25	16384.617
26	16384.635
27	16384.650
28	16384.668
29	16384.684
2A	16384.701
2B	16384.717
2C	16384.734
2D	16384.750
2E	16384.768
2F	16384.783
30	16384.801
31	16384.816
32	16384.834
33	16384.850
34	16384.867
35	16384.885
36	16384.900
37	16384.918
38	16384.934
39	16384.951
3A	16384.967
3B	16384.984
3C	16385.000
3D	16385.018
3E	16385.033
3F	16385.051
40	16385.066
41	16385.084
42	16385.100
43	16385.117

FAR (HEX)	FRCO
44	16385.135
45	16385.150
46	16385.168
47	16385.184
48	16385.201
49	16385.217
4A	16385.234
4B	16385.250
4C	16385.268
4D	16385.283
4E	16385.301
4F	16385.316
50	16385.334
51	16385.350
52	16385.367
53	16385.385
54	16385.400
55	16385.418
56	16385.434
57	16385.451
58	16385.467
59	16385.484
5A	16385.500
5B	16385.518
5C	16385.533
5D	16385.551
5E	16385.566
5F	16385.584
60	16385.600
61	16385.617
62	16385.635
63	16385.650
64	16385.668
65	16385.684

FAR (HEX)	FRCO
66	16385.701
67	16385.717
68	16385.734
69	16385.750
6A	16385.768
6B	16385.783
6C	16385.801
6D	16385.816
6E	16385.834
6F	16385.850
70	16385.867
71	16385.885
72	16385.900
73	16385.918
74	16385.934
75	16385.951
76	16385.967
77	16385.984
78	16386.000
79	16386.018
7A	16386.033
7B	16386.051
7C	16386.066
7D	16386.084
7E	16386.100
7F	16386.117
80	16386.135
81	16386.150
82	16386.168
83	16386.184
84	16386.201
85	16386.217
86	16386.234
87	16386.250

FAR (HEX)	FRCO
88	16386.268
89	16386.283
8A	16386.301
8B	16386.316
8C	16386.334
8D	16386.350
8E	16386.367
8F	16386.385
90	16386.400
91	16386.418
92	16386.434
93	16386.451
94	16386.467
95	16386.484
96	16386.500
97	16386.518
98	16386.533
99	16386.551
9A	16386.566
9B	16386.584
9C	16386.600
9D	16386.617
9E	16386.635
9F	16386.650
A0	16386.668
A1	16386.684
A2	16386.701
A3	16386.717
A4	16386.734
A5	16386.750

FAR (HEX)	FRCO
A6	16386.768
A7	16386.783
A8	16386.801
A9	16386.816
AA	16386.834
AB	16386.850
AC	16386.867
AD	16386.885
AE	16386.900
AF	16386.918
B0	16386.934
B1	16386.951
B2	16386.967
B3	16386.984
B4	16387.000
B5	16387.018
B6	16387.033
B7	16387.051
B8	16387.066
B9	16387.084
BA	16387.100
BB	16387.117
BC	16387.135
BD	16387.150
BE	16387.168
BF	16387.184
C0	16387.201
C1	16387.217
C2	16387.234
C3	16387.250

FAR (HEX)	FRCO
C4	16387.268
C5	16387.283
C6	16387.301
C7	16387.316
C8	16387.334
C9	16387.350
CA	16387.367
CB	16387.385
CC	16387.400
CD	16387.418
CE	16387.434
CF	16387.451
D0	16387.467
D1	16387.484
D2	16387.500
D3	16387.518
D4	16387.533
D5	16387.551
D6	16387.566
D7	16387.584
D8	16387.600
D9	16387.617
DA	16387.635
DB	16387.650
DC	16387.668
DD	16387.684
DE	16387.701
DF	16387.717
E0	16387.734
E1	16387.750

FAR (HEX)	FRCO
E2	16387.768
E3	16387.783
E4	16387.801
E5	16387.816
E6	16387.834
E7	16387.850
E8	16387.867
E9	16387.885
EA	16387.900
EB	16387.918
EC	16387.934
ED	16387.951
EE	16387.967
EF	16387.984
F0	16388.002
F1	16388.018
F2	16388.035
F3	16388.051
F4	16388.068
F5	16388.084
F6	16388.102
F7	16388.117
F8	16388.135
F9	16388.152
FA	16388.168
FB	16388.186
FC	16388.201
FD	16388.219
FE	16388.234
FF	16384.000

7 PERIPHERAL COUNTER 1 AND COUNTER 2

The PCD3745A has two on-chip 16-bit peripheral counters: Counter 1 and Counter 2. Both counters can count pulses in the frequency range of 0 to 1 MHz and both will operate in all modes of the microcontroller (Idle, Stop and Operating modes).

The count process and the interrupt on overflow function for each counter is enabled/disabled by setting the appropriate ECx and ECxI bits in the Peripheral Counter Control Register (PCCR). The count process starts with setting the ECx bit to a logic 1 and can be stopped in every state by resetting the ECx bit to a logic 0. The counter inputs are CLK1 for Counter 1 and CLK2 for Counter 2. Each counter input is connected to a Schmitt trigger in order to reduce noise susceptibility. A falling edge of the pulses on these inputs will increment the enabled counters by one. The 16-bit counters are also byte-wise read and writeable, e.g. they can be set to a specific value, for example to count less than 2^{16} events (refer to Table 13 for register addresses).

The 16-bit counters and the PCCR (see Table 8) are set to 0000H and 00H respectively, after reset.

Counting events during a write access may be lost. During a read access they are considered when the length of the count pulse is greater than $2/f_{xtal}$ + 500 ns. To ensure correct operation it is recommended to disable the count process during a read or write operation to the counter registers.

In the count mode, if the ECxI bit is set, an overflow (count transition from FFFFH to 0000H) of the counter will set the CxF bit, which starts the interrupt sequence. CxF is wired ORed with CE/$\overline{T0}$ and consequently the effect is the same as an external interrupt. Within this interrupt sequence the interrupt source must be searched and CxF should be reset to enable the microcontroller to service future interrupts. CxF is set by hardware or software but can be reset by software.

The operation of the 16-bit counters when used in a metering application is shown in Fig.5.

Note: If the counter value is set from 0000H to FFFFH by software and the status 0000H was reached either by clocking (overflow) or by hardware reset the subsequent clock pulse (CLKx) will NOT set the interrupt flag (C1F or C2F) in the PCCR register!

7.1 Peripheral Counter Control Register (PCCR)

Table 8 Peripheral Counter Control Register (address 40H)

7	6	5	4	3	2	1	0
EC1	EC1I	0	C1F	EC2	EC2I	0	C2F

Table 9 Description of PCCR bits

BIT	SYMBOL	DESCRIPTION
7	EC1	**Enable Counter 1.** If EC1 = 1, the counter is enabled and increments upwards every HIGH-to-LOW transition on pin CLK1. If EC1 = 0, the incrementing stops and the counter keeps the accumulated value. This bit is set/reset by software.
6	EC1I	**Enable Counter 1 Interrupt Flag.** When EC1I is set to a logic 1, the C1F event requests an interrupt. This bit is set/reset by software.
5	0	not used
4	C1F	**Counter 1 Interrupt Flag.** If C1F = 1, then a counter overflow has occurred in Counter 1. Set by hardware and software; reset by software.
3	EC2	**Enable Counter 2.** If EC2 = 1, the counter is enabled and increments upwards every HIGH-to-LOW transition on pin CLK2. If EC2 = 0, the incrementing stops and the counter keeps the accumulated value. This bit is set/reset by software.
2	EC2I	**Enable Counter 2 Interrupt Flag.** When EC2I is set to a logic 1, the C2F event requests an interrupt. This bit is set/reset by software.
1	0	not used
0	C2F	**Counter 2 Interrupt Flag.** If C2F = 1, then a counter overflow has occurred in Counter 2. Set by hardware and software; reset by software.

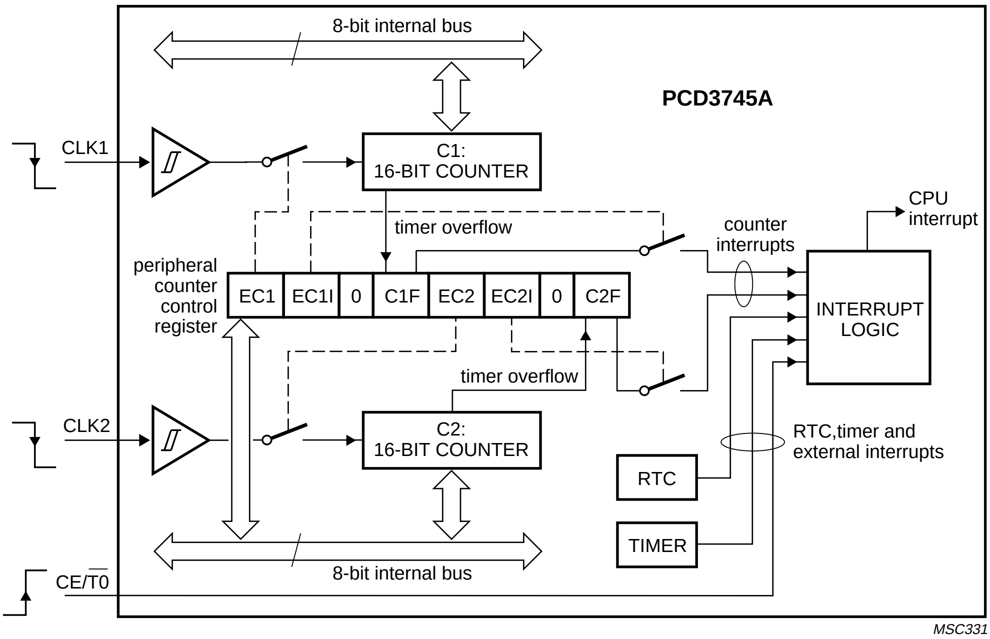


Fig.5 Operation of the 16-bit counters used in metering applications.

8 THE RTC, COUNTER 1 AND COUNTER 2 INTERRUPTS

As well as the CE/$\overline{T0}$ interrupt three additional interrupt events are defined which have the same effect as an external interrupt (see *"PCD33xxA family data sheet"*).

- **Real Time Clock.** This interrupt is controlled by the Clock Interrupt Flag (CIF) and the Enable Clock Interrupt (ECI) bit both of which reside in the Clock Control Register (see Tables 3 and 4)
- **Counter 1.** This interrupt is controlled by the Counter 1 Interrupt Flag (C1F) and the Enable Counter 1 Interrupt Flag (EC1I) both of which are located in the Peripheral Counter Control Register (see Tables 8 and 9)
- **Counter 2.** This interrupt is controlled by the Counter 2 Interrupt Flag (C2F) and the Enable Counter 2 Interrupt Flag (EC2I) both of which are located in the Peripheral Counter Control Register (see Tables 8 and 9).

To use these interrupt sources the external interrupt must be enabled (EN I). Interrupt servicing is exactly the same as for an external interrupt. The interrupt routine must include instructions that will determine the interrupt source and remove the cause of the derivative interrupt by explicitly clearing CIF, C1F or C2F.

By not clearing these flags the microcontroller is unable to detect interrupts of the same type. In the interrupt routine the CE/$\overline{T0}$ interrupt has to be deduced from the fact that neither CIF or C1F or C2F is set. If the specific interrupt is not used, CIF, C1F or C2F may be directly tested by the program. Obviously, CIF, C1F or C2F can also be asserted under program control, e.g. to generate a software interrupt.

Although the clock interrupt and Counter 1 and Counter 2 are part of a derivative function they are linked to the external interrupt (see Fig.6).

A clock, Counter 1 or Counter 2 interrupt request is serviced under the following circumstances:

- No interrupt routine is being processed
- No external interrupt request is pending
- The enable clock interrupt and enable Counter 1 and Counter 2 interrupt bit in the derivative Clock Control Register and Peripheral Counter Control Register respectively is set.

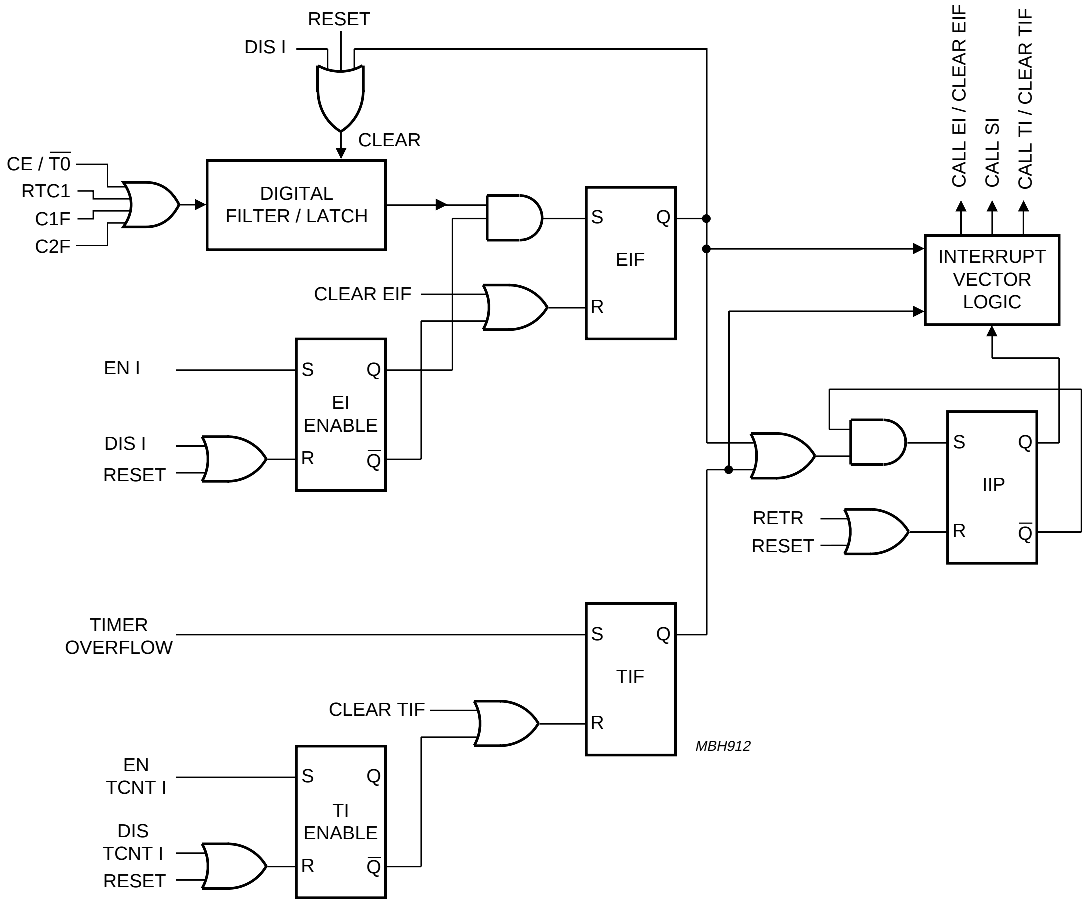


Fig.6 Simplified interrupt logic schematic (the R input overrules the S input for all flags).

9 REDUCED POWER MODES

9.1 Idle mode

In Idle mode, the Real-time clock, Counter 1 and Counter 2 sections remain operative. In addition to the description given in the *"PCD33xxA family data sheet"*, Idle mode may be left by a clock or a counter interrupt event (see Section 8).

9.2 Stop mode

In Stop mode the Real-Time Clock, Counter 1, Counter 2 and the 32 kHz crystal oscillator sections remain operative (depending on the state of the RUN and ECx bits in CLCR and PCCR). In addition to the description given in the *"PCD33xxA family data sheet"*, Stop mode may be left by a clock or a counter interrupt event (see Section 8).

10 INSTRUCTION SET RESTRICTIONS

RAM space is restricted to 224 bytes; care should be taken to avoid accesses to non-existing RAM locations.

11 TIMING

The PCD3745A operates over a clock frequency range of 1 to 16 MHz.

12 RESET

In addition to the conditions given in the *"PCD33xxA family data sheet"*, all derivative registers are cleared in the reset state.

13 SUMMARY OF CONFIGURATIONS

Table 10 Port configuration (see notes 1 and 2)

TYPE	PORT 0								PORT 1							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
PCD3745A	3R	3R	3S	3S	3R	3R	3R	3R	1S	1S	1S	1S	1R	1R	1R	1S

Notes

1. 1 = standard I/O; 3 = push-pull Output.
2. Port state after reset: S = Set (HIGH) and R = Reset (LOW).

Table 11 Product configurations

FEATURE	DESCRIPTION
Program/data code	any mix of instructions and data up to OTP memory size of 4.5 kbytes
Oscillator transconductance	fixed at LOW transconductance (g_{mL}); the maximum crystal clock frequency is 6 MHz

14 OTP PROGRAMMING

The programming of the PCD3745A OTP is based on the OM4260 programmer (Ceibo MP-51) which is available from Philips. The OM4260 works in conjunction with various adapters and supports the package types listed in Table 12.

The low voltage OTP program memory used is of Anti-Fuse-PROM type and cannot be erased after programming. Thus, the complete OTP memory cannot be tested by the factory, but only partially via a special test array. The average expected yield is 97%.

Detailed information on the OTP programming is available in the *“PCD3755x Application Note”*, available from Philips Sales offices.

Table 12 OTP programming overview

DEVICE	PHILIPS TYPE NUMBER	CEIBO TYPE NUMBER	SUPPORTED PACKAGE
Ceibo MP-51	OM4260	MP-51 programmer base	–
PCD3745A	OM5007	adapter DIP	DIP28
	OM5030	adapter SO	SO28
	OM5037; note 1	socket converter LQFP32	LQFP32

Note

1. As the OM5037 is only a socket converter, the OM5007 is also needed to program the PCD3745A in the LQFP32 package.

15 SUMMARY OF DERIVATIVE REGISTERS

Table 13 Register map

ADDRESS (HEX)	REGISTER	7	6	5	4	3	2	1	0
00 to 1F	not used	–	–	–	–	–	–	–	–
20	Clock Control Register (CLCR)	SITS	TST2	TST1	ERCO	RUN	ITS	CIF	ECI
21	Frequency Adjustment Register (FAR)	FAR7	FAR6	FAR5	FAR4	FAR3	FAR2	FAR1	FAR0
22 to 3F	not used	–	–	–	–	–	–	–	–
40	Peripheral Counter Control Register (PCCR)	EC1	EC1I	0	C1F	EC2	EC2I	0	C2F
41	Counter 1 Low Byte (C1LB)	C1LB7	C1LB6	C1LB5	C1LB4	C1LB3	C1LB2	C1LB1	C1LB0
42	Counter 1 High Byte (C1HB)	C1HB7	C1HB6	C1HB5	C1HB4	C1HB3	C1HB2	C1HB1	C1HB0
43	Counter 2 Low Byte (C2LB)	C2LB7	C2LB6	C2LB5	C2LB4	C2LB3	C2LB2	C2LB1	C2LB0
44	Counter 2 High Byte (C2HB)	C2HB	C2HB	C2HB	C2HB	C2HB	C2HB	C2HB	C2HB
45 to FF	not used	–	–	–	–	–	–	–	–

16 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); see notes 1 and 2.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.8	+7.0	V
V_I	all input voltages	–0.5	V_{DD} + 0.5	V
I_I, I_O	DC input or output current	–10	+10	mA
P_{tot}	total power dissipation	–	125	mW
P_O	power dissipation per output	–	30	mW
I_{SS}	ground supply current	–50	+50	mA
T_{stg}	storage temperature	–65	+150	°C
T_j	operating junction temperature	–	90	°C

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over the operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise stated.

17 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

18 DC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = –25 to +70 °C; f_{xtal} = 3.58 MHz; f_{RTC} = 32768 Hz; all voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (see Figs 8, 9, 10, 11, 12 and 13)						
V_{DD}	supply voltage					
	operating		1.8	–	6	V
	RAM data retention in Stop mode		1.0	–	6	V
I_{DD}	operating supply current	V_{DD} = 3 V; note 1	–	0.35	0.7	mA
$I_{DD(ID)}$	supply current Idle mode	V_{DD} = 3 V; note 1	–	0.25	0.5	mA
$I_{DD(stp)}$	supply current Stop mode	T_{amb} = 25 °C; counters and RTC not running; notes 1 and 2	–	1.0	5.0	µA
		T_{amb} = –25 to +70 °C; counters and RTC not running; notes 1 and 2	–	–	10	µA
		T_{amb} = 25 °C; counters and RTC running at 33 kHz; notes 1 and 2	–	3.0	6.0	µA
Inputs						
V_{IL}	LOW-level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	–1	–	+1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Port outputs (see Figs 14, 15 and 16)						
I_{OL}	LOW-level port sink current	V_{DD} = 3 V; V_O = 0.4 V	0.7	3.5	–	mA
I_{OH}	HIGH-level port pull-up source current	V_{DD} = 3 V; V_O = 2.7 V	–10	–30	–	µA
		V_{DD} = 3 V; V_O = 0 V	–	–140	–300	µA
I_{OH}	HIGH-level port push-pull source current	V_{DD} = 3 V; V_O = 2.6 V	–0.7	–3.5	–	mA
Real-time clock 32 kHz oscillator						
g_m	transconductance	$V_{i(p-p)}$ < 50 mV	2	10	50	µS
δf/f	frequency adjustment		–0.6	–	+0.6	ppm
$C_{I(RTC1)}$	RTC1 pin input capacitance		–	10	–	pF
$C_{O(RTC2)}$	RTC2 pin output capacitance		–	10	–	pF
Clock inputs of peripheral counters (CLK1 and CLK2)						
$V_{th(LH)}$	positive-going threshold voltage	V_{DD} = 5 V; T_{amb} = +25 °C; see Fig.7	–	$0.6V_{DD}$	–	V
$V_{th(HL)}$	negative-going threshold voltage	V_{DD} = 5 V; T_{amb} = +25 °C; see Fig.7	–	$0.4V_{DD}$	–	V
t_W	pulse width	notes 3 and 4; see Fig.7	500	–	–	ns
f_c	count frequency	note 4	0	–	1	MHz
XTAL oscillator						
g_{mL}	LOW transconductance	V_{DD} = 5 V; see Fig.18	0.2	0.4	1.0	mA/V
R_f	feedback resistor		0.3	1.0	3.0	MΩ

Notes

1. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; outputs open:
   a) Maximum values: external clock at XTAL1 and XTAL2 open-circuit.
   b) Typical values: at 25 °C; crystal connected between XTAL1 and XTAL2.
2. V_{DD} = 1.8 V; RESET, T1 and CE/$\overline{T0}$ at V_{SS}.
3. For proper operation of the counters the count pulse width (t_W), negative and positive, should be 500 ns. If the intention is to access the counters in read mode during counting, the count pulse width should be at least $2/f_{xtal}$ + 500 ns.
4. Verified on sample bases. Not tested during production.

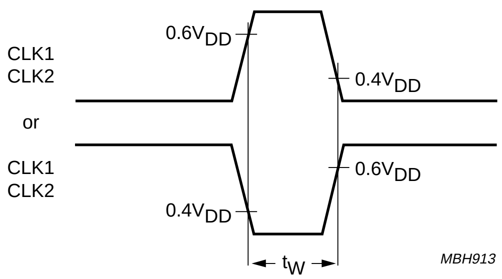
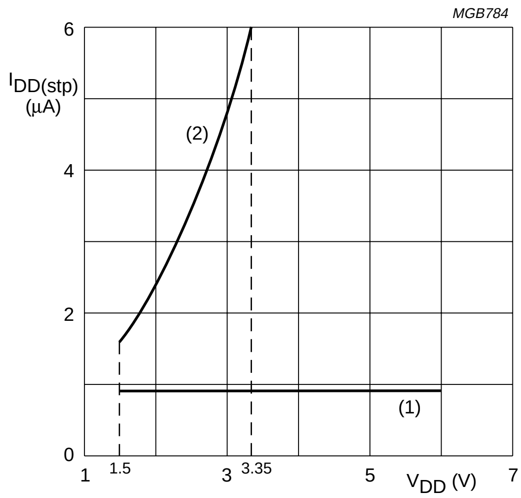


Fig.7 Definition of count pulse width (t_W).



(1) RTC stopped; –25 to 70 °C.

(2) RTC running; –25 to 70 °C.

Fig.8 Typical supply current (I_{DD}) in Stop mode as a function of supply voltage (V_{DD}).

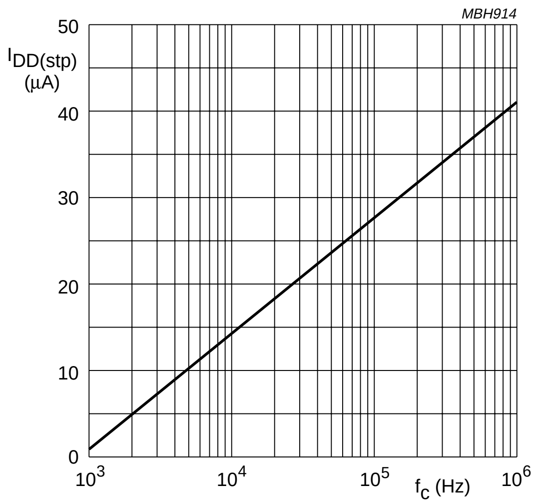
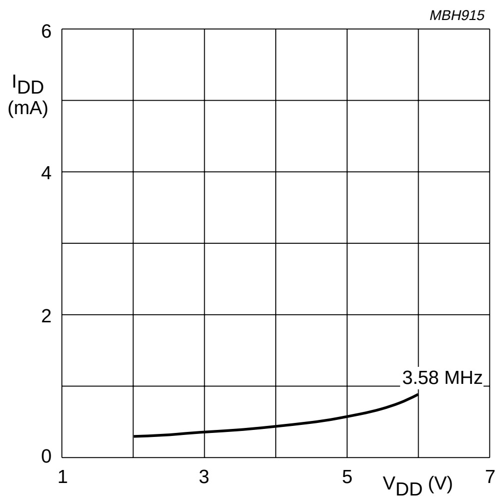
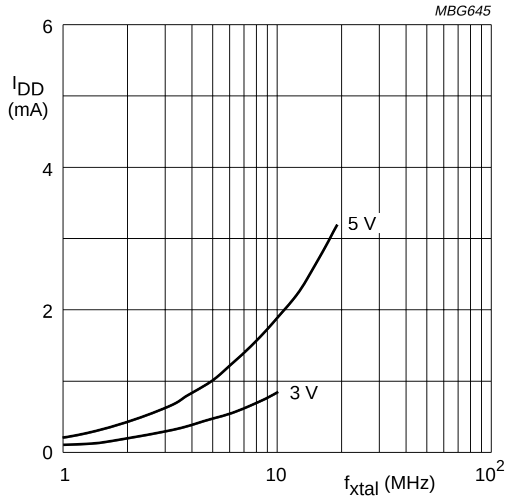


Fig.9 Typical supply current ($I_{DD(stp)}$) in Stop mode as a function of counter frequency, both counters running in parallel. (V_{DD} = 3 V; T_{amb} = +25 °C),



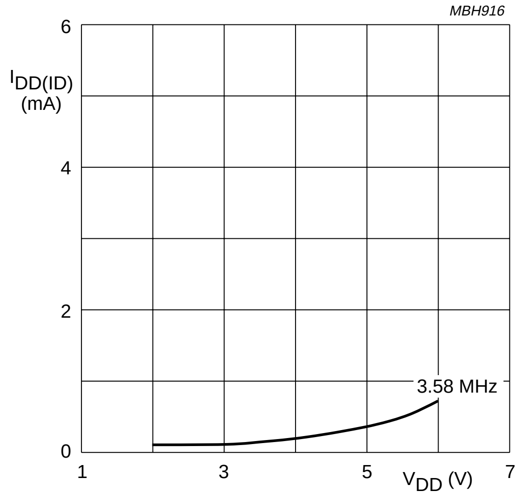
Measured with crystal between XTAL1 and XTAL2.

Fig.10 Typical operating supply current (I_{DD}) as a function of supply voltage (V_{DD}).



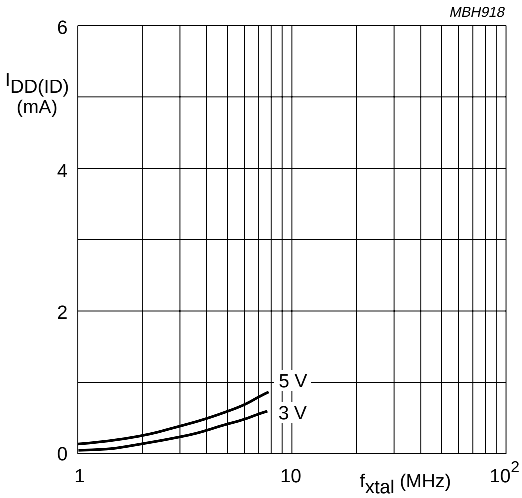
Measured with function generator on XTAL1.

Fig.11 Typical operating supply current (I_{DD}) as a function of clock frequency (f_{xtal}).



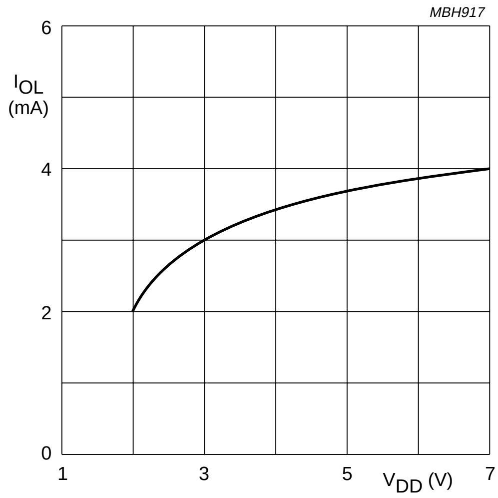
Measured with crystal between XTAL1 and XTAL2.

Fig.12 Typical supply current ($I_{DD(ID)}$) in Idle mode as a function of supply voltage (V_{DD}).



Measured with function generator on XTAL1.

Fig.13 Typical supply current ($I_{DD(ID)}$) in Idle mode as a function of clock frequency (f_{xtal}).



V_O = 0.4 V.

Fig.14 Typical LOW level port output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

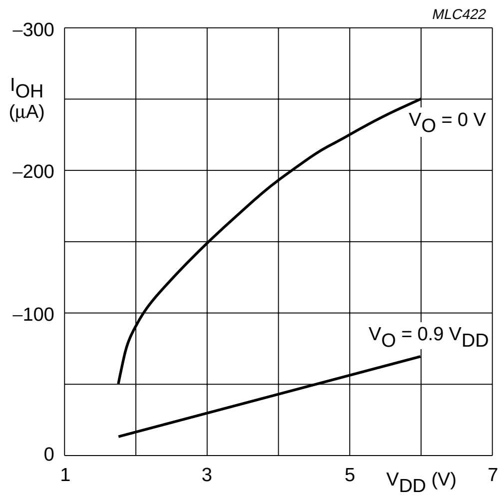
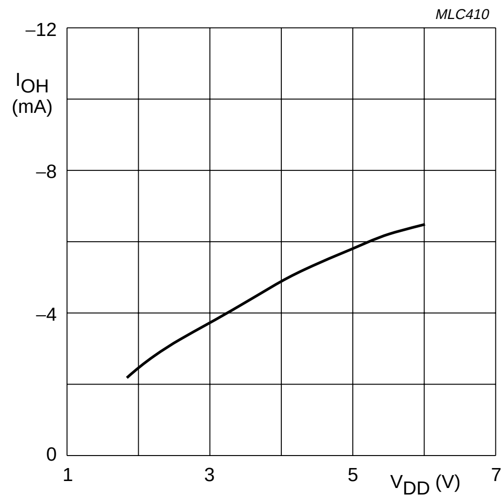


Fig.15 Typical HIGH level output pull-up source current (I_{OH}) as a function of supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V.

Fig.16 Typical HIGH level push-pull output source current (I_{OH}) as a function of supply voltage (V_{DD}).

19 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = –25 to +70 °C; all voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs		–	30	–	ns
f_{xtal}	clock frequency	see Fig.17	1	–	16	MHz

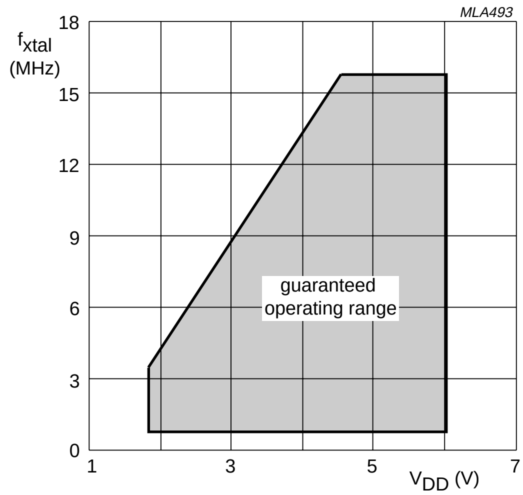


Fig.17 Maximum clock frequency (f_{xtal}) as a function of supply voltage (V_{DD}).

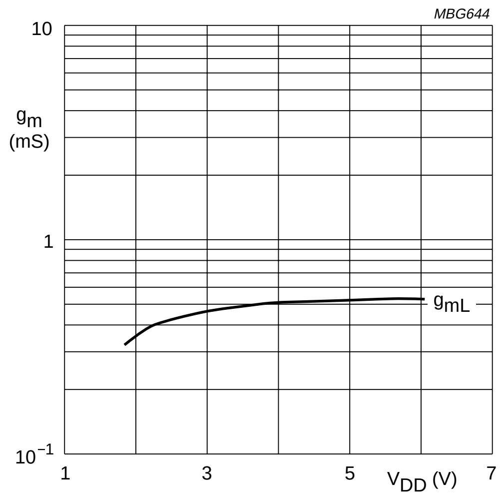


Fig.18 Typical transconductance of XTAL oscillator as a function of supply voltage (V_{DD}).

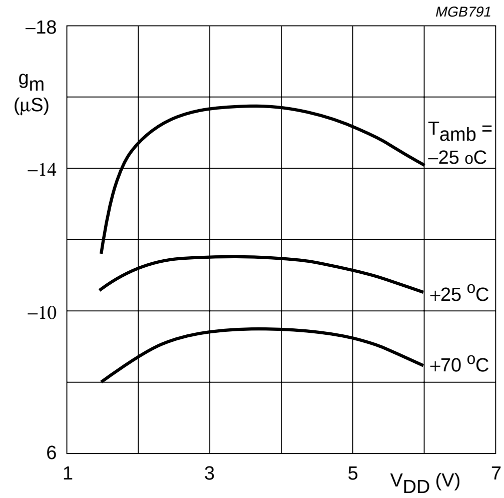
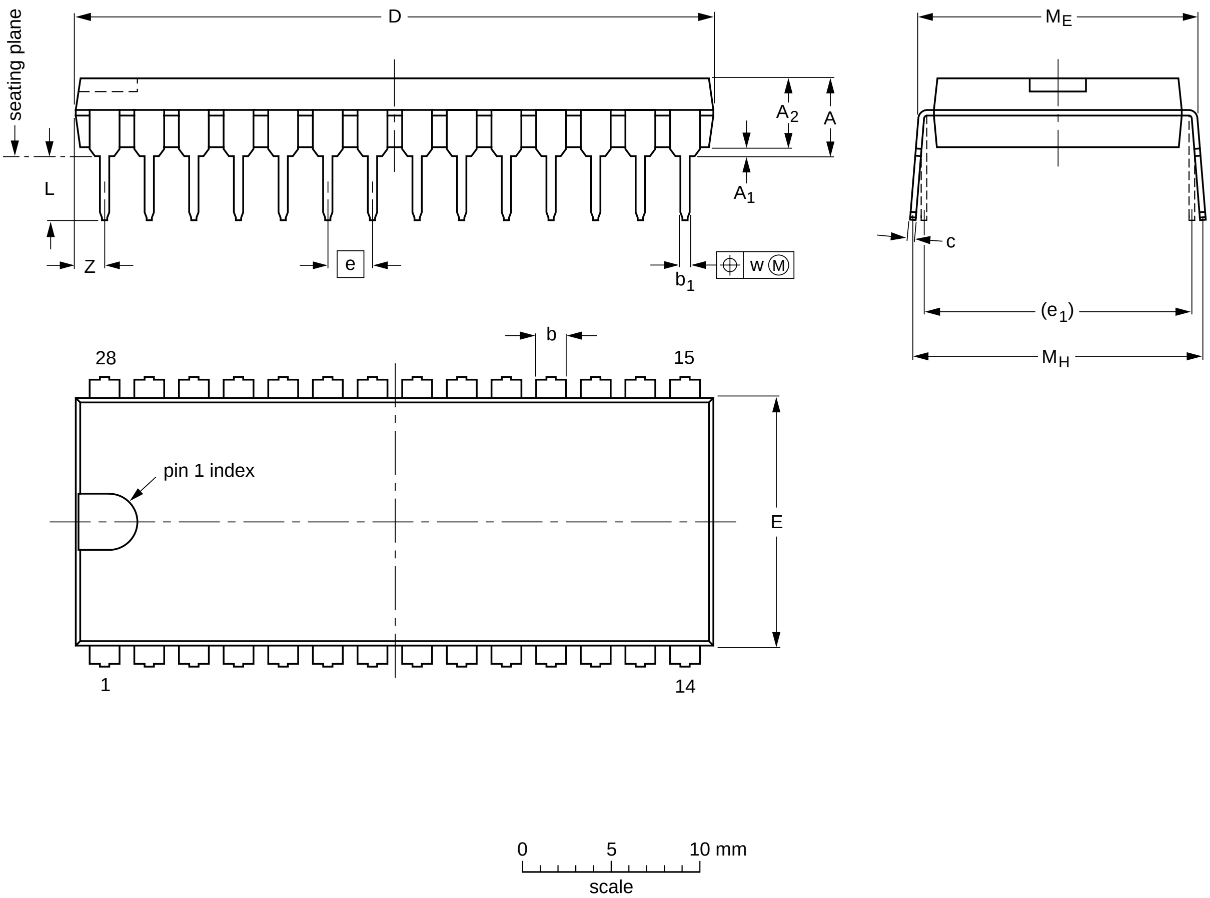


Fig.19 Typical RTC oscillator transconductance as a function of supply voltage (V_{DD}).

20 PACKAGE OUTLINES

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

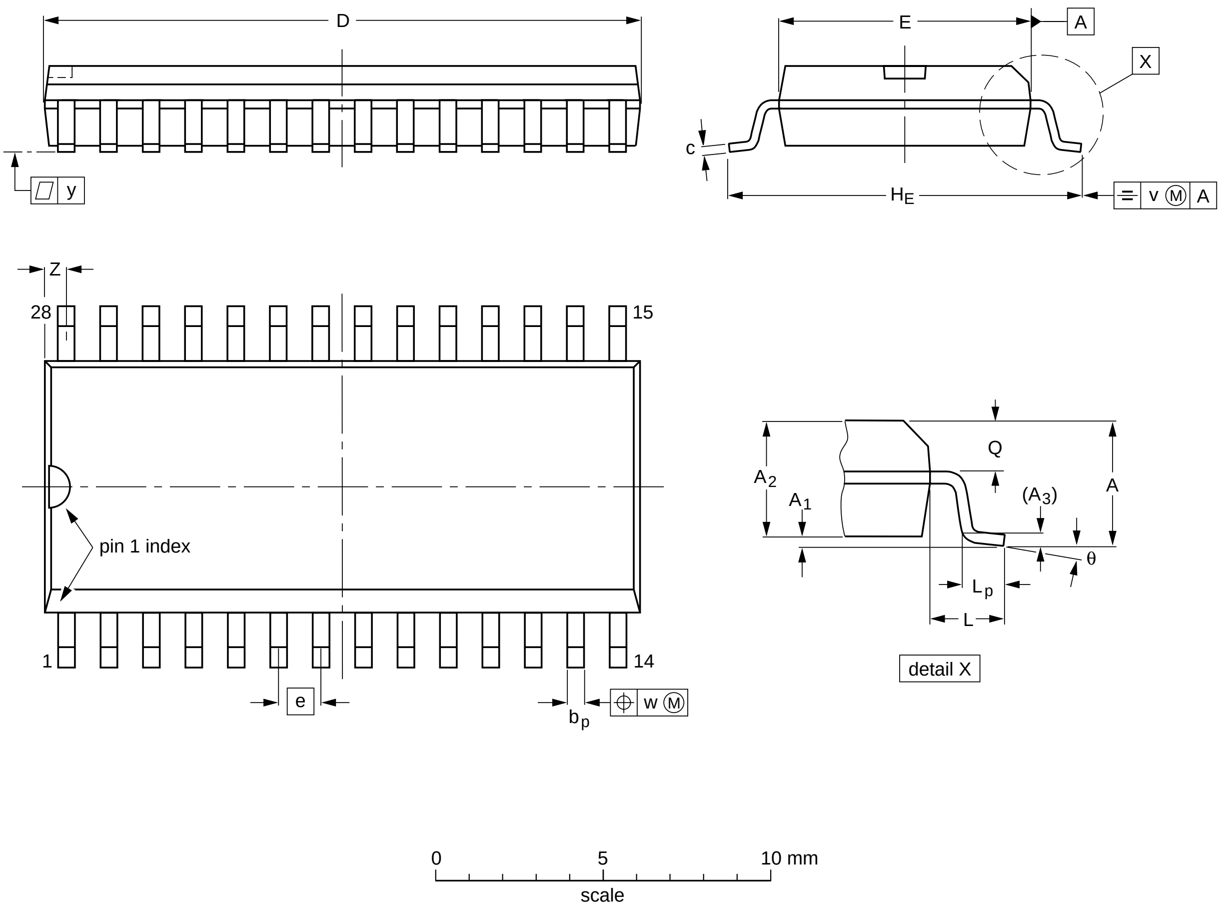
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

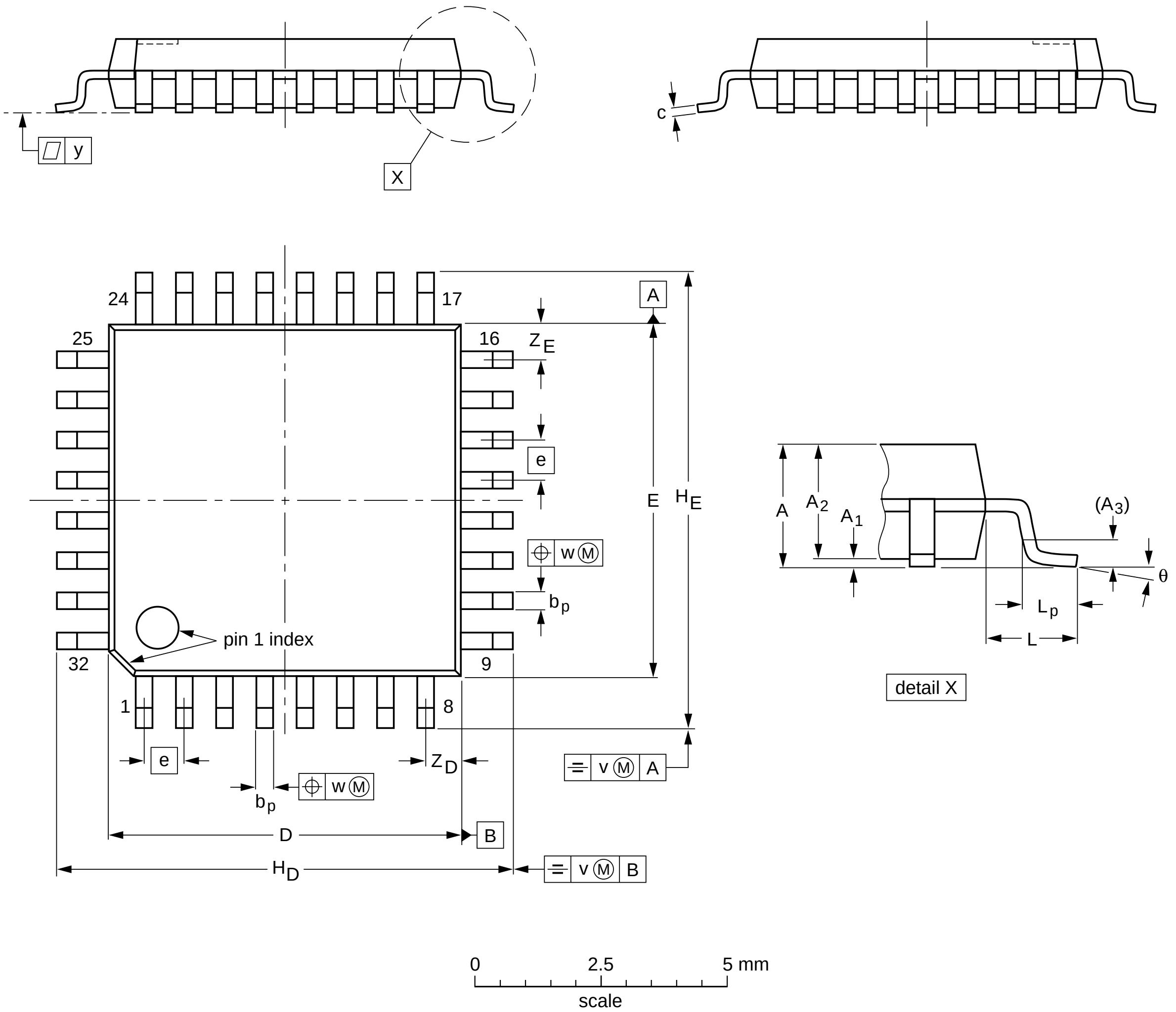
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm **SOT358-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT358 -1						~~95-12-19~~ 97-08-04

21 SOLDERING

21.1 Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“Data Handbook IC26; Integrated Circuit Packages”* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

21.2 Through-hole mount packages

21.2.1 SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

21.2.2 MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

21.3 Surface mount packages

21.3.1 REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

21.3.2 WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

21.3.3 MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

21.4 Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW[1]	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable[2]	–	suitable
Surface mount	BGA, SQFP	not suitable	suitable	–
	HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable[3]	suitable	–
	PLCC[4], SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended[4][5]	suitable	–
	SSOP, TSSOP, VSO	not recommended[6]	suitable	–

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
3. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

22 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

23 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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