PULSE AND DTMF DIALLER

GENERAL DESCRIPTION

The PCD4413A is a single-chip silicon gate CMOS integrated circuit with an on-chip oscillator for a 3,58 MHz crystal. It is a dual-standard dialling circuit for either pulse dialling (PD) or dual tone multi-frequency (DTMF) dialling.

Input data is derived from any standard matrix keyboard for dialling in either PD or DTMF mode.

In DTMF mode bursts as well as pauses are timed to a minimum, in manual dialling the maximum depends on the key depression time.

Features

- Pulse and DTMF dialling
- 23-digit memory capacity
- Three dialling modes; pulse, DTMF and data transmission (DTMF)
- Two function keys; * and FL (flash)
- DTMF timing:
  manual dialling – minimum duration for bursts and pauses
- On-chip voltage reference for supply and temperature independent tone output
- On-chip filtering for low output distortion (CEPT CS 203 compatible)
- On-chip oscillator uses low-cost 3,58 MHz (tv colour burst) crystal
- Uses standard single-contact or double-contact (common left open) keyboard
- Keyboard entries fully debounced
- Flash (register recall) output

QUICK REFERENCE DATA

Operating supply voltage	V_{DD}	2,5 to 6,0	V
Standby supply voltage	V_{DDO}	1,8 to 6,0	V
Low standby current (on hook) at V_{DDO} = 1,8 V	I_{DDO}	max. 5	μA
Operating currents			
conversation mode	I_{DDC}	max. 150	μA
pulse dialling mode	I_{DDP}	max. 200	μA
DTMF dialling mode	I_{DDF}	max. 0,9	mA
DTMF output voltage level (r.m.s. values)			
HIGH group	$V_{HG(rms)}$	typ. 192	mV
LOW group	$V_{LG(rms)}$	typ. 150	mV
Pre-emphasis of group	ΔV_G	typ. 2,1	dB
Total harmonic distortion	THD	−25	dB
Operating ambient temperature range	T_{amb}	−25 to + 70	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102G,N,PE).

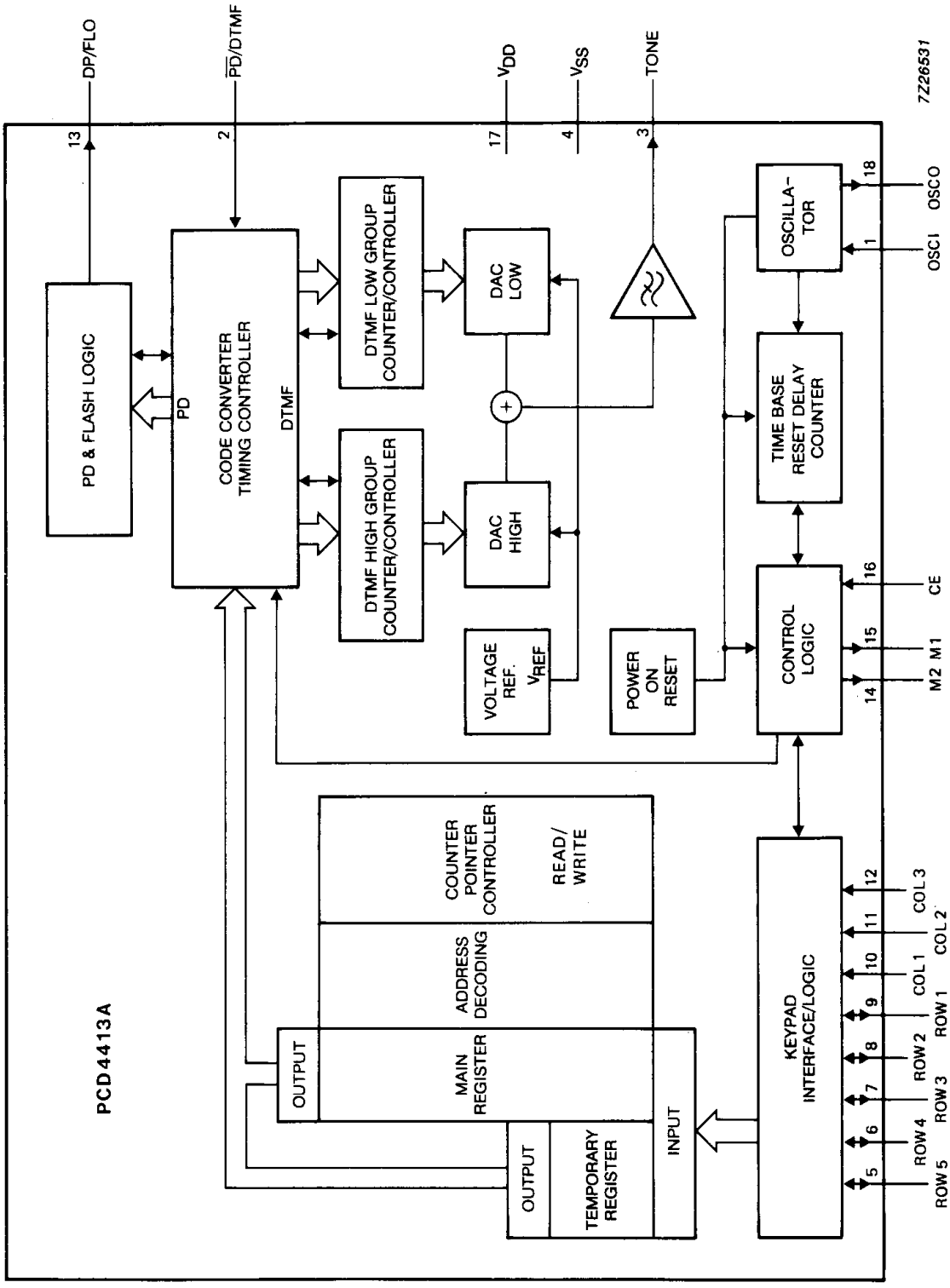


Fig. 1 Block diagram.

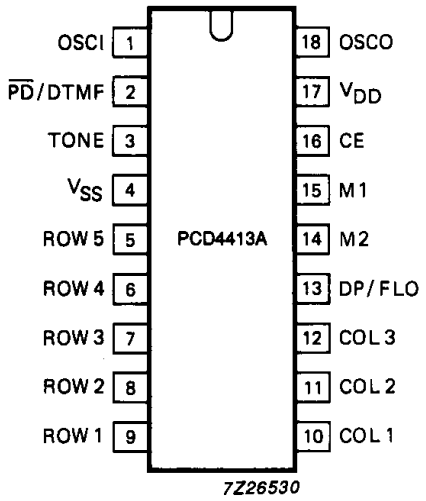


Fig. 2 Pinning diagram.

PINNING

1	OSCI	oscillator input
2	$\overline{PD}$/DTMF	select pin; pulse or DTMF dialling
3	TONE	single or dual tone frequency output
4	V_{SS}	negative supply
5	ROW 5	scanning row keyboard input/outputs
6	ROW 4	
7	ROW 3	
8	ROW 2	
9	ROW 1	
10	COL 1	sense column keyboard inputs with internal pull-ups
11	COL 2	
12	COL 3	
13	DP/FLO	dialling pulse and flash output
14	M2	strobe; active HIGH during transmission
15	M1	muting output
16	CE	chip enable input
17	V_{DD}	positive supply
18	OSCO	oscillator output

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

The positive supply of the circuit (V_{DD}) must meet the voltage requirements as indicated in the characteristics.
To avoid undefined states of the device when powered-on, an internal reset circuit clears the control logic and counters.

The power-on-reset signal has the highest priority. It blocks and resets the complete circuit without delay regardless of the state of chip enable input (CE).

Clock oscillator (OSCI, OSCO)

The time base for the PCD4413A for both PD and DTMF modes is a crystal controlled on-chip oscillator which is completed by connecting a 3,58 MHz crystal between the OSCI and OSCO pins.

Chip Enable (CE)

The CE input enables the circuit and is used to initialize the IC.

CE = LOW provides the static standby condition. In this state the clock oscillator is disabled, the keyboard input is inhibited and all registers and logic are reset with the exception of the Write Address Counter (WAC) which points to the last entered digit (see Fig. 4).
The current drawn is I_{DDO} (standby current) during hook-on.

CE = HIGH activates the clock oscillator and the circuit changes from static standby condition to the conversation mode. The current consumption is I_{DDC} until the first digit is entered from the keyboard. Then a dialling or redialling operation starts. The operating current is I_{DDP} if in the pulse dialling mode, or I_{DDF} if the DTMF dialling mode is selected.

If the CE input is taken to a LOW level for more than time t_{rd} (see Fig. 7, Fig. 8 and timing data) the system changes to the static standby state and the oscillator stops running. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit and reset pulses are not produced.

Mode selection ($\overline{PD}$/DTMF)

DTMF mode

If $\overline{PD}$/DTMF = V_{DD} the dual tone multi-frequency dialling mode is selected. Each pushbutton activated corresponds to a combination of two tones, each one out of four possible LOW and HIGH group frequencies. The frequencies are transmitted with a constant amplitude, regardless of power supply variations, and filtered off harmonic content to fulfil the CEPT CS 203 recommendations.

The duration of bursts and pauses is the actual pushbutton depress time, but not less than the minimum transmission time (t_t) or minimum pause time (t_p).

PD/Data transmission mode

If PD/DTMF = V_{SS} the pulse-data mode is selected. Starting with numeric keys digits will be dialled out in pulse dialling mode, until key * is depressed which selects the data transmission mode (the * tone is not transmitted). All keys (including * and #) will now be transmitted in DTMF tones.

There are two ways to leave the data transmission mode:

- Reactivate chip enable (CE); HIGH to LOW then HIGH again
- Pressing the flash (FL) key

Keyboard inputs/outputs

The sense column inputs COL 1 to COL 3 and the scanning row outputs ROW 1 to ROW 5 of the PCD4413A are directly connected to the keyboard as shown in Fig. 3.
All keyboard entries are debounced on both the leading and trailing edges for approximately time t_e as shown in Fig. 7, 8 and 9. Each entry is tested for validity.

When a pushbutton is pressed, keyboard scanning starts and only returns to the sense mode after release of the pushbutton.

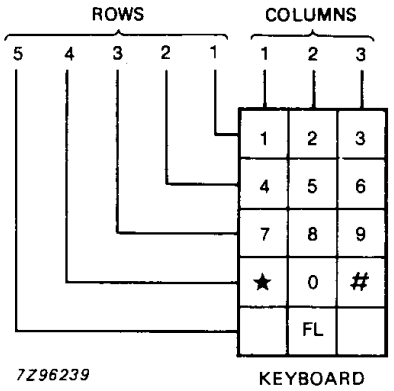


Fig. 3 Keyboard organization.

Row 5 of the keyboard contains the special function key FL — flash or register recall.

Flash

Flash (or register recall) is activated by the FL key and can be used in DTMF, pulse and data transmission modes. Pressing the FL pushbutton will produce a timed line-break of t_{FL} at the DP/FLO output. During the conversation mode this flash pulse entry will act as a chip enable.

The flash pulse resets the read address counter (RAC).

TONE output (DTMF mode)

The single and dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an on-chip active RC low-pass filter.

Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 1 shows the frequency tolerance of the output tones for DTMF signalling.

FUNCTIONAL DESCRIPTION (continued)

Table 1 Frequency tolerance of the output tones for DTMF signalling

row/ column	standard frequency Hz	tone output frequency Hz (1)	frequency deviation	
			%	Hz
row 1	697	697,90	+0,13	+0,90
row 2	770	770,46	+0,06	+0,46
row 3	852	850,45	−0,18	−1,55
row 4	941	943,23	+0,24	+2,23
col 1	1209	1206,45	−0,21	−2,55
col 2	1336	1341,66	+0,42	+5,66
col 3	1477	1482,21	+0,35	+5,21

(1) Tone output frequency when using a 3,579 545 MHz crystal.

When the DTMF mode is selected output tones are timed in manual dialling with a minimum duration of bursts and pauses, and in redial with a calibrated timing. Single tones may be generated for test purposes (CE = HIGH). Each row and column has one corresponding frequency. High group frequencies are generated by connecting the column to V_{SS}. Low group frequencies are generated by forcing the row to V_{DD}. The single tone frequency will be transmitted during activation time, but it is neither calibrated nor stored.

Dial pulse and flash output (DP/FLO)

This is a combined output which provides control signals for proper timing in pulse dialling or for a calibrated break in both dialling modes (flash or register recall).

Mute output (M1)

During pulse dialling the mute output becomes active HIGH for the period of the inter-digit pause, break time and make time. It remains at this level until the last digit is pulsed out.

During DTMF dialling the mute output stays HIGH for the period of the transmit and pause time. During Flash the mute output is active HIGH and remains at this level for the period of flash and flash hold-over time.

Mute output ($\overline{M1}$)

Inverted output of M1. In the PCD4413A it is only available as a bonding option of M1.

Strobe output (M2)

Active HIGH output during actual dialling; i.e. during break and make time in pulse dialling, or during tone transmission in DTMF dialling.

Data transmission mode

Timing in the data transmission mode is the same as the manual dialling mode.

DIALLING PROCEDURES (see also Figs 5 and 6)

Dialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address (see Fig. 4). By entering first a numeric digit, the Write Address Counter (WAC) will be set to the first address, the decoded digit will be stored in the register and the WAC incremented to the next address. Any subsequent keyboard entry will be decoded and stored in the main register after validation. All entries are debounced on both the leading and trailing edges for at least time t_e as shown in Figs 7, 8 and 9. Each entry is tested for validity before being deposited in the main register.

In pulse dialling mode only the 0 to 9 keys result in dialling operations.

* is a special function key:

** key*

- Used to switch from dialling mode to data transmission mode. The * tones will not be transmitted.

In DTMF and data transmission mode keys 0 to 9, * and # result in associated DTMF tones (see Table 1).

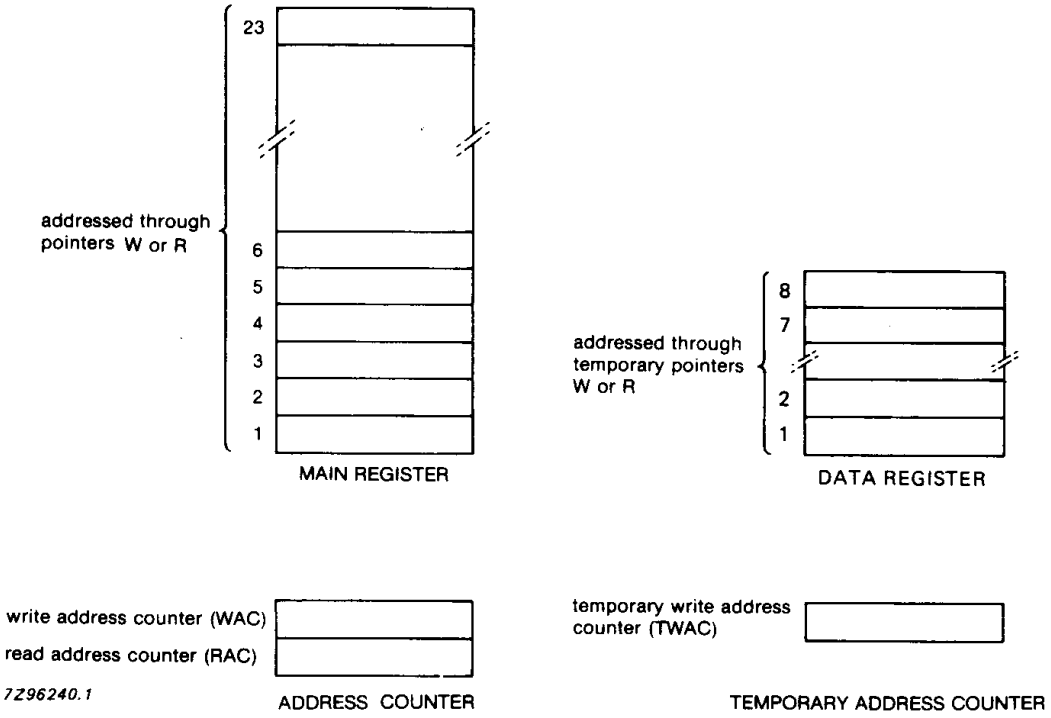


Fig. 4 Memory organization.

DIALLING PROCEDURES (continued)

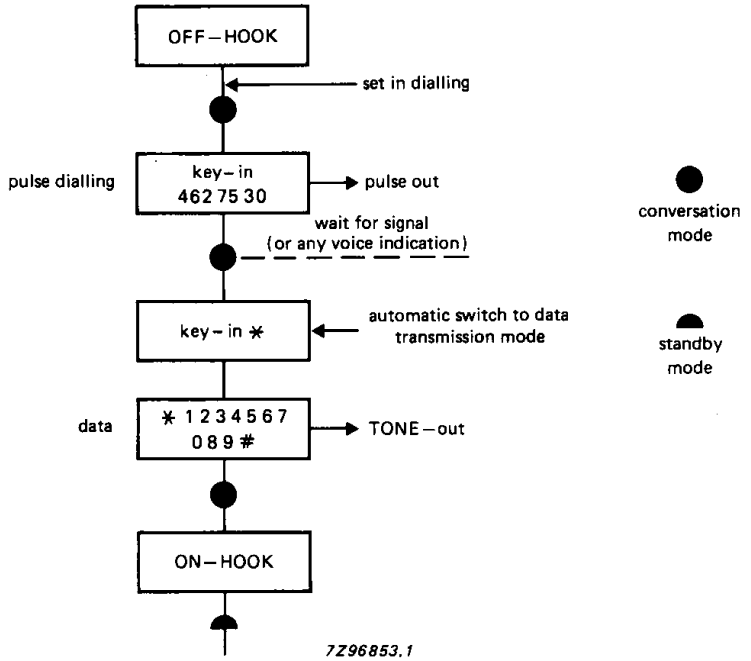


Fig. 5 Pulse and data transmission mode.

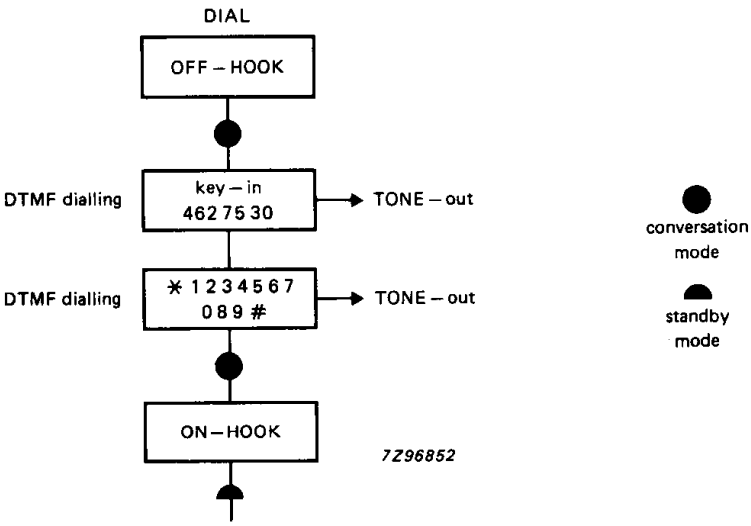


Fig. 6 DTMF mode.

TIMING

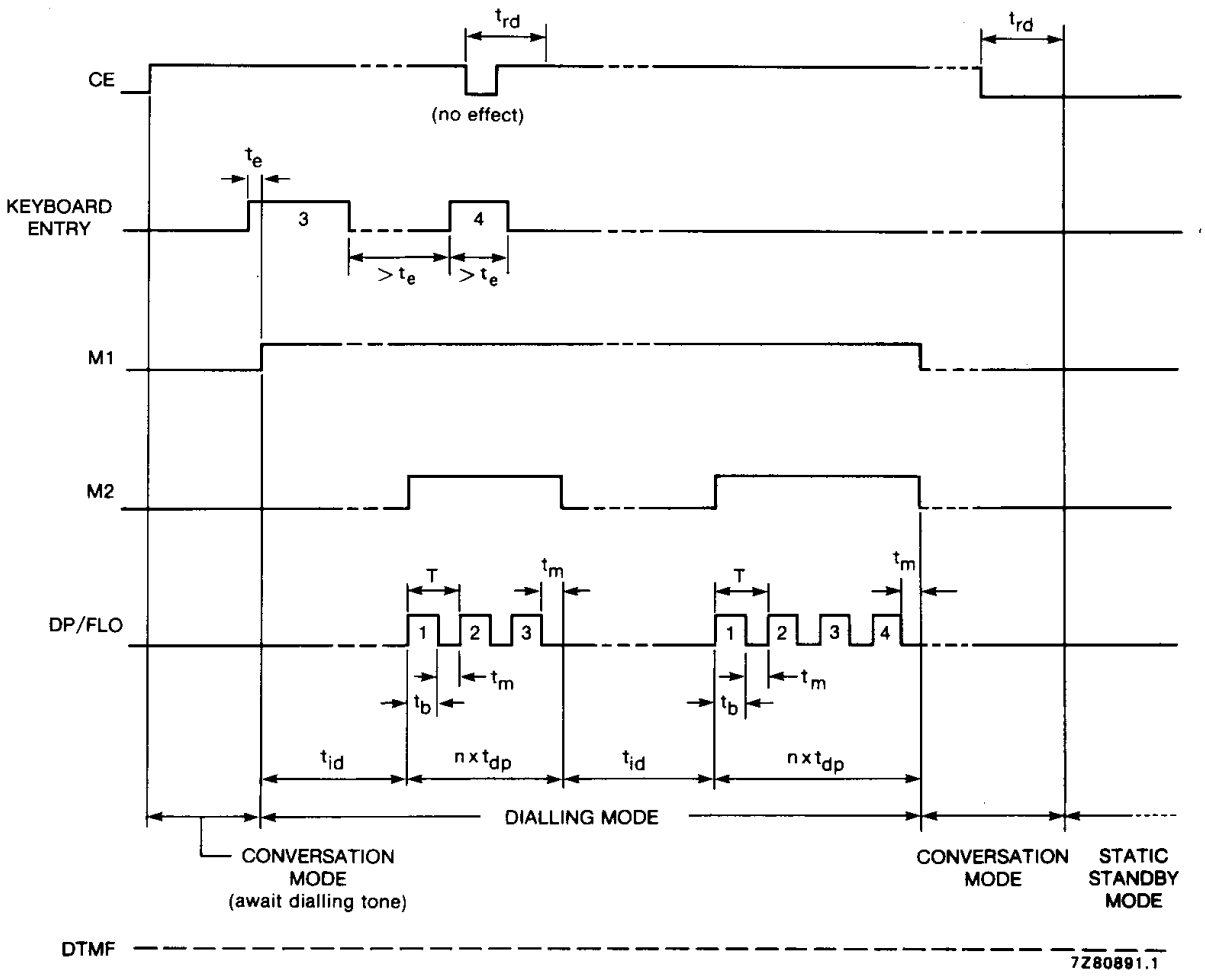


Fig. 7 Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; pulse dialling ($\overline{PD}$/DTMF = V_{SS}).

DEVELOPMENT DATA

TIMING (continued)

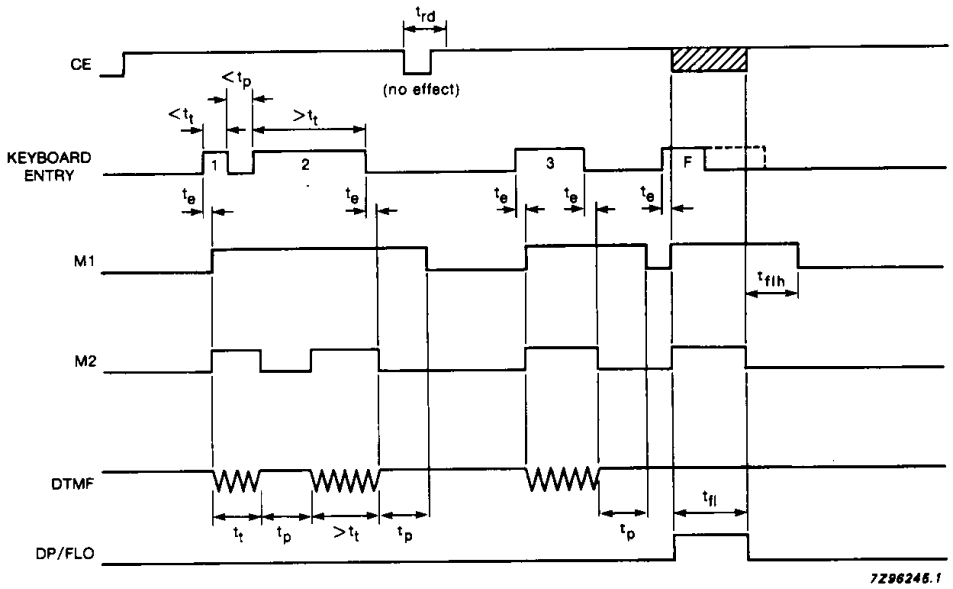


Fig. 8 Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; DTMF dialling ($\overline{PD}$/DTMF = V_{DD}).

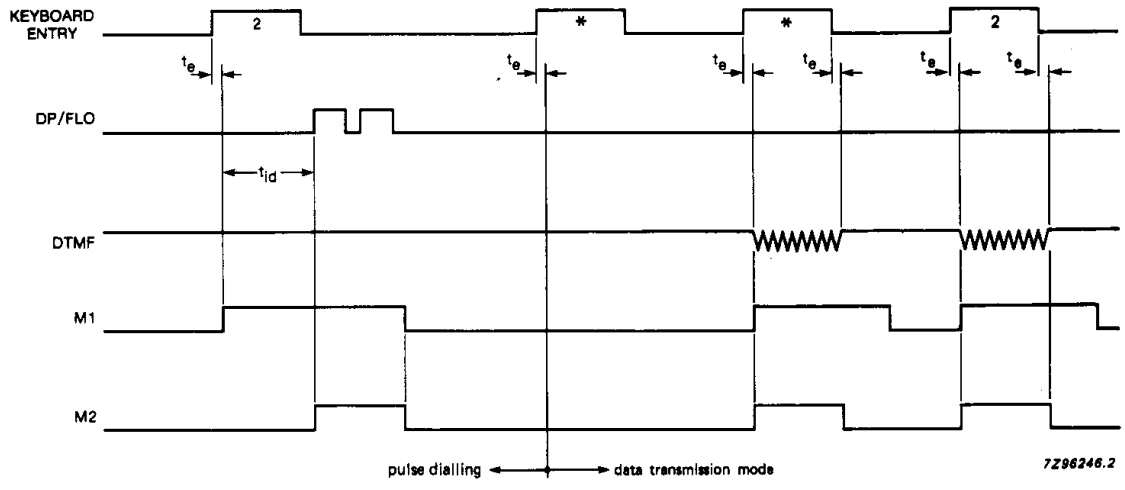


Fig. 9 Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; pulse dialling and data transmission mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,8 to 8	V
Supply current	I_{DD}	max.	50	mA
DC current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
All input voltages	V_I		−0,8 V to V_{DD} + 0,8	V
Total power dissipation	P_{tot}	max.	300	mW
Power dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579545 MHz; R_S = 100 Ω max.; T_{amb} = −25 to + 70 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Standby supply voltage	V_{DDO}	1,8	–	6,0	V
Operating supply current					
conversation mode (oscillator ON)	I_{DDC}	–	–	150	μA
pulse dialling or flash	I_{DDP}	–	–	200	μA
DTMF dialling (tone ON)	I_{DDF}	–	–	0,9	mA
DTMF dialling (tone OFF)	I_{DDF}	–	–	200	μA
Standby supply current (oscillator OFF; note 1) at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DDO}	–	–	5	μA
INPUTS					
Input voltage LOW (any pin)	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH (any pin)	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current; CE	$\lvert I_{IL}\rvert$	–	–	1	μA
Keyboard inputs					
Keyboard ON resistance	R_{KON}	–	–	2	kΩ
Keyboard OFF resistance	R_{KOFF}	1	–	–	MΩ
OUTPUTS					
Output sink current at $V_{OL} = V_{SS} + 0{,}5$ V					
M1, M2, DP/FLO	I_{OL}	0,7	–	–	mA
Output source current at $V_{OH} = V_{DD} - 0{,}5$ V					
M1, M2, DP/FLO	$-I_{OH}$	0,6	–	–	mA
TIMING AND FREQUENCY					
Clock start-up time	t_{on}	–	4	–	ms
Debounce time	t_e	–	12	–	ms
Reset delay time	t_{rd}	152	160	168	ms

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 10) at V_{DD} = 2,5 to 6 V					
DTMF output voltage levels (r.m.s. value)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Frequency deviation	$\Delta f/f$	−0,6	–	+ 0,6	%
DC voltage level	V_{DC}	–	$\frac{1}{2}V_{DD}$	–	V
Output impedance	$\lvert Z_O \rvert$	–	0,1	0,5	kΩ
Load resistance	R_L	10	–	–	kΩ
Pre-emphasis of group	ΔV_G	1,85	2,1	2,35	dB
Total harmonic distortion at T_{amb} = 25 °C (note 2)	THD	–	−25	–	dB
Transmission and pause time					
Manual and data transmission dialling mode	t_t	65	–	–	ms
	t_p	65	–	–	ms
Flash pulse duration	t_{FL}	252	254	256	ms
Flash hold-over time	t_{flh}	30	32	34	ms
Pulse dialling (PD)					
Dialling pulse frequency	f_{dp}	9,8	10	10,4	Hz
Inter-digit pause	t_{id}	800	840	880	ms
Break time (note 3)	t_b	58	60	62	ms
Make time (note 3)	t_m	38	40	42	ms

DEVELOPMENT DATA

Notes to the characteristics

1. Crystal connected between OSCI and OSCO; CE at V_{SS} and all other pins open-circuit.
2. Related to the level of the LOW group frequency component (CEPT CS 203).
3. Mark-to-space ratio 3 : 2.

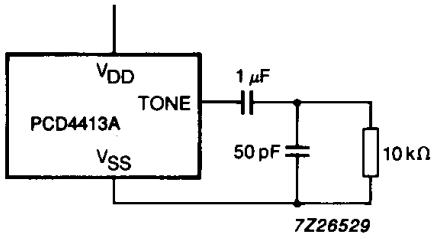
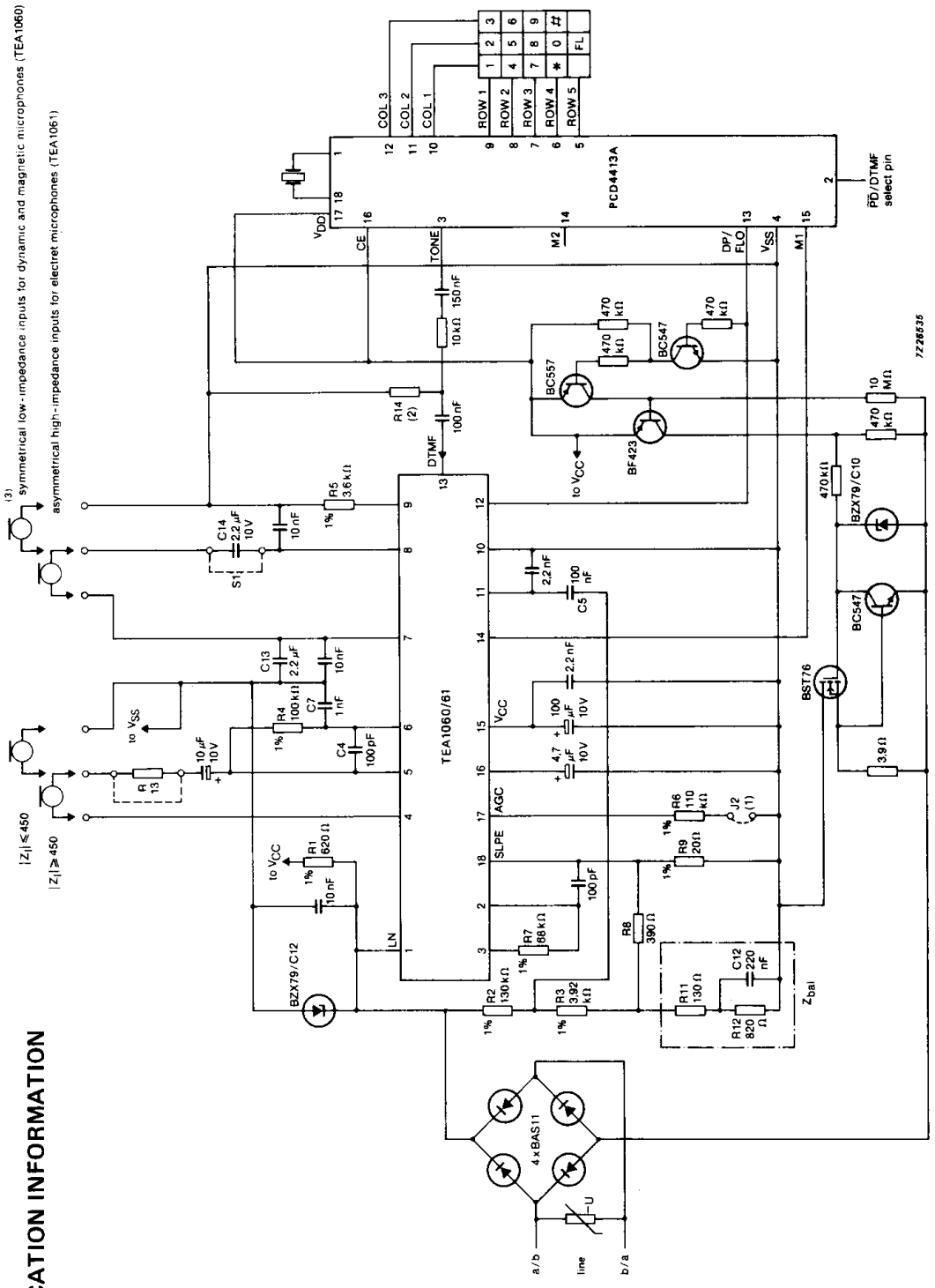


Fig. 10 Tone output test circuit.

APPLICATION INFORMATION



(1) Automatic line compensation obtained by connecting R6 to V_{SS}.
(2) The value of resistor R14 is determined by the required level at LN and the DTMF gain of the TEA1060/61.
(3) Omit C13 and C14; insert S1.

Fig. 11 Application diagram of the full electronic basic telephone set.