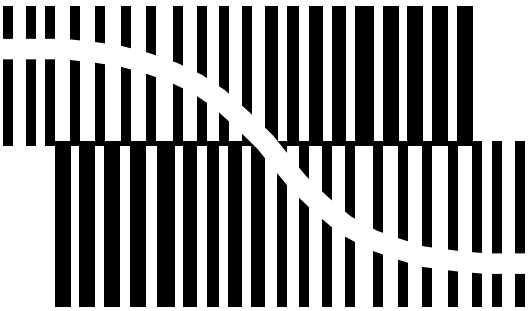
DATA SHEET



PCD5032
ADPCM CODEC for digital cordless telephones

Product specification
Supersedes data of August 1993
File under Integrated Circuits, IC17

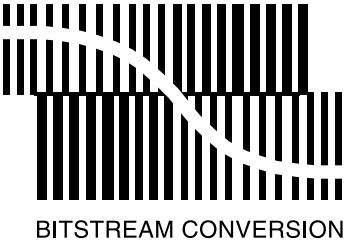
1997 Apr 03

Philips
Semiconductors

PHILIPS

ADPCM CODEC for digital cordless telephones

PCD5032



CONTENTS

ADPCM CODEC for digital cordless telephones

PCD5032

1 FEATURES

- G.721 compliant ADPCM encoding and decoding
- 'Bitstream' analog-to-digital and digital-to-analog conversion
- On-chip receive and transmit filter
- On-chip ringer and tone generator
- Programmable gain of receive and transmit path
- Serial ADPCM interface with independent timing for maximum flexibility
- Linear PCM data accessible for digital echo cancelling
- Programmable via I^2C-bus interface
- Fast receiver mute input via pin
- On-chip reference voltage
- On-chip symmetrical supply for electret microphone
- Few external components
- Low power consumption in standby mode
- Low supply voltage (single supply 2.7 V up to 5.5 V)
- CMOS technology
- Minimized EMC on digital outputs.

2 APPLICATIONS

- Digital Enhanced Cordless Telephony (DECT)
- CT2 cordless
- Speech compression.

3 GENERAL DESCRIPTION

The PCD5032 is a CMOS device designed for use in Digital Enhanced Cordless Telephone systems (DECT), but also suitable for other cordless telephony applications such as CT2. The PCD5032 performs analog-to-digital and digital-to-analog conversion, ADPCM encoding and decoding compliant to CCITT recommendation *"G.721 (blue book, 1988)*". The PCD5032 contains on-chip microphone and earpiece amplifiers. The device can be used in both handset and base station designs.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5032H	QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body $14 \times 14 \times 2.2$ mm	SOT205-1
PCD5032T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

5 BLOCK DIAGRAM

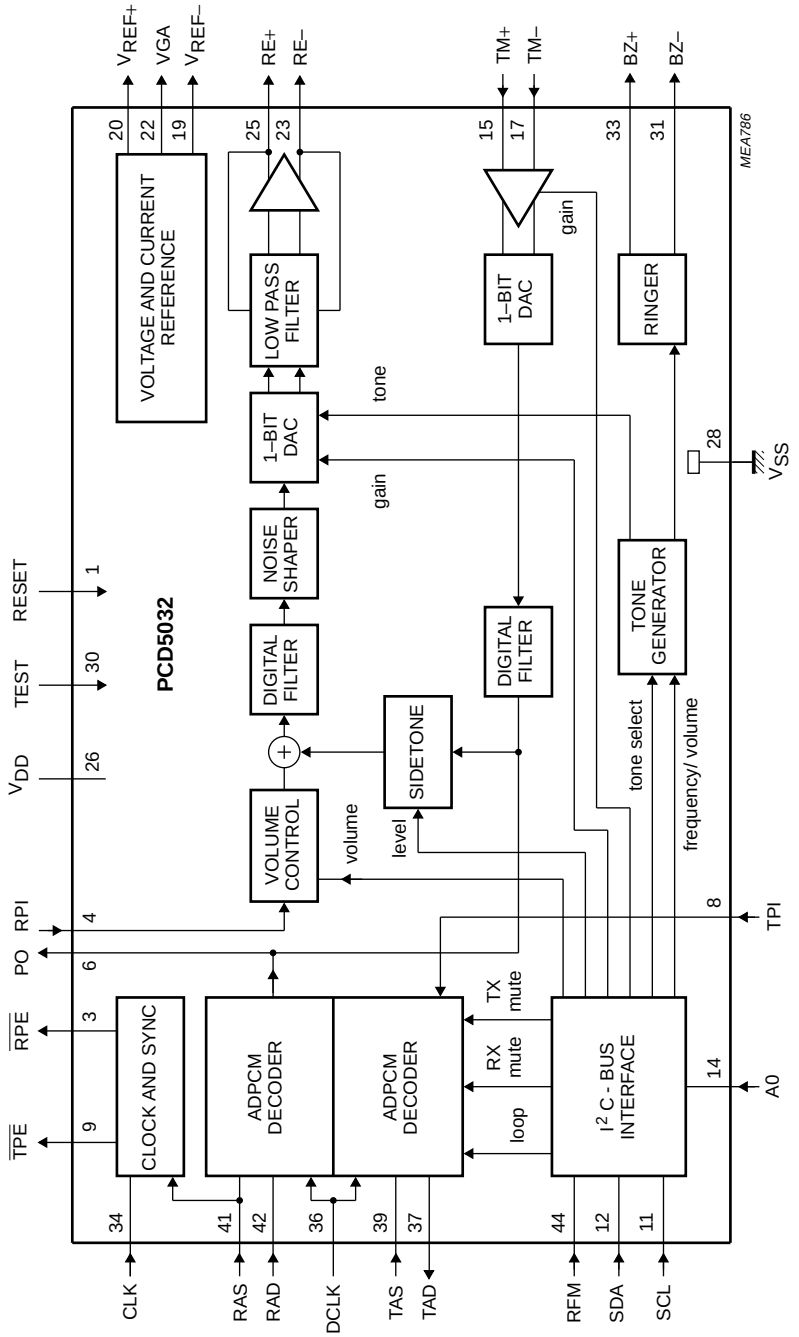


Fig.1 Block diagram (pin numbers are for QFP44 package).

6 PINNING

SYMBOL	PIN(1)(2)		TYPE	DESCRIPTION
	QFP44	SO28		
RESET	1	4	I	reset input; active HIGH
n.c.	2	–	–	not connected
$\overline{RPE}$	3	5	O	receiver PCM output enable (active LOW); direction from ADPCM interface to earpiece
RPI	4	6	I	receiver PCM input; direction from ADPCM interface to earpiece
n.c.	5	–	–	not connected
PO	6	7	O	PCM data output
n.c.	7	–	–	not connected
TPI	8	8	I	transmitter PCM input; direction from microphone to ADPCM interface
$\overline{TPE}$	9	9	O	transmitter PCM output enable (active LOW); direction from microphone to ADPCM interface
n.c.	10	–	–	not connected
SCL	11	10	I	serial clock input; I^2C-bus
SDA	12	11	I	serial data input; I^2C-bus
n.c.	13	–	–	not connected
A0	14	12	I	address select input; I^2C-bus
TM+	15	13	I	transmitter audio positive input (microphone)
n.c.	16	–	–	not connected
TM–	17	14	I	transmitter audio negative input (microphone)
n.c.	18	–	–	not connected
V_{REF-}	19	15	O	negative reference voltage output; internally generated, intended for electret microphone supply
V_{REF+}	20	16	O	positive reference voltage output; internally generated, intended for electret microphone supply
n.c.	21	–	–	not connected
VGA	22	17	O	analog signal ground output
RE–	23	18	O	receiver audio negative output (earpiece)
n.c.	24	–	–	not connected
RE+	25	19	O	receiver audio positive output (earpiece)
V_{DD}	26	20	P	positive supply voltage (2.7 V to 5.5 V)
n.c.	27	–	–	not connected
V_{SS}	28	21	P	negative supply voltage (0 V)
n.c.	29	–	–	not connected
TEST	30	22	I	test mode input; to be connected to V_{SS} in normal application
BZ–	31	23	O	ringer negative output
n.c.	32	–	–	not connected
BZ+	33	24	O	ringer positive output
CLK	34	25	I	clock input
n.c.	35	–	–	not connected

SYMBOL	PIN(1)(2)		TYPE	DESCRIPTION
	QFP44	SO28		
DCLK	36	26	I	data clock input (ADPCM)
TAD	37	27	O	transmitter ADPCM data output; direction from microphone to ADPCM interface
n.c.	38	–	–	not connected
TAS	39	28	I	transmitter ADPCM sync input; direction from microphone to ADPCM interface
n.c.	40	–	–	not connected
RAS	41	1	I	receiver ADPCM sync input; direction from ADPCM interface to earpiece
RAD	42	2	I	receiver ADPCM data input; direction from ADPCM interface to earpiece
n.c.	43	–	–	not connected
RFM	44	3	I	receiver fast mute input; direction from ADPCM interface to earpiece

Notes

1. QFP44 package:
   Pins 1, 3, 4, 6, 8, 9, 11, 12, 14, 30, 34, 36, 37, 39, 41, 42 and 44 are digital pins.
   Pins 15, 17, 23, 25, 31 and 33 are analog pins.
   Pins 19, 20, 22, 26, and 28 are general pins.
2. SO28 package:
   Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 22, 25, 26, 27 and 28 are digital pins.
   Pins 13, 14, 18, 19, 23 and 24 are analog pins.
   Pins 15, 16, 17, 20 and 21 are general pins.

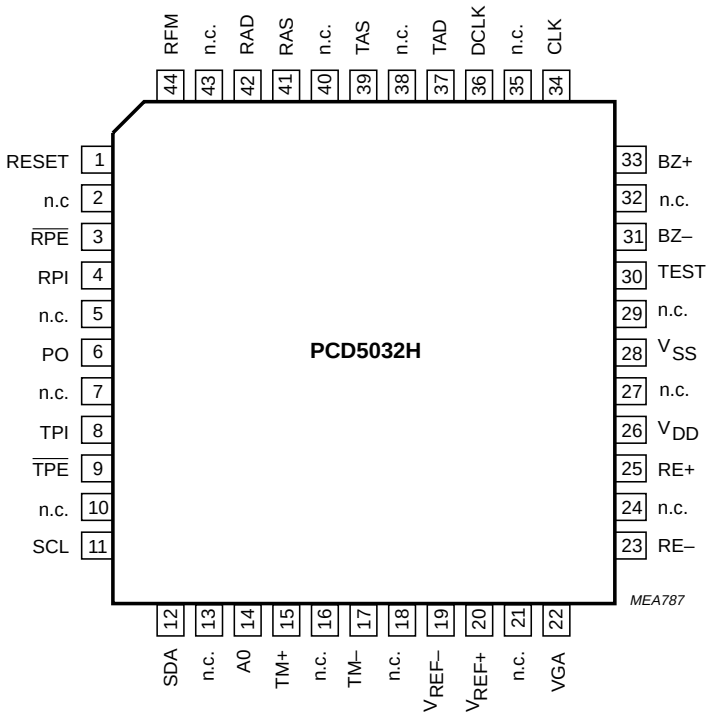


Fig.2 Pin configuration QFP44 (SOT205-1).

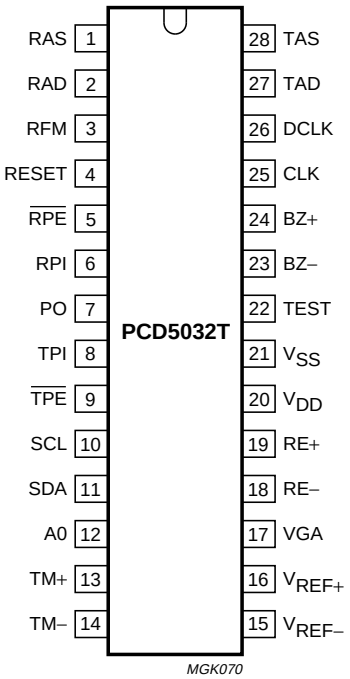


Fig.3 Pin configuration SO28 (SOT136-1).

7 FUNCTIONAL DESCRIPTION

7.1 Digital interfaces

7.1.1 ADPCM INTERFACE

The ADPCM receive and transmit data pins, RAD and TAD, carry 4-bit words of serial data. The received and transmitted data are controlled separately by the synchronization pins RAS and TAS.

On detection of a HIGH level on RAS (with a rising edge on DCLK), the receiver will read 4 ADPCM bits on the next 4 HIGH-to-LOW transitions of DCLK. Likewise, on reception of a HIGH level on TAS, the transmitter will output 4 ADPCM bits on the next 4 LOW-to-HIGH transitions of DCLK. Figure 4 is the ADPCM timing diagram. During the time that the ADPCM data output (TAD) is not activated, it will be in a high-impedance state, enabling a bus structure to be used in a multi-line base station. Input RAD has an internal pull-down resistor.

The minimum frequency on the DCLK input is $\frac{1}{54}f_{CLK}$. The maximum value equals the clock frequency, and any value in between may be chosen. The RAS signal controls the start of each conversion in a frame at an 8 kHz rate. The master clock 'CLK' must be locked to the frequency of 'RAS', with a ratio $f_{CLK} = 432 \times f_{RAS}$.

7.1.2 PCM INTERFACE

To enable additional data processing in a base station both transmit and receive linear PCM data paths are accessible.

For the receive direction the PCM data is output on pin PO and read from pin RPI. For the transmit direction the PCM data is output on pin PO and read from pin TPI. To enable bus structures to be used in base stations the PCM output PO is in high-impedance state when not active. Inputs TPI and RPI have internal pull-down.

In a typical handset application, pin PO is directly connected to RPI and TPI. If additional data processing is required (echo cancellation in a base station, for example), a data processing unit may be placed between PO and RPI or between PO and TPI.

The data format is serial, 2's complement, MSB first. PO outputs 16 bits (14 data bits followed by 2 zeroes). TPI and RPI read 14 data bits. The bit frequency is 3456 kHz (CLK). Data output PO changes on the falling edge of CLK (see Figs. 5 and 6).

For interfacing to digital signal processors, signals $\overline{\text{TPE}}$ and $\overline{\text{RPE}}$ (both active LOW) mark the position of the transmit and receive PCM data on pin PO (see Fig.7). $\overline{\text{TPE}}$ and $\overline{\text{RPE}}$ change on the rising edge of CLK.

Outputs $\overline{\text{RPE}}$ and $\overline{\text{TPE}}$ have low impedance only from half a CLK cycle after the active state. The rest of the time they are in high impedance state. Thus a wired-OR configuration can be made when only one DSP serial input port is used for reading both transmit and receive data. An external pull-up is required.

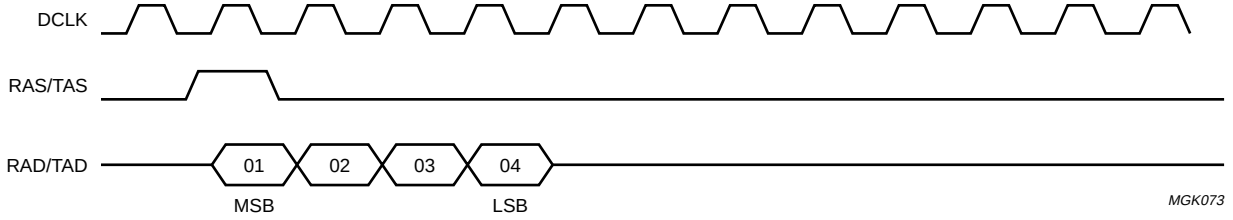


Fig.4 ADPCM timing.

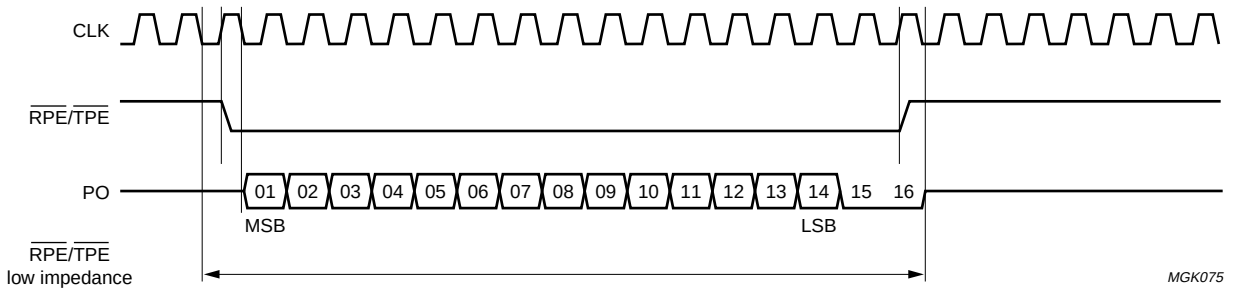


Fig.5 PCM output timing.

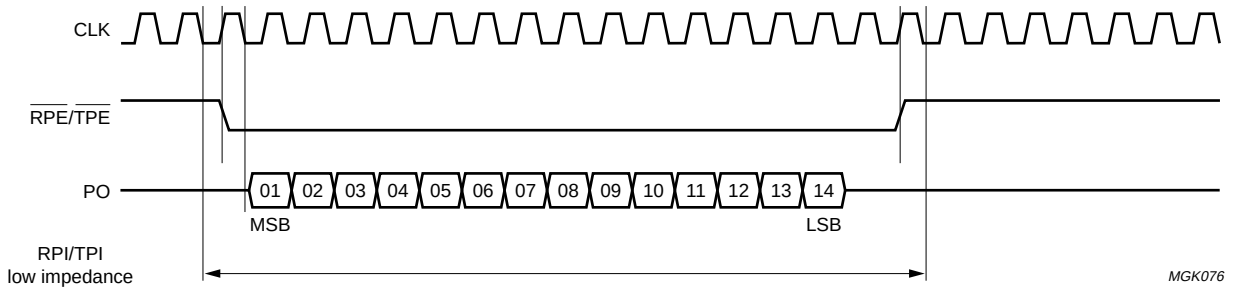


Fig.6 PCM input timing.

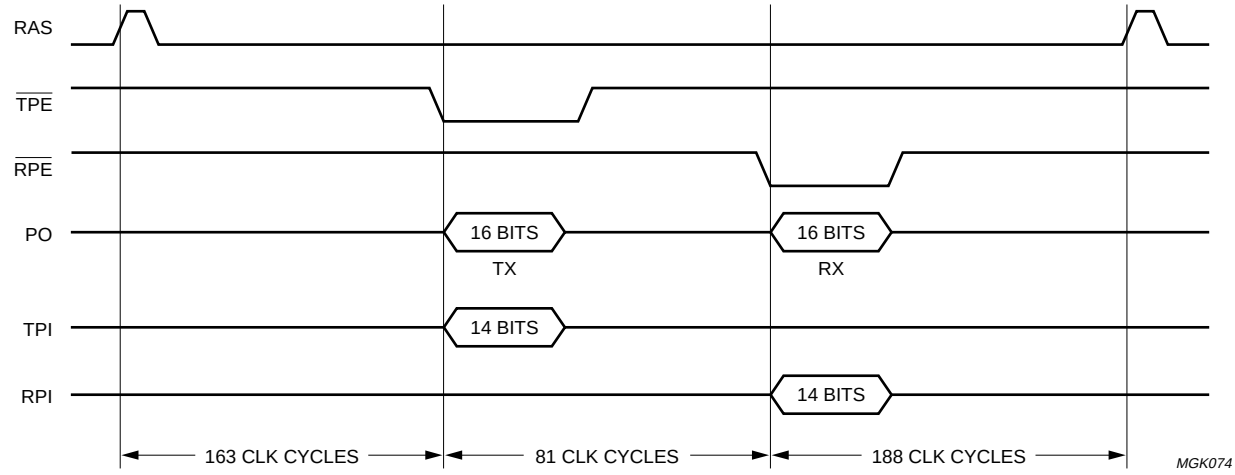


Fig.7 PCM timing.

7.1.3 I²C-BUS INTERFACE

The mode of operation and transmitter/receiver gain is programmed through the I²C-bus serial interface. The I²C-bus address of the device is shown in Fig.8.

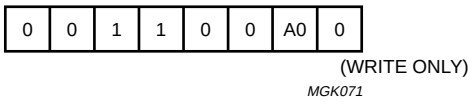


Fig.8 I²C-bus address.

With the address select pin A0 it is possible to have two independently programmed PCD5032 CODECs in a base station (two outside lines). If more CODECs are used in a base station then the address pin can be used as a select signal. Detailed description of the I²C-bus specification is given in the brochure *"The I²C-bus and how to use it"*. This may be ordered using the code 9398 393 40011.

Each function can be accessed by writing one 8-bit word to the ADPCM CODEC. For this reason the 8-bit word is divided into two fields:

- bit 7, bit 6: function
- bit 5 to bit 0: value/setting.

Table 1 gives an overview of the I²C-bus programming options.

Table 1 Overview of I²C-bus programming options

FUNCTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Operation mode	0	0	–	–	TONE	PON	T1	T0
Receiver control	0	1	RV2	RV1	RV0	RG2	RG1	RG0
Transmitter control	1	0	ST1	ST0	MUTE	TG2	TG1	TG0
Ringer	1	1	BF2	BF1	BF0	BV2	BV1	BV0

Table 1 definitions:

- **TONE**: 'tone/ringer' section for tone generator output; tones can be sent to ringer or receiver DAC
- **PON**: power-on (active)
- **T1 and T0**: test loops
- **RG2 to RG0**: receiver gain
- **TG2 to TG0**: transmitter gain
- **RV2 to RV0**: receiver volume
- **BV2 to BV0**: tone volume
- **BF2 to BF0**: tone frequency
- **ST1 to ST0**: sidetone level.

Programming the ADPCM CODEC is possible in active mode as well as in standby mode. A reset clears all I²C-bus registers.

7.1.4 FAST MUTE

The RFM (Receiver Fast Mute) pin enables fast muting of the received signal if erroneous data is present on the ADPCM interface.

Muting is done in the same way as the receiver mute via the I²C-bus. The input data of the ADPCM decoder is blanked, so that the ADPCM decoder output signal goes to zero. To ensure immediate silence on the analog outputs RE+ and RE–, the linear PCM input data of the receive filter is set to zero as well.

If the mute signal is switched off again, then the ADPCM decoder output settles gradually from the zero to the appropriate PCM signal level. No audible clicks will occur.

The sidetone level is not affected by the mute function.

7.2 Analog parts and I²C-bus programming

7.2.1 INPUT AND OUTPUT

The analog input pins TM+ and TM– can be connected directly to a microphone. For electret microphones capacitive coupling is required (see Chapter 12, Fig.13). The earpiece must be a low-ohmic device (>100 Ω differential).

The microphone and earpiece amplifiers have the possibility of gain control via the I²C-bus interface. Further the sending and receiving direction can be muted separately. Analog gain control for the receive path can be set in steps of 1 dB. Digital volume control can be set in 6 dB steps. Table 2 gives an overview of the gain control options.

Table 2 Overview of gain control options

FUNCTION	I²C-CODE	GAIN	NOTE
Receiver gain (relative)	01XXX101	–3 dB	
	01XXX110	–2 dB	
	01XXX111	–1 dB	
	01XXX000	0 dB	default
	01XXX001	+1 dB	
	01XXX010	+2 dB	
	01XXX011	+3 dB	
	01XXX100	+4 dB	
Receiver volume	01000XXX	0 dB	default
	01001XXX	–6 dB	
	01010XXX	–12 dB	
	01011XXX	–18 dB	
	01100XXX	–24 dB	
	01101XXX	–30 dB	
	01110XXX	–36 dB	
	01111XXX	RX MUTE	
Transmitter gain (relative)	10XXX101	–3 dB	
	10XXX110	–2 dB	
	10XXX111	–1 dB	
	10XXX000	0 dB	default
	10XXX001	+1 dB	
	10XXX010	+2 dB	
	10XXX011	+3 dB	
	10XXX100	+4 dB	
Transmitter mute	10XX1XXX	TX MUTE	default OFF

7.2.2 SIDETONE

With the I²C-bus interface the (local) sidetone level can be set to –12, –18, –24 dB, or switched off. See Table 3. The sidetone level is independent of the receiver volume control setting.

7.2.3 TONE GENERATOR AND RINGER

The PCD5032 contains a programmable tone generator which can be used for generating ringer tones (BZ+, BZ–) or local information tones in the receive path (RE+, RE–).

By setting the TONE bit (bit 3) in the operation mode register, the tone output will be directed to the receiver DAC, otherwise the tones will be sent to the ringer output stage. Table 4 shows the possible frequency and volume settings.

Table 3 Sidetone level options

FUNCTION	I²C-CODE	OPTION	NOTE
Sidetone	1000XXXX	No local sidetone	default
	1001XXXX	Level = –12 dB	
	1010XXXX	Level = –18 dB	
	1011XXXX	Level = –24 dB	

Table 4 Tone output frequency/volume options

FUNCTION	I²C-CODE	OPTION	NOTE
Volume (relative)	11XXX000	Signal off	default
	11XXX001	–29 dB	sinewave
	11XXX010	–23 dB	sinewave
	11XXX011	–17 dB	sinewave
	11XXX100	–11 dB	sinewave
	11XXX101	–5 dB	sinewave
	11XXX110	–0 dB	sinewave
	11XXX111	+4 dB	squarewave
Frequency	11000XXX	400 Hz	
	11001XXX	421 Hz	
	11010XXX	444 Hz	
	11011XXX	800 Hz	
	11100XXX	1000 Hz	
	11101XXX	1067 Hz	
	11110XXX	1333 Hz	
	11111XXX	2000 Hz	

The ringer output (BZ) is differential and is intended for low-ohmic devices. If the ringer is switched off then both outputs are low. The output signal is a pulse density modulated block wave (on a 32 kHz basic pulse rate) to generate a sinewave-like output signal, see Fig.9. Volume is controlled by changing the pulse width of each pulse. In the square wave mode a full square wave is generated and results in the maximum volume. The volume settings (in dB) are given for the first harmonic signal component.

7.3 Modes of operation

The ADPCM CODEC has a ‘Standby mode’, an ‘Active mode’ and three operating modes: ‘Normal mode’ and two loop modes. Table 5 gives details of setting the various modes via the I²C-bus.

7.3.1 STANDBY MODE

After a reset the ADPCM CODEC will by default be in standby mode. All I²C-bus settings will be cleared. Standby mode can also be explicitly set using the code shown in Table 5.

In standby mode all circuits are switched off, except for the I²C-bus interface. Before going to standby mode the PCD5032 performs a reset of the ADPCM transcoder, digital filters and auxiliary logic functions. The I²C-bus interface registers are not cleared.

7.3.2 ACTIVE MODE

Active mode is set using the code shown in Table 5. Once active mode has been set, the ADPCM CODEC is by default in normal mode, but can explicitly be set to one of the two test loops or back to normal mode using the codes shown in Table 5.

7.3.3 TEST LOOPS

Both test loops can be used for test or evaluation purposes.

Loop 1 is intended for testing the audio path and A/D, D/A converters, the ADPCM transcoder is not addressed in this mode. The ADPCM data is directly looped back towards the radio interface.

The PCM data is looped from transmit filter output to receive filter input.

Loop 2 is intended for testing the audio path including ADPCM encoding and decoding.

7.3.4 RESET

After an external reset pulse the circuit will perform an internal reset procedure. The reset pulse must be active for at least 10 CLK cycles. 125 μs (the duration of 1 cycle at 8 kHz) after RESET has gone LOW, the internal reset is completed and the PCD5032 goes into standby mode. At that moment the ADPCM CODEC is ready to be programmed.

A reset clears all I²C-bus registers and resets the ADPCM transcoder, digital filters and auxiliary logic functions.

Table 5 Modes of operation

FUNCTION	I²C-CODE	DESCRIPTION	NOTE
Standby mode	00XXX0XX	Power-down	default after reset
Active mode	00XXX1XX	Active	
Normal mode	00XXXX00	Normal operation	default after active mode set
Loop 1	00XXXX01	Loopback on ADPCM side and on PCM side without using ADPCM transcoder	
Loop 2	00XXXX10	Loopback on TM+/TM– through ADPCM transcoder	

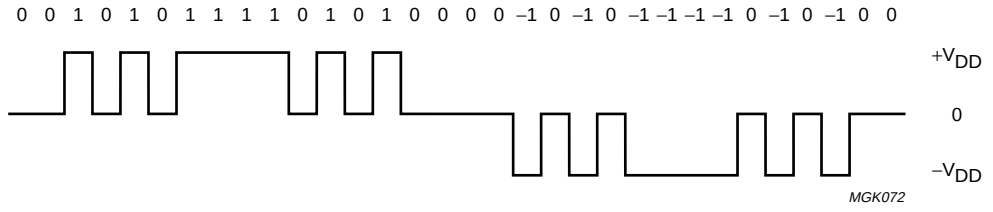


Fig.9 Tone output example.

8 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices. Details of recommended precautions are given in *"Handling MOS devices",* which is published in the General Information section of several of Philips data handbooks.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+6.5	V
I_{DD}	supply current	–150	+150	mA
V_I	all input voltages	–0.5	V_{DD} + 0.5	V
I_I	DC input current			
	BZ+, BZ–	–150	+150	mA
	RE+, RE–	–50	+50	mA
	all other pins	–10	+10	mA
I_O	DC output current			
	BZ+, BZ–	–150	+150	mA
	RE+, RE–	–50	+50	mA
	all other pins	–10	+10	mA
P_{tot}	total power dissipation	–	500	mW
T_{stg}	storage temperature	–65	+150	°C
T_{amb}	operating ambient temperature	–25	+70	°C

10 DC AND AC CHARACTERISTICS

V_{DD} = 2.7 to 5.5 V; V_{SS} = 0 V; CLK = 3456 kHz; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified. Specifications valid in active mode, except standby supply current.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
V_{DD}	operating supply voltage		2.7	–	5.5	V
I_{DD}	operating supply current	no load; T_{amb} = 25°C; note 1	–	7	14	mA
I_{stb}	standby supply current	T_{amb} = 25°C; note 1	–	20	100	µA
I_{LI}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	−1	–	+1	µA
VGA	analog signal ground voltage		$0.48V_{DD}$	$0.5V_{DD}$	$0.52V_{DD}$	V
V_{REF+}	positive reference voltage	note 2	0.8	1.0	1.2	V
V_{REF-}	negative reference voltage	note 2	−0.8	−1.0	−1.2	V
Digital I/O						
V_{IL}	LOW level input voltage	note 3	0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	note 3	$0.7V_{DD}$	–	V_{DD}	V
V_{OL}	LOW level output voltage	note 3	–	–	0.4	V
V_{OH}	HIGH level output voltage	note 3	V_{DD} −o.4	–	V_{DD}	V
$R_{pd(int)}$	internal pull-down resistance	note 3	–	150	–	kΩ
f_{DCLK}	DCLK frequency	note 4	$\frac{1}{54}f_{CLK}$ = 64	–	f_{CLK}	kHz
f_{RAS}, f_{TAS}	RAS, TAS frequency	note 4	–	8	–	kHz
I²C-bus timing						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SW}	tolerable pulse spike width		–	–	50	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{SU;STA}$	set-up time repeated START		4.7	–	–	µs
$t_{HD;STA}$	hold time START condition		4.0	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	rise time SDA and SCL		–	–	1.0	µs
t_f	fall time SDA and SCL		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	set-up time STOP condition		4.0	–	–	µs
Analog inputs; note 5						
$Z_{i(TM+)}$	input impedance, TM+	note 6	–	125	–	kΩ
$Z_{i(TM-)}$	input impedance, TM−	note 6	–	125	–	kΩ
V_i	nominal input level	RMS value; note 7	–	12	–	mV
$V_{i(max)}$	maximum input signal	RMS value; note 8	–	56	–	mV
$G_{v(min)}$	minimum voltage gain		−4	−3	−2	dB
$G_{v(max)}$	maximum voltage gain		+3	+4	+5	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$G_{v(step)}$	voltage gain, step size		–	1	–	dB
THD_{TX}	total harmonic distortion (transmitted)	note 9	–	–	–40	dB
Receiver audio output						
Z_o	output impedance	note 6	–	10	–	Ω
$V_{o(rms)}$	output signal level (RMS value)	0 dBm0; note 10	–	550	–	mV
		3.14 dBm0; note 11	–	1250	–	mV
$G_{v(min)}$	minimum voltage gain		–4	–3	–2	dB
$G_{v(max)}$	maximum voltage gain		+3	+4	+5	dB
$G_{v(step)}$	voltage gain, step size		–	1	–	dB
G_{vol}	volume control range		–36	–	0	dB
$G_{vol(step)}$	volume step size		–	6.0	–	dB
THD_{RX}	total harmonic distortion (received)	note 12	–	–	–40	dB
Ringer output; notes 5 and 13						
Z_o	output impedance		–	14	29	Ω
G_{vol}	volume control range		–29	–	+4	dB

Notes

1. All outputs left open. I_{DD} measured with all inputs connected to V_{SS}, except: CLK and DCLK connected to 3.456 MHz; RAS and TAS connected to 8 kHz. I_{stb} measured with all inputs connected to V_{SS}, except: TM+, TM– left open.
2. The reference voltage is available on V_{REF+} and $V_{REF–}$ and is measured with respect to VGA. The voltage outputs are intended for electret microphone supply and can deliver 400 μA.
3. Digital inputs and outputs are CMOS-levels compatible. The outputs and inputs can sink or source 1 mA. Pull-down resistors are present at pins RPI, TPI, TEST, RAD.
4. Any frequency between min. and max. is allowed for DCLK. The signals CLK and RAS/TAS must be frequency-locked and will have a ratio of f_{CLK}/f_{RAS} = 432
5. All analog input/output voltages are measured differentially. The circuit is designed for use with an electret microphone.
6. Frequency band is 300 Hz to 3400 Hz. Maximum load capacitance = 100 pF differentially, or 200 pF each pin.
7. Nominal signal level gives –10 dBm0 on the PCM interface (G.711/G.712). Value given for TX gain setting 0 dB.
8. Nominal signal level gives 3.14 dBm0 on the PCM interface, with larger input signals the digital output will be saturated. Value given for TX gain setting 0 dB.
9. Transmitter gain setting = 0 dB and input signal level = 40 mV (RMS) (will generate 0 dBm0 on PCM interface according to G.711).
10. PCM signal level is 0 dBm0 and RX gain setting 0 dB. With a load of 300 Ω between RE+ and RE– the signal level results in an output power of 1 mW. The maximum output current is 10 mA.
11. PCM signal level is +3.14 dBm0 and RX gain setting +4 dB. The maximum output current is 10 mA.
12. PCM signal level is 0 dBm0 (G.711).
13. For maximum output power the load resistance should equal the typical output impedance (specified at I_{LOAD} –20 mA). The absolute maximum value of output power given in Chapter 9 defines the minimum load resistance.

11 FILTER CHARACTERISTICS

V_{DD} = 2.7 to 5.5 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmitter						
R_{PB}	passband ripple (300 to 3000 Hz)		–	–	0.5	dB
	frequency response	f = 50 Hz	–35	–	–2	dB
		f = 3400 Hz	–35	–	–2	dB
		f = 4600 Hz	–35	–	–2	dB
		f = 8000 Hz	–60	–	–2	dB
Analog-to-Digital converter						
S/N	signal-to-noise ratio	Fig.10; notes 1 and 2	35	–	–	dB
Digital-to-Analog converter						
S/N	signal-to-noise ratio	Fig.10; notes 1 and 2	35	–	–	dB
Group delay						
$t_{d(TX)}$	transmitter	note 3	–	–	400	µs
$t_{d(RX)}$	receiver	note 3	–	–	525	µs
$t_{d(g)}$	group delay distortion (Loop 1)	Fig.11	tbf	tbf	tbf	µs

Notes

1. Frequency band is 300 Hz to 3400 Hz. Maximum load capacitance = 100 pF differentially, or 200 pF each pin.
2. Measured with psophometric filter (CCITT G.223). Only fulfilled at V_{DD} noise level less than 40 mV (peak value) (0 to 20 kHz). Measured on sample basis at V_{DD} = 3.0 V, T_{amb} = 25 °C, compliant with G.712. Signal level is −40 dBm0 on PCM interface; 0.4 mV (RMS) on analog input. Gain setting is 0 dB.
3. Group delay includes ADPCM/PCM conversion; signal frequency = 1.5 kHz. Value given is for RAS/TAS signals asserted simultaneously.

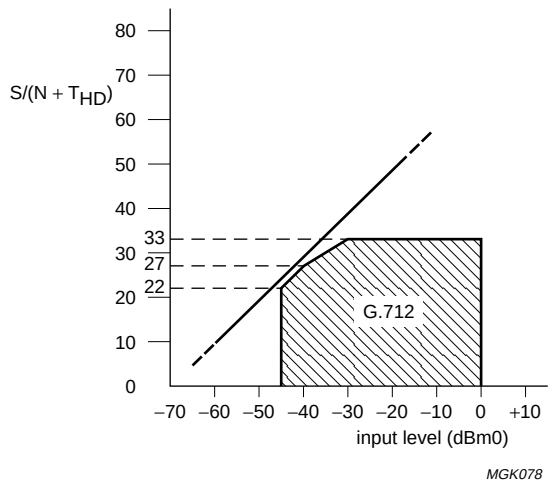


Fig.10 Typical performance of AD and DA in cascade.

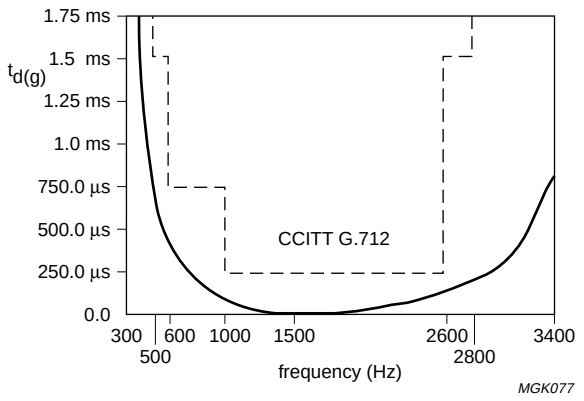


Fig.11 Group delay distortion: Transmit and Receive (loop measurement).

12 APPLICATION INFORMATION

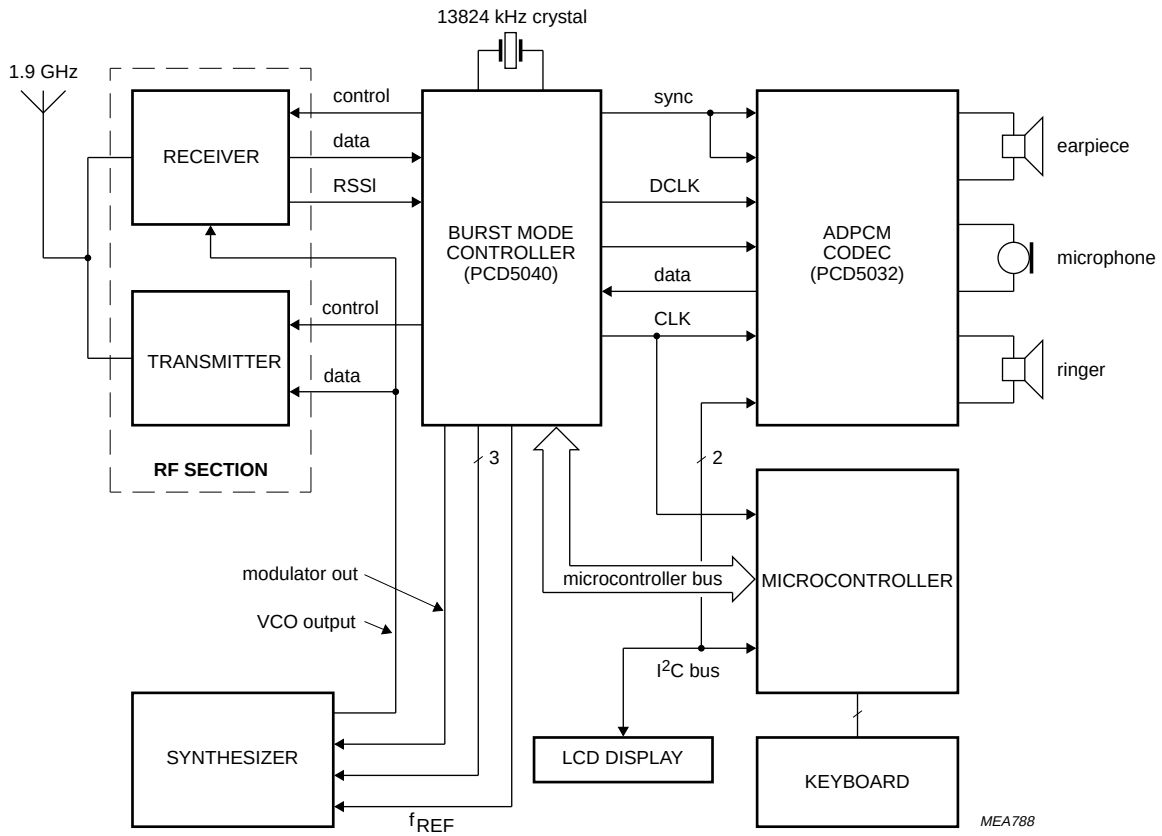


Fig.12 Typical block diagram for a DECT handset.

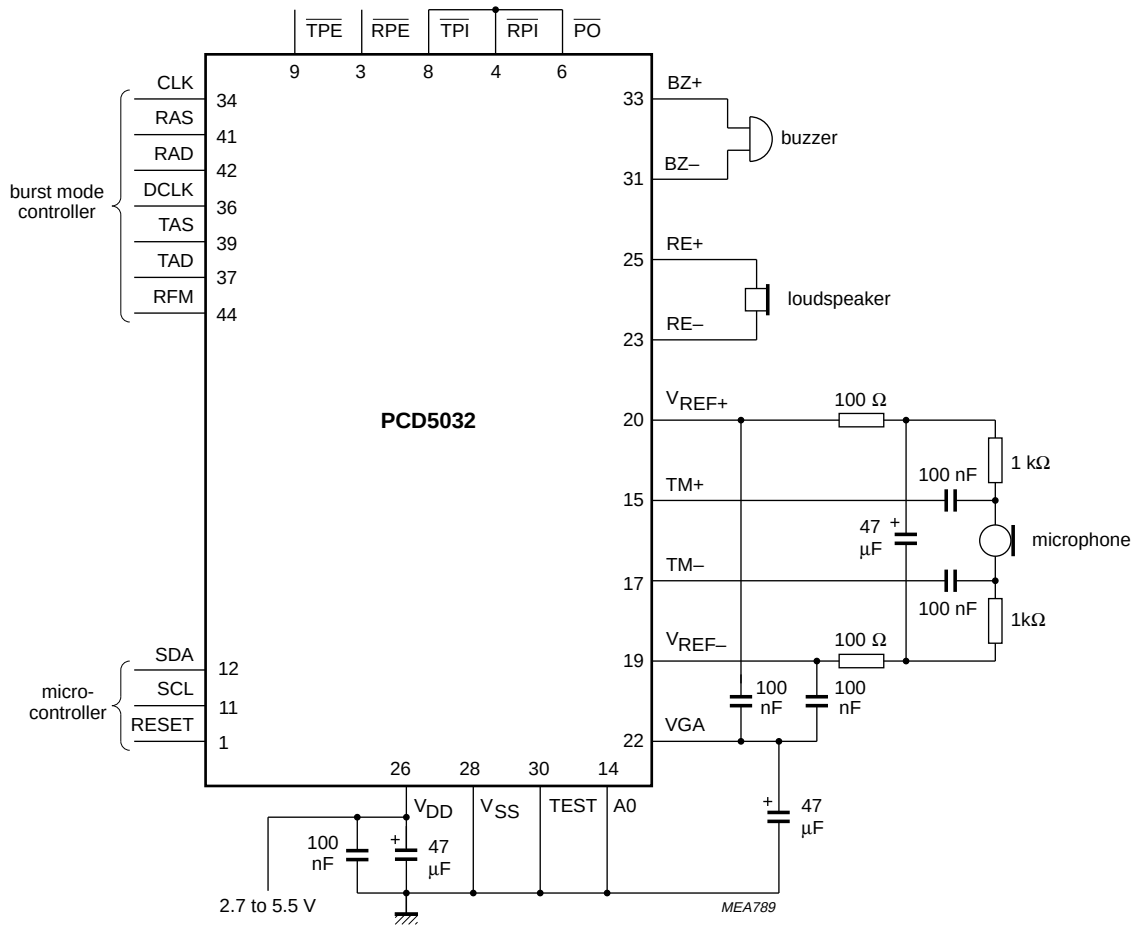
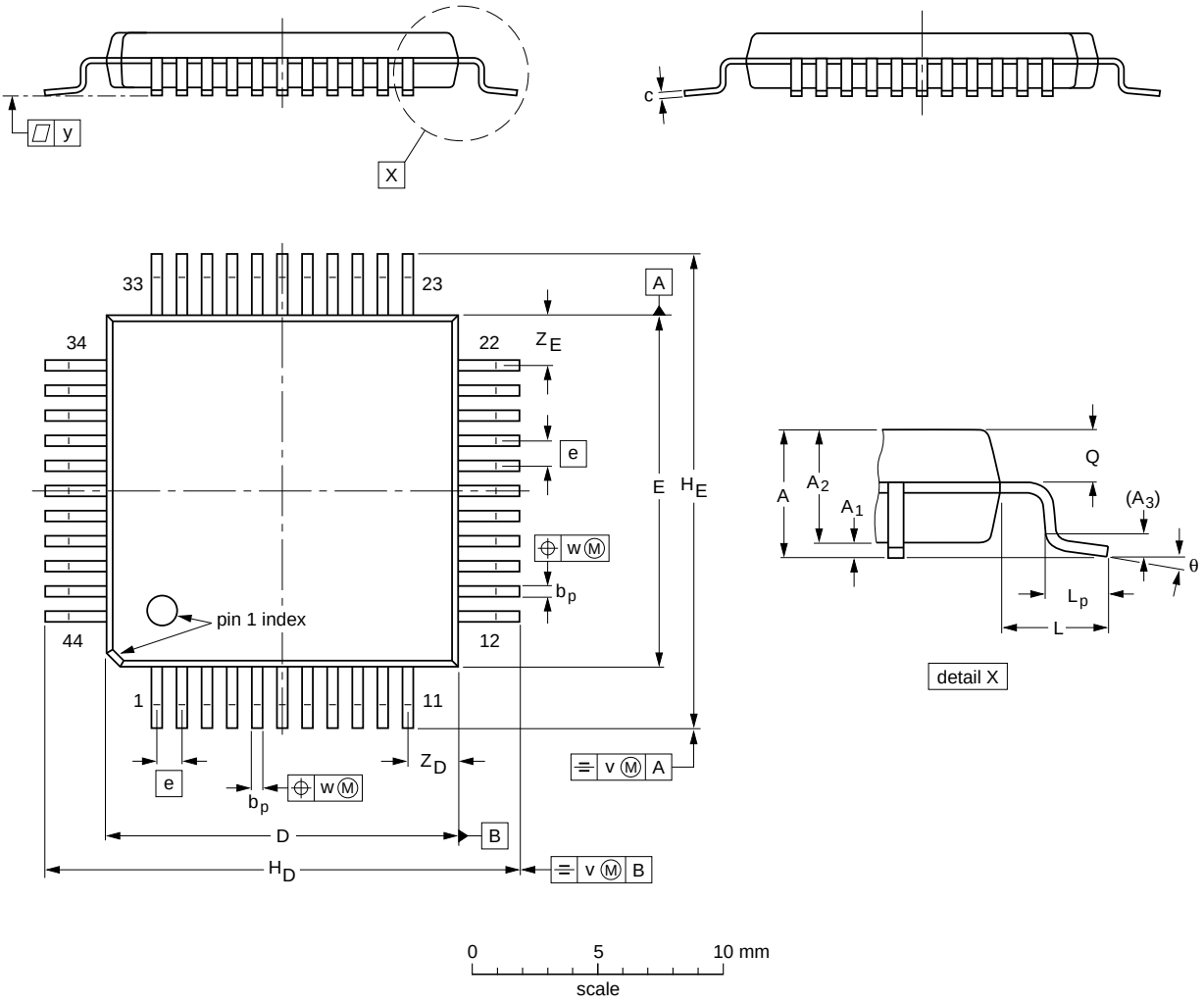


Fig.13 Typical handset application diagram for the PCD5032 in QFP44 package.

13 PACKAGE OUTLINES

QFP44: plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 x 14 x 2.2 mm **SOT205-1**



DIMENSIONS (mm are the original dimensions)

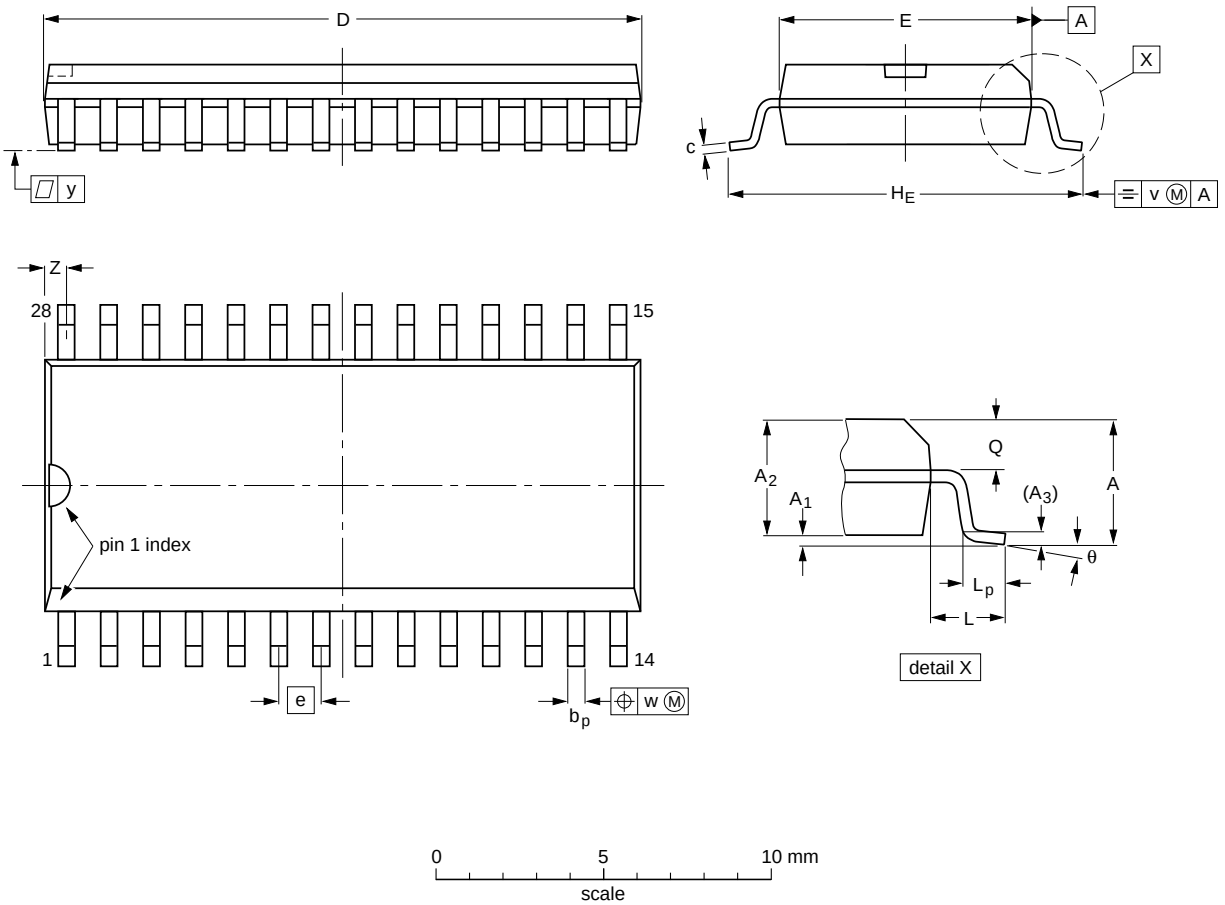
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.60	0.25 0.05	2.3 2.1	0.25	0.50 0.35	0.25 0.14	14.1 13.9	14.1 13.9	1	19.2 18.2	19.2 18.2	2.35	2.0 1.2	1.2 0.9	0.3	0.15	0.1	2.4 1.8	2.4 1.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT205-1	133E01A					~~92-11-17~~ 95-02-04

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~91-08-13~~ 95-01-24

14 SOLDERING

14.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

14.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP and SO packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Manual"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

14.3 Wave soldering

14.3.1 QFP

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

14.3.2 SO

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

14.3.3 METHOD (QFP AND SO)

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

15 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

16 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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