

256 × 4-BIT STATIC RAM

GENERAL DESCRIPTION

The PCD5101 is a very low-power 1024-bit static CMOS random access memory, organized as 256 words by 4 bits. It is suitable for low power and high speed applications where battery standby power is required to ensure non-volatility of data. All inputs and outputs are fully TTL compatible and pinning is compatible with 2101-type NMOS static RAMs and 5101-type CMOS static RAMs.

There are two chip enable inputs, $\overline{CE1}$ and CE2, selection being made when $\overline{CE1}$ is LOW and CE2 is HIGH. The memory has an output disable function, OD, which allows the inputs/outputs to be used separately, or to be tied together for use in common data I/O systems.

Features

- Operating supply voltage range
- Low data retention voltage
- Low power consumption in both operating and standby modes
- Access time 150 ns at $V_{DD} = 5\text{ V}$; 400 ns at $V_{DD} = 3\text{ V}$
- Three-state outputs
- All inputs and outputs directly TTL compatible
- Choice of two package types

2,5 to 5,5 V
min. 1 V

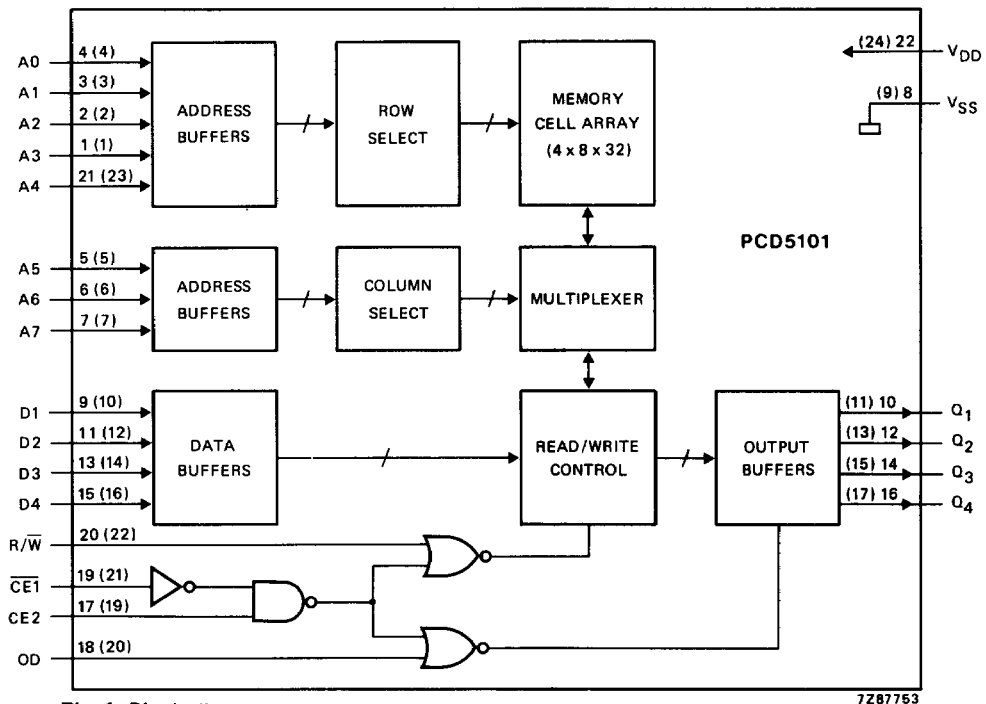


Fig. 1 Block diagram: pin numbers in parentheses are for PCD5101T; other pin numbers are applicable to PCD5101P.

PACKAGE OUTLINES

PCD5101P: 22-lead DIL; plastic (SOT116).

PCD5101T: 24-lead mini-pack; plastic (SO24; SOT137A).

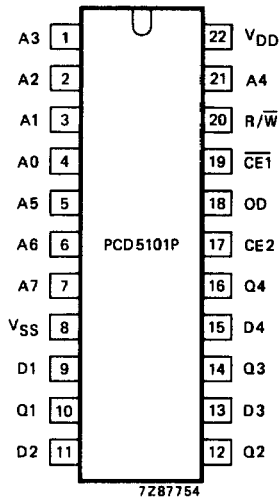


Fig. 2 Pinning diagram for PCD5101P.

PINNING

- D1 } data inputs
- D2 }
- D3 }
- D4 }
- A0 } address inputs
- A1 }
- A2 }
- A3 }
- A4 }
- A5 }
- A6 }
- A7 }
- R/W read/write input
- CE1 } chip enable inputs
- CE2 }
- OD output disable
- Q1 } data outputs
- Q2 }
- Q3 }
- Q4 }
- V_{DD} positive supply
- V_{SS} negative supply
- n.c. not connected

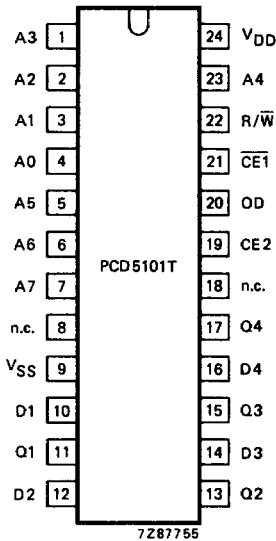


Fig. 3 Pinning diagram for PCD5101T.

OPERATING MODES**Table 1** Mode selection

$\overline{\text{CE1}}$	CE2	$\text{R}/\overline{\text{W}}$	OD	mode of operation	output state
H	X	X	X	standby	high impedance
X	L	X	X	standby	high impedance
L	H	L	H	write	high impedance
L	H	L	L	write	equal to input data
L	H	H	L	read	data valid
L	H	H	H	read	high impedance

Separate input/output: write cycle $\text{OD} = \text{X}$; read cycle $\text{OD} = \text{L}$.

Common input/output: write cycle $\text{OD} = \text{H}$; read cycle $\text{OD} = \text{L}$.

H = HIGH voltage level

L = LOW voltage level

X = don't care

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	-0,3 to 8,0 V
Input voltage range (any pin)	V_{I}	$V_{\text{SS}} - 0,3$ to $V_{\text{DD}} + 0,3$ V
Operating temperature range	T_{amb}	-25 to +70 °C
Storage temperature range	T_{stg}	-55 to +125 °C

D.C. CHARACTERISTICS ($V_{DD} = 5\text{ V}$) $V_{DD} = 5 \pm 0,5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -25\text{ to } +70\text{ }^{\circ}\text{C}$

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	4,5	5,0	5,5	V
Operating supply current at $V_I = V_{DD}$ or V_{SS} ; $f = 1\text{ MHz}$; outputs open	I_{DD}	–	10	17	mA
at $V_I = 0,8$ or $2,0\text{ V}$; $f = 1\text{ MHz}$; outputs open	I_{DD}	–	10	17	mA
at $V_I = 0,8$ or $2,0\text{ V}$; $f = 5\text{ MHz}$; outputs open	I_{DD}	–	12	20	mA
Standby supply current at $CE2 = V_{SS}$	I_{SB}	–	0,02	5,0	μA
Input leakage current at $V_I = V_{SS}$ to V_{DD}	$ I_{IL} $	–	–	0,1	μA
Input voltage LOW	V_{IL}	–0,3	–	+0,8	V
Input voltage HIGH	V_{IH}	2,0	–	$V_{DD} + 0,3$	V
Output leakage current at $V_O = V_{SS}$ to V_{DD} ; OD = HIGH or chip disabled	$ I_{OL} $	–	–	0,2	μA
Output voltage LOW at $I_{OL} = 4,0\text{ mA}$	V_{OL}	–	–	0,4	V
Output voltage HIGH at $-I_{OH} = 2,0\text{ mA}$	V_{OH}	2,4	–	–	V

D.C. CHARACTERISTICS ($V_{DD} = 3\text{ V}$) $V_{DD} = 3 \pm 0,5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -25\text{ to } +70\text{ }^{\circ}\text{C}$

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	3,0	3,5	V
Operating supply current at $V_I = V_{DD}$ or V_{SS} ; $f = 1\text{ MHz}$; outputs open	I_{DD}	–	5	8	mA
at $V_I = 0,4$ or $1,6\text{ V}$; $f = 1\text{ MHz}$; outputs open	I_{DD}	–	5	8	mA
Standby supply current at $CE2 = V_{SS}$	I_{SB}	–	0,02	5,0	μA
Input leakage current at $V_I = V_{SS}$ to V_{DD}	$ I_{IL} $	–	–	0,1	μA
Input voltage LOW	V_{IL}	–0,3	–	+0,4	V
Input voltage HIGH	V_{IH}	1,6	–	$V_{DD} + 0,3$	V
Output leakage current at $V_O = V_{SS}$ to V_{DD} ; OD = HIGH or chip disabled	$ I_{OL} $	–	–	0,2	μA
Output voltage LOW at $I_{OL} = 1,0\text{ mA}$	V_{OL}	–	–	0,3	V
Output voltage HIGH at $-I_{OH} = 1,0\text{ mA}$	V_{OH}	1,7	–	–	V

A.C. TEST CONDITIONS ($V_{DD} = 5\text{ V}$)

Input pulse levels	0,8 V to 2,0 V
Input rise and fall times	5 ns
Input timing reference levels	1,5 V
Output timing levels	1,5 V
Output timing levels for high/low impedance	1,2 V and 2,8 V
Output load (2 TTL inputs and load capacitance C_L)	Fig. 4

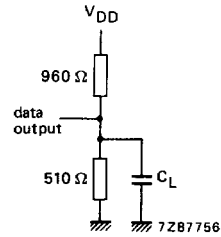


Fig. 4 Test load.

A.C. CHARACTERISTICS ($V_{DD} = 5\text{ V}$)

$V_{DD} = 5 \pm 0,5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -25\text{ to }+70\text{ }^\circ\text{C}$; loads as per Fig. 4 with $C_L = 100\text{ pF}$ unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	150	—	—	ns
Address access time	t_{AA}	—	—	150	ns
Chip enable $\overline{CE1}$ to output	t_{CO1}	—	—	150	ns
Chip enable CE2 to output	t_{CO2}	—	—	150	ns
Output disable OD to output	t_{OD}	—	—	70	ns
Data output to high impedance state at $C_L = 5\text{ pF}$	t_{DF}	10	—	70	ns
Previously read data valid with respect to address change	t_{OH1}	10	—	—	ns
Previously read data valid with respect to chip enable	t_{OH2}	10	—	—	ns
Write cycle					
Write cycle time	t_{WC}	150	—	—	ns
Write delay time	t_{AW}	0	—	—	ns
Chip enable $\overline{CE1}$ to write	t_{CW1}	120	—	—	ns
Chip enable CE2 to write	t_{CW2}	120	—	—	ns
Data set-up time	t_{DW}	70	—	—	ns
Data hold time	t_{DH}	0	—	—	ns
Write pulse duration	t_{WP}	70	—	—	ns
Write recovery time	t_{WR}	0	—	—	ns
Output disable OD set-up time	t_{DS}	70	—	—	ns

A.C. TEST CONDITIONS ($V_{DD} = 3\text{ V}$)

Input pulse levels	0,4 V to 1,6 V
Input rise and fall times	5 ns
Input timing reference levels	1,0 V
Output timing levels	1,0 V
Output timing levels for high/low impedance	0,7 V and 1,7 V
Output load	Fig. 5

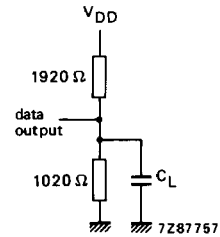


Fig. 5 Test load.

A.C. CHARACTERISTICS ($V_{DD} = 3\text{ V}$)

$V_{DD} = 3 \pm 0,5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -25\text{ to }+70\text{ }^{\circ}\text{C}$; loads as per Fig. 5 with $C_L = 100\text{ pF}$ unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	400	—	—	ns
Address access time	t_{AA}	—	—	400	ns
Chip enable $\overline{CE1}$ to output	t_{CO1}	—	—	400	ns
Chip enable CE2 to output	t_{CO2}	—	—	400	ns
Output disable OD to output	t_{OD}	—	—	200	ns
Data output to high impedance state at $C_L = 5\text{ pF}$	t_{DF}	10	—	200	ns
Previously read data valid with respect to address change	t_{OH1}	10	—	—	ns
Previously read data valid with respect to chip enable	t_{OH2}	10	—	—	ns
Write cycle					
Write cycle time	t_{WC}	400	—	—	ns
Write delay time	t_{AW}	0	—	—	ns
Chip enable $\overline{CE1}$ to write	t_{CW1}	300	—	—	ns
Chip enable CE2 to write	t_{CW2}	300	—	—	ns
Data set-up time	t_{DW}	200	—	—	ns
Data hold time	t_{DH}	0	—	—	ns
Write pulse duration	t_{WP}	200	—	—	ns
Write recovery time	t_{WR}	0	—	—	ns
Output disable OD set-up time	t_{DS}	200	—	—	ns

WAVEFORMS

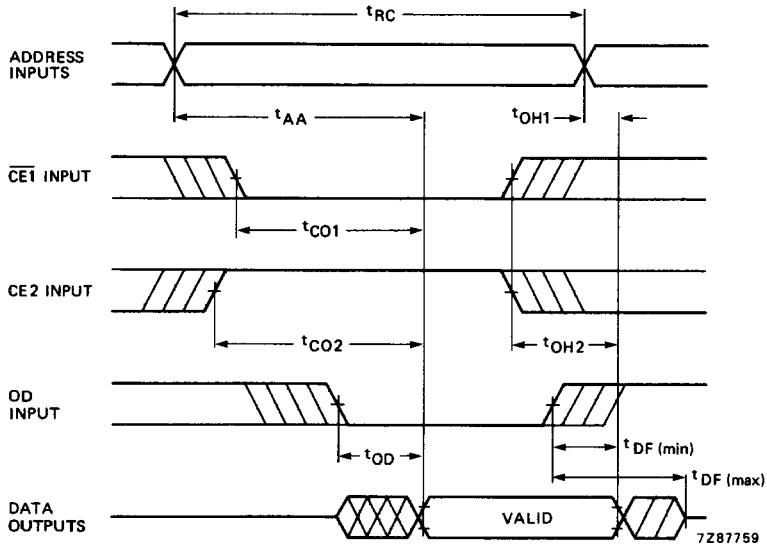


Fig. 6 Read cycle timing; $R/\bar{W} = \text{HIGH}$.

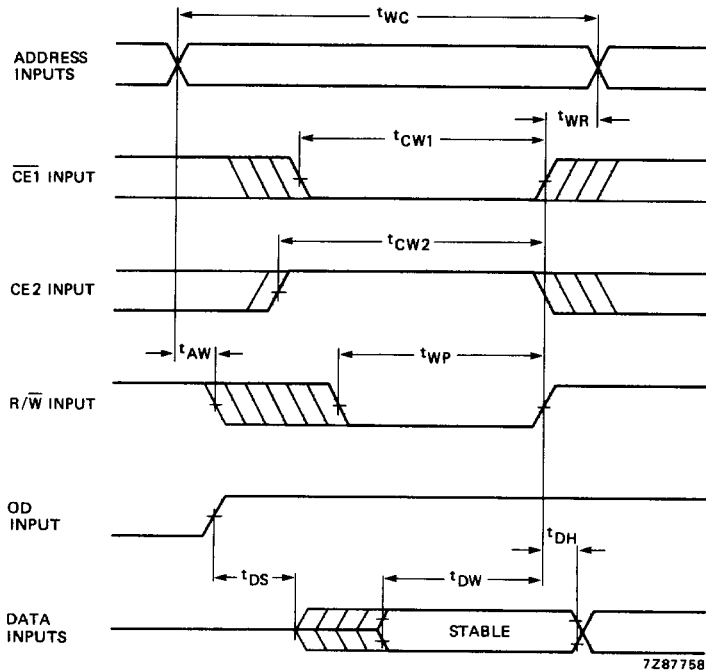


Fig. 7 Write cycle timing.

LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS

 $CE2 \leq 0,2 \text{ V}; T_{amb} = -25 \text{ to } +70 \text{ }^\circ\text{C}.$

parameter	symbol	min.	typ.	max.	unit
Supply voltage for data retention	V_{DR}	1,0	—	5,5	V
Data retention current at $V_{DD} = 1,5 \text{ V}$	I_{DR}	—	0,02	2,0	μA
Chip deselect to data retention time	t_{CDR}	0	—	—	ns
Operation recovery time	t_R	0	—	—	ns

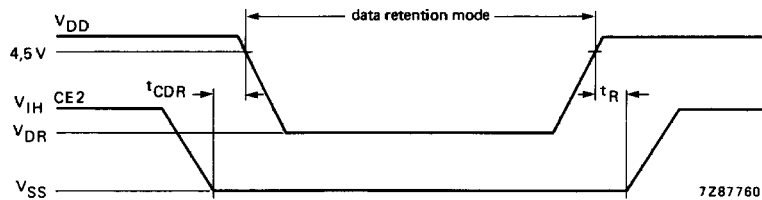


Fig. 8 Low supply voltage data retention characteristics.