LCD FLAT-PANEL ROW/COLUMN DRIVER

GENERAL DESCRIPTION

The PCF2201 is a row or column LCD driver, designed to drive LCD flat-panels at multiplex rates of up to 1 : 256. The PCF2201 converts serial or parallel 4-bit display data into parallel LCD drive waveforms, capable of driving up to 81 rows or 80 columns of an LCD matrix. The PCF2201 is cascadable, enabling it to drive any LCD flat-panel matrix. The PCF2201 is controlled by an alphanumeric/graphic controller.

Features

- Row or column drive capability
- 80 data latches
- 81 stage bidirectional shift register
- 81 LCD drive outputs
- Proprietary margin control drive output
- Low drive impedance
- LCD drive voltage of up to 25 V
- 5 V logic compatibility
- High speed operation (4 MHz)
- Multiplex rates of up to 1 : 256
- Externally adjusted bias voltages
- Maximum LCD voltage and V_{DD} may be separated
- 64/65 pin programmable output operation mode
- Low power consumption
- Overall flat-panel power consumption minimized
- Pin programmable right/left orientation for convenience of flat-panel construction
- Optimized pinning for single plane wiring
- Space-saving 120-lead Tape-Automated Bonding package
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINE

PCF2201V: 120-lead Tape-Automated Bonding (TAB) module (SOT235)

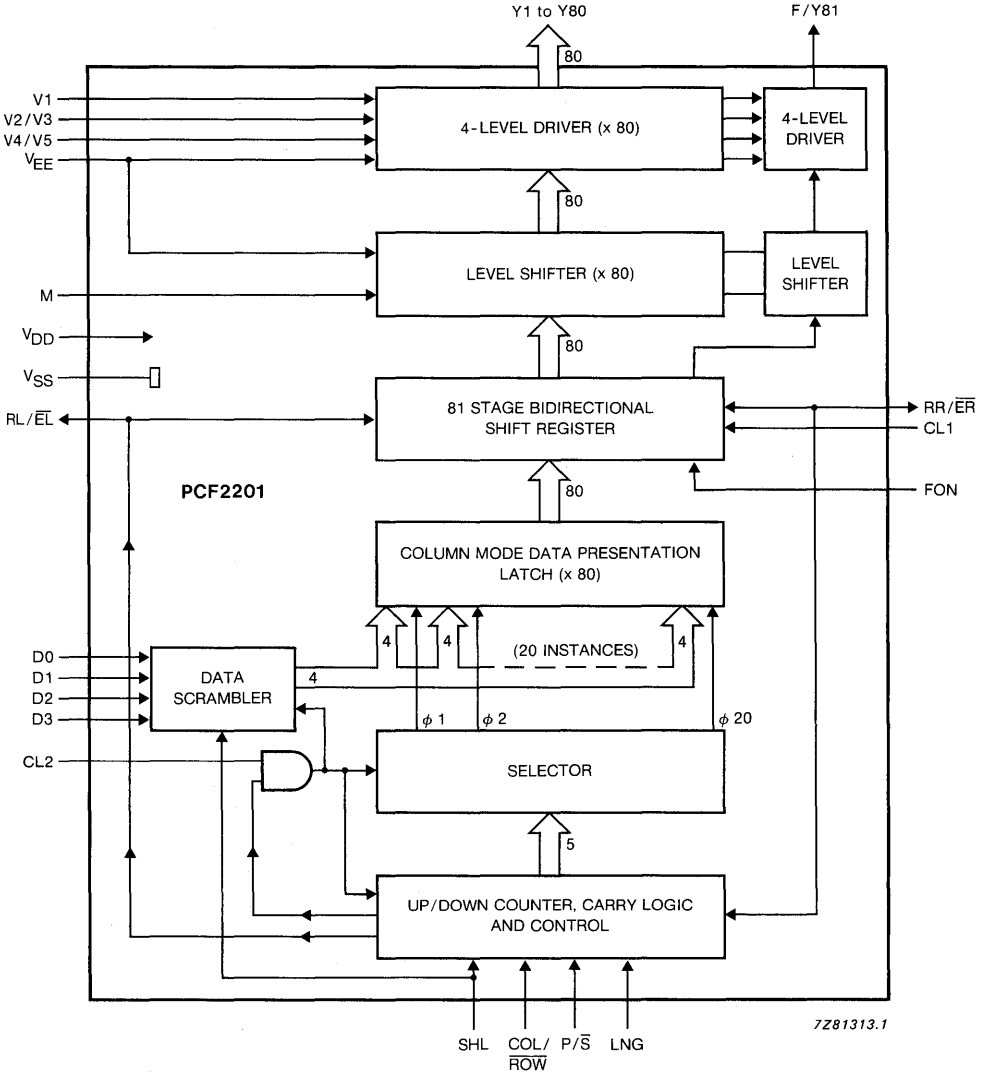


Fig. 1 Block diagram.

DEVELOPMENT DATA

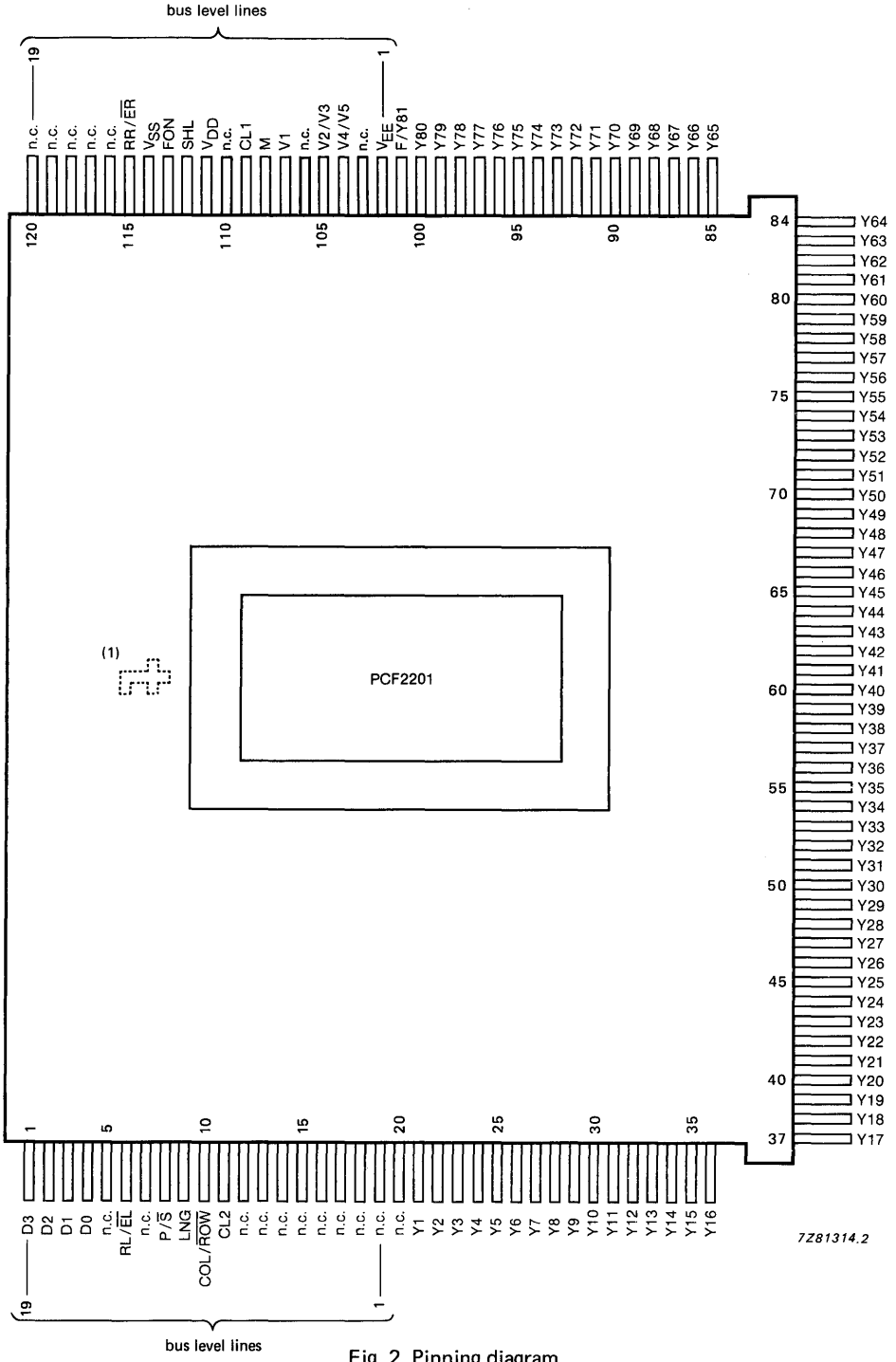


Fig. 2 Pinning diagram.

(1) mark orientation

PINNING FUNCTIONS

mnemonic	I/O	function
V_{DD}	P	Positive supply voltage (5 V)
V_{SS}	P	Logic ground (0 V)
V_1	P	Most positive LCD supply voltage ($\leqslant V_{DD}$), selection level
V_2/V_3	P	Upper non-selection level for row (V2) or column (V3) driver
V_4/V_5	P	Lower non-selection level for row (V5) or column (V4) driver
V_{EE}	P	Most negative LCD supply voltage (−20 V), selection level
Y1 to Y80	O	Liquid crystal driver outputs
CL1	I	Clock for 81 stage bidirectional shift register Loads parallel data from the data presentation latch and frame control in column driver mode Shifts data in row driver mode Negative edge triggered
CL2	I	Data transfer clock in column driver modes Data must be valid on the negative edge of CL2 Unused in row driver mode (may be left open)
COL/$\overline{\text{ROW}}$	I	Column/row driver mode select
P/$\overline{\text{S}}$	I	Parallel/serial mode select for column drivers Tie to V_{SS} in row driver mode
SHL	I	Shift direction select
D0 to D3	I	Data inputs in column driver modes Unused in row driver mode (may be left open) Filling order:

COL/$\overline{\text{ROW}}$	P/$\overline{\text{S}}$	SHL	D0	D1	D2	D3
H	L	L	Y1, Y2, Y3,.	unused	unused	unused
H	L	H	Y80, Y79,...	(may be left open)	(may be left open)	(may be left open)
H	H	L	Y1, Y5, Y9,.	Y2, Y6, Y10,.	Y3, Y7, Y11,.	Y4, Y8, Y12,..
H	H	H	Y80, Y76,...	Y79, Y75,....	Y78, Y74,....	Y77, Y73,.....

Also in the **serial** column driver mode, a multiple of 4 data bits must always be transferred. Add dummy bits if necessary

DEVELOPMENT DATA

<table>
<tr><th>mnemonic</th><th>I/O</th><th>function</th></tr>
<tr><td>RL/$\overline{EL}$
RR/$\overline{ER}$</td><td>I/O</td><td>Left/right serial input/outputs in row driver mode, left/right enable input/outputs in column driver modes
<table>
<tr><th>COL/$\overline{ROW}$</th><th>P/$\overline{S}$</th><th>SHL</th><th>RL/$\overline{EL}$</th><th>RR/$\overline{ER}$</th><th>comments</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>I</td><td>O</td><td>shift direction:
RL/$\overline{EL}$ –> RR/$\overline{ER}$ (Y1 –> F/Y81)</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>O</td><td>I</td><td>shift direction:
RR/$\overline{ER}$ –> RL/$\overline{EL}$ (F/Y81 –> Y1)</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>I</td><td>O</td><td>RR/$\overline{ER}$ goes LOW 80 CL2 pulses after RL/$\overline{EL}$</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>O</td><td>I</td><td>RL/$\overline{EL}$ goes LOW 80 CL2 pulses after RR/$\overline{ER}$</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>I</td><td>O</td><td>RR/$\overline{ER}$ goes LOW 20 CL2 pulses after RL/$\overline{EL}$</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>O</td><td>I</td><td>RL/$\overline{EL}$ goes LOW 20 CL2 pulses after RR/$\overline{ER}$</td></tr>
</table>
In the serial column mode, the device accepts one bit of display data at each CL2 pulse after RL/$\overline{EL}$ (or RR/$\overline{ER}$ respectively) goes LOW
When 80 bits of display data have been accepted, the device accepts no further display data and takes its output RR/$\overline{ER}$ (or RL/$\overline{EL}$ respectively) LOW, thereby enabling the next PCF2201 to accept display data
The sequence is reset when CL1 is HIGH and CL2 is LOW

In the parallel column mode, the device accepts one nibble of display data at each CL2 pulse after RL/$\overline{EL}$ (or RR/$\overline{ER}$ respectively) goes LOW
When 20 nibbles of display data have been accepted, the device accepts no further display data and takes its output RR/$\overline{ER}$ (or RL/$\overline{EL}$ respectively) LOW, thereby enabling the next PCF2201 to accept display data.
The sequence is reset when CL1 is HIGH and CL2 is LOW</td></tr>
<tr><td>LNG</td><td>I</td><td>Length control
<table>
<tr><th>COL/$\overline{ROW}$</th><th>LNG</th><th>SHL</th><th>description</th><th>valid Yi</th><th>undefined Yi</th></tr>
<tr><td>L
L</td><td>L
L</td><td>L
H</td><td>65-bit row mode
operation</td><td>Y1...Y65
Y17...Y80, F/Y81</td><td>Y66...Y80, F/Y81
Y1...Y16</td></tr>
<tr><td>L
L</td><td>H
H</td><td>L
H</td><td>81-bit row mode
operation</td><td>Y1...Y80, F/Y81
Y1...Y80, F/Y81</td><td>–
–</td></tr>
<tr><td>H
H</td><td>L
L</td><td>L
H</td><td>64-bit column
mode operation</td><td>Y1...Y64
Y17...Y80</td><td>Y65...Y80
Y1...Y16</td></tr>
<tr><td>H
H</td><td>H
H</td><td>L
H</td><td>80-bit column
mode operation</td><td>Y1...Y80
Y1...Y80</td><td>–
–</td></tr>
</table>
In 80/81-bit operation, the device behaves as previously described
In 64/65-bit operation, the device behaves as if all resources have been reduced to 64/65 instances; i.e. 16 outputs (determined by SHL) can no longer be accessed and should be left open circuit.</td></tr>
</table>

PINNING FUNCTIONS (continued)

<table>
<tr><th>mnemonic</th><th>I/O</th><th>function</th></tr>
<tr><td>F/Y81*</td><td>O</td><td>Frame output in column driver mode
It continuously delivers the select or non-select column driver LCD voltages depending on the state of the frame control
The frame output is used to blank the flat-panel display margin outside the actual LCD matrix
Liquid crystal driver output, number 81 in row driver mode</td></tr>
<tr><td>FON</td><td>I</td><td>Frame control
Defines the contents of the shift register cell corresponding to F/Y81 in column driver mode
Tie to V_{DD} or V_{SS} in row driver mode</td></tr>
<tr><td>M</td><td>I</td><td>Signal to convert LCD drive waveform into a.c.:
<table>
<tr><th>COL/$\overline{\text{ROW}}$</th><th>SR data</th><th>M</th><th>output level (Y_i or F/Y81)</th><th>note</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>V_2/V_3</td><td rowspan="4">row driver</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>V_4/V_5</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>V_{EE}</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>V_1</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>V_2/V_3</td><td rowspan="4">column driver</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>V_4/V_5</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>V_1</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>V_{EE}</td></tr>
</table></td></tr>
<tr><td>n.c.</td><td>–</td><td>not connected</td></tr>
</table>

* Patent application pending.

FUNCTIONAL DESCRIPTION

4-level driver

One of the liquid crystal driver levels (V_1, V_2/V_3, V_4/V_5 and V_{EE}) is output onto lines Y1 to Y80 and F/Y81 depending on the state of the relevant level shifter.

Level shifter

The level shifter converts logic level driver information into LCD level selection signals. The LCD level selection signals are dependent on the contents of the 81 stage bidirectional shift register and the state of signals M and COL/$\overline{\text{ROW}}$.

81 stage bidirectional shift register

In row driver mode the bidirectional shift register is used for the row line scan. In column driver mode the bidirectional shift register is used to hold column data until the next line is assembled in the data presentation latch.

Column mode data presentation latch

The column mode data presentation latch provides temporary storage during transfer of column data required for the next row.

Data scrambler

In serial column data transfer, the data scrambler converts 1-bit data to parallel 4-bit nibbles. Data is rearranged by the data scrambler according to the orientation (left or right) of the chip, as defined by pin SHL.

Selector

The selector generates latch clocks $\phi 1$ to $\phi 20$ for the presentation latch. Selection is determined by the state of the up/down counter and the carry logic.

Up/down counter, carry logic and control

Incoming column data storage locations are determined by the up/down counter making use of enable lines (RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$) and the length control select (LNG). The carry logic inhibits the data transfer clock (CL2) in inactive column drivers, thereby reducing power dissipation. When data transfer to one column driver is completed, the subsequent column driver is enabled by the carry logic. The control part co-ordinates the up/down counter and carry logic, depending upon the condition of the device (SHL, COL/$\overline{\text{ROW}}$, P/$\overline{\text{S}}$, LNG, RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	V_{SS} −0,3 to V_{SS} + 7		V
LCD supply voltage range	V_{EE}	V_{DD} −30 to V_{DD}		V
V_1, V_2/V_3 voltage range (note 1)	V_U	$\frac{V_{DD} + V_{EE}}{2}$ −1 to V_{DD}		V
V_4/V_5 voltage range (note 1)	V_L	V_{EE} to $\frac{V_{DD} + V_{EE}}{2}$ − 1		V
Input voltage range (CL1, CL2, COL/$\overline{\text{ROW}}$, P/$\overline{\text{S}}$, SHL, D0, D1, D2, D3, RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$, LNG, FON, M)	V_I	V_{SS} −0,3 to V_{DD} + 0,3		V
Output voltage range (RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$)	V_O	V_{SS} −0,3 to V_{DD} + 0,3		V
Driver output voltage range (F/Y81, Y1 to Y80)	V_Y	V_{EE} −0,3 to V_{DD} + 0,3		V
DC input current	$\pm I_I$	max.	20	mA
DC output current	$\pm I_O$	max.	25	mA
V_{DD}, V_{SS}, V_1, V_2/V_3, V_4/V_5 or V_{EE} current	$\pm I_{SUP}$	max.	20	mA
Power dissipation per package	P_{tot}	max.	400	mW
Power dissipation per output	P_o	max.	100	mW
Storage temperature range	T_{stg}		−65 to + 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 4,5 to 5,5 V;

V_{EE} = 0 to −20 V; $V_{DD} \geqslant V_1 \geqslant V_2/V_3 \geqslant \frac{V_{DD} + V_{EE}}{2} - 1\ V \geqslant V_4/V_5 \geqslant V_{EE}$; f_M = 100 Hz

T_{amb} = −40 to + 85 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Positive supply voltage		V_{DD}	4,5	–	5,5	V
Negative LCD supply voltage		V_{EE}	V_{DD}−25	–	V_{DD}−5	V
Static supply current	$f_{CL1} = f_{CL2}$ = 0 Hz; COL/$\overline{\text{ROW}}$ = H; M = L; note 2	I_{DD1}	–	15	40	μA
Operating supply current	COL/$\overline{\text{ROW}}$ = H; f_{CL1} = 25 kHz; f_{CL2} = 4 MHz; note 2	I_{DD2}	–	0,4	1	mA
Operating supply current	COL/$\overline{\text{ROW}}$ = H; RL/$\overline{\text{EL}}$ = H (SHL = L) or RR/$\overline{\text{ER}}$ = H (SHL = H); f_{CL1} = 25 kHz; note 2	I_{DD3}	–	50	150	μA
Operating supply current	COL/$\overline{\text{ROW}}$ = L; f_{CL1} = 100 kHz; note 2	I_{DD4}	–	75	200	μA
Logic						
Input voltage LOW		V_{IL}	0	–	0,3 V_{DD}	V
HIGH		V_{IH}	0,7 V_{DD}	–	V_{DD}	
Output voltage LOW to RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$	I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH to RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$	I_O = 0 mA	V_{OH}	V_{DD}−0,05	–	–	V
Output current LOW to RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$	V_{OL} = 1 V	I_{OL}	1	–	–	mA

DC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output current HIGH RL/$\overline{EL}$ and RR/$\overline{ER}$	$V_{OH} = V_{DD}-1$ V	I_{OH}	–	–	1	mA
Leakage current at CL1, CL2, COL/$\overline{ROW}$, P/$\overline{S}$, SHL, D0 to D3, RL/$\overline{EL}$, RR/$\overline{ER}$, LNG, FON and M		$\pm I_{L1}$	–	–	1	μA
Input capacitance	note 3	C_I	–	–	7	pF
LCD outputs						
Leakage current at V_1, V_2/V_3, V_4/V_5		$\pm I_{L2}$	–	–	2	μA
Resistance ON between V_1, V_2/V_3, V_4/V_5, V_{EE} and Y1 to Y80, F/Y81	$I_O = 100$ μA; $V_{EE} = V_{DD}-25$ V note 4	R_{ON}	–	–	2	kΩ

AC CHARACTERISTICS (note 5)

$V_{SS} = 0$ V; $V_{DD} = 4{,}5$ to $5{,}5$ V;
$V_{EE} = 0$ to -20 V; $V_{DD} \geqslant V_1 \geqslant V_2/V_3 \geqslant \frac{V_{DD} + V_{EE}}{2} - 1\text{ V} \geqslant V_4/V_5 \geqslant V_{EE}$;

$f_M = 100$ Hz; see Figs 4 and 5; $T_{amb} = -40$ to $+85$ °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Column driver data transfer rate		f_{CL2}	–	–	4	MHz
CL2 HIGH time		t_{CL2H}	100	–	–	ns
CL2 LOW time		t_{CL2L}	100	–	–	ns
CL2 rise time		t_{CL2r}	–	–	25	ns
CL2 fall time		t_{CL2f}	–	–	25	ns
Row driver clock rate		f_{CL1}	–	–	100	kHz
CL1 HIGH time		t_{CL1H}	275	–	–	ns
CL1 LOW time		t_{CL1L}	5	–	–	μs
CL1 rise time		t_{CL1r}	–	–	50	ns
CL1 fall time		t_{CL1f}	–	–	50	ns

DEVELOPMENT DATA

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Column data set-up time	COL/$\overline{\text{ROW}}$ = H	t_{SUC}	50	–	–	ns
Column data hold time	COL/$\overline{\text{ROW}}$ = H	t_{HDC}	30	–	–	ns
Row data set-up time	COL/$\overline{\text{ROW}}$ = L	t_{SUR}	200	–	–	ns
Row data hold time	COL/$\overline{\text{ROW}}$ = L	t_{HDR}	0	–	–	ns
Enable HIGH to CL2 set-up time	COL/$\overline{\text{ROW}}$ = H	t_{ECH}	90	–	–	ns
Enable LOW to CL2 set-up time	COL/$\overline{\text{ROW}}$ = H	t_{ECL}	85	–	–	ns
Propagation delay to enable HIGH	COL/$\overline{\text{ROW}}$ = H	t_{PEH}	–	–	185	ns
Propagation delay to enable LOW	COL/$\overline{\text{ROW}}$ = H	t_{PEL}	–	–	140	ns
CL2 to CL1 time	COL/$\overline{\text{ROW}}$ = H	t_{CL21}	50	–	–	ns
CL1 to CL2 time	COL/$\overline{\text{ROW}}$ = H	t_{CL12}	50	–	–	ns
Overlap time of CL2 = LOW and CL1 = HIGH	COL/$\overline{\text{ROW}}$ = H	t_{ov}	275	–	–	ns
Propagation delay HIGH to RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$	COL/$\overline{\text{ROW}}$ = L	t_{PLH}	20	–	200	ns
Propagation delay LOW to RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$	COL/$\overline{\text{ROW}}$ = L	t_{PHL}	20	–	200	ns
Propagation delay to Y1 . . .Y80, F/Y81	$V_{EE} = V_{DD}$ −20 V	t_{PY}	–	–	3	μs

Notes to characteristics

1. Maintain $V_{DD} \geqslant V_1 \geqslant V_2/V_3 \geqslant \frac{V_{DD} + V_{EE}}{2} - 1\ V \geqslant V_4/V_5 \geqslant V_{EE}$.
2. Outputs open, inputs at V_{SS} or V_{DD}.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.
5. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

Fig. 3 Test loads.

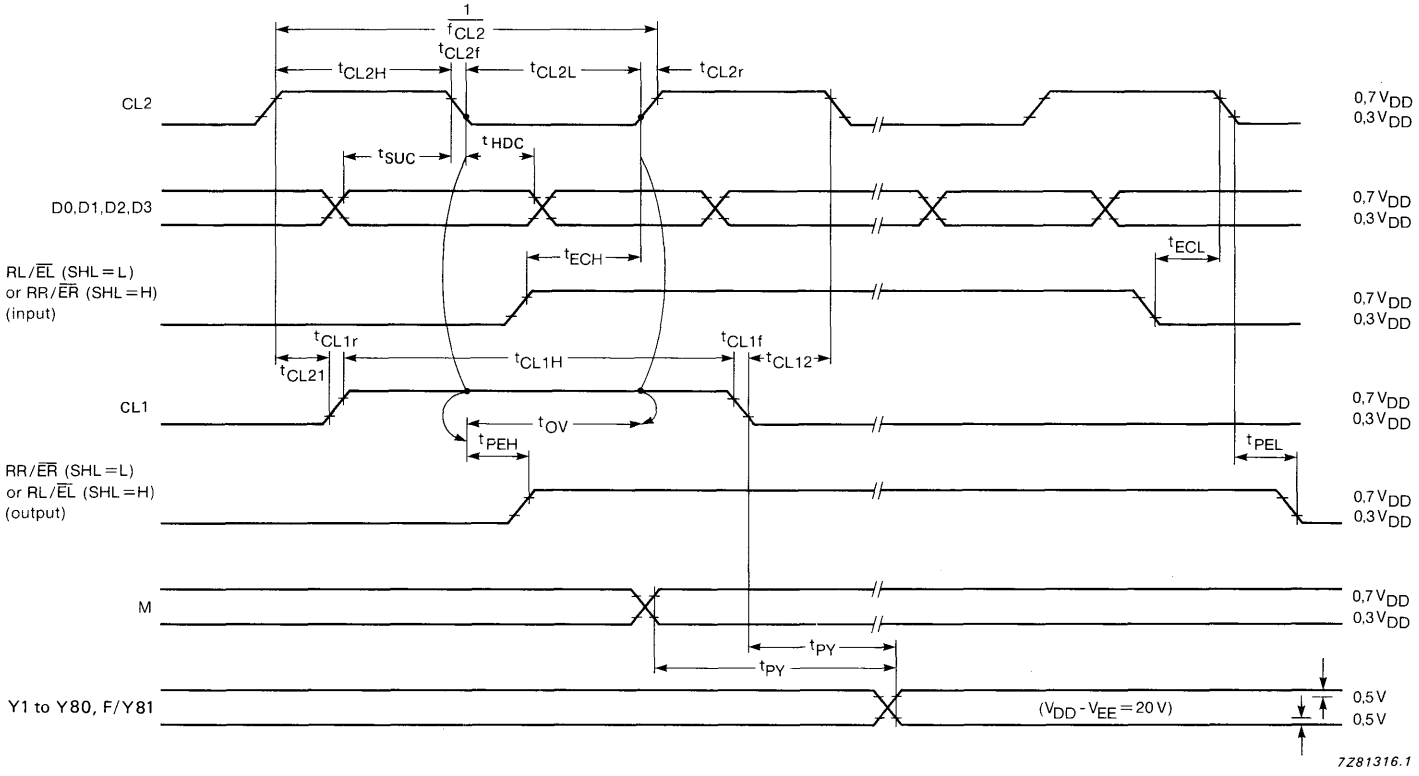


Fig. 4 Column driver timing waveforms.

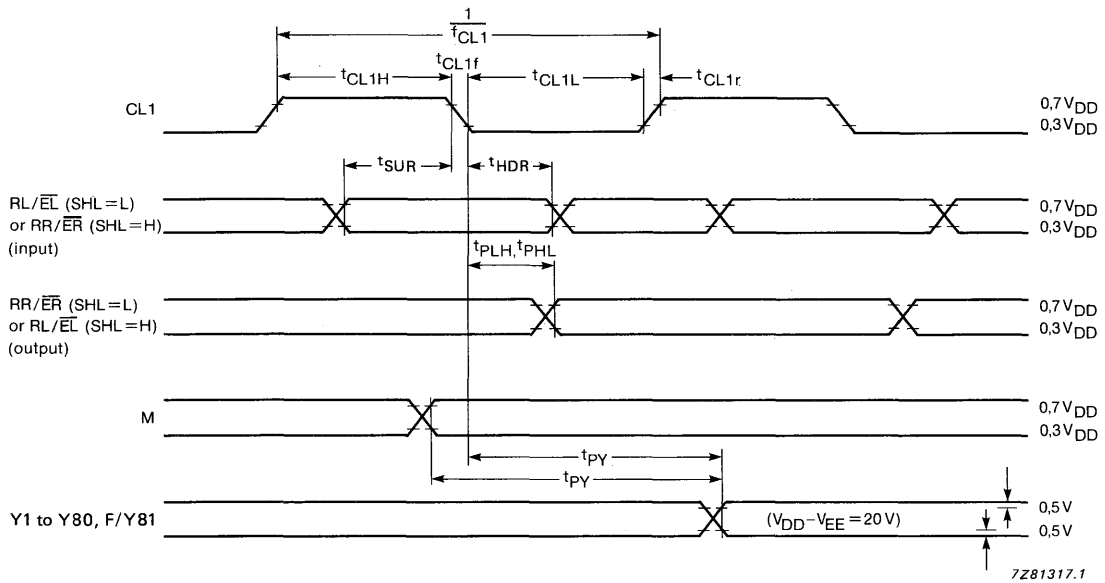


Fig. 5 Row driver timing waveforms.

APPLICATION INFORMATION

Generation of LCD bias levels

Optimum contrast for LCD flat-panels is achieved when the bias levels are selected using the formulae in Table 1. The multiplex rate is denoted by the variable n ($n \geqslant 9$). V_{th} is defined as the LCD threshold voltage, typically where the LCD exhibits approximately 10% contrast. The ratio of the 'ON' voltage to the 'OFF' voltage is discrimination (D) and is a measure of the flat-panel contrast at a given multiplex rate.

Table 1 LCD flat-panel bias levels for optimum contrast ($V_{op} = V1 - V_{EE}$)

$\frac{V_2}{V_{op}} = \frac{\sqrt{n}}{\sqrt{n}+1}$	$\frac{V_3}{V_{op}} = \frac{\sqrt{n}-1}{\sqrt{n}+1}$	$\frac{V_4}{V_{op}} = \frac{2}{\sqrt{n}+1}$	$\frac{V_5}{V_{op}} = \frac{1}{\sqrt{n}+1}$
$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}}$		$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n}+\frac{\sqrt{n}-1}{n(\sqrt{n}+1)}}$	
$D = \frac{V_{on(rms)}}{V_{off(rms)}} = \frac{\sqrt{n-1}}{\sqrt{n}-1}$		$\frac{V_{op}}{V_{th}} = \frac{\sqrt{n}+1}{\sqrt{2(1-1/\sqrt{n}}}$	

The intermediate bias levels are generated by a resistive divider (see Fig. 6). Capacitors (C) are used to smooth out switching transients. Considerable power consumption may result by using this arrangement when driving a large LCD flat-panel, because of the low impedance of the resistive divider.

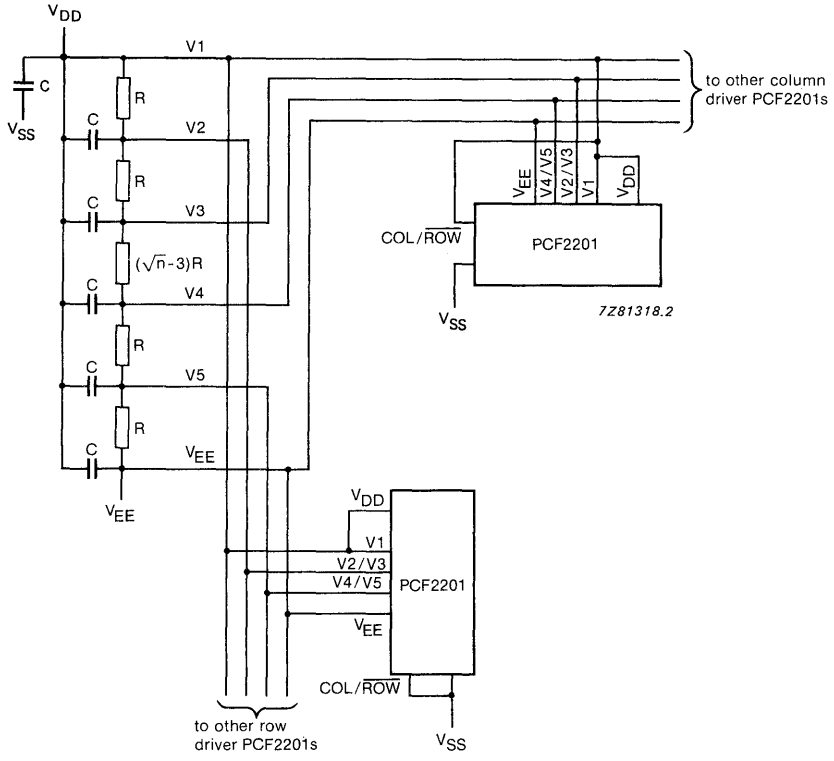


Fig. 6 Unbuffered LCD biasing level generation.

DEVELOPMENT DATA

A better solution for LCD flat-panel biasing is presented in Fig. 7. The operational amplifiers provide low impedance biasing with a low power consumption. The fairly high impedance which can be implemented at the resistive divider, helps maintain low power consumption. One diode voltage drop seperates V1 from V_{DD} to compensate for the limited common mode voltage range (V+ −1,5 V) when the operational amplifiers are powered between V_{DD} and V_{EE}.

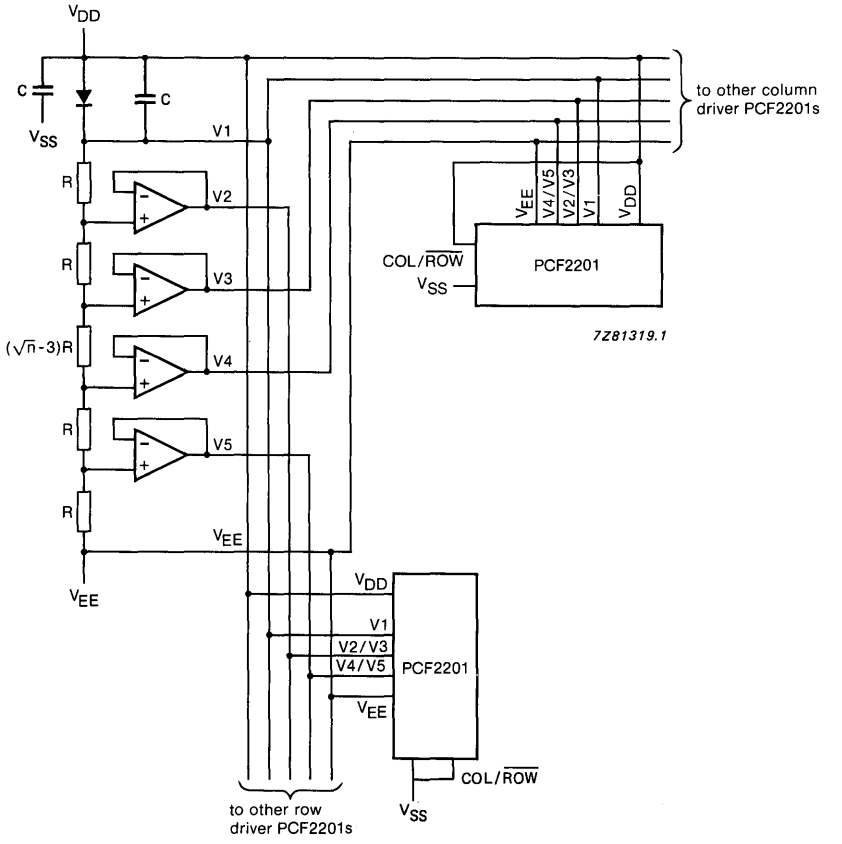


Fig. 7 Buffered LCD bias level generation.

Typical LCD flat-panel application

Alphanumeric/graphic computer terminals with LCD flat-panel screens using 200 x 640 dots are very popular. The format of 200 x 640 is compatible with the standard 25 lines by 80 characters at 8 x 8 dot character fonts. Fig. 8 gives a possible circuit using 19 PCF2201's, with upper and lower half screens used for good contrast. The use of half screens reduces the multiplex rate to 1:100 (Fig. 9 gives the timing information).

DEVELOPMENT DATA

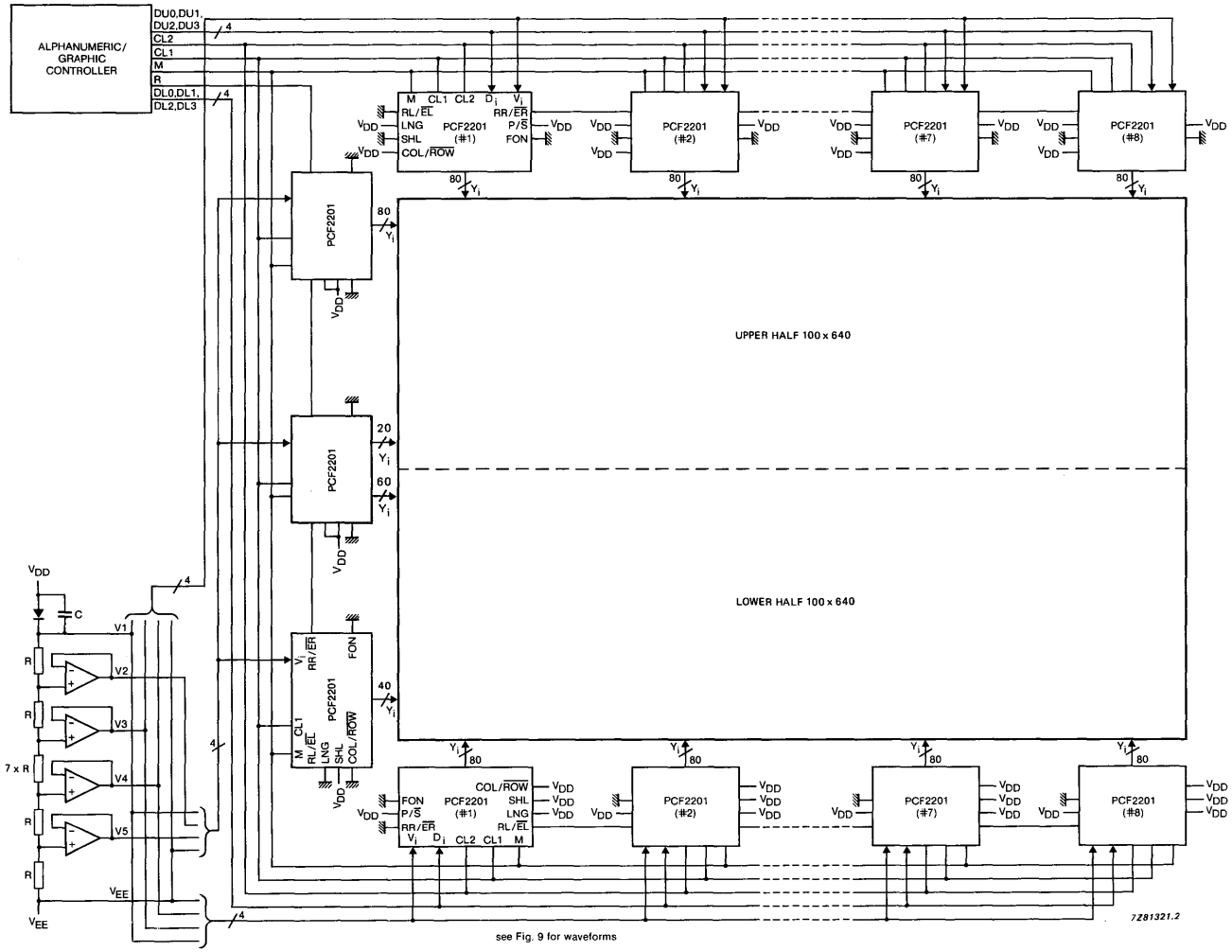


Fig. 8 LCD flat-panel with 1:100 multiplex rate in upper and lower half screens.

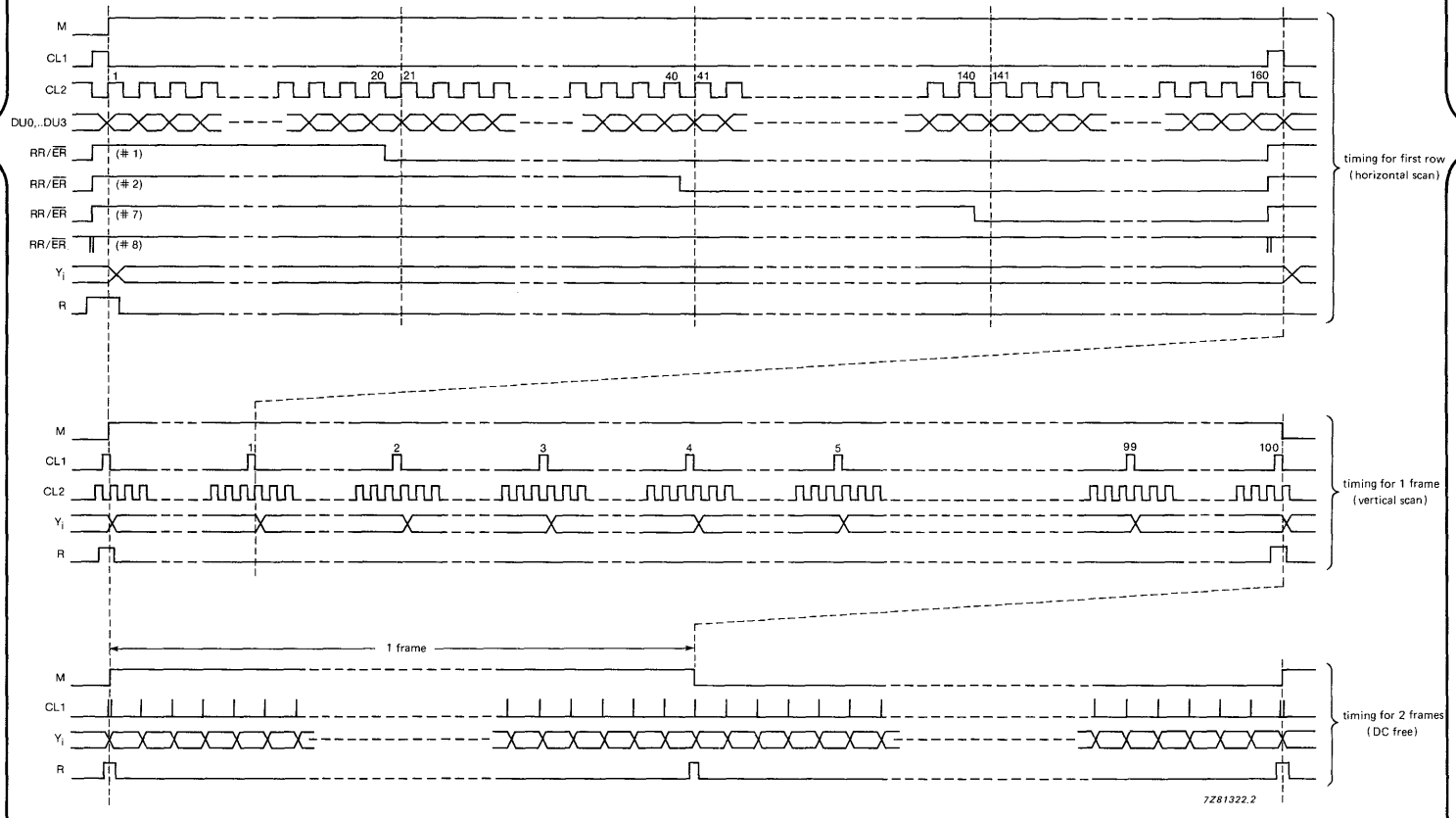
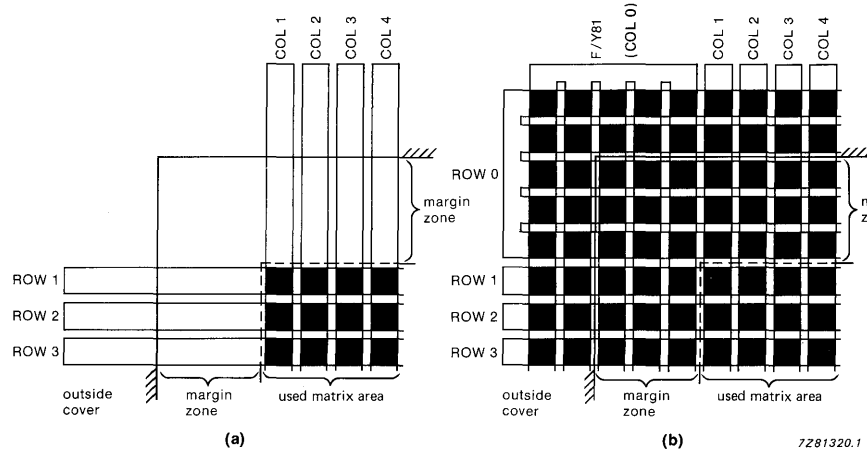


Fig. 9 Timing for the upper half screen of the LCD flat-panel (Fig. 8). For the lower half screen, replace RR/$\overline{ER}$, DU0, DU1, DU2 and DU3 with RL/$\overline{EL}$, DL0, DL1, DL2, DL3.

Margin control

The used area of the flat-panel matrix is normally smaller than the LCD glass surface. Connection lines outside of the used area of the matrix carry row or column LCD signals (see Fig. 10A). This 'null' state differs slightly in colour from the 'OFF' state pixel for twisted nematic LCD. The structural change in the margin zone is noticeable.

When a high contrast Philips LCD flat-panel of the supertwisted birefringence effect (SBE) type is employed, the situation becomes critital. The colour of the 'OFF' state appears blue and the colour of the 'ON' state appears grey or white. Therefore inverted information is sent to the display, generating dark (blue) characters on a light (grey) background. The margin zone is treated as an extension of the used matrix area (see Fig. 10B), to avoid the margin zone appearing as a dark blue frame. This is extended out to a region where the LCD glass can be covered up. The additional row requires an increase in the multiplex rate from n to n + 1, the additional column is realized by the frame output of the furthest left and right column drivers of the flat-panel. This removes the requirement for additional column drivers packages to provide margin control.



(A) without margin control

(B) with margin control

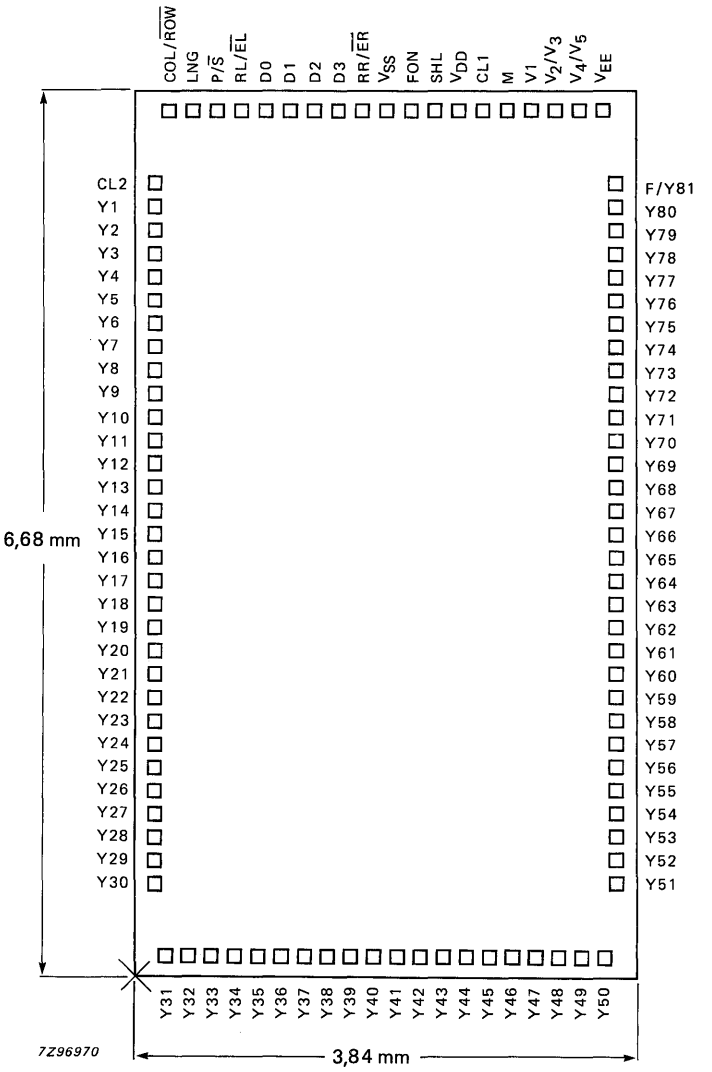
Fig. 10 Upper left corner of the LCD flat-panel.

Single plane wiring

The pinning of the PCF2201 tape-automated bonding package has been selected for ease of wiring. One side of this package contains no pins. The adjacent logic level lines are arranged so that they can be bussed in a single plane on the printed circuit board, which allows single sided substrates to be used.

For ease of wiring layout it is suggested to use the bus-level numbers (see Fig. 2) since most supply lines can be run through at the same level. On the actual package there are 120 pins, of which 19 pins are not internally connected. These extra pins are due to single plane wiring gaps and enhance stability in surface mounting.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 25,65 mm^2

Bonding pad dimensions: 104 μm x 104 μm

Fig. 11 Bonding pad locations.

DEVELOPMENT DATA

Table 2 Bonding pad centre locations (dimensions in μm)

All x/y co-ordinates are referenced to the bottom left corner, see Fig. 11.

pad	X	Y	pad	X	Y
D3	1556	6526	Y43	2364	154
D2	1372	6526	Y44	2540	154
D1	1188	6526	Y45	2716	154
D0	1004	6526	Y46	2892	154
RL/$\overline{EL}$	820	6526	Y47	3068	154
P/$\overline{S}$	636	6526	Y48	3244	154
LNG	452	6526	Y49	3420	154
COL/$\overline{ROW}$	268	6526	Y50	3596	154
CL2	156	5982	Y51	3684	702
Y1	156	5806	Y52	3684	878
Y2	156	5630	Y53	3684	1054
Y3	156	5454	Y54	3684	1230
Y4	156	5278	Y55	3684	1406
Y5	156	5102	Y56	3684	1582
Y6	156	4926	Y57	3684	1758
Y7	156	4750	Y58	3684	1934
Y8	156	4574	Y59	3684	2110
Y9	156	4398	Y60	3684	2286
Y10	156	4222	Y61	3684	2462
Y11	156	4046	Y62	3684	2638
Y12	156	3870	Y63	3684	2814
Y13	156	3694	Y64	3684	2990
Y14	156	3518	Y65	3684	3166
Y15	156	3342	Y66	3684	3342
Y16	156	3166	Y67	3684	3518
Y17	156	2990	Y68	3684	3694
Y18	156	2814	Y69	3684	3870
Y19	156	2638	Y70	3684	4046
Y20	156	2462	Y71	3684	4222
Y21	156	2286	Y72	3684	4398
Y22	156	2110	Y73	3684	4574
Y23	156	1934	Y74	3684	4750
Y24	156	1758	Y75	3684	4926
Y25	156	1582	Y76	3684	5102
Y26	156	1406	Y77	3684	5278
Y27	156	1230	Y78	3684	5454
Y28	156	1054	Y79	3684	5630
Y29	156	878	Y80	3684	5806
Y30	156	702	F/Y81	3684	5982
Y31	252	154	V_{EE}	3580	6526
Y32	428	154	V_4/V_5	3396	6526
Y33	604	154	V_2/V_3	3212	6526
Y34	780	154	V1	3028	6526
Y35	956	154	M	2844	6526
Y36	1132	154	CL1	2660	6526
Y37	1308	154	V_{DD}	2476	6526
Y38	1484	154	SHL	2292	6526
Y39	1660	154	FON	2108	6526
Y40	1836	154	V_{SS}	1924	6526
Y41	2012	154	RR/$\overline{ER}$	1740	6526
Y42	2188	154			