PCF50606HN/xA/N1 PCF50606HN/xB/N1 PCF50605HN/xA/N1 PCF50605HN/xB/N1

Controller for Power Supply and Battery Management

Rev. 2.2 — 9 April 2004 Preliminary Specification

1. General description

The PCF50606 and PCF50605 are highly integrated solutions for power supply generation, battery management, and dedicated mobile system functions. A built-in step down DC/DC converter provides a highly power efficient supply for a digital core, while 2 additional DC/DC converters and 5 low dropout regulators are available to supply all other functions in mobile systems. Furthermore, the PCF50606 provides a 10-bit ADC and touch screen readout support. Both devices enables a very efficient system deep sleep state since it incorporates a real time clock and several wake up functions. They can be controlled by a host controller via an I2C serial interface and several dedicated pins. An intelligent interrupt system signals the host controller about many power management events.

Whenever PCF50606 is mentioned in this document, this refers to both PCF50605 and PCF50606, unless a difference is noted. This document describes bondout versions A and B; a separate specification is available of bondout version E.

! Next to this specification document, several application notes exist which describe application advices and known limitations. It is strongly recommended to read these documents before starting design activities.

2. Features

- The PCF50606 operates from a 1 cell Li-Ion/Li-Polymer or a 3 cell NiCd/NiMH battery pack.
- A serial interface (I2C) provides the exchange of information for the control data and status between the PCF50606 and the host controller.
- Low power 32786Hz Xtal oscillator.
- Internal current controlled oscillator that generates the internal system clock.
- Interrupt controller that generates the interrupt request for the host controller. All interrupt sources can be masked.
- A 8s watchdog timer (hereafter WDT), which shuts down the PCF50606 when it expires after it is activated once. This watchdog can be reset through the I2C interface.
- A fully integrated 500mA step-down converter (hereafter DCD) with programmable output voltages, mask programmable reset voltage and operation mode. This DC/DC converter generates typically the host controller core supply voltage or is used as pre-regulator for sub 2V regulators to improve the power efficiency of such a configuration.

- A fully integrated DC/DC converter (hereafter DCUD) with programmable output voltages, mask programmable reset voltage and operation mode. This converter can be configured as a step-up with currents up to 250mA and as step down converter, with currents up to 500mA. This converter is typically used as back-light / White LED supply in step-up mode. In step down configuration this converter generates low supply voltages or is used as pre-regulation stage for linear regulators to improve the power efficiency.
- A DC/DC step down controller (hereafter DCDE) with build-in drivers for external power fets for high current outputs, programmable output voltage and mask programmable reset voltage and operation mode. This converter is typically used to generate high current supply voltages for memory systems or accessories.
- One 150mA low-dropout (LDO) voltage regulator (IOVDD) with programmable output voltage and mask programmable reset voltage. This regulator also supplies all pins of PCF50606 interfacing to the host controller.
- Three 150mA LDO voltage regulators (D1VDD till D3VDD) with programmable output voltage. Its reset value is mask programmable.
- One 150 mA LDO voltage regulator (LPVDD) with programmable output voltage and mask programmable reset voltage and operation mode. In its ECO mode (low power operation mode), it can be kept activated permanently, independent of the activation state of the PCF50606.
- Dynamic Voltage Management is supported on the DCD step-down converter. This allows to switch between pre-defined (through the I2C interface) output voltage settings under control of the PWREN inputs.
- Battery voltage monitor (hereafter BVM) to detect a too low main battery voltage with programmable threshold levels.
- Main battery charger (hereafter MBC) to charge Li-ion/Li-polymer batteries and 3 cell NiMH/NiCd batteries.
  - Constant Current / Constant Voltage charging method for Li-ion/Li-pol batteries with external adjusted fast charge current and programmable maximum battery voltage
  - supports fully autonomous charging of Li-ion/Li-polymer batteries without interaction of the host controller or a fully host controlled charging sequence.
  - Supports the use of controlled charger plug through build in switch mode.
  - Includes extensive safety features, including charger over voltage and over current detection, battery voltage and temperature monitoring and a dedicated watchdog / charge timer circuit.
- Includes a backup battery charger (hereafter BBC). A rechargeable backup battery can be charged from the main battery. For charging, a programmable constant voltage mode is supported.
- 10 bits analog to digital converter with analog input multiplexer. The built-in voltage divider on the BATVOLT input allows direct connection of the battery voltage to this input
  - The built-in voltage divider and subtractor circuit on the BATVOLT / ADCIN1 inputs allows direct connection of the battery voltage to these pin, without external voltage dividers and without resolution losses.
  - The accessory detection comparator connected to the ADCIN2 input issues an interrupt when an accessory is connected.

- The ADC can be synchronized to any combination of the PWREN and TXON signals. This allows to synchronize the ADC sampling to the host controller operation mode and/or the ‘TDMA’ frame of a wireless link.

- The touchscreen interface provides the read-out of a resistive 4 wire touchscreen.
  - generates an interrupt when the touchscreen is pressed.
  - biases the touchscreen during X and Y coordinate measurements and multiplexes the touchscreen terminal to the ADC input.
  - Combined X and Y position or P1 and P2 plate resistor measurements are executed through a single I2C command.
- The Real Time Clock module (hereafter RTC) uses the 32 kHz clock to provide time reference and alarm functions with wake up control for the handset.
- One pulse-width modulator (hereafter PWM): generating a output voltage with programmable duty cycle and frequency.
- Two LED modulators (hereafter LED) capable of generating 8 different blinking patterns with 4 different repetition periods.
- General Purpose Outputs (hereafter GPO), programmable through the serial interface. Two of these GPOs are CMOS outputs supplied from the IOVDD supply.

  The other GPOs are open drain NMOST outputs, capable of handling the full battery voltage range and high sink currents.

  The GPOs can be programmed continuously low or high. In addition the GPO outputs can be controlled by the LED or PWM modulator and several other signals like PWROK.
- The temperature high sensor provides thermal protection for the whole chip.
- Enhanced ESD protection (4kV) on all pins that connect to the main battery pack.

3. Applications

- PDA’s
- Portable audio systems
- Multimedia phones

4. Quick reference data

Table 1: Quick reference data

V_{SS} = REFGND = GND = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VBAT}	Main battery input voltage		0	-	6.0	V
V_{VBACK}	Backup battery input voltage		0	-	6.0	V
V_{CHGVIN}	Charger input voltage	DC	0	-	15.0	V
V_{VINT}	Internal supply voltage	V_{VBAT} > 3.0 V	2.5	2.7	2.9	V
		V_{VBAT} <2.7V and (V_{VBACK}>3.0 or V_{CHGVIN}>3.0)	2.4		3.0	V
$V_{VERYLOWBAT}$	Main battery presence threshold voltage		-	2.7	-	V
$V_{LOWBACK}$	Backup battery presence threshold voltage		-	1.3	-	V
V_{LOWCHG}	Charger presence threshold voltage		-	2.7	-	V
F_{CLKCCO}	High clock frequency	32 kHz clock available	-3%	3.6	+3%	MHz
		32 kHz clock not available	-10%	3.6	+10%	MHz

Table 2: Overview power supplies

V_{SS} = REFGND = GND = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.

Supply Name	Nominal current	Min. voltage	Max voltage	Voltage steps	Reset voltage	ECO Mode	Configu-ration	PSRR [1]	Size ext. capacitor
Programmable power supplies									
IOREG	150 mA	1.80 V	3.30 V	100 mV	[2]	yes	-	60 dB	470 nF
D1REG	150 mA	0.90 V	3.30 V	100 mV	[2]	yes	-	60 dB	470 nF
D2REG	150 mA	0.90 V	3.30 V	100 mV	[2]	yes	-	60 dB	470 nF
D3REG	150 mA	0.90 V	3.30 V	100 mV	[2]	yes	-	60 dB	470 nF
LPREG	150 mA	0.90 V	3.30 V	100 mV	[2]	yes	-	60 dB	470 nF
Programmable DC/DC converters									
DCD	500 mA	0.90 V	3.30 V	25 mV / 300mV	[2]	yes	down	-	[3]
DCDE	[4]	0.90 V	3.30 V	300 mV	[2]	yes	down	-	[3]
DCUD	500 mA (down) 250mA (up)	0.90 V	5.50 V	300mV / 100 mV	[2]	yes	up or down	-	[3]

[1] Typical value, 100 Hz < f < 1000 Hz.

[2] For reset settings of different types, see Section 8.24 “PCF50606 variants”

[3] External components are determined by the application requirements

[4] Output currents are determined by external components

Table 3: Total power consumption overview

V_{SS} = REFGND = GND = 0 V; V_{VBAT}= 3.6 V; V_{VBACK} < 5.7 V; 32 kHz oscillator or external clock available; unless otherwise specified.

External Loads not included in calculations unless specified

Conditions	Symbol	Description	Typ	Max	Unit
NOPOWER state supply from main battery V_{VBAT} < $V_{VERYLOWBAT}$ V_{VBACK} < $V_{LOWBACK}$	$I_{TOT,NOP}$	Total current, T_{amb} = +25 °C	10	20	µA
	$I_{TOT,NOP}$	Total current, T_{amb} = +25 °C, no 32 kHz clock available	80	120	µA
	$I_{TOT,NOP}$	Total current, T_{amb} = -40 to +85 °C		30	µA
SAVE state supply from backup battery V_{VBACK} > $V_{LOWBACK}$ LPREG = OFF	$I_{TOT,SAVE}$	Total current, T_{amb} = +25 °C	25	40	µA
	$I_{TOT,SAVE}$	Total current, T_{amb} = +25 °C, no 32 kHz clock available	80	120	µA
	$I_{TOT,SAVE}$	Total current, T_{amb} = -40 to +85 °C		55	µA
STANDBY state: supply from main battery V_{VBAT} > $V_{VERYLOWBAT}$ LPREG = OFF	$I_{TOT,STDBY}$	Total current, T_{amb} = +25 °C	30	55	µA
	$I_{TOT,STDBY}$	Total current, T_{amb} = +25 °C, no 32 kHz clock available	55	65	µA
	$I_{TOT,STDBY}$	Total current, T_{amb} = -40 to +85 °C		80	µA
ACTIVE state 1 (ECO) Supply from main battery V_{VBAT} = 3.6V All supply modules in ECO mode, no load	$I_{TOT,ACTECO}$	Total current, T_{amb} = +25 °C	600		µA
	$I_{TOT,ACTECO}$	Total current, T_{amb} = -40 to +85 °C	800		µA
ACTIVE state 2 (SLEEP): Supply from main battery V_{VBAT} = 3.6V IOREG in ECO mode, all other supply modules in OFF mode, no load	$I_{TOT,ACTSLP}$	Total current, T_{amb} = +25 °C	75	110	uA
	$I_{TOT,ACTSLP}$	Total current, T_{amb} = +25 °C, no 32 kHz clock available	105	130	uA
	$I_{TOT,ACTSLP}$	Total current, T_{amb} = -40 to +85 °C		150	uA
ACTIVE state 3 (ON): Supply from main battery V_{VBAT} = 3.6V All supply modules in ON mode, no load	$I_{TOT,ACTON}$	Total current, T_{amb} = +25 °C	1000	1200	uA
	$I_{TOT,ACTON}$	Total current, T_{amb} = -40 to +85 °C		1500	uA

4.1 Definitions and abbreviations

Table 4: Definitions and abbreviations

Abbreviation	Description
C	Unit used to indicate a battery charging current. 1C is the current which fully charges an empty battery in 1 hour.
ACD	accessory detection
ADC	Analog to Digital Converter
BBC	Backup Battery Charger
BVM	Battery Voltage Monitor
CCO	Current Controlled Oscillator
CLKCCO	Internal high clock frequency generated by the CCO.
CDM	Calibration Data Memory
CGU	Clock Generator Unit
DxREG	Dx linear regulator
DCD	DC/DC down converter with internal switches
DCDE	DC/DC down converter with external switches
DCUD	DC/DC configurable as UP or DOWN converter with internal switches
EOC	End-of-Charge
GPO(OD)	General Purpose Output (with Open Drain)
I2C	Inter IC serial interface
INT	Interrupt handler
IOREG	IO linear regulator
ISM	Internal Supply Module
LDO	Low Drop-Out (used for linear regulators)
LEDx	Light-Emitting-Diode driver
V_{LOWBAT}	Threshold for the decision that the main battery voltage is high enough for full operation
LPREG	Low-power linear regulator
MBC	Main Battery Charger
mode	Module activity definition: OFF,ECO or ON
n.a.	Not applicable; not relevant in this context
OCR	On-Chip Reference voltage (and current) generator
OOC	On/Off Controller
OSC32	32 kHz Oscillator module
PWMx	Pulse-Width-Modulator
R&C	Register bit type “read and clear”. After a read access, the read bit is cleared.
R/W	Register bit type “read and write”. The bit can be written and read.
REFGND	Ground Voltage Reference for all internal analog circuits; unless otherwise stated all voltages in this specification refer to REFGND.
RTC	Real-Time Clock
state	System activity definition: NOPOWER, SAVE, STANDBY, ACTIVE
TSC	Touch Screen Control

Table 4: Definitions and abbreviations *...continued*

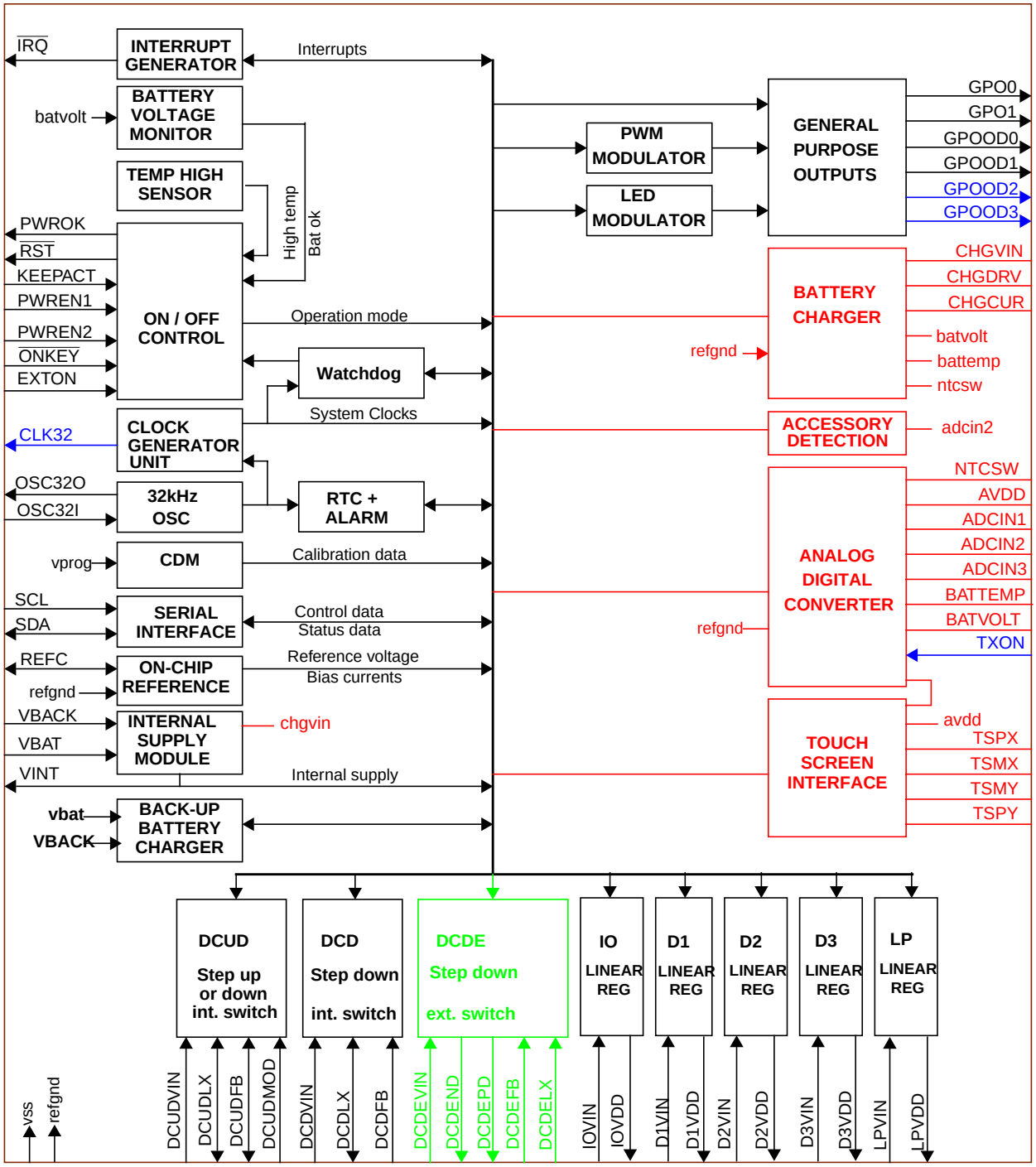
Abbreviation	Description
t.b.s.	To be specified: will be specified in the final Product Specification.
THS	Temperature High Sensor
$V_{LOWBACK}$	Threshold for the decision that the backup battery is present
$V_{VERYLOWBAT}$	Threshold for the decision that the main battery is present
V_{VBAT}	Main Battery Voltage
V_{VINT}	Internal supply Voltage
V_{CHGVIN}	Charger Voltage
V_{VBACK}	Backup Battery Voltage

5. Ordering information

Type number	Package	Description
PCF50605HN/xA/N1	HVQFN56 (SOT684-2)	PCF50605, bondout version A
PCF50605HN/xB/N1	HVQFN56 (SOT684-2)	PCF50606, bondout version B
PCF50606HN/xA/N1	HVQFN56 (SOT684-2)	PCF50606, bondout version A
PCF50606HN/xB/N1	HVQFN56 (SOT684-2)	PCF50606, bondout version B

[1] 'x' in type number code relates to the specific variant, see section 8.24.

6. Functional diagram



(1) black parts are common for all PCF50606 and PCF50605 versions.
PCF50606_A bondout version includes the blue & red parts; PCF50606_B bondout version includes the green & red parts;
PCF50605_A bondout version includes the blue parts; PCF50605_B bondout version includes the green parts.

Fig 1. Functional Diagram PCF50606 and PCF50605

7. Pinning information

7.1 Pin description

Signal	Version				Description	I/O [1]	Supply	Remark
	1 [2]	2 [3]	3 [4]	4 [5]				
BASIC FUNCTIONALITY								
VBAT	x	x	x	x	Supply pin for internal supply regulator and battery voltage monitor	I, A	-	
VBACK	x	x	x	x	Back-up battery or capacitor connection	IO, A	-	
VSS	x	x	x	x	Ground / substrate connection	I, A	-	connected to the package ground plane
REFGND	x	x	x	x	Reference ground	I, A	-	
VINT	x	x	x	x	internal supply voltage decoupling	IO, A	-	
REFC	x	x	x	x	internal reference voltage decoupling	IO, A	-	
$\overline{\text{ONKEY}}$	x	x	x	x	Power On Key input	I, D, PU	VINT	debounced
$\overline{\text{RST}}$	x	x	x	x	Reset	O, D, PU	IOVDD	
$\overline{\text{IRQ}}$	x	x	x	x	interrupt	O, D, OD	IOVDD	
PWROK	x	x	x	x	Power OK status output	O, D	IOVDD	
OSC32I	x	x	x	x	32k xtal oscillator input	I, A	VINT	
OSC32O	x	x	x	x	32k xtal oscillator output	O, A	VINT	
CLK32	x		x		32.786Hz clock output	O, D	IOVDD	
SCL	x	x	x	x	I2C clock input	I, D	IOVDD	No ESD diodes to IOVDD, can be pull up to VBAT
SDA	x	x	x	x	I2C data	IO, D	IOVDD	No ESD diodes to IOVDD, can be pull up to VBAT
KEEPACT	x	x	x	x	Feedback from host processor	I, D	IOVDD	
PWREN1	x	x	x	x	Operation state selection 1	I, D	IOVDD	
PWREN2	x	x	x	x	Operation state selection 2	I, D	IOVDD	
EXTON	x	x	x	x	External activation input	I, D	-	debounced can be pulled up to 6V
SUPPLIES								
IOVIN	x	x	x	x	Input for IO regulator	I, A	-	
IOVDD	x	x	x	x	IO regulator output	O, A	-	Supplies the digital I, O and IO pins of the PCF50606
LPVIN	x	x	x	x	Input for LP regulator	I, A	-	
LPVDD	x	x	x	x	LP regulator output	O, A	-	
D1VIN	x	x	x	x	input for D1 regulator	I, A	-	
D1VDD	x	x	x	x	D1 regulator output	O, A	-	
D2VIN	x	x	x	x	input for D2 regulator	I, A	-	

Signal	Version				Description	I/O [1]	Supply	Remark
	1 [2]	2 [3]	3 [4]	4 [5]				
D2VDD	x	x	x	x	D2 regulator output	O, D	-	
D3VIN	x	x	x	x	input for D3 regulator	I, A	-	
D3VDD	x	x	x	x	D3 regulator output	O, A	-	
DCDVIN	x	x	x	x	Input of DCDC step down	I, A	-	
DCDLX	x	x	x	x	Coil DCDC step down	IO, A	-	
DCDGND	x	x	x	x	Ground DCDC step down switches	IO, A	-	connected to the package ground plane
DCDFB	x	x	x	x	Output sense of DCDC step down	I, A	-	
DCUDVIN	x	x	x	x	Input of DCDC step up or down	I, A	-	
DCUDLX	x	x	x	x	Coil DCDC step up or down	IO, A	-	
DCUDFB	x	x	x	x	DCDC step up or down output / feedback input	IO, A	-	
DCUDGND	x	x	x	x	Ground DCDC step up or down switches	IO, A	-	connected to the package ground plane
DCUDMOD	x	x	x	x	DCDC step up or down mode selection input	I, D	VINT	
DCDEVIN		x		x	Input of DCDC step down with external transistors	I, A	-	
DCDEPD		x		x	External PMOST driver Output DCDC step down with ext. trans.	O, D	DCDEVIN	
DCDEND		x		x	External NMOST driver Output DCDC step down with ext. trans.	O, D	DCDEVIN	
DCDEFB		x		x	DCDC step down with external transistors feedback input	I, A	-	
DCDELX		x		x	DCDC step down with external transistors coil feedback input	I, A	-	
DCDEGND		x		x	Ground DCDC step down with external switches	IO, A	-	connected to the package ground plane
ADC								
AVDD	x	x	x	x	ADC supply / touch screen bias voltage	I, A		
BATVOLT	x	x			Battery voltage ADC input, Battery voltage sense input for charger and low battery voltage monitor	I, A	-	Built-in voltage divider and subtractor circuit Shared input with MBC module
BATTEMP	x	x			Battery temperature input	I, A	-	Shared input with MBC module
ADCIN1	x	x			Additional high voltage ADC input	I, A	-	Built-in voltage divider and subtractor circuit
ADCIN2	x	x			Additional ADC input	I, A	-	with accessory detection comparator
ADCIN3	x	x			Additional ADC input	I, A	-	
TXON	x				ADC synchronization input	I, D	IOVDD	

Signal	Version				Description	I/O [1]	Supply	Remark
	1 [2]	2 [3]	3 [4]	4 [5]				
TOUCH SCREEN								
TSPX	x	x			positive Xplate terminal touch screen	IO, A	AVDD	
TSMX	x	x			negative Xplate terminal touch screen	IO, A	AVDD	
TSPY	x	x			positive Yplate terminal touch screen	IO, A	AVDD	
TSMY	x	x			negative Yplate terminal touch screen	IO, A	AVDD	
TSGND	x	x			Touch screen ground	I, A	-	connected to the package ground plane
CHARGER								
CHGVIN	x	x			Charger voltage input	I, A	-	
CHGDRV	x	x			Drive of external circuit	O, A	-	
CHGCUR	x	x			Charge current feedback	O, A	-	
NTCSW	x	x			Switched bias voltage for external NTC bridge	O, A	-	Combined with ADC module
GENERAL PURPOSE OUTPUTS								
GPO0	x	x	x	x	General purpose output	O, D	IOVDD	By default this pin is BATOK
GPO1	x		x		General purpose output	O, D	IOVDD	
GPOOD0	x	x	x	x	General purpose open drain output	O, D,OD		
GPOOD1	x	x	x	x	General purpose open drain output	O, D,OD		
GPOOD2	x		x		General purpose open drain output	O, D,OD		
GPOOD3	x		x		General purpose open drain output	O, D,OD		

[1] Coding:
I = input, O = Output, IO = in/output
A = analog, D = digital
PU = pull-up, PD = pull-down, OD = open drain

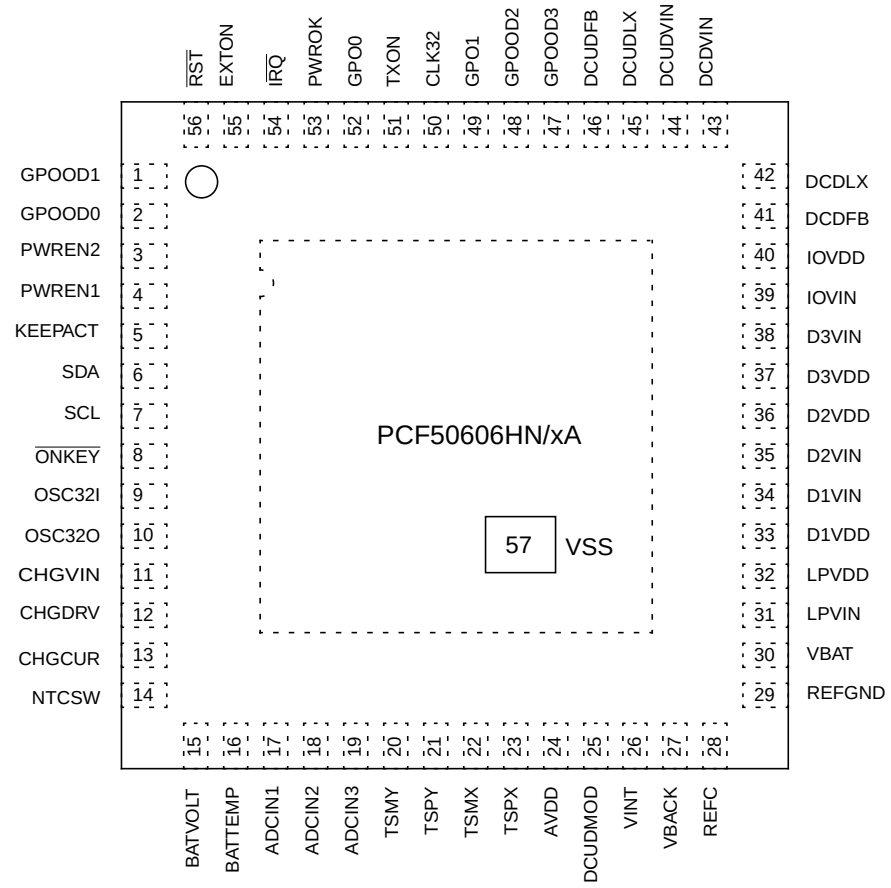
[2] Non marked pins are not available on the PCF50606-A bond-out version

[3] Non marked pins are not available on the PCF50606-B bond-out version

[4] Non marked pins are not available on the PCF50605-A bond-out version

[5] Non marked pins are not available on the PCF50605-B bond-out version

7.2 Pinning



(1) This diagram is a TOP side (or die side) view.

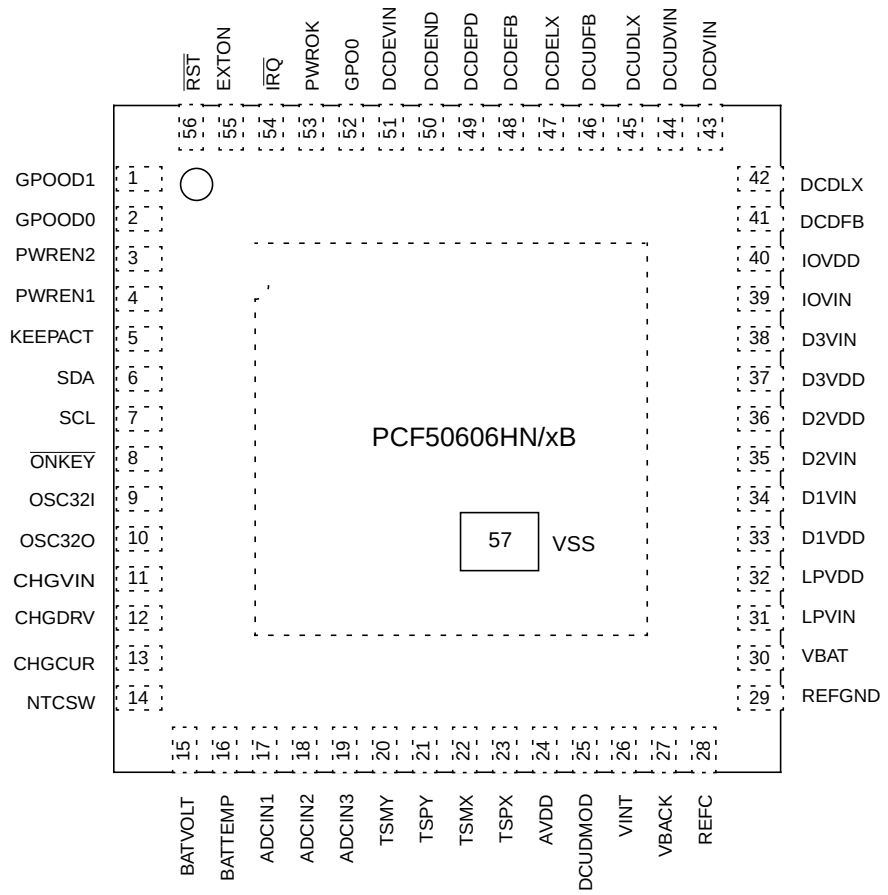
(2) Pin 1 is indicated with a dot in the upper left corner

(3) For mechanical specification of HVQFN56 package, see figure 67 “Package outline SOT684-2 (HVQFN56 with 5.20 x 5.20 mm nominal diepad size)”

(4) Pin 57 is the groundplane at the bottom of the package. It must be connected to the PCB groundplane.

(5) The ‘x’ in the type number refers to the variant, see section 8.24.

Fig 2. Pin configuration PCF50606_A, bond-out version A in HVQFN56 package



(1) This diagram is a TOP side (or die side) view.

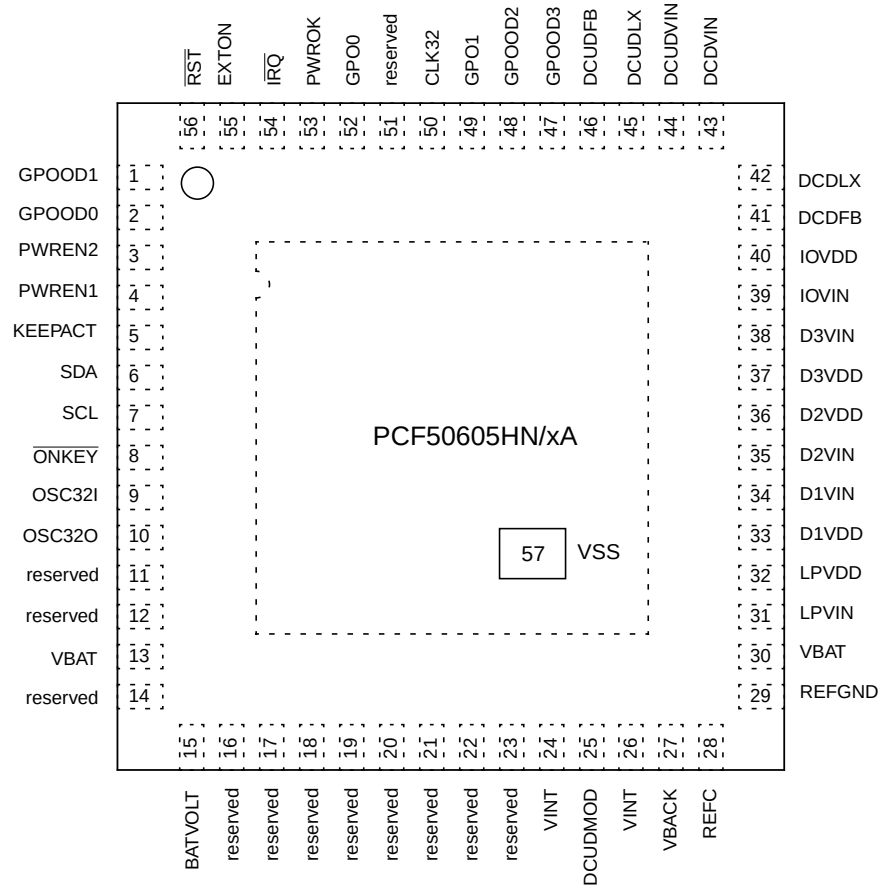
(2) Pin 1 is indicated with a dot in the upper left corner

(3) For mechanical specification of HVQFN56 package, see figure 67 “Package outline SOT684-2 (HVQFN56 with 5.20 x 5.20 mm nominal diepad size)”

(4) Pin 57 is the groundplane at the bottom of the package. It must be connected to the PCB groundplane.

(5) The ‘x’ in the type number refers to the variant, see section 8.24.

Fig 3. Pin configuration PCF50606_B, bond-out version B in HVQFN56 package



(1) This diagram is a TOP side (or die side) view.

(2) Pin 1 is indicated with a dot in the upper left corner

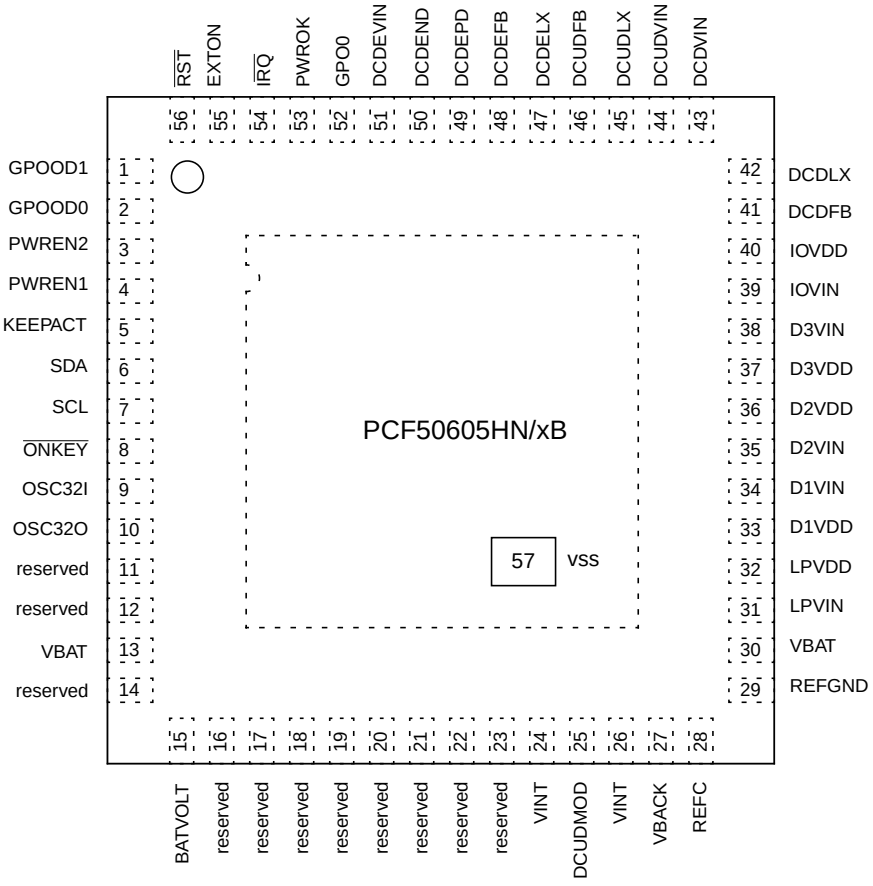
(3) For mechanical specification of HVQFN56 package, see figure 67 “Package outline SOT684-2 (HVQFN56 with 5.20 x 5.20 mm nominal diepad size)”

(4) Reserved pins should not be connected in the application

(5) Pin 57 is the groundplane at the bottom of the package. It must be connected to the PCB groundplane.

(6) The ‘x’ in the type number refers to the variant, see section 8.24.

Fig 4. Pin configuration PCF50605_A bond out version A in HVQFN56 package



(1) This diagram is a TOP side (or die side) view.

(2) Pin 1 is indicated with a dot in the upper left corner

(3) For mechanical specification of HVQFN56 package, see figure 67 “Package outline SOT684-2 (HVQFN56 with 5.20 x 5.20 mm nominal diepad size)”

(4) Reserved pins should not be connected in the application

(5) Pin 57 is the groundplane at the bottom of the package. It must be connected to the PCB groundplane.

(6) The ‘x’ in the type number refers to the variant, see section 8.24.

Fig 5. Pin configuration PCF50605_B bond out version B in HVQFN56 package

8. Functional description

8.1 On/Off control (OOC)

8.1.1 Activity states

The PCF50606 has 4 activity states:

- NOPOWER
  In the NOPOWER state the main battery, backup battery, charger supplies are below their threshold levels. None of the internal circuits has sufficient power to perform any function. The PCF50606 waits until either the main battery voltage, the backup battery voltage, or the charger voltage raises above the threshold.
- SAVE
  In the SAVE state, the PCF50606 is supplied by either the backup battery or the charger. The main battery voltage is still below its threshold. Only a minimum of modules are activated: the internal supply, the 32 kHz oscillator, the real-time clock, and the LPREG in ECO mode when enabled. All other power supplies are turned off and the external reset signal $\overline{RST}$ is de-asserted.
- STANDBY
  In the STANDBY state, the PCF50606 is supplied by the main battery. All power supplies are turned off (except for the LPREG in ECO mode if enabled) and the external reset $\overline{RST}$ signal is asserted, however all monitoring and control functions in the IC are activated.
- ACTIVE
  In the active state the PCF50606 is fully functional. The host controller has full control through the serial I^2C interface.

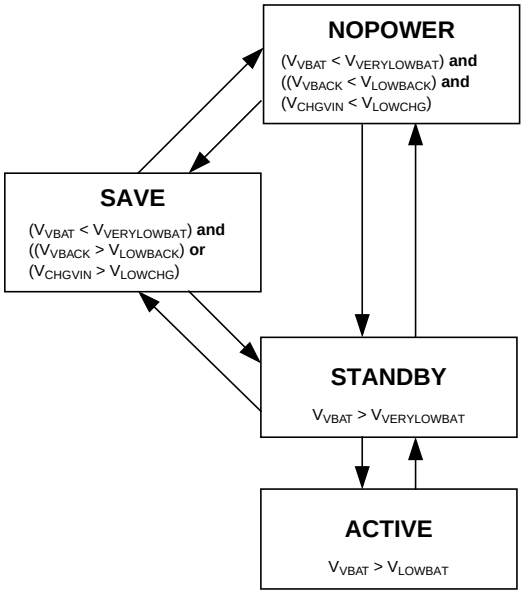


Fig 6. PCF50606 state diagram

Figure 6 shows the PCF50606 state diagram and Table 5 the module activity in each state.

Table 5: activity states and module activity

Module	NOPOWER	SAVE	STANDBY	ACTIVE
System control modules				
ISM	OFF	ON	ON	ON
OCR	OFF	ON	ON	ON
OSC32	OFF	ON	ON	ON
CCO	OFF	OFF/ON [2]	OFF/ON [2]	OFF/ON [3]
RTC	OFF	ON	ON	ON
OOC	OFF	OFF	ON	ON
INT	OFF	OFF	ON	ON
THS	OFF	OFF	OFF	ON
I2C	OFF	OFF	OFF	ON/OFF [4]
PWM	OFF	OFF	OFF	OFF/ON [1]
LED	OFF	OFF/ON [5] [6]	OFF/ON [5] [6]	OFF/ON [6]
GPO	OFF	OFF	ON	ON
GPOOD	OFF	ON	ON	ON
Supply modules				
DCD	OFF	OFF	OFF	ON/BYP/OFF [6]
DCDE	OFF	OFF	OFF	ON/BYP/OFF [6]
DCUD	OFF	OFF	OFF	ON/BYP/OFF [6]
IOREG	OFF	OFF	OFF	ON/ECO/OFF [6]
D1REG	OFF	OFF	OFF	ON/ECO/OFF [6]
D2REG	OFF	OFF	OFF	ON/ECO/OFF [6]
D3REG	OFF	OFF	OFF	ON/ECO/OFF [6]
LPREG	OFF	ECO/OFF [6]	ECO/OFF [6]	ON/ECO/OFF [6]
Battery Management modules				
BVM	OFF	OFF	ON	ON
MBC	OFF	ON [5]	ON [5]	OFF/ON [1] [5]
BBC	OFF	OFF	ON/OFF [1]	ON/OFF [1]
Others				
ADC	OFF	OFF	OFF	OFF/ON [1]
ACD	OFF	OFF	OFF	OFF/ON [1]

[1] When modules can have different activity modes in a activity state, the reset value is the first mentioned; the following modes can be programmed by the host controller.

[2] Module is enabled when no 32 kHz oscillator or external 32 kHz clock is available.

[3] Module is only enabled when a module requiring a high clock is active: DCD, DCDE, DCUD, I2C.

[4] Module is disabled when IOVDD in ECO mode.

[5] Module can be enabled when valid charger voltage is detected.

[6] Values after power-on reset are dependent on variant of IC. See Table 76 “Reset Settings”.

8.1.2 Transitions between activity states

The On/Off control controls the transitions between the activity states of the PCF50606.

Transition from NOPOWER to STANDBY:

The PCF50606 resides in the NOPOWER state when no source of power is available. When, in this situation, a charged main battery is inserted (battery voltage exceeds the $V_{VERYLOWBAT}$ threshold) a direct transition from NOPOWER to STANDBY occurs.

Transition from STANDBY to NOPOWER:

The PCF50606 goes from STANDBY directly back to NOPOWER when the main battery is discharged below the $V_{VERYLOWBAT}$ threshold and no other source of power is available.

A complete reset of the chip occurs when PCF50606 returns to the NOPOWER state.

Transition from NOPOWER to SAVE:

The PCF50606 resides in the NOPOWER state when no source of power is available. The PCF50606 enters the SAVE state when the main battery is empty V_{VBAT} below the $V_{VERYLOWBAT}$ threshold and either:

- Charged backup battery is inserted (V_{VBACK} exceeds the $V_{LOWBACK}$ threshold)
- Charger is connected (V_{CHGVIN} exceeds the V_{LOWCHG} threshold)

Transition from SAVE to NOPOWER:

The PCF50606 returns to the NOPOWER state when the backup battery voltage drops below the $V_{LOWBACK}$ threshold or when the charger is disconnected.

A complete reset of the chip occurs when PCF50606 returns to the NOPOWER state.

Transitions from SAVE to STANDBY:

When the PCF50606 is in SAVE state it waits until the main battery is above the $V_{VERYLOWBAT}$ threshold before it enters the STANDBY state.

Transitions from STANDBY to SAVE:

The PCF50606 returns to the SAVE state when the main battery voltage drops below the $V_{VERYLOWBAT}$ and another source of power, like charger or backup battery, is available.

In the SAVE state all data is retained, no reset occurs.

Transitions from STANDBY to ACTIVE:

Once the PCF50606 is in the STANDBY state it is ready to become active.

The PCF50606 switches from STANDBY to ACTIVE state when one of the following events occurs:

- The user pressing the onkey ($\overline{\text{ONKEY}}$ active low)
- Presence of a RTC alarm interrupt.
- Presence of a charger connect interrupt
- Presence of the EXTON wake-up condition
- A ‘pen-down’ detection by the touchscreen controller

A precondition for the transition to ACTIVE state is that no fault situations, like high temperature (see Section 8.17 “Temperature High Sensor (THS)”) or low battery (see Section 8.15 “Battery voltage monitor (BVM)”), are asserted.

The ‘RTC alarm’, ‘charger connect’ and ‘touch screen pressed’ events remain valid as long as the corresponding interrupt bits are set in the INT module. The interrupt bits are cleared by a read access to the INT register.

The ‘RTC alarm’ and ‘charge connect’ start up conditions can be disabled by setting the corresponding interrupt masking register.

The ‘touch screen pressed’ start up condition can be disabled by setting the corresponding bit in one of the ADC/TSC control registers (default is no startup at touch screen press).

In the ACTIVE state all power supplies with the ON mode are default operation mode in ACTIVE are switched on, see also Table 5 on page 17. Approximately 100ms after the supplies have been stabilized the $\overline{\text{RST}}$ is released and the host controller can start up. The PCF50606 requires the KEEPACT signal to be set by the host controller within 100ms after the $\overline{\text{RST}}$ has been released. In case this feedback does not happen (host controller did not start up correctly), the PCF50606 returns to the STANDBY state and the power supplies are switched off.

Transitions from ACTIVE to STANDBY:

The user can issue a request to the system to go back to STANDBY state by pressing the onkey for more than 1 second. An ONKEY1S interrupt is generated and the host controller should switch the system to STANDBY by either:

- Setting the GOSTDBY bit in the OOCC register
- Forcing the KEEPACT signal low

The transition to STANDBY gives the host controller ~1 ms to shut down before the PCF50606 enters the STANDBY state and all supplies except LPREG are switched off, depending on the state of bit STDBACT in the LPREGC2 register.

A transition from ACTIVE to STANDBY also occurs when any of the following (error) conditions is not served in within 8 seconds by the host controller.

- The $\overline{\text{ONKEY}}$ is pressed longer than 1 second. The ONKEY1S interrupt is generated in this case. The ONKEY1S interrupt from a previous $\overline{\text{ONKEY}}$ press however, must have been cleared.
- A low battery condition is detected. A LOWBAT interrupt is generated in this case. The LOWBAT interrupt from a previous LOWBAT condition must have been cleared. More information can be found in Section 8.15 “Battery voltage monitor (BVM)”.

A transition from ACTIVE to STANDBY also occurs when any of the following (error) conditions is not served within 1 second by the host controller.

- A high temperature condition is detected. A HIGHTEMP interrupt is generated in this case. The HIGHTEMP interrupt from a previous HIGHTEMP condition however, must have been cleared. More information can be found in Section 8.17 “Temperature High Sensor (THS)”.

An immediate transition from ACTIVE to STANDBY is initiated when any of the following (error) conditions occurs.

- The expiration of the Watchdog module. More information can be found in Section 8.1.8 “Watchdog timer”.
- When the battery voltages drops below the $V_{VERYLOWBAT}$ threshold (see Table 94 on page 123).

A 8 second time-out timer is started each time any of the listed error conditions occurs. This time-out timer can be reset by the host controller by writing a ‘1’ to the RESTOT control bit in the OOCC register. This resets and stops the time-out timer in case all interrupts related to the listed (error) conditions are cleared. In other situations the time out timer starts a new time-out period.

Note that some of the control register, indicated as type ‘O’ are automatically reset when a transition from ACTIVE to STANDBY state occurs:

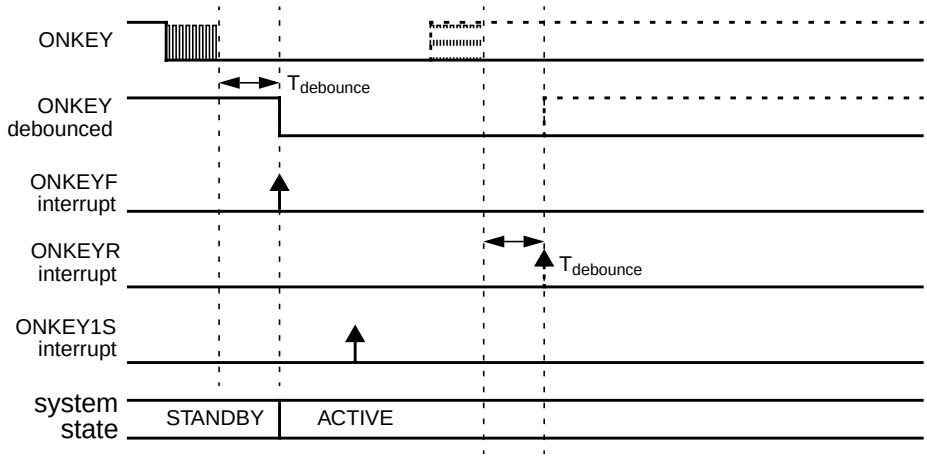
The control registers marked with ‘S’ keep their data in all states except NOPOWER.

8.1.3 ONKEY behavior

The OOC monitors the $\overline{\text{ONKEY}}$ input signal to detect the ONKEY wake-up or a ONKEY de-activation condition. The ONKEY signal is debounced (programmable debounce time) and generates the ONKEYF, ONKEYR and ONKEY1S interrupts as shown in figure 7 and figure 8.

Note that transition to STANDBY on the $\overline{\text{ONKEY}}$ input signal is interrupt driven. Suppose that a transition to STANDBY has taken place on basis of the ONKEY1S interrupt, that at the next startup of the chip, the ONKEY1S interrupt must be cleared by reading the corresponding interrupt register. If this is omitted, the transition to STANDBY on ONKEY1S is not working.

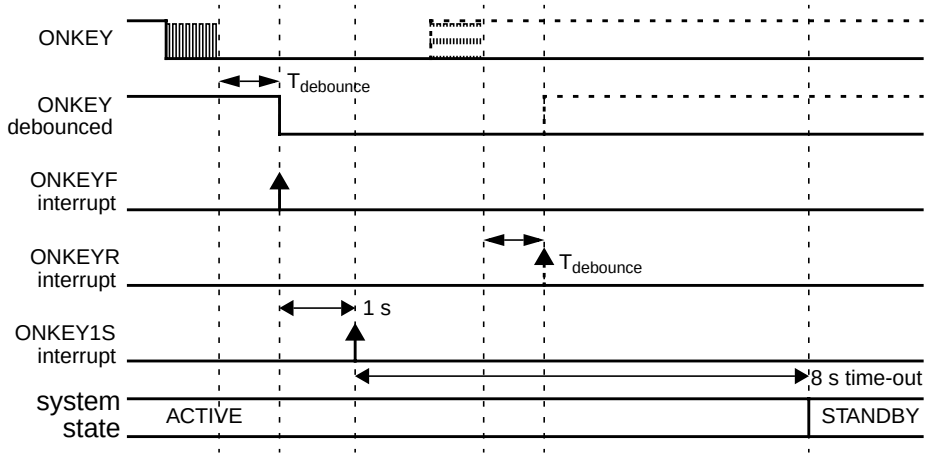
The actual status of the ONKEY pin is available in the OOCS register (ONKEY status bit).



(1) The debounced signal keeps the old value until the new value has been stable for at least the applicable debounce time. Any spike (> 30 µs) in the original signal will reset the debounce timer again. This filter suppresses all signal changes that are shorter than the debounce time.

(2) A STANDBY to ACTIVE transition is initiated by the ONKEY

Fig 7. ONKEY behavior when pressed during STANDBY state



(1) The debounced signal keeps the old value until the new value has been stable for at least the applicable debounce time. Any spike (> 30 µs) in the original signal will reset the debounce timer again. This filter suppresses all signal changes that are shorter than the debounce time.

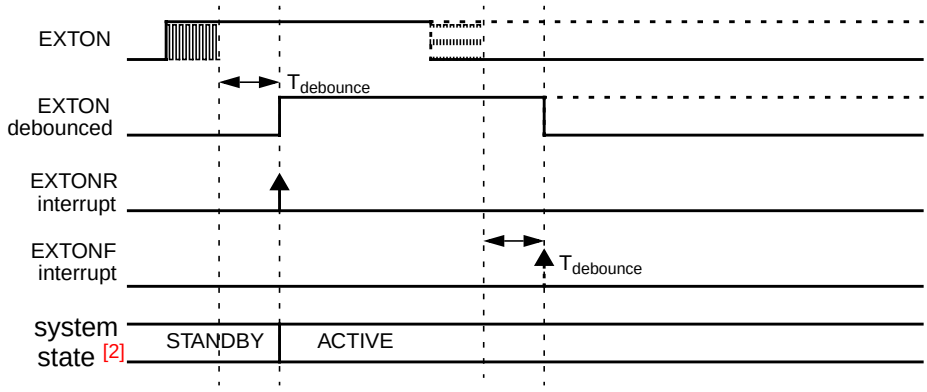
(2) An ACTIVE to STANDBY transition is initiated by the OOC a 1 s pressed ONKEY is not served by the host controller

Fig 8. ONKEY behavior when pressed during ACTIVE state, no reaction from the host controller

8.1.4 EXTON wake-up

The OOC monitors the EXTON input signal to detect the EXTON wake-up condition. A programmable debounce filter is available to debounce signals coming from mechanical switches. The status of the EXTON wake-up condition pin is available in the OOCS register.

The EXTON wake-up condition is programmable through the OOCC register, providing a transfer from STANDBY to ACTIVE state at a high (e.g. presence of a USB cable, VBUS connected to EXTON) or a low (e.g. grounding of the EXTON pin by an accessory) input voltage.



(1) The debounced signal keeps the old value until the new value has been stable for at least the applicable debounce time. Any spike (> 30 µs) in the original signal will reset the debounce timer again. This filter suppresses all signal changes that are shorter than the debounce time.

(2) Wake-up from input high level of EXTON enabled (EXTONWAK=10)

Fig 9. EXTON behavior

8.1.5 Reset generation

The OOC generates an internal PCF50606 reset as well as an external reset each time the system goes from STANDBY to ACTIVE. All registers for the regulators and converters are reset to their default values.

The external reset signal $\overline{RST}$ is kept low for 100 ms or 150 ms after the PCF50606 enters the ACTIVE state dependent on the power sequencing settings, see Section 8.4.2 “Power Supply Sequencer” on page 41. This ensures that the connected system is kept in reset during the start-up of the power supply systems.

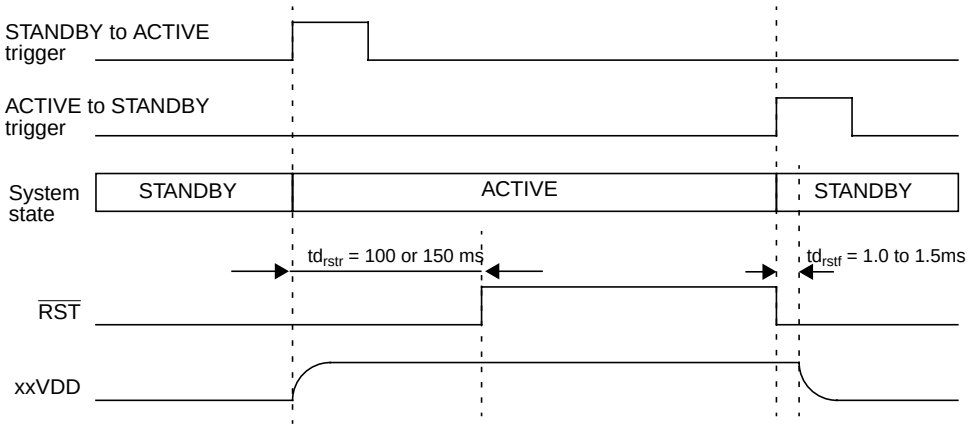


Fig 10. Reset generation timing diagram (STANDBY - ACTIVE - STANDBY transitions)

The external reset signal $\overline{RST}$ is forced low again by the PCF50606 when after any of the ACTIVE to STANDBY triggers is detected (KEEPACT is low or the GOSTBY bit is set). A small delay (1.0 to 1.5ms) is built-in to allow the host controller to shut down after it initiated the ACTIVE to STANDBY transition.

A special condition occurs when the main battery voltage drops below the $V_{VERYLOWBAT}$ limit of typically 2.7 V; the reset ($\overline{RST}$=0) is asserted without delay in order to shut down the host controller immediately.

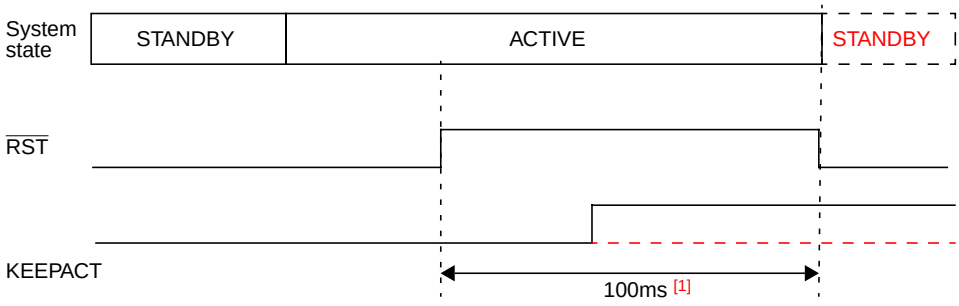
The reset is asserted ($\overline{RST}$=0) also when one or more supply voltages are below their PowerOk threshold level if the PWRFRST bit is set, see also Section 8.4.3 “Power Supply Monitoring” on page 42.

The $\overline{RST}$ pin is an open drain output with build in pull up resistor. A mechanical reset switch can be connected between the $\overline{RST}$ pin and the VSS to provide a manual reset button to the application.

Note: The build in pull-up resistor is not biased in case the IOVDD supply is de-activated. However the open drain output itself remains functional in this case.

8.1.6 KEEPACT control

After the transition from STANDBY to ACTIVE the PCF50606 expects that the KEEPACT signal is forced high by the host controller. When this is not the case within 100ms after the external reset signal RST is deasserted the PCF50606 will return to the STANDBY state. The required timing for the KEEPACT signal is shown in Figure 11.



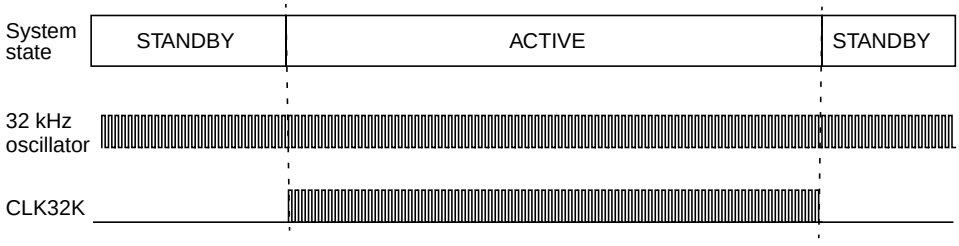
(1) The KEEPACT signal must be set in this interval to maintain the ACTIVE state

Fig 11. KEEPACT timing

8.1.7 CLK32 output (only available for bondout A)

The 32.678Hz clock frequency is available as system clock on the CLK32 pin when it is activated by setting the CLK32ON bit in the OOCC1 control register. The CLK32 pin is pulled low when it is not activated.

The CLK32 output is only activated in the ACTIVE state of the PCF50606, as shown by the timing diagram, see Fig 12.



(1) Before the supplies are turned on, the internal 32 kHz clock is already stable. The external CLK32 becomes available when the IOVDD supply is powered up.

Fig 12. Timing diagram of CLK32 output (STANDBY - ACTIVE - STANDBY transition)

8.1.8 Watchdog timer

The OOC contains a watchdog timer. By default the watchdog is not activated. It can be activated by setting the WDTRST bit in the OOCC register high. Once this bit has been set, the watchdog is enabled and needs to be cleared once every 8 seconds when the PCF50606 is in ACTIVE state. The PCF50606 performs an automatic ACTIVE to STANDBY transition when the watchdog expires.

The watchdog timer is reset at a ACTIVE to STANDBY transition of the PCF50606 and it is stopped (no incremental clocking) in the STANDBY state. A new 8 s watchdog period will not start again when the PCF50606 enters the ACTIVE state again after a wake up event. For activating the watchdog timer after entering the active state, the WDTRST bit in the OOCC register has to be set again.

In ACTIVE state, it is possible to stop and reset the watchdog timer by resetting bit WDTEXP in the OOCS register, see Table 7 on page 29.

The WDTEXP bit in the status register returns the state of the WDT module. This bit is set when the watchdog expires and is not reset when the PCF50606 enters the STANDBY state. The WDTEXP can be read back in the next ACTIVE state to inform the host controller that the watchdog initiated the previous ACTIVE to STANDBY state transition.

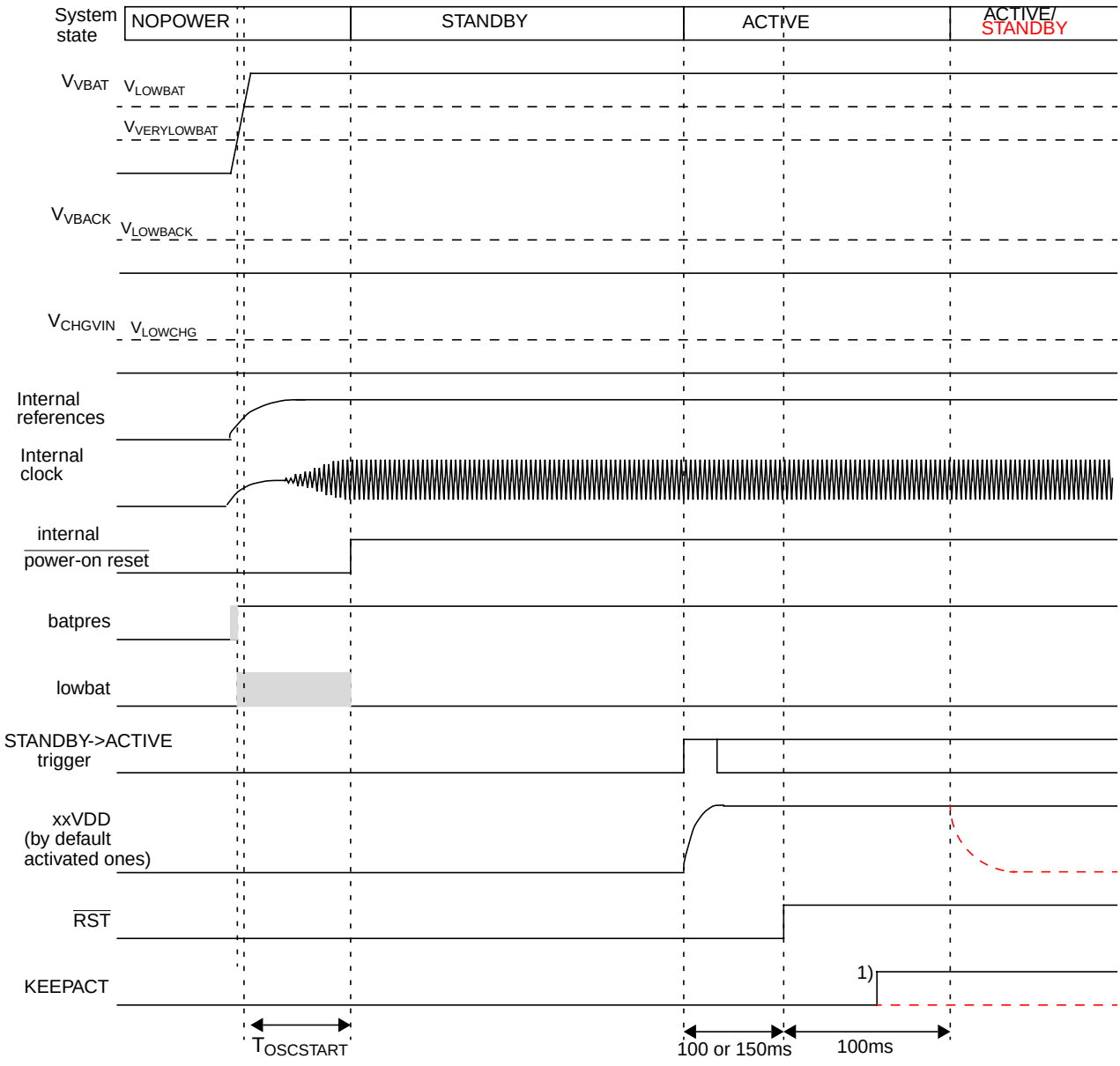
8.1.9 Initial system start up behavior

The PCF50606 executes a pre-defined start up sequence at initial start up, meaning the first time that power is applied to the circuit. At the end of the start up sequence the PCF50606 is in the STANDBY state. The transition to the ACTIVE state occurs when one of the ACTIVE conditions is detected, see also Section 8.1.2 on page 17.

In case the PCF50606 is started up by inserting a charger plug into the system, the start up sequence ends when the PCF50606 is in ACTIVE state. In this case the regulators and converters are activated according to the default operation modes as listed in Table 5 on page 17.Several start up sequences are shown in the following paragraphs.

CASE 1: Insertion of a charged main battery, no backup battery available.

When the charged main battery is inserted the internal circuitry will start up since the battery voltage is above the $V_{VERYLOWBAT}$ threshold. After some time the internal references are available and the system clock starts running. The internal power-on reset will be deasserted and the PCF50606 enters the STANDBY state. The full start up sequence is shown in Figure 13.
From this state the PCF50606 waits for any of the STANDBY to ACTIVE triggers, see also Section 8.1.2 on page 17.

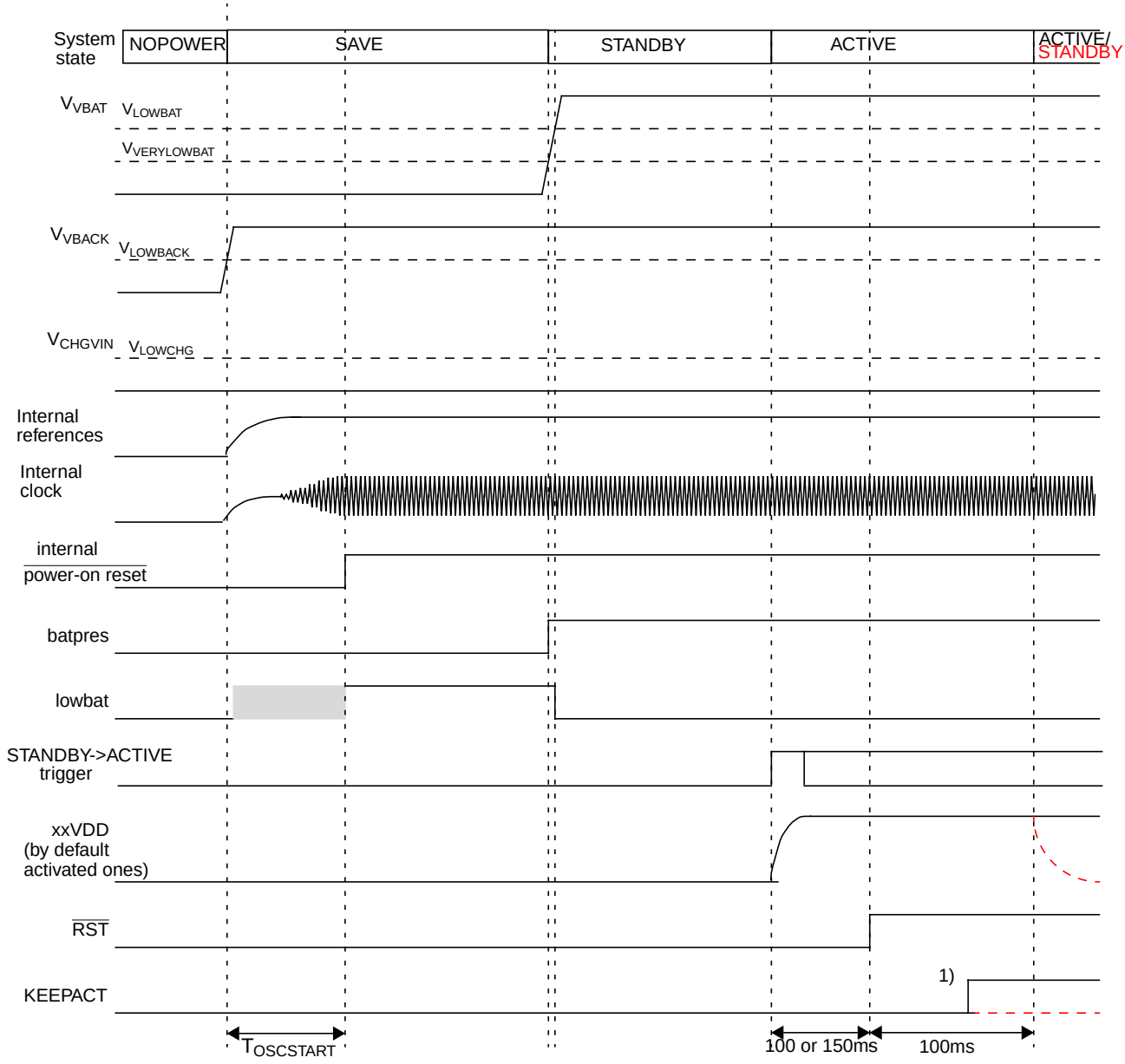


(1) The KEEPACT signal must be set by the host controller within 100ms after the reset is deasserted to maintain the ACTIVE state

Fig 13. Insertion of a charged main battery, no backup battery

CASE 2: Insertion of a charged backup battery followed by insertion of a charged main battery, no charger connected (see Figure 14).

As soon as the backup battery is connected the internal circuitry will start up since voltage is above the $V_{LOWBACK}$ threshold. After a time $T_{OSCSTART}$ (see Table 93 "Characteristics 32 kHz oscillator") the internal references are available and the system clock is running. The internal power-on reset will be deasserted and the PCF50606 enters the SAVE state. The PCF50606 remains in the SAVE state until a charged main battery is connected. The transition from SAVE to STANDBY occurs when the main battery voltage exceeds the $V_{VERYLOWBAT}$ threshold.

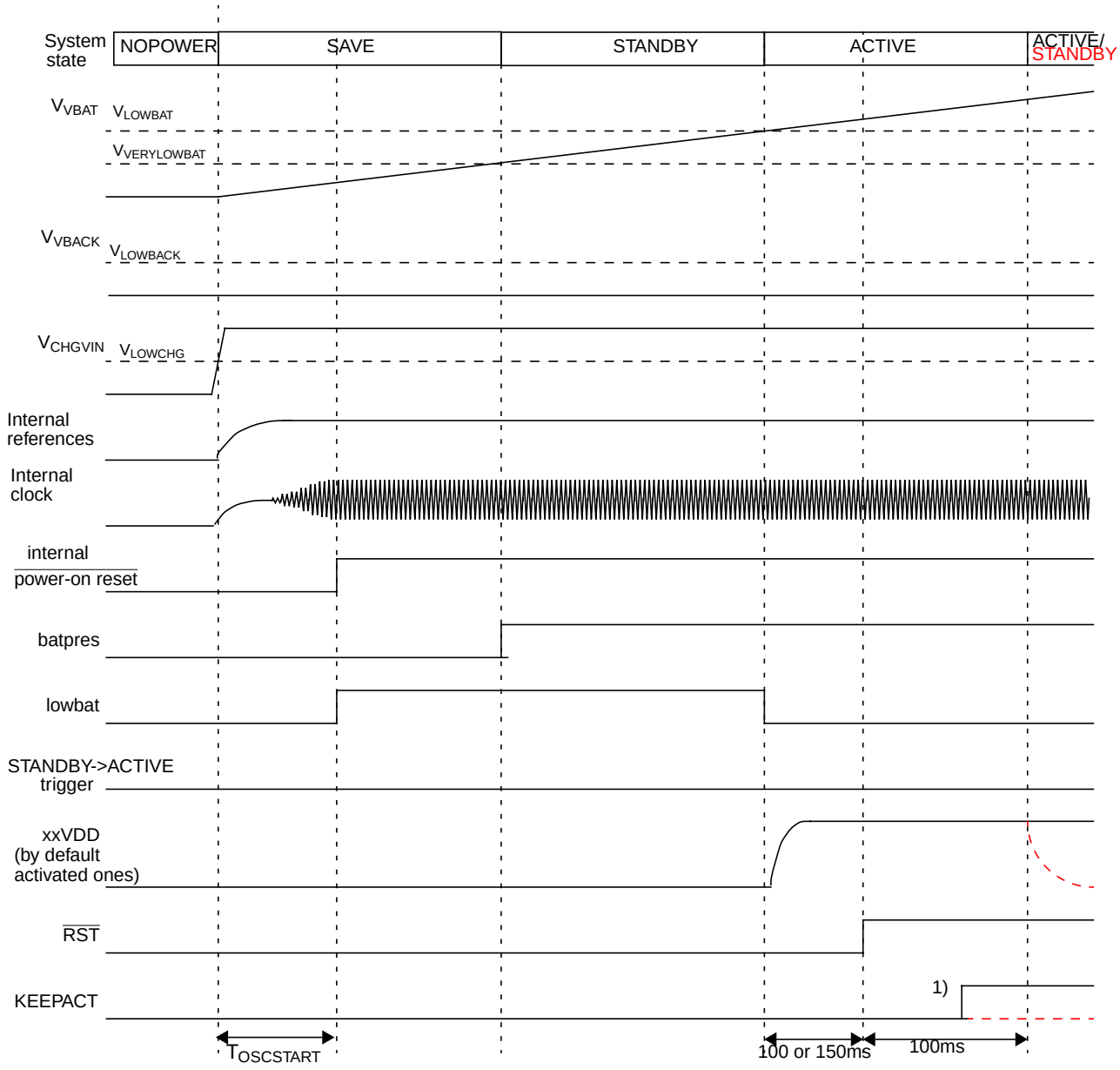


(1) The KEEPACT signal must be set by the host controller within 100ms after the reset is deasserted to maintain the ACTIVE state

Fig 14. Insertion of a charged backup battery followed by a charged main battery

CASE 3: Connection of a charger when the main battery is empty and no backup battery is available (see Figure 15).

As soon as the charger is connected the internal circuitry will start up. After a time $T_{OSCSTART}$ (see Table 93 “Characteristics 32 kHz oscillator”) the internal references are available and the system clock is running. The internal power-on reset will be deasserted and the PCF50606 enters the SAVE state. The MBC module starts charging of the main battery. The transition from SAVE to STANDBY occurs when the main battery voltage exceeds the $V_{VERYLOWBAT}$ threshold and the STANDBY to ACTIVE transition when the battery voltage reaches the V_{LOWBAT} threshold.



(1) The KEEPACT signal must be set by the host controller within 100ms after the reset is deasserted to maintain the ACTIVE state

Fig 15. Connect the charger when the battery is empty, no backup battery

8.1.10 Identification

The PCF50606 has a special register to identify the version and variant of the IC.

Bits 7-4 identify the silicon version and bits 3-0 the variant. If the silicon version is odd (bit 4 equals '1') then the variant number must be read as variant +16. The real variant number can also be read directly from bits 4-0 (so 5 LSB bits instead of 4).

Table 6: ID register

BIT	Mode	Symbol	Value	Description
3-0	R	VARIANT	[1]	ROM identification to distinguish PCF50606 variants
7-4	R	VERSION	xxxx	ROM identification to distinguish PCF50606 versions

[1] For VARIANT values, see Section 8.24 "PCF50606 variants".

8.1.11 Control and status registers

Table 7: OOCS register

BIT	Mode	Symbol	Reset	Description
0	R	ONKEY	[1]	$\overline{\text{ONKEY}}$ pin status
1	R	EXTON	[1]	EXTON pin status
2	R/W	PWROKRST	0	Reset activation during power failure situations (PWROK=0) 0: RSTN is not asserted in supply voltage failure situations 1: RSTN is asserted in supply voltage failure situations
3	R	BATOK	[1]	Presence of main battery: 0: $V_{VBAT} < V_{LOWBAT}$ 1: $V_{VBAT} > V_{LOWBAT}$
4	R	BACKOK	[1]	Presence of backup battery: 0: $V_{VBACK} < V_{LOWBACK}$ 1: $V_{VBACK} > V_{LOWBACK}$
5	R	CHGOK	[1]	Presence of charger: 0: $V_{CHGVIN} < V_{LOWCHG}$ 1: $V_{CHGVIN} > V_{LOWCHG}$
6	R	TEMPOK	[1]	Status of IC temperature: 0: $T_{IC} > T_{TH(THS)}$ 1: $T_{IC} < T_{TH(THS)}$
7	R	WDTEXP	[2]	Status of the watchdog timer 0: watchdog stopped 1: watchdog active

[1] This bit represents the status at the moment of the I2C read action.

[2] The WDTEXP bit is cleared by setting the WDTRST bit in the OOCC2 register.

Table 8: OOCC1 register

BIT	Mode	Symbol	Reset [1]	Description
0	R/W	GOSTDBY	0	0: no effect 1: When in ACTIVE state, go to the STANDBY state. NOTE: This bit is reset when system is in STANDBY state.
1	R/W	TOTRST	0	0: no effect 1: resets the time-out timer. Once time-out timer is reset this bit will be automatically cleared.
2	R/W	CLK32ON	[2]	Activation of the CLK32 output on the CLK32 PIN 0: CLK32 switched off (low level) 1: CLK32 activated
3	R/W	WDTRST	0	0: stops the watchdog timer 1: resets and enables the watchdog timer.
4	R/W	RTCWAK	0	Wake up condition for the RTC 0: no wake-up 1: RTC alarm
5	R/W	CHGWAK	1	Wake up condition for the Charger 0: no wake-up 1: Charger insertion
7-6	R/W	EXTONWAK	01	Wake up condition for the EXTON pin 00: no wake-up 01: high level on EXTON 10: low level on EXTON 11: reserved

[1] The register is reset at the initial start up of the PCF50606 (register type ‘S’).

[2] For reset values, see Section 8.24 “PCF50606 variants”

Table 9: OOCC2 register

BIT	Mode	Symbol	Reset [1]	Description
1-0	R/W	ONKEYDB	01	Debounce time for $\overline{\text{ONKEY}}$ 00: no debounce 01: 14 ms 10: 62 ms 11: 500 ms
3-2	R/W	EXTONDB	01	Debounce time for EXTON 00: no debounce 01: 14 ms 10: 62 ms 11: 500 ms
7-4	reserved		[2]	

[1] The register is reset at the initial start up of the PCF50606 (register type ‘S’).

[2] Reserved bits should be written ‘0’, the return values are not defined.

8.2 Serial interface (I2C)

The serial interface of the PCF50606 is the I²C-bus. A detailed description of the I²C-bus specification, including applications, is given in the brochure: *The I2C-bus and how to use it*, order no. 9398 393 40011 or *I2C Peripherals Data Handbook IC12.*

8.2.1 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy. In bus configurations with ICs on different supply voltages, the pull-up resistors shall be connected to the highest supply voltage. The I²C-bus supports incremental addressing. This enables the system controller to read or write multiple registers in only one I²C-bus action. The PCF50606 supports the I²C-bus up to 400 kbit/s.

The I²C-bus system configuration is shown in Figure 16. A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’. The PCF50606 is a slave only device.

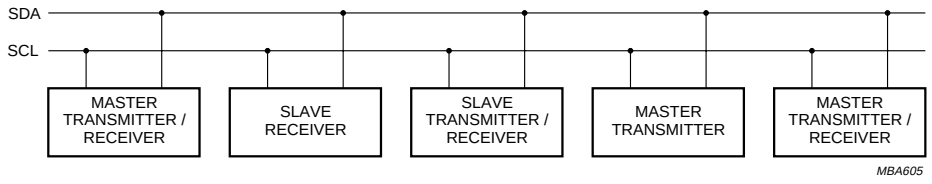


Fig 16. I²C-bus system configuration.

8.2.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P); see Figure 17.

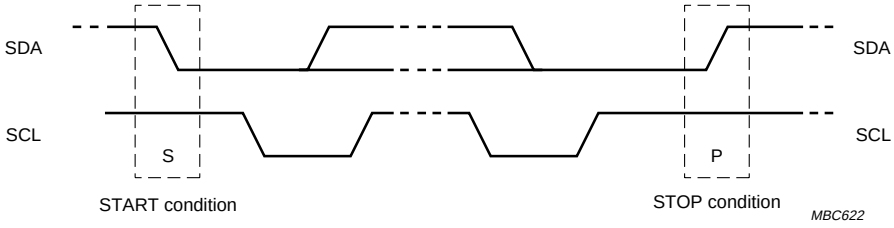


Fig 17. START and STOP conditions on the I²C-bus.

8.2.3 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal; see Figure 18.

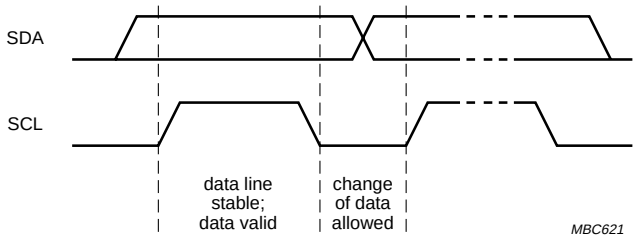


Fig 18. Bit transfer on the I²C-bus.

8.2.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the receiver generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

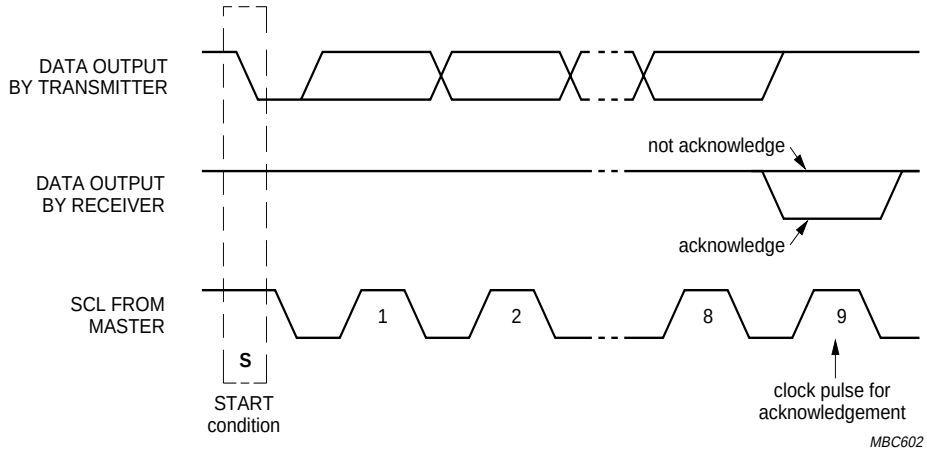


Fig 19. Acknowledge on the I²C-bus.

8.2.5 Internal timing of a write sequence

It takes five system clock cycles (typically 1.4 µs) from the falling edge of the acknowledge for the programmed values to become effective in the modules.

8.2.6 I²C-bus protocol

Addressing: Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The address for both the PCF50605 as well as the PCF50606 versions is 0001000x (10H/11H). The least significant bit is the read/$\overline{\text{write}}$ indicator.

The PCF50606HN/xA/N1 PCF50606HN/xB/N1 PCF50605HN/xA/N1 PCF50605HN/xB/N1 acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal. The data signal SDA is a bidirectional line.

The PCF50606HN/xA/N1 PCF50606HN/xB/N1 PCF50605HN/xA/N1 PCF50605HN/xB/N1 slave address is shown in Figure 20.

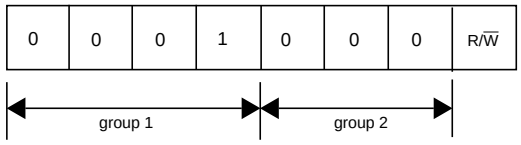


Fig 20. Slave address.

Read/write cycles: The I²C-bus configuration for the different PCF50606HN/xA/N1 PCF50606HN/xB/N1 PCF50605HN/xA/N1 PCF50605HN/xB/N1 read and write cycles are shown in Figure 21, 22 and 23. The word address is a eight bit value that defines which register is to be accessed next.

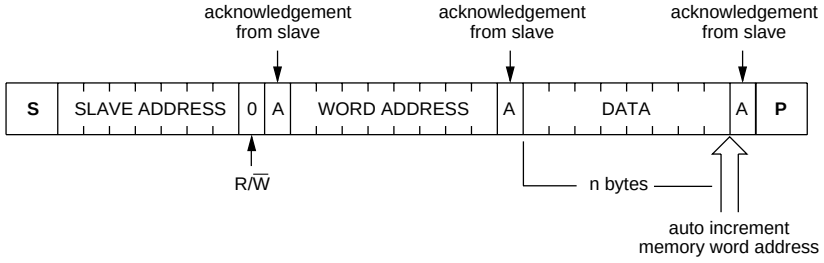
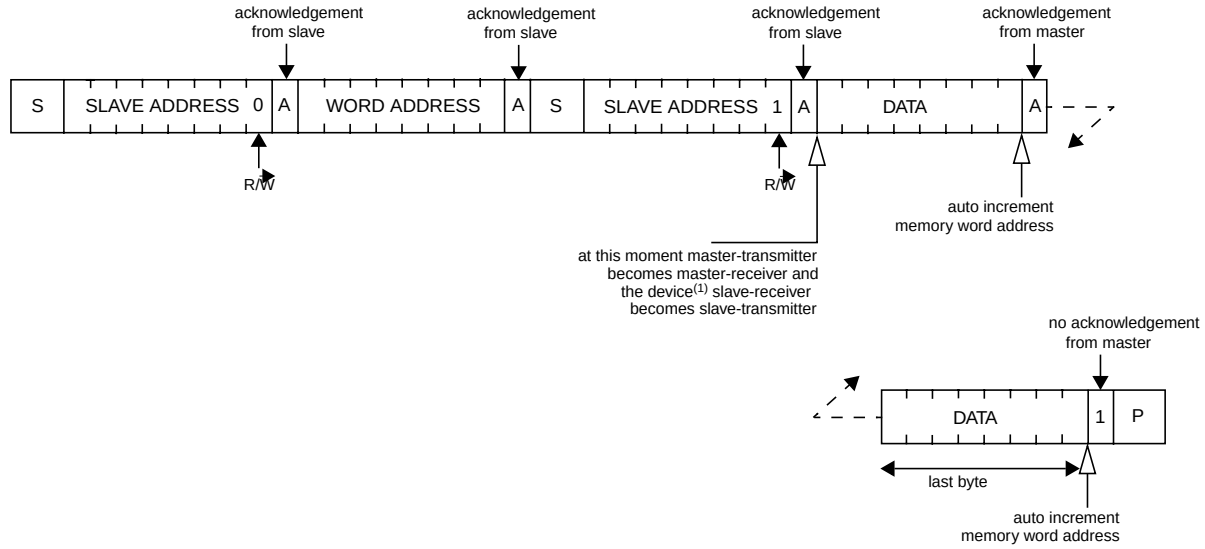


Fig 21. Master transmits to slave receiver (write mode).



(1) PCF50606

Fig 22. Master reads after setting word address (write word address; read data).

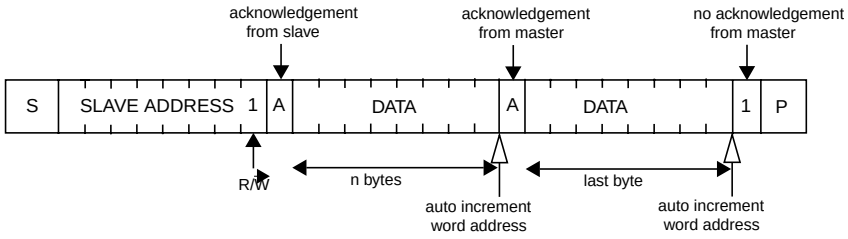


Fig 23. Master reads slave immediately after first byte (read mode).

8.2.7 De-activation of the I2C module

The I2C module of the PCF50606 is only enabled in the ACTIVE operation state of the PCF50606. However the I2C module is disabled in the ACTIVE state if the IOREG is placed in ECO or OFF operation mode, see also Section 8.4 “Power supply control”.

8.3 Interrupt controller (INT)

The PCF50606 uses the interrupt controller (INT) to indicate to the system controller that the status of the PCF50606 has changed, and that an action of the system controller is required. Interrupts can be generated by several modules of the PCF50606. The interrupt generator handles all interrupts with the same priority; prioritizing shall be done by the system controller software.

There are no timing requirements for interrupt service response times. All events that require immediate actions are performed by the PCF50606 without any action by the system controller.

The function of the interrupt module is to capture, mask and combine the interrupt signals from the modules that can generate an interrupt. All interrupts are combined in the interrupt signal $\overline{IRQ}$. The $\overline{IRQ}$ signal is implemented as an open drain output and requires an external pull-up resistor.

The interrupt module is powered in all states (except NOPOWER) and retains the register values. Events that occur in the STANDBY state, are captured and can be read out by the system controller once the system is in the ACTIVE state.

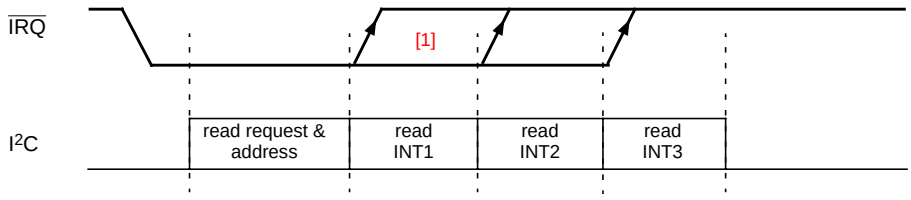
The $\overline{IRQ}$ signal is asserted in the ACTIVE state whenever one or more PCF50606 interrupts are active.

Each interrupt register (8 bits) is cleared when it is read (R&C) through the I^2C-bus interface. New interrupts that occur during a R&C action are captured in a intermediate register.

The system controller shall read all interrupt registers in one I^2C read action. This effectively clears all interrupts that are active. The $\overline{IRQ}$ line becomes inactive HIGH, as soon as the last register containing an active interrupt has been addressed (see Figure 24).

In case a new interrupt occurs during the read sequence of the interrupt registers, the $\overline{IRQ}$ line becomes inactive HIGH as in the previous case. Then, at least 16 system clock cycles after the read sequence of the INT3 register started, the $\overline{IRQ}$ line is activated again (see Figure 25). This feature allows the system controller to capture new interrupts, whether the interrupt detection is level or edge sensitive.

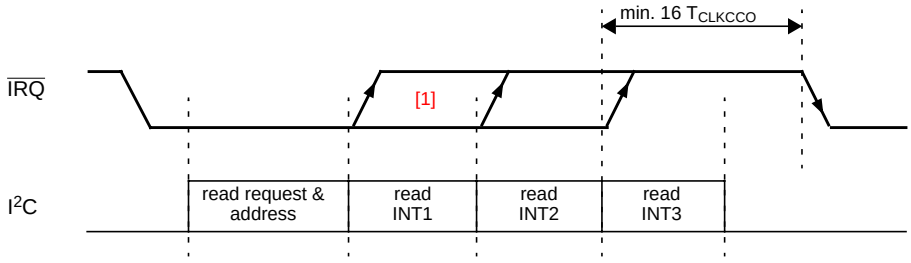
All interrupts can be masked: this effectively prevents that $\overline{IRQ}$ is asserted for masked interrupts. Masking is implemented with a mask bit in the mask registers for each interrupt source. Nevertheless, the interrupt status registers still provide the actual interrupt status of the masked interrupts, which allows polling of the interrupt status registers. Note that if the mask bit is cleared for an active interrupt, the $\overline{IRQ}$ line goes low within 16 system clock cycles.



(1) $\overline{IRQ}$ becomes inactive high as soon as the read sequence of the last INTx register containing an active interrupt starts.

(2) Read access can be done with or without incremental addressing.

Fig 24. Interrupt timing; no interrupt captured during read sequence



(1) $\overline{IRQ}$ becomes inactive high as soon as the read sequence of the last INTx register containing an active interrupt starts.

(2) Read access can be done with or without incremental addressing.

Fig 25. Interrupt timing; interrupt captured during read sequence

8.3.1 Control registers

Table 10: INT1 register

BIT	Mode	Symbol	Reset	Description
0	R&C	ONKEYR	[1]	ONKEY rising edge detected (with selectable debounce function [2])
1	R&C	ONKEYF	[1]	ONKEY falling edge detected (with selectable debounce function [2])
2	R&C	ONKEY1S	[1]	ONKEY at least 1 second low
3	R&C	EXTONR	[1]	EXTON rising edge detected
4	R&C	EXTONF	[1]	EXTON falling edge detected
5	reserved		[3]	
6	R&C	SECOND	[1]	RTC periodic second interrupt
7	R&C	ALARM	[1]	RTC alarm time is reached

[1] This bit represents the status at the moment of the I2C read action.

[2] For the programming of the debounce function, see Table 9 “OOCC2 register”

[3] Reserved bits should be written ‘0’, the return values are not defined.

Table 11: INT2 register

BIT	Mode	Symbol	Reset	Description
0	R&C	CHGINS	[1]	Charger with valid voltage has been inserted
1	R&C	CHGRM	[1]	Charger has been disconnected
2	R&C	CHGFOK	[1]	Battery ready for fast charge: voltage and temperature within fast charging limits
3	R&C	CHGERR	[1]	Error occurred in charge mode, Charging sequence restarted
4	R&C	CHGFRDY	[1]	Fast charge phase completed
5	R&C	CHGPROT	[1]	Charging protection interrupt
6	R&C	CHGWD10S	[1]	Charger watchdog will expire in 10 seconds.
7	R&C	CHGWDEXP	[1]	Charger watchdog expires

[1] This bit represents the status at the moment of the I2C read action.

Table 12: INT3 register

BIT	Mode	Symbol	Reset	Description
0	R&C	ADCRDY	[1]	ADC finished the conversion, ADC data can be read
1	R&C	ACDINS	[1]	An accessory is inserted
2	R&C	ACDREM	[1]	An accessory is removed
3	R&C	TSCPRES	[1]	The touch screen is touched when touch screen module is in interrupt mode
5-4	reserved		[3]	
6	R&C	LOWBAT	[1]	BVM has detected a low battery voltage (with selectable debounce filter of 62 ms [2])
7	R&C	HIGHTMP	[1]	THS has detected a high temperature condition (debounced with 62 ms)

[1] This bit represents the status at the moment of the I2C read action.

[2] For the programming of the debounce function, see Table 47 “BVMC register”

[3] Reserved bits should be written ‘0’, the return values are not defined.

Table 13: INT1M register

BIT	Mode	Symbol	Reset [1]	Description
0	R/W	ONKEYRM	0	0: Interrupt enabled 1: Mask the ONKEYR interrupt
1	R/W	ONKEYFM	0	0: Interrupt enabled 1: Mask the ONKEYF interrupt
2	R/W	ONKEY1SM	0	0: Interrupt enabled 1: Mask the ONKEY1S interrupt

Table 13: INT1M register *...continued*

BIT	Mode	Symbol	Reset[1]	Description
3	R/W	EXTONRM	0	0: Interrupt enabled 1: Mask EXTON rising edge interrupt
4	R/W	EXTONFM	0	0: Interrupt enabled 1: Mask EXTON failing edge interrupt
5	reserved		[2]	
6	R/W	SECONDM	0	0: Interrupt enabled 1: Mask the SECOND interrupt
7	R/W	ALARMM	0	0: Interrupt enabled 1: Mask the ALARM interrupt

[1] The register is reset at the initial start up of the PCF50606 (register type 'S').

[2] Reserved bits should be written '0', the return values are not defined.

Table 14: INT2M register

BIT	Mode	Symbol	Reset[1]	Description
0	R&C	CHGINSM	0	0: Interrupt enabled 1: Mask the charger insertion interrupt
1	R&C	CHGRMM	0	0: Interrupt enabled 1: Mask the charger removal interrupt
2	R/W	FCHGOKM	0	0: Interrupt enabled 1: Mask the charge ok interrupt
3	R/W	CHGERRM	0	0: Interrupt enabled 1: Mask the fast charge error interrupt
4	R/W	CHGFRDYM	0	0: Interrupt enabled 1: Mask the fast charge ready
5	R/W	CHGPROTM	0	0: interrupt enabled 1: Mask the charging protection interrupt
6	R/W	CHGWD10SM	0	0: Interrupt enabled 1: Mask the charger watchdog pre-alert interrupt
7	R/W	CHGWDEXPM	0	0: Interrupt enabled 1: Mask the charger watchdog expiration interrupt

[1] The register is reset at the initial start up of the PCF50606 (register type 'S').

Table 15: INT3M register

BIT	Mode	Symbol	Reset[1]	Description
0	R/W	ADCRDYM	0	0: Interrupt enabled 1: Mask the ADC ready interrupt
1	R/W	ACDINSM	0	0: Interrupt enabled 1: Mask the accessory insertion interrupt
2	R/W	ACDREMM	0	0: Interrupt enabled 1: Mask the accessory removal interrupt

Table 15: INT3M register *...continued*

BIT	Mode	Symbol	Reset [1]	Description
3	R/W	TSCPRESM	0	0: Interrupt enabled 1: Mask the touch screen press interrupt
5-4	reserved			
6	R/W	LOWBATM	0	0: Interrupt enabled 1: Mask the LOWBAT interrupt
7	R/W	HIGHTMPM	0	0: Interrupt enabled 1: Mask the HIGHTMP interrupt

[1] The register is reset at the initial start up of the PCF50606 (register type 'S').

8.4 Power supply control

The power supply modules of the PCF50606 are fully programmable through the I2C interface. This section describes generic features like on/off modes and sequencing. Module-specific settings like output voltage, control methods and dynamic voltage management (DCD module) are described in their specific sections.

8.4.1 Power supply on/off modes

The linear regulator modules support three operation modes:

- OFF mode

  The regulator is disabled which minimizes the current consumption of the regulator. The output capacitor is typically discharged by the external load.

- ON mode

  The regulator is fully operational. The programmed output voltage is generated and the module provided the full output current capability.

- ECO mode

  The economic (ECO) mode is a power saving mode of the regulators. The regulator is operational and generates the programmed output voltage. The maximum output current is limited in this mode, which allows to reduce the current consumption of the regulator in this mode.

The DC/DC step down converters support also three operation modes of which the OFF and ON mode are identical to the operation modes of the regulators.

- OFF mode

  The converter is disabled and the current consumption of the module is minimized. The output voltage stage can be configured in three modes:

  – Float mode

    In this mode the PMOST switch is switched off, which leaves the output node floating. Typically the output node is discharged in this situation by the output load.

  – ByPass mode

    In the ByPass mode the PMOST switch is closed by the controller, which pulls the output node to the input voltage.

– PullDown mode

In the PullDown mode the PMOST switch is switched off while the output node is actively pulled down to VSS.
Note this mode is only supported by the DCD converter.

- ON mode

The DC/DC converter is fully operational. The programmed output voltage is generated and the module provides the full output current capability.

- ECO mode

The economic (ECO) mode is a power saving mode of the DC/DC converter. The converter operates only in Pulse Frequency Mode (PFM) using a low power hysteretic controller, reducing the quiescent current in this mode. The maximum output current is limited in this mode.

The operation mode can be set for each DC/DC converter and regulator module separately. The operation mode of a DC/DC converter or linear regulator depends in first instance on the activity state of the PCF50606. All regulators/converters are in OFF mode, if the PCF50606 operates in NOPOWER, STANDBY or SAVE state.

The OPMOD and VOUT control bits are reset in the STANDBY state. This ensures that the intended set of regulators is enabled with their default output voltages each time a transition to the ACTIVE state is made.

The LPREG provides the possibility to generate a permanent supply independently from the operation mode of the PCF50606, when operated in the ECO mode. In this mode an output voltage is generated in ACTIVE, STANDBY and SAVE state.

When the PCF50606 is in ACTIVE state, the operation mode for each converter or regulator module is determined by the PWREN1 and PWREN2 control signals as defined by the OPMOD control bits located in the control register for each regulator. This control method allows to change the operation mode of several converter and/or regulators using the PWRENx control signals. This provide two advantages. First all operation mode can be changed at the same time and secondly the number of I2C transfers is reduced. Table 16 shows the operation mode for the different OPMOD and PWREN1/PWREN2 combinations for the regulators and DC/DC converters.

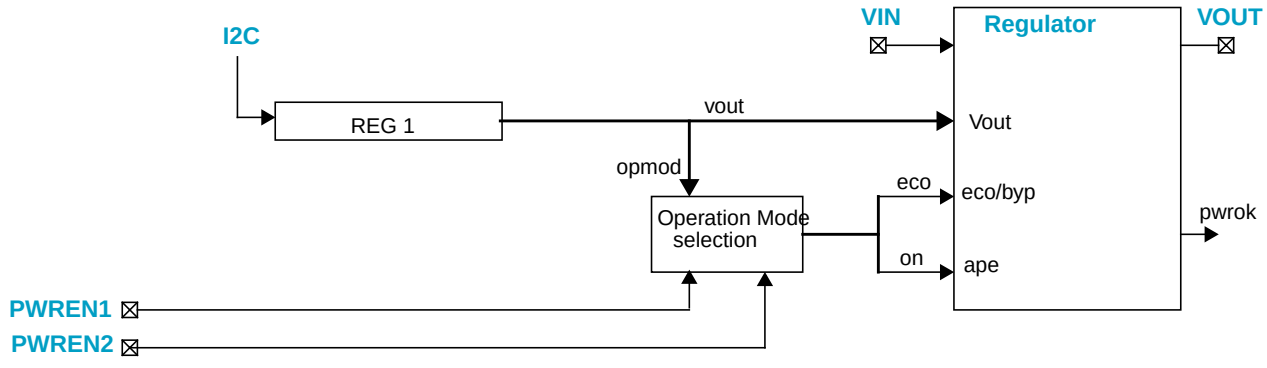


Fig 26. Operation Mode control system

Table 16: Operation modes of the regulators / converters (PCF50606 in ACTIVE state)

PWREN1	PWREN2	OPMOD bits 7 -5							
		000	001	010	011	100	101	110	111
0	0	OFF	ECO	ECO	OFF	OFF	OFF	OFF	ON
0	1	OFF	ON	ECO	ON	OFF	OFF	OFF	ON
1	1	OFF	ON	ECO	ON	ON	OFF	ON	ON
1	0	OFF	ON	ECO	ON	ON	ON	OFF	ON

The reset values for all the OPMOD control bits is mask programmable (see Table 76 “Reset Settings”).

8.4.2 Power Supply Sequencer

The DC/DC converters and regulators can be activated during a STANDBY to ACTIVE or ACTIVE to STANDBY transition in two phases. The PSSC register selects the activation phase for each converter or regulator.

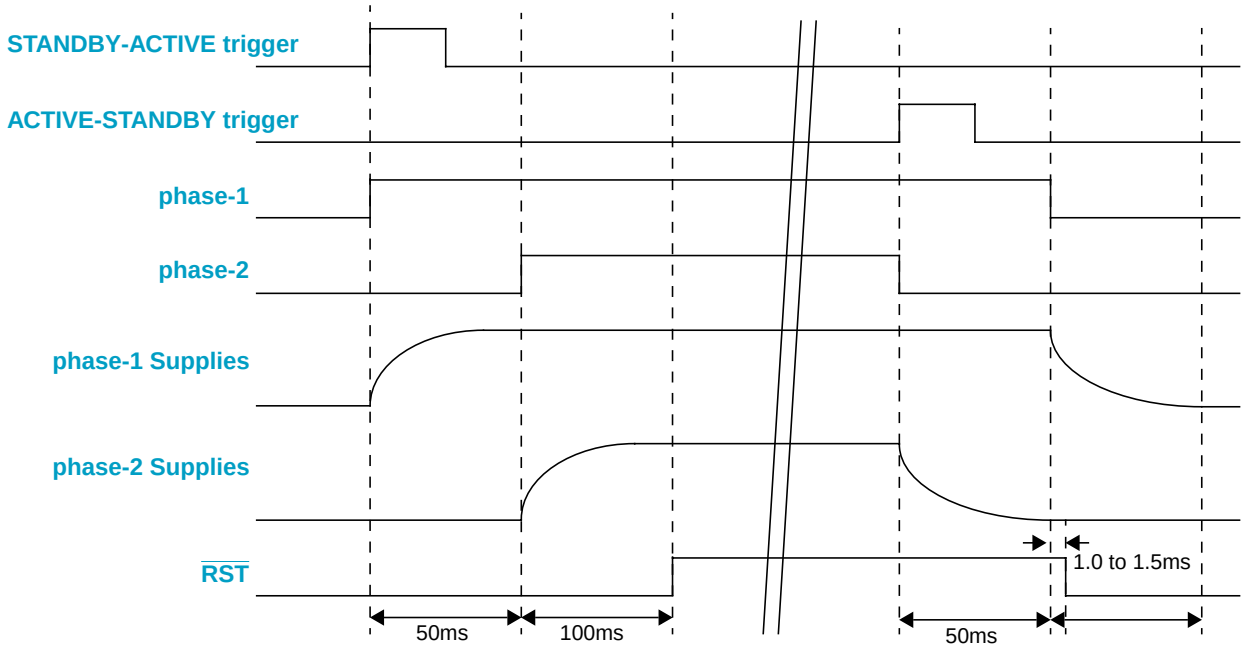


Fig 27. Timing diagram of power sequencing when entering and leaving the ACTIVE state.

The second phase is skipped when all power supplies are activated in the first phase

Control registers

Table 17: PSSC Power sequencing register

BIT	Mode	Symbol	Reset [1]	Description
0	R/W	DCDPH2	[2]	0: DCD converter activates in phase 1 1: DCD converter activates in phase 2
1	R/W	DCDEPH2	[2]	0: DCDE converter activates in phase 1 1: DCDE converter activates in phase 2
2	R/W	DCUDPH2	[2]	0: DCDU converter activates in phase 1 1: DCDU converter activates in phase 2
3	R/W	IOPH2	[2]	0: IO regulator activates in phase 1 1: IO regulator activates in phase 2
4	R/W	D1PH2	[2]	0: D1 regulator activates in phase 1 1: D1 regulator activates in phase 2
5	R/W	D2PH2	[2]	0: D2 regulator activates in phase 1 1: D2 regulator activates in phase 2
6	R/W	D3PH2	[2]	0: D3 regulator activates in phase 1 1: D3 regulator activates in phase 2
7	R/W	LPPH2	[2]	0: LP regulator activates in phase 1 1: LP regulator activates in phase 2

[1] The register is reset at the initial start-up of the PCF50606 (register type 'S')

[2] For reset values, see Section 8.24 "PCF50606 variants".

8.4.3 Power Supply Monitoring

The PWROK output provides an indicating of correct supply voltage generation to the host controller. The PWROK is set when all generated supply voltage have reached at least 90% of the programmed output voltage. The number of monitored supply voltages can be adapted through the PWROK control register.

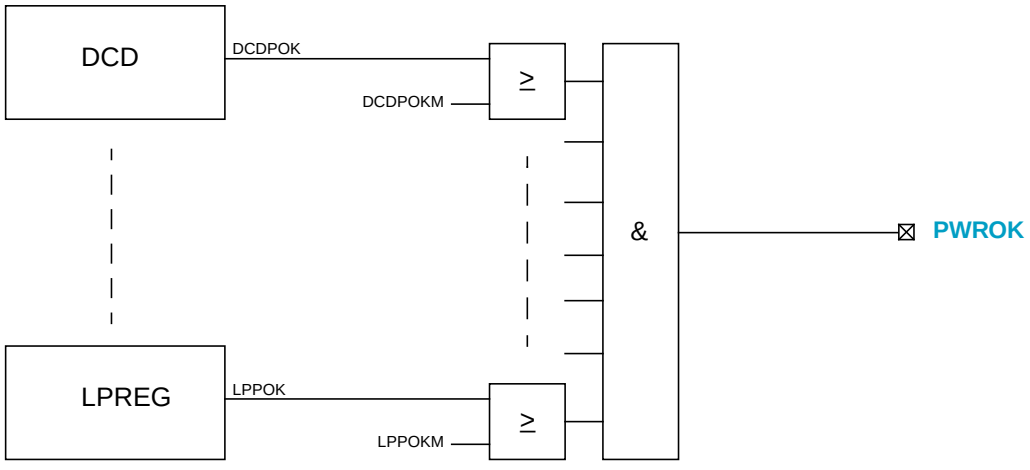


Fig 28. Block diagram of the PWROK signaling.

An external reset can be generated in low supply voltage situation by setting the PWROKRST bit, see also Section 8.1.5 "Reset generation" on page 22.

Note that the PWROK signal is forced low during the settling time of the regulators / converters when these modules are activated or when the output voltage is re-programmed (via I2C or PWREN control) to a higher setting.

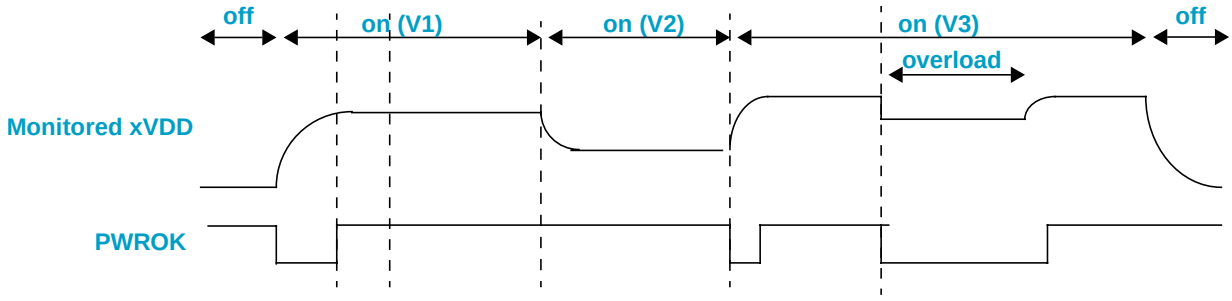


Fig 29. timing diagram of the Power Supply Monitoring

Control registers

Table 18: PWROKM Power Ok masking register

BIT	Mode	Symbol	Reset	Description
0	R/W	DCDPOKM	0	Masks PWROK monitoring of the DCD converter
1	R/W	DCDEPOKM	0	Masks PWROK monitoring of the DCDE converter
2	R/W	DCUDPOKM	0	Masks PWROK monitoring of the DCUD converter
3	R/W	IOPOKM	0	Masks PWROK monitoring of the IOREG regulator
4	R/W	D1POKM	0	Masks PWROK monitoring of the D1REG regulator
5	R/W	D2POKM	0	Masks PWROK monitoring of the D2REG regulator
6	R/W	D3POKM	0	Masks PWROK monitoring of the D3REG regulator
7	R/W	LPPOKM	0	Masks PWROK monitoring of the LPREG regulator

[1] The register is reset at the initial start-up of the PCF50606 (register type 'S')

[2] When all bits are masked, the PWROK output will be pulled high, in active mode, as long as IOVDD is enabled.

Table 19: PWROKS Power Ok status register

BIT	Mode	Symbol	Reset	Description
0	R	DCDPOK	[1]	PWROK status DCD converter
1	R	DCDEPOK	[1]	PWROK status DCDE converter
2	R	DCUDPOK	[1]	PWROK status DCUD converter
3	R	IOPOK	[1]	PWROK status IOREG regulator
4	R	D1POK	[1]	PWROK status D1REG regulator

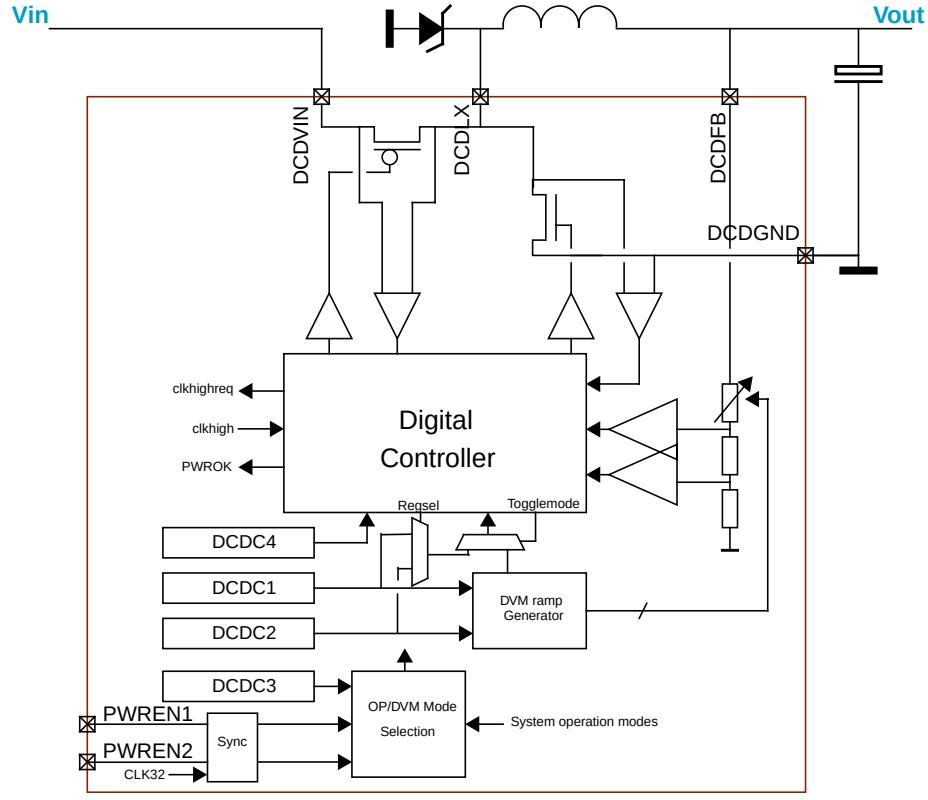
Table 19: PWROKS Power Ok status register *...continued*

BIT	Mode	Symbol	Reset	Description
5	R	D2POK	[1]	PWROK status D2REG regulator
6	R	D3POK	[1]	PWROK status D3REG regulator
7	R	LPPOK	[1]	PWROK status LPREG regulator

[1] This bit represents the status at the moment of the I2C read action.

8.5 DC/DC step down converter (DCD)

The DC/DC step down converter supports three operation modes: ON, OFF and ECO mode. Synchronous rectification is implemented to reduce the power losses caused by the schottky diode.



(1) .

Fig 30. Block diagram DCDC step down convertor (DCD) with internal switches

8.5.1 Operation modes

In ON mode the DC/DC converter operates either in PWM or PFM mode.The PFM mode is entered for low output current situations to maintain a high efficiency.

The switching frequency of the converter is constant during the PWM mode, but varies with the load current in the PFM mode. The DCD converter can be forced to operate continuously in PWM mode by setting the PWMMOD bit independent of the load current. This mode of operation leads to a decreased efficiency at low load currents. The converter can also be forced to operate continuously in PFM mode by setting the PFMMOD bit. Both options must never be activated together since this will lead to instable behaviour.

In OFF mode the converter is stopped. The PMOST switch is either closed (ByPass mode), opened without pull down (float mode) or opened with pull down to VSS (Pull-Down mode) dependent of the OFFMOD bits.

In the PassBy mode the PMOST switch is closed, so the output is connected through the PMOST switch and the inductor to the input voltage. It is strongly recommended to first increase the output voltage of the DCD converter in ON mode to the battery voltage or the highest programmable output voltage before the ByPass mode is entered to will prevent large inrush currents when the ByPass mode is entered (the current limiting circuitry is not activated in the ByPass mode).

In the PullDown mode an NMOST switch connected to the DCDLX pin is closed to discharge the output capacitor to the VSS node through the external inductor.

The OFF mode is either entered directly on command of the host controller (I2C write action) or on changes of the operation mode of the PCF50606 (see paragraph 8.4) resulting from changes of the PWRENx inputs.

In ECO mode the converter only operates in PFM mode using a low power hysteretic controller. This mode of operation reduces the quiescent current, but also reduces the maximum output current.

8.5.2 Dynamic voltage management

The DC/DC step down (DCD) module provides two methods to switch between two pre-programmable output voltages. The regular Dynamic Voltage Management (DVM) behavior is controlled by the PWREN1 and PWREN2 inputs. This allows to simultaneous change the operation mode and output voltage of the DCD. The second method, the voltage toggle mode, enables the possibility to toggle between output-voltages at startup of the DCD converter. This enables a new supply voltage for a digital core voltage of a processor after a sleep period during which no bus communication can take place.
The DVM/Toggle mode control circuitry is shown in Fig 31.

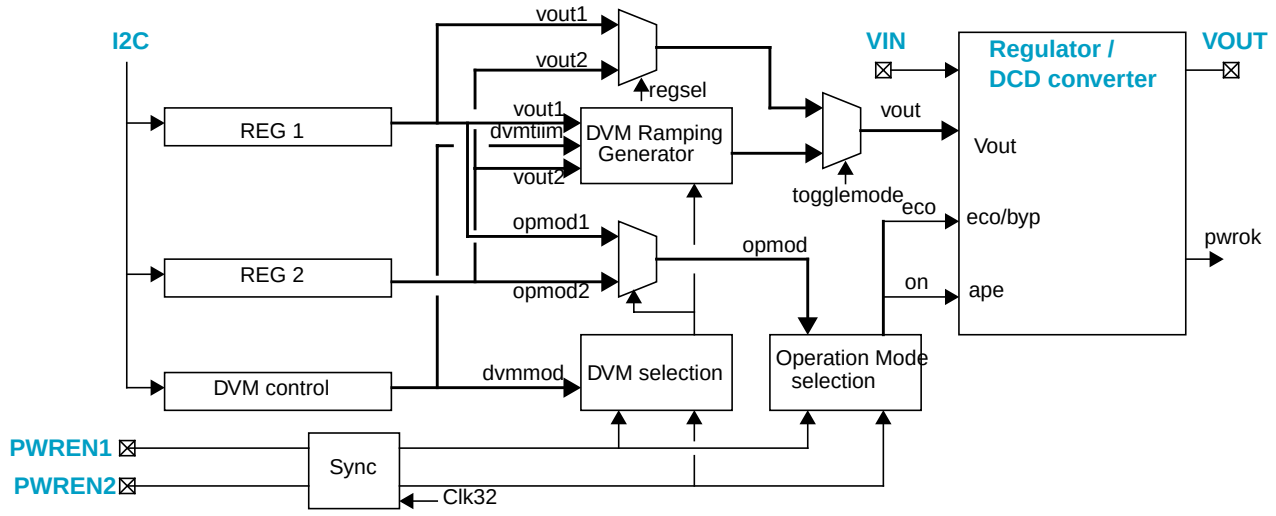


Fig 31. Dynamic Voltage Management control system

The DCD module has two identical control registers REG1 and REG2, containing the VOUT and OPMOD control bits. A third control register, containing the DVMMOD bits, determines the relation between the PWREN1 / PWREN2 input signals and the control register of the DCD module, as shown in Table 20 “Dynamic Voltage Management control of the DCD step down converter”.

Table 20: Dynamic Voltage Management control of the DCD step down converter

PWREN1	PWREN2	DVMMOD bits 2 - 0							
		000	001	010	011	100	101	110	111
0	0	REG1	REG1	REG1	REG1	REG1	REG1	REG1	REG2
0	1	REG1	REG1	REG2	REG1	REG2	REG2	REG1	REG2
1	1	REG1	REG2	REG2	REG2	REG2	REG1	REG1	REG2
1	0	REG1	REG2	REG1	REG1	REG2	REG2	REG2	REG2

The transition speed ramping from the REG1 to REG2 setting and vice versa is programmable through the DVMTIM bits. The transition occurs instantaneous at the programmed PWREN1/PWREN2 combination if the DVMTIM bits equal 00x0.

Other DVMTIM settings will generate a controlled ramping from the REG1 to REG2 settings and vice versa in which the DVMTIM bits define the ramping speed in µs/control step.

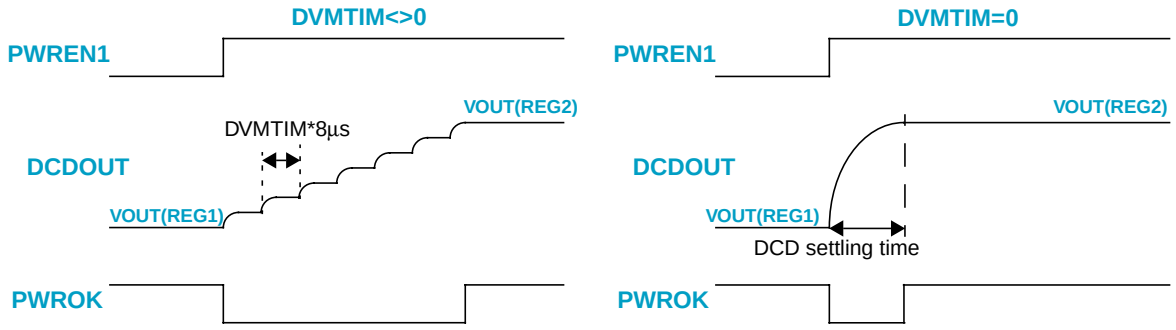


Fig 32. Dynamic Voltage Management transition of the DCD regulator, triggered by PWREN1 (e.g. DVMMOD=001) Left: controlled ramping (DVMTIM<>0), right: instantaneous switching (DVMTIM=0)

The behavior of a regulator output and its PWROK signal during a Dynamic Voltage Management transition is shown in Figure. 32

In the voltage toggle mode, the DCD converter will have to be activated and deactivated by the PWREN1 signal. Each time the DCD converter is deactivated by the PWREN1 signal (negative edge on PWREN1), the output voltage definition of the converter is swapped to the other control register. The next time the converter is activated, the output voltage will be defined by the other register. This enables presetting of a new output voltage, which is used when the DCD converter is activated next time. This mode is especially useful for digital processor cores, which must be powered down before a new core supply voltage can be applied. To activate this Voltage Toggle mode, bit 6 TOGGLEMODE in register DCDC4 has to be set. Bit 7 REGSEL of register DCDC4 indicates the register that is in use to determine the output voltage of the DCD converter.

8.5.3 Control registers

Table 21: DCDC1 control register

BIT	Mode	Symbol	Reset [1]	Description
4-0	R/W	VOUT1	[2]	Output voltage 00000 = 0.900V 10000 = 1.300V 00001 = 0.925V 10001 = 1.325V 00010 = 0.950V 10010 = 1.350V 00011 = 0.975V 10011 = 1.375V 00100 = 1.000V 10100 = 1.400V 00101 = 1.025V 10101 = 1.425V 00110 = 1.050V 10110 = 1.450V 00111 = 1.075V 10111 = 1.475V 01000 = 1.100V 11000 = 1.500V 01001 = 1.125V 11001 = 1.800V 01010 = 1.150V 11010 = 2.100V 01011 = 1.175V 11011 = 2.400V 01100 = 1.200V 11100 = 2.700V 01101 = 1.225V 11101 = 3.000V 01110 = 1.250V 11110 = 3.300V 01111 = 1.275V 11111 = 3.600V
7-5	R/W	OPMOD1	[2]	Operation mode, see table 16

[1] The register is reset each time the PCF50606 enters the STANDBY state (register type ‘O’)

[2] For reset values, see Section 8.24 “PCF50606 variants”.

Table 22: DCDC2 control register

BIT	Mode	Symbol	Reset [1]	Description
4-0	R/W	VOUT2	[2]	Output voltage 00000 = 0.900V 10000 = 1.300V 00001 = 0.925V 10001 = 1.325V 00010 = 0.950V 10010 = 1.350V 00011 = 0.975V 10011 = 1.375V 00100 = 1.000V 10100 = 1.400V 00101 = 1.025V 10101 = 1.425V 00110 = 1.050V 10110 = 1.450V 00111 = 1.075V 10111 = 1.475V 01000 = 1.100V 11000 = 1.500V 01001 = 1.125V 11001 = 1.800V 01010 = 1.150V 11010 = 2.100V 01011 = 1.175V 11011 = 2.400V 01100 = 1.200V 11100 = 2.700V 01101 = 1.225V 11101 = 3.000V 01110 = 1.250V 11110 = 3.300V 01111 = 1.275V 11111 = 3.600V
7-5	R/W	OPMOD2	[2]	Operation mode, see, see table 16

[1] The register is reset each time the PCF50606 enters the STANDBY state (register type ‘O’)

[2] For reset values, see Section 8.24 “PCF50606 variants”

Table 23: DCDC3 DVM mode control register

BIT	Mode	Symbol	Reset [1]	Description
2-0	R/W	DVMMOD	000	DVM mode, see table 20
7-3	R/W	DVMTIM	00000	DVM ramping speed DVMTIM = 0: instantaneous switching DVMTIM <>0: DVMTIM*8us / step

[1] The register is reset at the initial start-up of the PCF50606 (register type 'S')

Table 24: DCDC4 control register

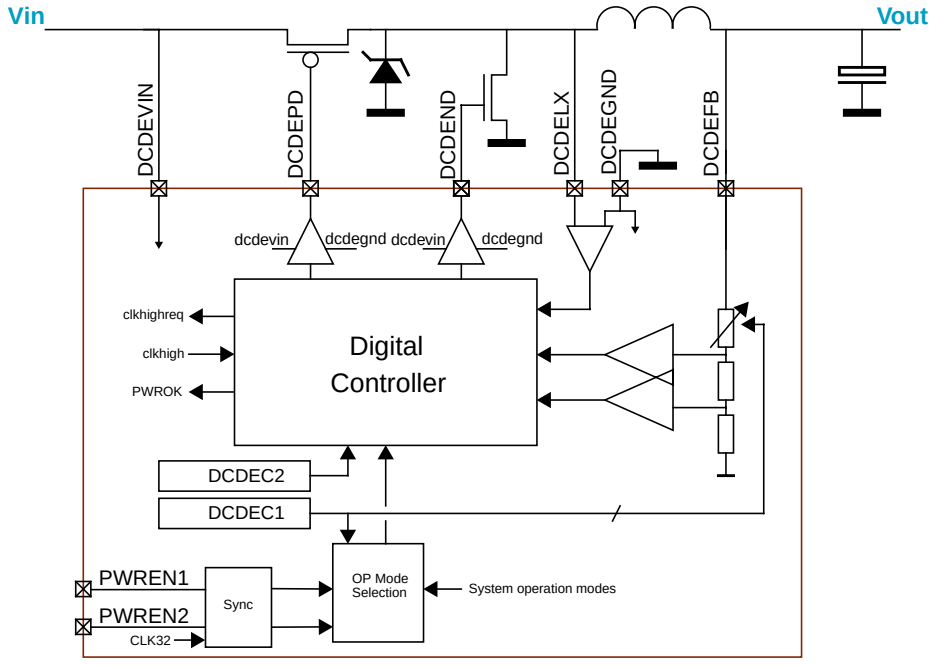
BIT	Mode	Symbol	Reset [1]	Description
1-0	R/W	PFMMOD / PWMMOD	00	PFM or PWM mode only in ON mode 00 : automatic mode selection 01 : PWM mode only 10 : PFM mode only 11 : Invalid combination
3-2	R/W	OFFMOD	00	OFF mode behavior 00: Float mode 01: ByPass mode 10: PullDown mode
5-4	R/W	CURLIM	11	Current limit setting 00: 0.50 A 01: 0.75 A 10: 1.00 A 11: 1.25 A
6	R/W	TOGGLE MODE	0	0: Toggle mode disabled 1: Toggle mode enabled
7	R/W	REGSEL	[2]	0: Register DCDC1 defines the output voltage and operation mode 1: Register DCDC2 defines the output voltage and operation mode

[1] The register is reset at the initial start-up if the PCF50606 (register type 'S')

[2] This bit represents the status at the moment of the I2C read action.

8.6 DC/DC step down converter (DCDE) with external switches

This DC/DC step down converter contains the controller, analog circuitry and external switch drivers for a high current step down converter. The synchronous rectification technique ensures high power efficiency at low output voltage.



(1) .

Fig 33. Block diagram DCDC step down convertor with external power switches (DCDE)

The DC/DC step down converter supports three operation modes: OFF mode (Converter switched off, Vout floating or equal to Vin), ECO mode (Converter activated, Vout as programmed) and ON mode (Converter activated, Vout as programmed).

In ON mode the DC/DC converter operates either in PWM or PFM mode.The PFM mode is entered for low output current situations to maintain a high efficiency.

The switching frequency of the converter is constant during the PWM mode, but changes during the PFM mode. The DCDE converter can be forced to operate continuously in PWM mode by setting the PWMMOD bit independent of the load current. This mode of operation leads to a decreased efficiency at low load currents. The converter can also be forced to operate continuously in PFM mode by setting the PFMMOD bit. Both options must never be activated together since this will lead to instable behaviour.

In OFF mode the converter is stopped. The PMOST switch is either closed (ByPass mode) or opened (Float mode), dependent on the OFFMOD bit.

In the ByPass mode the external PMOST switch is closed, so the output is connected through the PMOST switch and the inductor to the input voltage. It is strongly recommended to first increase the output voltage of the DCDE converter in ON mode to the battery voltage or the highest programmable output voltage before the ByPass mode is entered to will prevent large inrush currents when the ByPass mode is entered (the current limiting circuitry is not activated in the DCDE converter).

The OFF mode is either entered directly on command of the host controller (I2C write action) or on changes of the operation mode of the PCF50606 (see paragraph 8.4) resulting from changes of the PWRENx inputs.

In ECO mode the converter only operates in PFM mode using a low power hysteretic controller. This mode of operation reduces the quiescent current, but also reduces the maximum possible output current.

8.6.1 Control registers

Table 25: DCDEC1 control register

BIT	Mode	Symbol	Reset [1]	Description
3-0	R/W	VOUT	[2]	Output voltage 0000 = 0.9V 0001 = 1.2V 0010 = 1.5V 0011 = 1.8V 0100 = 2.1V 0101 = 2.4V 0110 = 2.7V 0111 = 3.0V 1000 = 3.3V 1001 = 3.3V 1010 = 3.3V 1011 = 3.3V 1100 = 3.3V 1101 = 3.3V 1110 = 3.3V 1111 = 3.3V
4	reserved		[3]	
7-5	R/W	OPMOD	[2]	Operation mode, see table 16

[1] The register is reset each time the PCF50606 enters the STANDBY state (register type ‘O’)

[2] For reset values, see Section 8.24 “PCF50606 variants”.

[3] Reserved bits should be written ‘0’, the return values are not defined.

Table 26: DCDEC2 control register

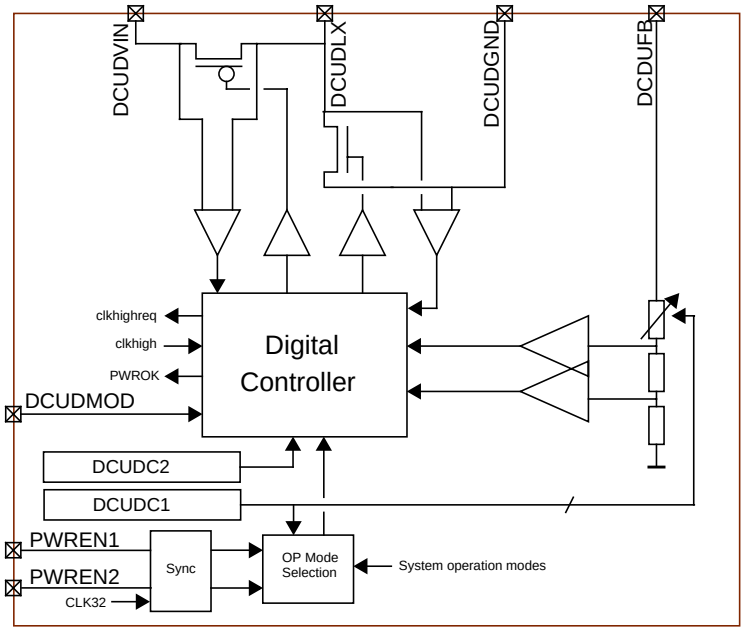
BIT	Mode	Symbol	Reset [1]	Description
1-0	R/W	PFMMOD / PWMMOD	00	PFM or PWM mode only in ON mode 00 : automatic mode selection 01 : PWM mode only 10 : PFM mode only 11 : Invalid combination
2	R/W	OFFMOD	0	OFF mode behavior 0: float mode 1: ByPass mode
7-3	R/W	reserved	[2]	

[1] The register is reset at initial start-up of the PCF50606 (register type 'S')

[2] Reserved bits should be written '0', the return values are not defined.

8.7 DC/DC step up or down converter (DCUD)

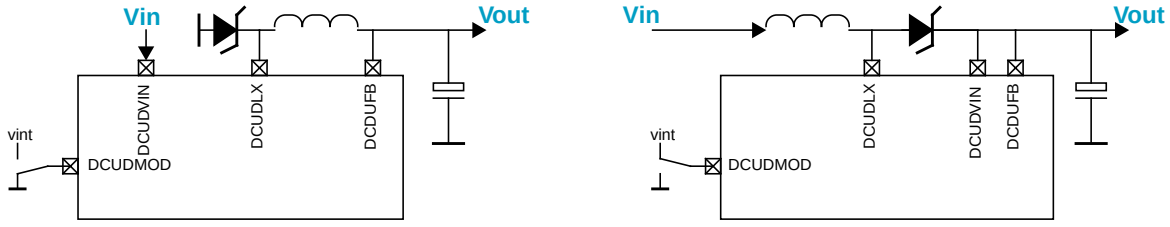
This DC/DC converter with internal switches can be configured as up or down converter and is suitable for down converters up to 500mA and up converters up to 250mA. It supports synchronous rectification to reduce the power losses caused by the schottky diode.



(1) .

Fig 34. Block diagram DCDC step up or down convertor

The converter type is defined by the DCUDMOD control input. If this input is connected to the interval supply voltage (VINT pin) the converter will operate as a step up converter. The connection of the external DC/DC components (inductor, capacitor and schottky diode) depends on the selected converter type, as is shown in Figure. 35.



(1) .

Fig 35. Connection diagram DCDC step up or down, integrated switches, left step down configuration, right step up configuration

The DC/DC step up-or-down converter supports three operation modes: ON, ECO and OFF mode.

In ON mode the DC/DC converter operates either in PWM or PFM mode.The PFM mode is entered for low output current situations to maintain a high efficiency.

The DCUD converter can be forced to operate continuously in PWM mode by setting the PWMMOD for all load currents. This leads to a constant switching frequency, but leads to decreased efficiency at low load currents. The DCUD converter can also be forced to operate continuously in PFM mode by setting the PFMMOD bit. Both options must never be activated together since this will lead to instable behaviour.

In ECO mode the converter only operates in PFM mode using a low power hysteretic controller. This mode of operation reduces the quiescent current, but also reduces the maximum output current.

In OFF mode the converter is stopped. The PMOST switch is either closed (ByPass mode) or opened without pull down (float mode), dependent on the OFFMOD bit.

In the ByPass mode the PMOST switch is closed, so the output is connected through the PMOST switch and the inductor to the input voltage. When configured as a downconverter, it is strongly recommended to first increase the output voltage of the DCUD converter in ON mode to the battery voltage or the highest programmable output voltage before the ByPass mode is entered to prevent large inrush currents (the current limiting circuitry is not activated in the ByPass mode).

When used as step-up converter, in the OFF mode the output voltage of the converter (DCUDOUT) will be pulled to the input voltage of the converter through the external inductor and schottky diode. In ByPass mode the internal PMOST switch will short the external schottky diode, so only the inductor is connected in between the convertor input and output.

The OFF mode is either entered directly on command of the host controller (I2C write action) or on changes of the operation mode of the PCF50606 (see paragraph 8.4) resulting from changes of the PWRENx inputs.

8.7.1 Control registers

Table 27: DCUDC1 control register

BIT	Mode	Symbol	Reset [1]	Description
4-0	R/W	VOUT	[2]	Output voltage [3] [4] 00000 = 0.9V 00001 = 1.2V 00010 = 1.5V 00011 = 1.8V 00100 = 2.1V 00101 = 2.4V 00110 = 2.7V 00111 = 3.0V 01000 = 3.3V 01001 = 3.3V 01010 = 3.3V 01011 = 3.3V 01100 = 3.3V 01101 = 3.3V 01110 = 3.3V 01111 = 3.3V 10000 = 4.0V 10001 = 4.1V 10010 = 4.2V 10011 = 4.3V 10100 = 4.4V 10101 = 4.5V 10110 = 4.6V 10111 = 4.7V 11000 = 4.8V 11001 = 4.9V 11010 = 5.0V 11011 = 5.1V 11100 = 5.2V 11101 = 5.3V 11110 = 5.4V 11111 = 5.5V
7-5	R/W	OPMOD	[2]	Operation mode, see table 16

[1] The register is reset each time the PCF50606 enters the STANDBY state (register type ‘O’)

[2] For reset values, see Section 8.24 “PCF50606 variants”.

[3] Step-down configuration. The output voltage will be equal to the battery voltage at settings of VOUT higher than the actual battery voltage.

[4] Step-up configuration. The output voltage will be equal to the battery voltage at settings of VOUT lower than the actual battery voltage.

Table 28: DCUDC2 control register

BIT	Mode	Symbol	Reset [1]	Description
1-0	R/W	PFMMOD / PWMMOD	00	PFM or PWM mode only in ON mode 00 : automatic mode selection 01 : PWM mode only 10 : PFM mode only 11 : Invalid combination
2	R/W	OFFMOD	0	OFF mode behavior 0: Float mode 1: Bypass mode
3	R/W	reserved	[2]	
5-4	R/W	CURLIM	11	Current limit setting 00: 0.50 A 01: 0.75 A 10: 1.00 A 11: 1.25 A
7-6	R/W	reserved	[2]	

[1] The register is reset at the initial start-up of the PCF50606 (register type ‘S’)

[2] Reserved bits should be written ‘0’, the return values are not defined.

8.8 IOREG low drop-out linear regulator

This linear regulator is implemented as low drop-out voltage, series voltage regulator using a PMOST series element. It requires an external capacitor on the output to keep the regulator stable.

The IOREG linear regulator has programmable output voltages and supports the ECO mode. It acts as the supply for most digital I/O pins of PCF50606. As a result, care must be taken when changing the operation mode of this regulator:

1. I2C access to PCF50606 is only possible when IOREG is in ON mode. When put in ECO or OFF mode, the regulator capability in insufficient to power the I2C interface.
2. When IOREG is switched OFF, most pins which communicate to the host processor PCF50606 are inactive, including the KEEPACT and both PWREN pins. As a result, external signals will not be transferred to the internal on-off controller and the device will leave the ACTIVE state.

The VOUT and OPMOD control bits are reset in STANDBY state.

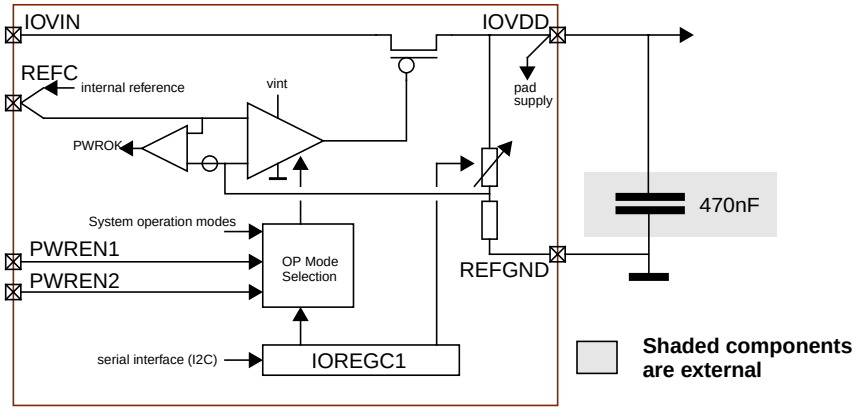


Fig 36. IO Regulator

8.8.1 Control register

Table 29: IOREGC register

BIT	MODE	Symbol	Reset[1]	Description	
4-0	R/W	VOUT	[2]	Output voltage	10000 = 2.5V
					10001 = 2.6V
				01001 = 1.8V	10010 = 2.7V
				01010 = 1.9V	10011 = 2.8V
				01011 = 2.0V	10100 = 2.9V
				01100 = 2.1V	10101 = 3.0V
				01101 = 2.2V	10110 = 3.1V
				01110 = 2.3V	10111 = 3.2V
				01111 = 2.4V	11000 = 3.3V
					others reserved
7-5	R/W	OPMOD	[2]	Operating mode	

[1] The register is reset each time the PCF50606 enters the STANDBY state (register type ‘O’).

[2] For reset values, see Section 8.24 “PCF50606 variants”.

8.9 D1REG, D2REG and D3REG low drop-out linear regulators

1. These linear regulators are implemented as low drop-out voltage, series voltage regulator using a PMOST series element.
2. These linear regulators require an external capacitor on the output to keep the regulator stable.
3. These linear regulators have programmable output voltages and support the ECO mode.
4. The VOUT and OPMOD control bits are reset in STANDBY state.

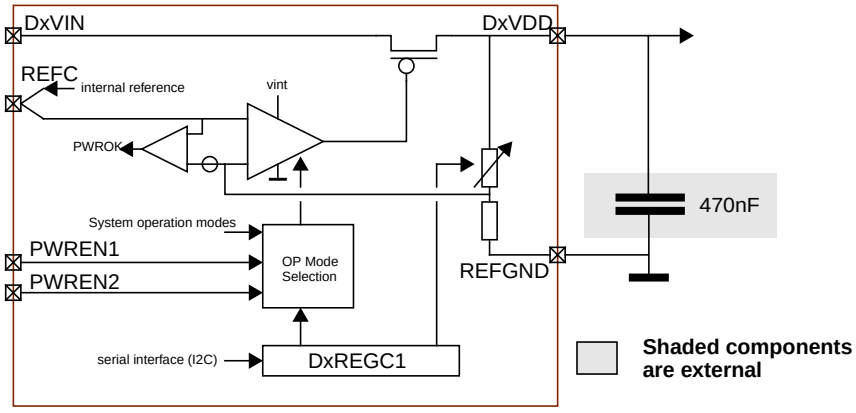


Fig 37. D1/D2/D3 Regulator

8.9.1 Control registers

Table 30: D1REGC1 register

BIT	MODE	Symbol	Reset[1]	Description
4-0	R/W	VOUT	[2]	Output voltage 00000 = 0.9V 00001 = 1.0V 00010 = 1.1V 00011 = 1.2V 00100 = 1.3V 00101 = 1.4V 00110 = 1.5V 00111 = 1.6V 01000 = 1.7V 01001 = 1.8V 01010 = 1.9V 01011 = 2.0V 01100 = 2.1V 01101 = 2.2V 01110 = 2.3V 01111 = 2.4V 10000 = 2.5V 10001 = 2.6V 10010 = 2.7V 10011 = 2.8V 10100 = 2.9V 10101 = 3.0V 10110 = 3.1V 10111 = 3.2V 11000 = 3.3V others reserved
7-5	R/W	OPMOD	[2]	Operating mode

[1] The register is reset each time the PCF50606 enters the STANDBY state (register type ‘O’).

[2] For reset values, see Section 8.24 “PCF50606 variants”.

Table 31: D2REGC1 register

BIT	MODE	Symbol	Reset[1]	Description
4-0	R/W	VOUT	[2]	Output voltage 00000 = 0.9V 00001 = 1.0V 00010 = 1.1V 00011 = 1.2V 00100 = 1.3V 00101 = 1.4V 00110 = 1.5V 00111 = 1.6V 01000 = 1.7V 01001 = 1.8V 01010 = 1.9V 01011 = 2.0V 01100 = 2.1V 01101 = 2.2V 01110 = 2.3V 01111 = 2.4V 10000 = 2.5V 10001 = 2.6V 10010 = 2.7V 10011 = 2.8V 10100 = 2.9V 10101 = 3.0V 10110 = 3.1V 10111 = 3.2V 11000 = 3.3V others reserved
7-5	R/W	OPMOD	[2]	Operating mode

[1] The register is reset each time the PCF50606 enters the STANDBY state (register type ‘O’).

[2] For reset values, see Section 8.24 “PCF50606 variants”.

Table 32: D3REGC1 register

BIT	MODE	Symbol	Reset [1]	Description
4-0	R/W	VOUT	[2]	Output voltage 00000 = 0.9V 00001 = 1.0V 00010 = 1.1V 00011 = 1.2V 00100 = 1.3V 00101 = 1.4V 00110 = 1.5V 00111 = 1.6V 01000 = 1.7V 01001 = 1.8V 01010 = 1.9V 01011 = 2.0V 01100 = 2.1V 01101 = 2.2V 01110 = 2.3V 01111 = 2.4V 10000 = 2.5V 10001 = 2.6V 10010 = 2.7V 10011 = 2.8V 10100 = 2.9V 10101 = 3.0V 10110 = 3.1V 10111 = 3.2V 11000 = 3.3V others reserved
7-5	R/W	OPMOD	[2]	Operating mode

[1] The register is reset each time the PCF50606 enters the STANDBY state (register type 'O').

[2] For reset values, see Section 8.24 "PCF50606 variants".

8.10 LPREG low drop-out linear regulator

1. This linear regulator is implemented as a low drop-out voltage, series voltage regulators using a PMOST series element.
2. This linear regulator requires an external capacitor on the output to keep the regulator stable.
3. This linear regulator has a programmable output voltage and supports the ECO mode. In ECO mode, the LPREG input is connected to either the VBAT, CHGVIN or VBACK pin via the ISM module (Figure 61).
4. This linear regulator can be enabled in ECO mode during the STANDBY or SAVE state. This is defined by the STDBYACT control bit in the LPREGC2 register.
5. The VOUT and OPMOD control bits are reset in STANDBY state when the RSTACT control bit in the LPREGC2 register is set.

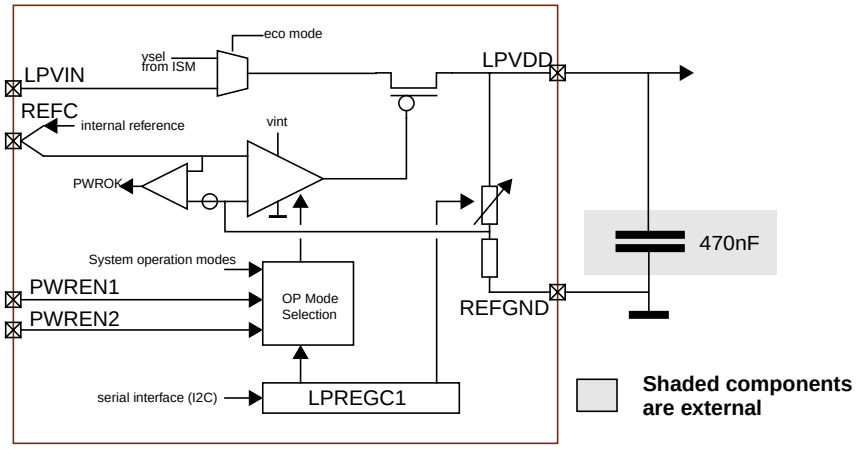


Fig 38. LP Regulator

8.10.1 Control registers

Table 33: LPREGC1 register

BIT	MODE	Symbol	Reset[2]	Description
4-0	R/W	VOUT	[3]	Output voltage 00000 = 0.9V 00001 = 1.0V 00010 = 1.1V 00011 = 1.2V 00100 = 1.3V 00101 = 1.4V 00110 = 1.5V 00111 = 1.6V 01000 = 1.7V 01001 = 1.8V 01010 = 1.9V 01011 = 2.0V 01100 = 2.1V 01101 = 2.2V 01110 = 2.3V 01111 = 2.4V 10000 = 2.5V 10001 = 2.6V 10010 = 2.7V 10011 = 2.8V 10100 = 2.9V 10101 = 3.0V 10110 = 3.1V 10111 = 3.2V 11000 = 3.3V others reserved
7-5	R/W	OPMOD	[3]	Operating mode

[1] If RSTACT=1 (LPREG2 control register) then this register is reset each time the PCF50606 enters the STANDBY state (register type ‘O’) else the register is reset at the initial start-up of the PCF50606 (register type ‘S’).

[2] The register is reset each time the PCF50606 enters the STANDBY state (register type ‘O’).

[3] For reset values, see Section 8.24 “PCF50606 variants”.

Table 34: LPREGC2 register

BIT	MODE	Symbol	Reset [1]	Description
0	R/W	STDBACT	[2]	Mode in STANDBY and SAVE state: 0: OFF 1: ECO
1	R/W	RSTACT	[2]	Reset LP regulator when system is in STANDBY: 0: No 1: Yes
7-2	reserved		[3]	

[1] The register is reset at the initial start-up of the PCF50606 (register type 'S').

[2] For reset values, see Section 8.24 "PCF50606 variants".

[3] Reserved bits should be written '0', the return values are not defined.

8.11 Main Battery Charger (MBC) (not present in PCF50605)

The Main Battery Charger module provides a complete constant-current / constant-voltage linear charger controller for lithium-ion (Li-ion) batteries. Nickel-cadmium (NiCd) and Nickel metal hydride (NiMH) batteries can also be charged with constant current.

An external circuit, consisting of a power PMOST and a low cost small signal NPN and some other components, is required to control the charge current, see Figure 43. The CC and CCCV control circuitry is fully integrated in the PCF50606 charging module.

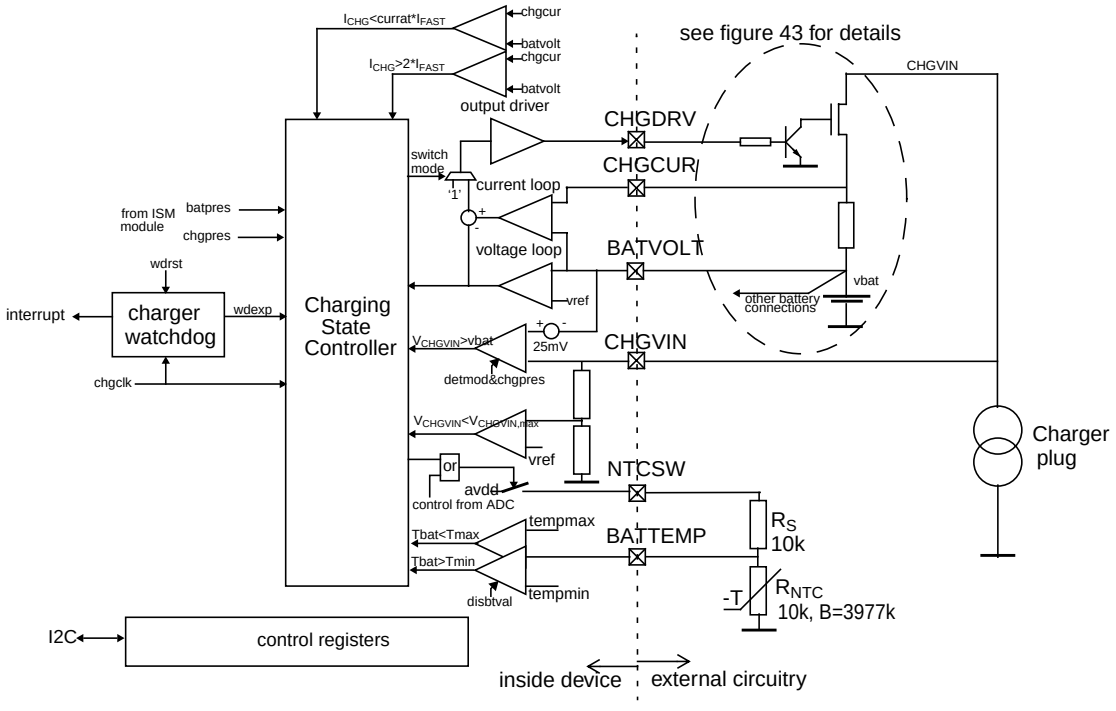


Fig 39. Main Battery Charger Block diagram

The charging process for Li-ion/Li-pol batteries can both be performed fully autonomous or under control of the host controller. The communication between the PCF50606 charger module and the host controller in the latter case is interrupt based, which simplifies the control of the PCF50606 and allows the host controller to go in sleep mode during the charging process. The default charging process is metal mask programmable, which allows to select the most appropriate charging control for a given application.

The fast charge current is determined by the value of the external sense resistor. The charge current in the qualification, pre and trickle charge phase is programmable as a ratio of the fast charge current.

The final float voltage is programmable through the control interface and allows to charge both 4.1V and 4.2V cells.

The charger module offers in addition the SW mode, in which the external circuit is driven in saturation and the full charger plug current is applied to the battery with low dissipation in the external circuit.

8.11.1 Supported charger plugs

The PCF50606 charger circuitry supports a regulated charger plug only. Its output voltage must be at least 0.5V above the battery voltage. Charging will work up to a maximum plug output voltage of 10V.

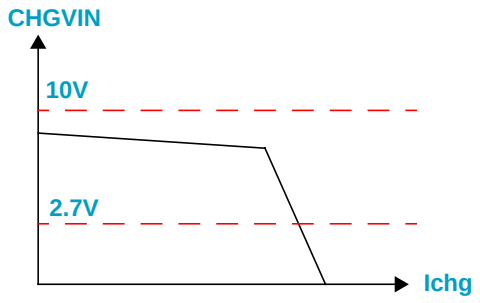


Fig 40. Basic characteristic of the supported charger plug type

8.11.2 Charger presence detection

A charger is detected in two steps. First the Internal Supply Module will set the chgpres signal when the voltage on the CHGVIN pin is higher than the V_{LOWCHG} threshold. The MBC module will activate in this case at regular intervals the comparator comparing the charger voltage with the battery voltage.

A charger is assumed to be present when the voltage on the CHGVIN pin is at least 100mV higher than the actual battery voltage. An interrupt (CHGINS) is issued at that moment. The charger versus battery voltage comparator is from this moment onwards activated continuously.

The disconnection of the charger is detected when the voltage on the CHGVIN pin is lower than the V_{LOWCHG} threshold or lower than the battery voltage + 100mV ~~for 14ms~~ in case the DETMOD bit equals 0. The CHGRM interrupt is issued when this

situation occurs. In case the DETMOD bit is set, the disconnection of the charger is detected and the CHGRM interrupt is issued when the voltage on the CHGVIN pin is lower than the V_{LOWCHG} threshold.

The charging process is on halt (no charge current) whenever DETMOD equals 0 if the charger voltage drops below the battery voltage + 100mV limit. This electronic diode function prevents the discharging of the battery into the charger plug in these low charger voltage situations. The charging continues again when the charger voltage raises beyond the battery voltage + 100mV limit again ~~within the 14ms debounce time~~.

Summarising charger detection and DETMOD value: on charger **insertion** the DETMOD bit is reset to its preprogrammed value and hence charger insertion is detected accordingly. Once the PMU is active the DETMOD bit can be programmed at another value and hence charger **removal** will be detected according to the latest actual DETMOD value.

8.11.3 Charging modes

The MBC module provides a precision current and voltage regulated charging system. Fig. 41 shows the typical charging profile and Fig.42 the flowchart of the charging process.

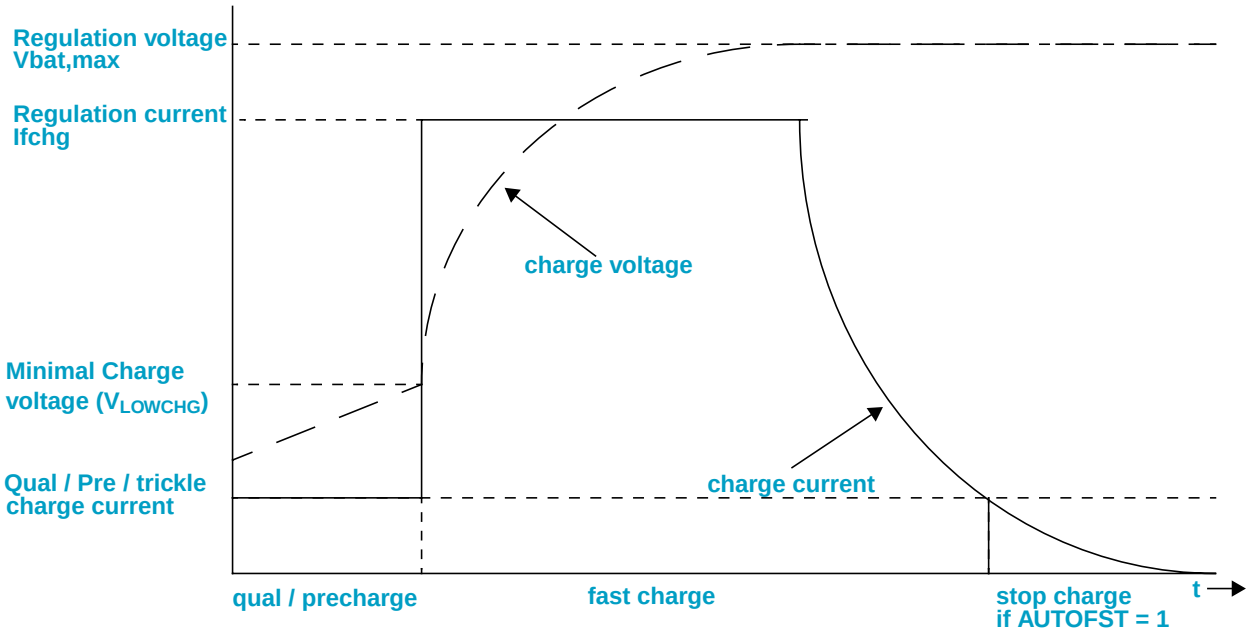


Fig 41. Typical charge profile

The fast charge current is set by the external sense resistor and equals:

$$Ifastchg = \frac{0.11V}{Rsense} \quad (1)$$

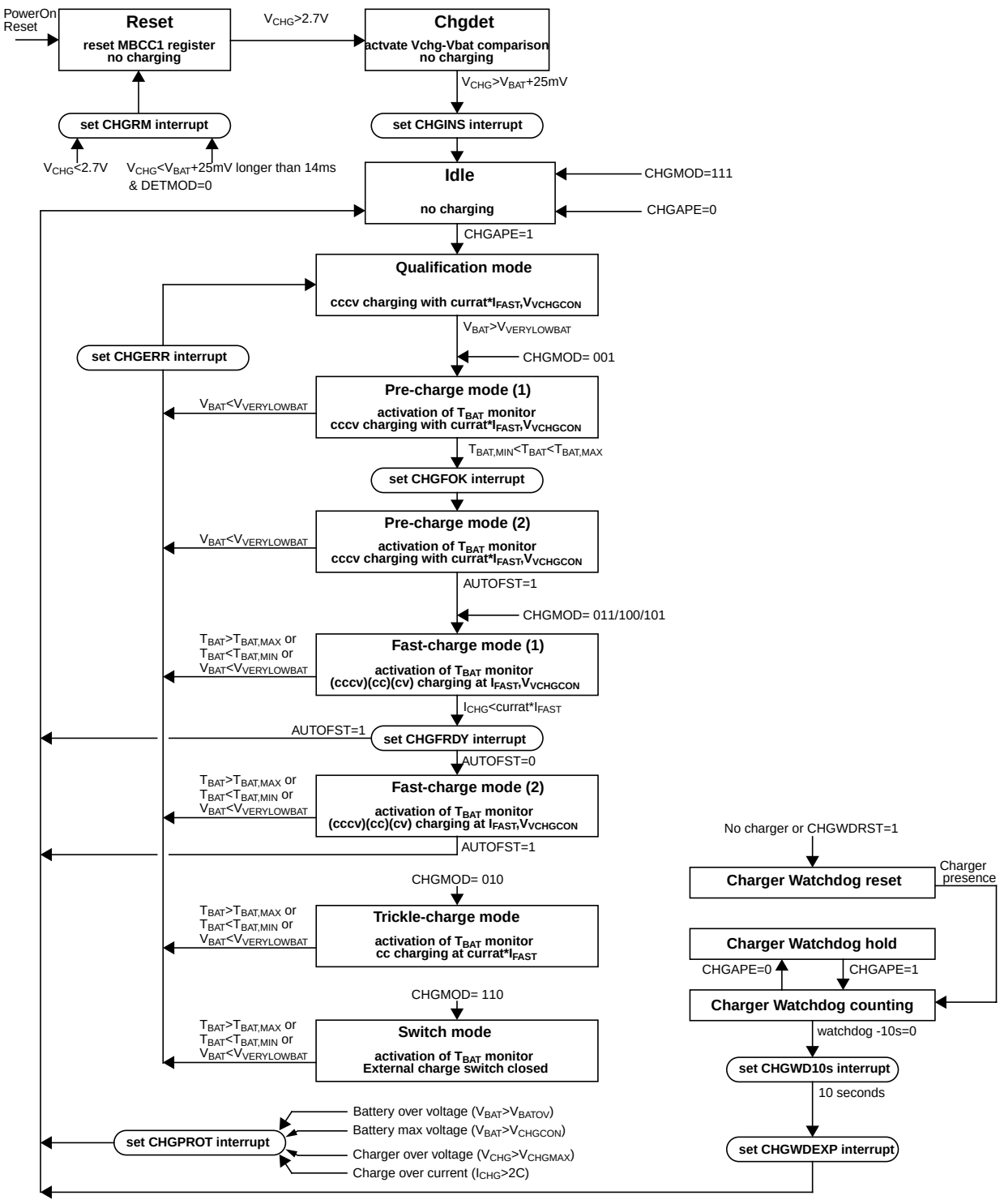


Fig 42. Main Battery Charger Flow Chart

Qualification mode:

At the beginning of the charging sequence, when the battery voltage is lower than the $V_{VERYLOWBAT}$ threshold (2.7V) a battery qualification is performed. The battery is charged with a small current (typical 0.1*Ifast), programmable by the CURRAT bits.

If the battery voltage does not raise above the $V_{VERYLOWBAT}$ threshold within the charger watchdog time, the battery is considered defective and the charging process is stopped.

When the battery voltage raises above the $V_{VERYLOWBAT}$ threshold the charging is continued in the pre-charge mode.

Pre charge mode:

This phase is similar to the qualification phase, however the battery temperature monitoring circuit is activated in this phase.

If the battery temperature is within the fast charge limits a CHGFOK interrupt is given and in case the AUTOFST bit is set the charging will be continued in the fast charge phase.

If the AUTOFST bit is not set the charging will be continued in the pre charge mode till the watchdog timer expires or the CHGMOD bits are set to 01, 10 or 11 by the host controller.

Fast charge mode:

Three types of fast charging mode are provided. In the first one, fast charge with CCCV control (CHGMOD=011) the battery is charged with a fixed current (typically 1C) set by the external sense resistor till the battery reached the programmed voltage limit. In this case the charging process will change from constant current to constant voltage.

The charging current will decrease during the constant voltage mode as the battery becomes more charged. An interrupt (CHGFRDY) is issued when the charging current drops below the programmed qualification / pre / trickle charger current level, determined by the CURRAT bits. If the AUTOFST bit is set, the charging process is stopped at this moment and the MBC module returns to the IDLE mode.

The fast charge mode will continue if the AUTOFST bit is not set till the charge mode is changed by the host controller, the CHGAPE bit is reset by the host controller or the watchdog timer expires.

Selection of the fast charge mode without Constant Current control (CHGMOD=100) will deactivate the charge current control loop. However the charging current is still monitored at the fixed 2C current limit. The charging process will be stopped immediately (IDLE mode) whenever the charging current increases above the 2C current limit. The voltage control loop is active in this mode preventing overcharging of the battery. This mode is typically used in applications where a charger plug with build in current limitation is used.

Selection of the fast charger mode without Constant Voltage control (CHGMOD=101) will switch off the voltage control loop of the charger module. However the battery voltage is still monitored at the programmed VCHGCON setting. The charging

process will be stopped immediately (IDLE mode) whenever the battery voltage raises above the programmed VCHGCON limit. This mode can be used in application where the battery voltage during charging is limited by the charger plug itself.

The charge current is controlled in this fast charge without CV mode by the current control loop. Also the charge current monitor is active, generation the CHGFRDY interrupt when the charge current drops below the programmed qualification / pre / trickle charger current level, determined by the CURRAT bits. Dependent on the value of the AUTOFST bit the charging process is stopped (AUTOFST=1) or continues in the fast charge mode (AUTOFST=0).

NiMH or NiCd battery packs can be fast charged in the fast charge mode with CCCV control using the highest battery voltage limit using the VCHGCON bits. Alternatively the fast charge mode without CV control can be used. In both cases the host controller has to stop the fast charge mode when it detects the desired end of charge criterion ($-\Delta V/\Delta t$ or similar EOC criteria) e.g. using the available ADC module.

Trickle charge mode:

The trickle charge mode, required to complete the charging process of NiMH and NiCd batteries is selected by setting the CHGMOD bits to 010. In this mode the battery is charge with a constant current (voltage control loop is disabled), determined by the value of the CURRAT bits.

The battery over voltage and charge over voltage/current monitors are enabled in this mode and will stop the charging process when any error situation occurs.

Switch mode:

In the switch mode (CHGMOD=110) the charger module forces the external circuitry fully in conduction. The full charger plug current is applied to the battery with a low loss, thus minimizing dissipation in the external circuitry.

The charging process is stopped and restarted in the qualification phase when the battery temperature goes outside the set limits, assuming that the battery temperature monitoring is activated (DISBTVAL=0).

The battery over voltage and charge over voltage/current monitors are enabled in this mode and will stop the charging process immediately whenever the battery voltage or the charging current exceed the set limits (VCHGCON voltage and 2C current).

8.11.4 Battery temperature monitoring

The battery temperature is monitored using a NTC inside or close to the battery pack. The PCF50606 provides a special switched output to supply the half bridge circuit consisting of the mentioned NTC and a fixed resistor. The battery temperature is activated in the pre-charge, fast charge and trickle charge mode. When the battery temperature goes outside the limits during these charge mode the charging sequence will be restarted.

The temperature must be within 0 ^{o}C and 55^{o}C to allow fast charging of the battery. These temperature limits correspond with $0.731*V_{NTCSW}$ and $0.261*V_{NTCSW}$ voltage limits on the BATTEMP input pin assuming a 10K at 25^{o}C NTC (32.56kΩ at 0^{o}C and 2.99kΩ at 55^{o}C) and a 10K fixed resistor half bridge circuit.

8.11.5 Charger over-voltage detection

The voltage on the pin CHGVIN is used to detect a charger over-voltage situation. The over-voltage protection of the MBC module is activated, stopping the charging process, when the voltage on the CHGVIN pin is above the max. charger voltage threshold.

8.11.6 Charger over-current protection

The voltage drop over the sense resistor is monitored by the charger over current comparator. The over current protection is activated, stopping the charging process, when the voltage drop over the external sense resistor increases above twice the nominal value.

8.11.7 Charger watchdog timer

A watchdog circuit stops the charging process after the programmed time. This ensures that the charging process is stopped whenever the host controller does not control the charging process, e.g. in case of a software crash.

Also the watchdog timer can be used as secondary End Of Charge condition (max charging time) since the charging process is stopped when the watchdog timer expires.

The watchdog circuit issues the CHGWD10S interrupt 10s before it expires. This allows the host controller to re-program the watchdog time before it expires. The CHGWDEXP interrupt is set when the watchdog really expires. The charging process can be re-started after expiration of the watchdog time by re-activation of the MBC module. This is done by setting the CHGAPE bit in the MBCC1 control register again.

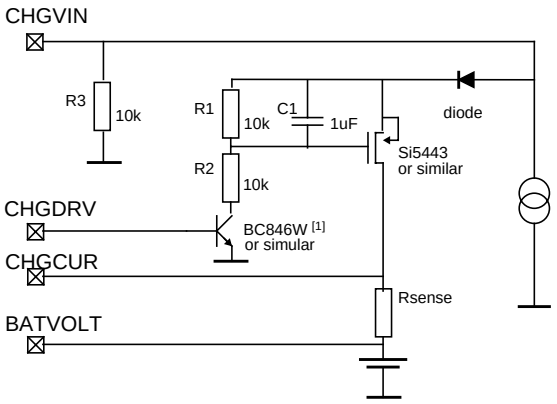
The watchdog timer is reset at every new charger insertion.

In addition the charger watchdog can be reset by the host controller by setting the CHGWDRST bit high in the MBCC1 control register. Note that the watchdog timer starts again a new time-out period in this case.

The watchdog timer is stopped when the CHGAPE bit is reset in the MBCC1 register. In this case the watch dog timer resumes from the ‘stopped’ timer value when the CHGAPE bit is set again in the MBCC1 register.

8.11.8 External components

A small discrete circuit must be used to control the charge current. The recommended implementation of this circuit is given in Figure 43.



(1) This transistor needs a minimal current gain of 50.

Fig 43. MBC external circuitry

The battery temperature is measured by an external NTC and an external resistor, connect in a half bridge configuration. The temperature limits set in the MBC logic are obtained for the following component values:

- R_S: 10k, 1%
- R_{NTC}: 10K, 1%, like Philips NTC (2322-640-63103)

8.11.9 Control registers

Table 35: MBCC1 register (charging mode control)

BIT	Mode	Symbol	Reset [1]	Description
0	R/W	CHGAPE	1	Enable Charging 0: Charging process is stopped and the MBC module is disabled 1: Charging process is enabled and will start when a charger is connected.
1	R/W	AUTOFST	[2]	Fast charge start mode 0: auto fast mode disabled 1: auto fast mode enabled
4-2	R/W	CHGMOD	111	Charge mode 000: qualification mode 001: pre charge mode 010: trickle charge mode 011: fast charge mode (CCCV) 100: fast charge mode (no CC) 101: fast charge mode (no CV) 110: switch mode (no CC, no CV) 111: idle mode Note: The actual charging mode is returned when this bit is read.

Table 35: MBCC1 register (charging mode control) *…continued*

BIT	Mode	Symbol	Reset [1]	Description
5	R/W	DETMOD	[2]	Charger detection mode 0: charger detected if $V_{CHGVIN}>V_{LOWCHG}$ & $V_{CHGVIN}>V_{VBAT}+25mV$ 1: charger detected if $V_{CHGVIN}>V_{LOWCHG}$
6	R/W	WDRST	0	Watchdog timer reset (Note: this bit is cleared when the watchdog timer is reset)
7	R/W			reserved

[1] This register is reset at every charger insertion and at the initial start up of the PCF50606 (register type ‘S/C’).

[2] For reset values, see Section 8.24 “PCF50606 variants”.

Table 36: MBCC2 register (watchdog and synchronization control)

BIT	Mode	Symbol	Reset [1]	Description	
4-0	R/W	WDTIME	10100 (60 min)	Maximum charging time	
				00000: no limit	10000: 48 min
				00001: 3 min	10001: 51 min
				00010: 6 min	10010: 54 min
				00011: 9 min	10011: 57 min
				00100: 12 min	10100: 60 min
				00101: 15 min	10101: 63 min
				00110: 18 min	10110: 66 min
				00111: 21 min	10111: 69 min
				01000: 24 min	11000: 72 min
				01001: 27 min	11001: 75 min
				01010: 30 min	11010: 78 min
				01011: 33 min	11011: 81min
				01100: 36 min	11100: 84 min
				01101: 39 min	11101: 87 min
				01110: 42 min	11110: 90 min
				01111: 45 min	11111: 93 min
7-5	R/W	reserved	[2]		

[1] This register is reset at the initial start up of the PCF50606 (register type ‘S’).

[2] Reserved bits should be written ‘0’, the return values are not defined.

Table 37: MBCC3 register

BIT	Mode	Symbol	Reset [1]	Description
3-0	R/W	VCHGCON	0000 (4.00 V)	Charge Control voltage 0000: 4.00 V 1000: 4.16 V 0001: 4.02 V 1001: 4.18 V 0010: 4.04 V 1010: 4.20 V 0011: 4.06 V 1011: 4.22 V 0100: 4.08 V 1100: 4.24 V 0101: 4.10 V 1101: 4.26 V 0110: 4.12 V 1110: 4.28 V 0111: 4.14 V 1111: 5.00 V
5-4		CURRAT	01 (0.1*I_{FAST})	Current setting qualification, pre and trickle charge mode 00: 0.05 * I_{FAST} 01: 0.10 * I_{FAST} 10: 0.20 * I_{FAST} 11: 0.40 * I_{FAST}
6	R	WDEXP		Watchdog expired
7	R/W	reserved	[2]	

[1] This register is reset at the initial start up of the PCF50606 (register type 'S').

[2] Reserved bits should be written '0', the return values are not defined.

Table 38: MBCS1 register

BIT	Mode	Symbol	Reset	Description
1-0	R	VBATSTAT	[1]	Battery voltage status 00: Vbat < Vbat,min 01: Vbat,min< Vbat < Vchgcon 10: Vchgcon < Vbat < Vbatov 11: Vbat > Vbatov
3-2	R	TBATSTAT	[1]	Battery temperature status 00: Tbat < Tbat,min 01: Tbat,min < Tbat < Tbat,max 11: Tbat,max < Tbat
5-4	R	CHGVIN STAT	[1]	Charger voltage status 00: too low if case DISCHGBAT= 0 then V_{CHGVIN}< $V_{CHGVIN,MIN}$ & V_{CHGVIN}>V_{BAT}+100mV else V_{CHGVIN}< $V_{CHGVIN,MIN}$ 01: within limits 11: too high (V_{CHGVIN}>$V_{CHGVIN,MAX}$)
7-6	R	CHGCUR STAT	[1]	Charging current status 00: I_{CHG} < currat*I_{FST} 01:currat*I_{FST} < I < 2*I_{FST} 11: 2* I_{FST} < I_{CHG}

[1] This bit represents the status at the moment of the I2C read action.

8.12 Backup Battery Charger (BBC)

The backup battery charger (BBC) is implemented as a voltage limited current source with a selectable output resistor. It offers the following features:

- Selectable output resistor to reduce the current at higher voltages.
- Four programmable charge currents.
- Two programmable maximum limiting voltages.
- The BBC can be enabled independently for the ACTIVE and STANDBY state.

The backup battery charger is enabled in ACTIVE state by writing a '1' to the BBCAPEACT control bit. To enable the BBC module in the STANDBY state the BBCAPESTB bit must be set.

The backup battery is charged from the main battery. The backup battery charging is stopped whenever the backup battery reaches the programmed maximum voltage ($V_{VBACK} > V_{LIM}$) or when the main battery voltage drops below the backup battery voltage ($V_{VBACK} > V_{VBAT}$). The charging is resumed whenever the stop-situation is not valid anymore.

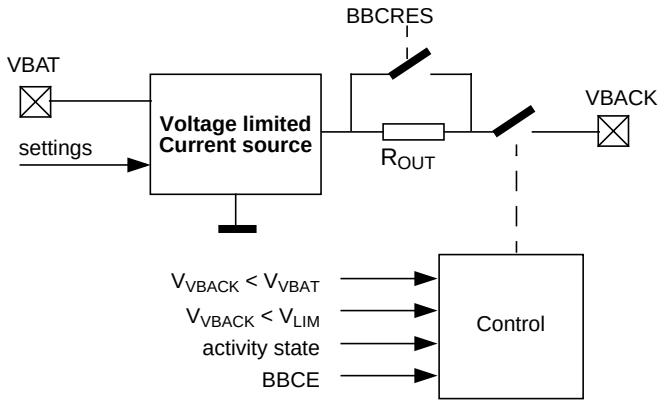


Fig 44. Backup battery charger

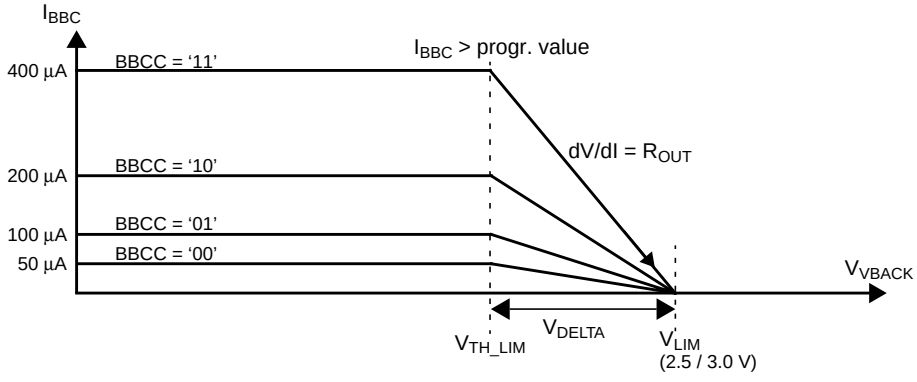


Fig 45. Backup battery charger characteristic with output resistor (BBCR = '0')

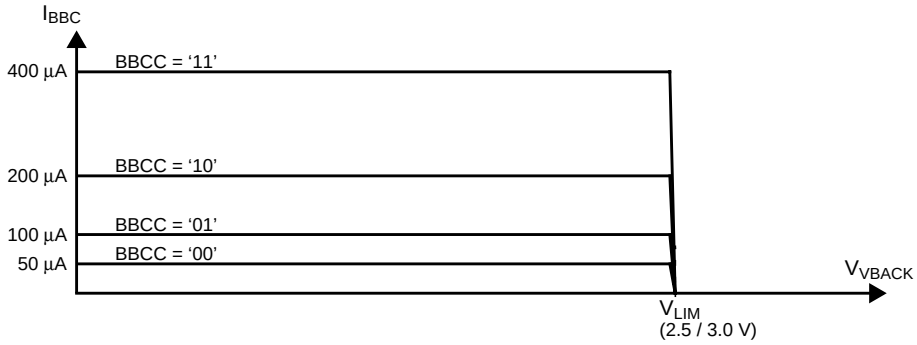


Fig 46. Backup battery charger characteristic without output resistor (BBCR = '1')

8.12.1 Control registers

Table 39: BBCC register

BIT	Mode	Symbol	Reset [1]	Description
0	R/W	BBCAPEACT	[2]	Backup battery charger in ACTIVE state: 0: Charger OFF 1: Charger ON
1	R/W	BBCAPESTB	[2]	Backup battery charger in STANDBY state: 0: Charger OFF 1: Charger ON
3-2	R/W	BBCCUR	[2]	Select backup battery charging current (I_{BBC}): 00: charging current 50 µA 01: charging current 100 µA 10: charging current 200 µA 11: charging current 400 µA
4	R/W	BBCVLIM	[2]	Select limiting voltage for backup battery charger (V_{LIM}): 0: 2.5 V 1: 3.0 V
5	R/W	BBCRES	[2]	Bypass output resistor: 0: output resistor active 1: resistor bypassed
7-6	reserved		[3]	

[1] This register is reset at the initial start up of the PCF50606 (register type'S').

[2] For reset values, see Section 8.24 "PCF50606 variants".

[3] Reserved bits should be written '0', the return values are not defined.

8.13 Analog / Digital Converter (ADC) and Touch Screen Control (TSC) (not present in PCF50605)

The ADC module consist of a 10 bits Analog to Digital converter with internal sample and hold and an input multiplexer offering 5 separate inputs. Two of these inputs can be preprocessed by either a voltage divider or a subtractor circuit, enabling an extended input range. The ADC also supports ratiometric measurements.

The touch screen interface is intended to control and read-out a 4-wire touch screen.It is capable of performing both X and Y position, pressure and plate resistance measurements. In addition the touch screen can be programmed to generate interrupts when the touch screen is pressed. The interrupt mode can be activated in the PCF50606 STAND-BY mode. An touch on the touchscreen will initiate the STAND-BY to ACTIVE transition in this case.

The ADC module and the touch screen module have a combined controller to simplify the control of both modules.

The ADC module can be configured as a 10 bit or 8 bit converter using the ADCRES control bit. The 8 bit conversion mode can be used when faster conversion times are needed and the digital result is not so critical. An 8 bit conversion is not only completed 2 clock cycles earlier than a 10 bit conversion, also the 8 bit result can be read with one I2C read cycle which reduces the data communication time considerably.

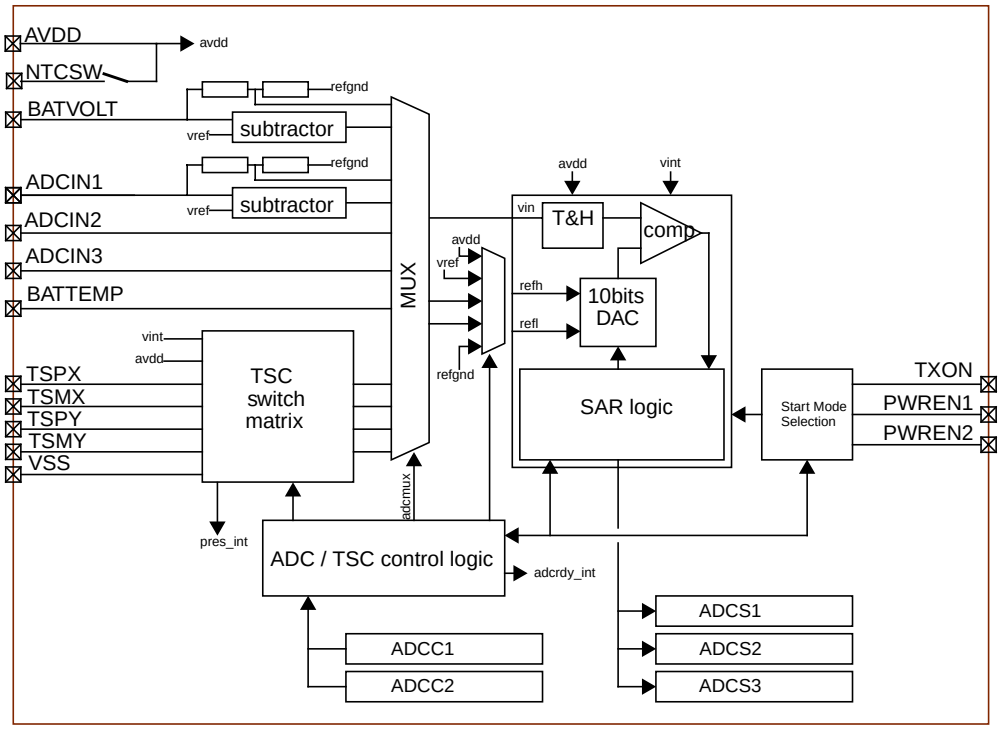


Fig 47. Block diagram ADC module

8.13.1 Analog / Digital Converter

The Analog to Digital Converter (ADC) is a 10 bit resistive DAC successive approximation converter combined with a input multiplexer and a track and hold circuit. The input multiplexer allows conversion of 10 different inputs. The track and hold circuit ensures stable input voltages at the input of the ADC during the conversion.

ADC input configurations:

The input voltage range of the ADCIN2, ADCIN3 and the BATTEMP input correspond to the basic ADC module input voltage range, which is between 0 and 2.4 Volt.

The BATVOLT input can be used to measure a voltage higher than 2.4V such as the battery voltage. Two possible preprocessing options are available:

- The input voltage is divided down by a factor of 2.5 by a resistive divider, allowing an input range of 6.0V. This resistive divider is only activated during the tracking and conversion periods of the ADC; in other cases the resistive divider is kept floating leading to negligible input currents. This mode is selected by setting the ADCMUX bits to 0000. The voltage on the BATVOLT input in this mode is given by the following relation:

(2)

$$Vbatvolt = \frac{ADCDAT(batvolt(fullscale))}{1024} \times 6.0V$$

- The input voltage is processed by a subtractor circuit leading to an ADC input range of 3.1V to 5.4V. This subtractor provides enhanced resolution in the fully charged battery voltage range and is very well suited to detect End Of Charge conditions like the -dV/dt event which occurs when fast charging NiCd or NiMH batteries. The mode is selected by setting the ADCMUX bits to 0001. In this mode, the voltage on the BATVOLT input is given by the following relation:

(3)

$$Vbatvolt = \frac{ADCDAT(batvolt(highres))}{1024} \times 2.4V + 3V$$

The ADCIN1 input circuitry is identical to the BATVOLT circuitry. It allows to measure up to 6.0V voltages on the ADCIN1 input when the ADCMUX bits are set to 0010. The high resolution mode of the ADCIN1 input is selected when the ADCMUX bits are set to 0011. This second high voltage input is typically used to measure the voltage drop over a series resistor connected in between the battery positive terminal and the power transistor output to determine the charging current, as shown in the following figure.

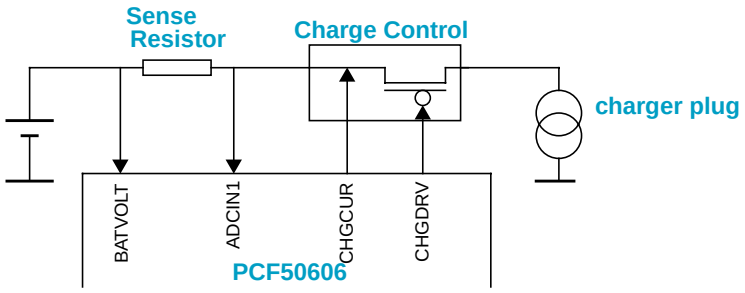


Fig 48. Typical application diagram for charging current measurement

The current through the sense resistor can be calculated from the ADC results using the following relation in case the high voltage inputs (ADCMUX=000 and ADCMUX=010) are selected during the measurement:

(4)

$$Rsense = \frac{ADCDAT(adcin1(fullscale)) - ADCDAT(Batvolt(fullsscale))}{1024} \times \frac{6.0V}{Rsense}$$

An increased resolution is obtained when the subtractor inputs are used. In this case, the current can be calculated using the following equation.

(5)

$$IRsense = \frac{ADCDAT(adcin1(highres)) - ADCDAT(Batvolt(highres))}{1024} \times \frac{2.4V}{Rsense}$$

The ADC module performs a sequential conversion of the BATVOLT and ADCIN1 input, both using the subtractor mode, when ADCMUX equals 1100. The results are stored in the ADCS1 (BATVOLT, most significant bits), ADCS3 (ADCIN1, most significant bits) and ADCS2 (least significant bits of BATVOLT and ADCIN1). This mode allows to start a charging current measurement with a single I2C write action.

The battery temperature is typically measured using an NTC, placed closed to the battery. The ADC and the MBC (main battery charger) module share this external NTC. The external NTC is connected in a half bridge configuration with a known fixed resistor between the NTCSW pin and the PCB ground. The internal node of the half bridge is connected to the BATTEMP input pin of the ADC module, see also figure 49.

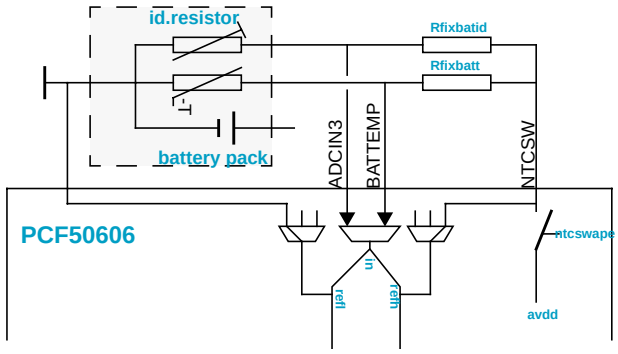


Fig 49. Typical application diagram for battery temperature and identification measurement

The ADC module uses the ratiometric measurement mode for the BATTEMP input input. In this mode the ADC result reflect the ratio of the external fixed and NTC resistor values.

(6)

$$Rntc = \frac{ADCDAT(battemp)}{1023 - ADCDAT(battemp)} \times Rfixbatt$$

The ADCIN3 input also supports the ratiometric measurement mode. This allows to use this input to determine the identification resistor value, present in some battery packs, as also indicated in figure 49.

The biasing of the resistor half bridge is provided by the NTCSW pin of the PCF50606. The biasing is activated at the initialization of an ADC conversion sequence (setting of the ADCSTART bit) when a ratiometric measurement is selected. An additional settling time (10µs or 100µs selected by the TRATSET bit) is added during ratiometric measurements between the ADCSTART command and the actual start of the conversion to allow the external circuitry to stabilize before the sample is taken.

In addition the NTCSW pin can be enabled through the serial interface by setting the NTCSWAPE bit. This allows to activate the NTC circuitry before an ADC conversion is started in case of a long settling time of the NTC circuit. The NTCSW bias is switched off automatically if the conversion is completed when the NTCSWAOFF bit is set, which reduces the number of I2C accesses.

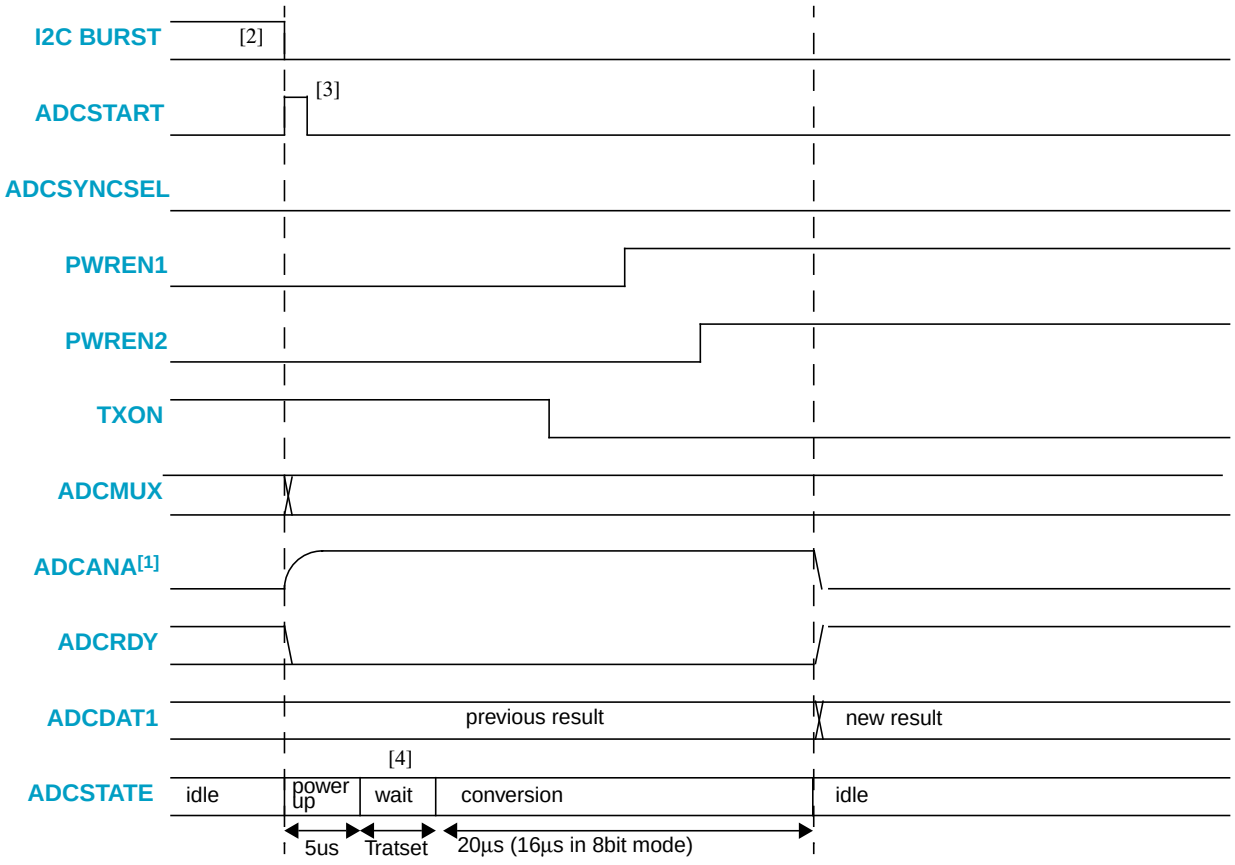
The ACDIN3 input can be used as a normal ADC input if the ratiometric mode is not selected.

ADC synchronization:

The power-up and the conversion time of the ADC equals 25µs. This allows to start a conversion and read back the result in two sequential I2C accesses (takes at least 40µs @ 400kbit I2C speed).

The conversion is started directly by setting the ADCSTART bit in the ADCC2 control register. However the ADC can also be synchronized to external events using the PWREN1, PWREN2 and/or TXON input signals. In this mode, activated by setting the

ADCSYNC bits, the ADC start circuit is armed through the ADCSTART bit. At the same time the analog input circuitry is activated. The actual sample of the input signal is taken with a small delay (Tsyncdel = 495µs to 510µs) after the first selected edge is detected on the selected synchronization input after completion of the programmed sampling time. If the ADC is set to be initiated by an external signal (synchronization mode), but the external signal is not generated, than the process for waiting on the external signal can be terminated by setting the EXTSYNCBREAK bit in the ADCC1 register.



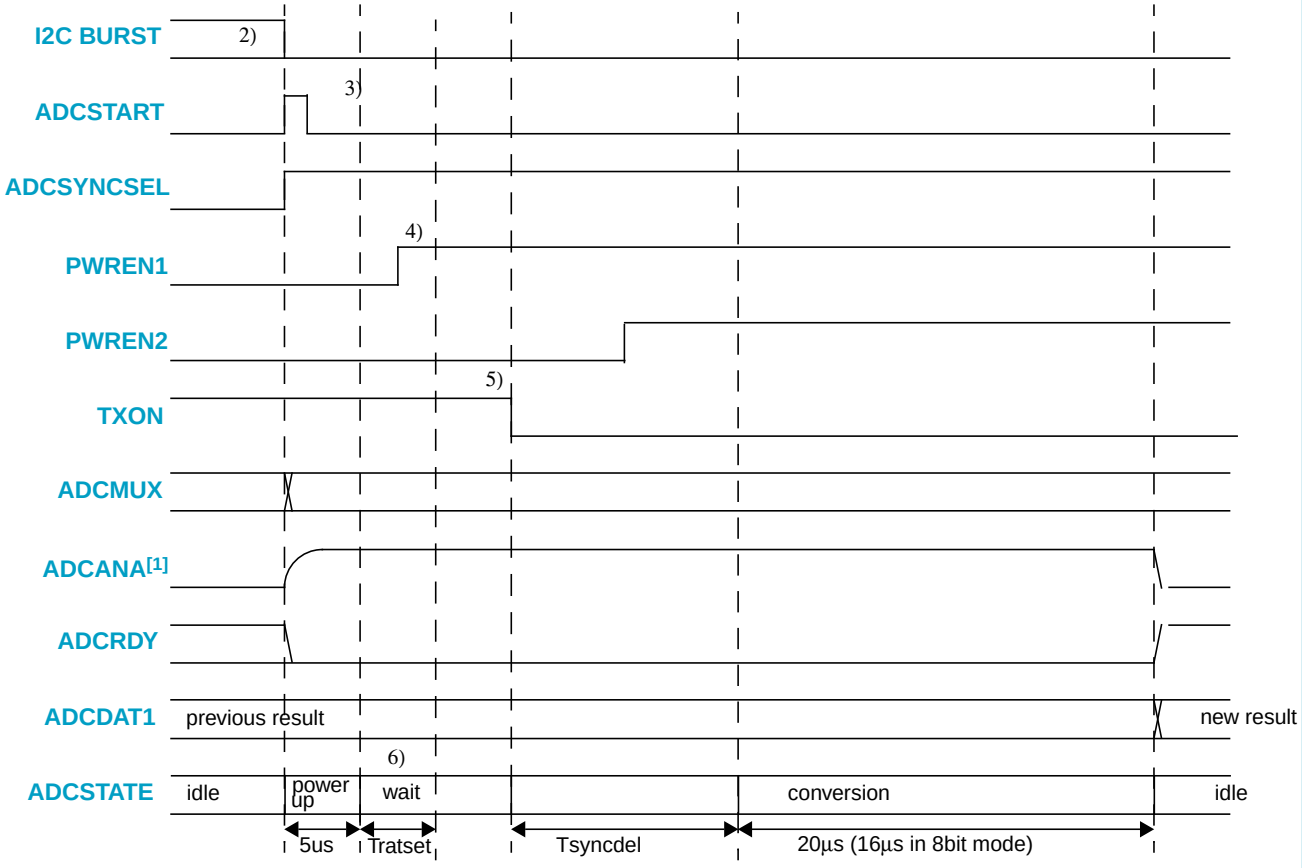
(1) ADCANA represents the state of the ADC analog sub system. It also reflects the operation mode of the input dividers, subtractors and the NTCSW output depending on the selected input.

(2) The ADCC2 register is written last.

(3) The ADCSTART bit is cleared by the ADC logic after the ADC sequence is started

(4) This ratiometric settling time is only included in case a ratiometric measurement is selected.

Fig 50. Timing diagram of the ADC, no external synchronization.



(1) ADCANA represents the state of the ADC analog sub system. It also reflects the operation mode of the input dividers, subtractors and the NTCSW output depending on the selected input.

(2) The ADCC2 register is written last.

(3) The ADCSTART bit is cleared by the ADC logic after the ADC sequence is started

(4) No conversion start will occur before the power-up and if applicable the ratiometric settling period are completed.

(5) The falling edge of TXON activates the conversion

(6) The ratiometric settling time is only included in case a ratiometric measurement is selected.

Fig 51. Timing diagram of the ADC, external synchronization mode selected.

8.13.2 Touch screen interface (TSC)

The touch screen interface provides fully integrated solution to control and read-out 4 wire resistive touch screens. This module supports both position and touch resistance measurements using the ratiometric conversion technique. In addition an interrupt can be generated when the touch screen is touched, which can wake-up the PCF50606 when it is in STANDBY state.

The block diagram of the touch screen interface is shown in Figure 52 “Touch screen interface block diagram”

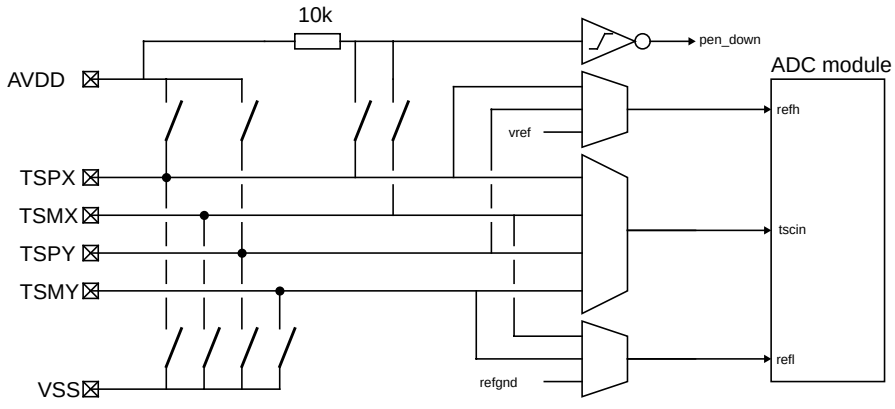


Fig 52. Touch screen interface block diagram

The touch screen interface connects to the touch screen by four wires: TSPX, TSMX, TSPY and TSMY.Each of these pins can be floating, powered or grounded in the touch screen switch matrix. The setting of each pin is determined by the read-out action on the touch screen.

Interrupt generation:

In interrupt mode both X touch screen terminals are connected through the internal switch matrix to a pull up resistor to the internal supply voltage and to the input of the interrupt comparator. The two Y touch screen terminals are connected to VSS via the internal switch matrix.

Whenever the touch screen is pressed, the X and Y plates makes contact with each other, leading to a decrease of the input voltage on the interrupt comparator and thus the generation of the pen_down interrupt.

The interrupt mode can be selected in all operation states of the PCF50606 since the touch screen is supplied through the internal supply. The touch screen circuitry will consume no current in this operation mode as long as the touch screen is not pressed.

Position measurement:

The position of the place, touched on the touch screen is determined through an X and a Y position measurement. Both measurements are performed using the ratiometric concept as shown in Figure 53.

The touch screen is powered in this mode by the externally applied AVDD supply. This can be any of the supply voltages generated by the PCF50606, typically the regulator generating the analog supply voltage for the application is supplying the AVDD.

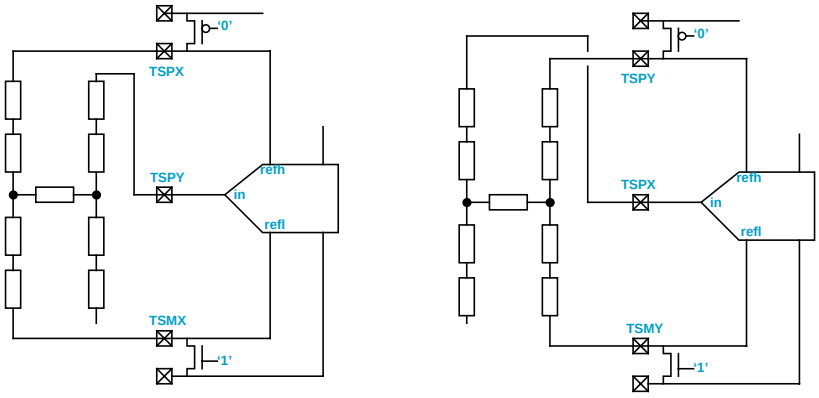


Fig 53. Simplified diagram of a ratiometric position measurement, left X position, right Y position

Touch resistance measurement:

The size of the touched area on the touch screen can be calculated from the contact resistance between the X and Y plate. This resistance is normally referred to as touch resistance.

Again the touch screen is powered through the AVDD supply in this mode.

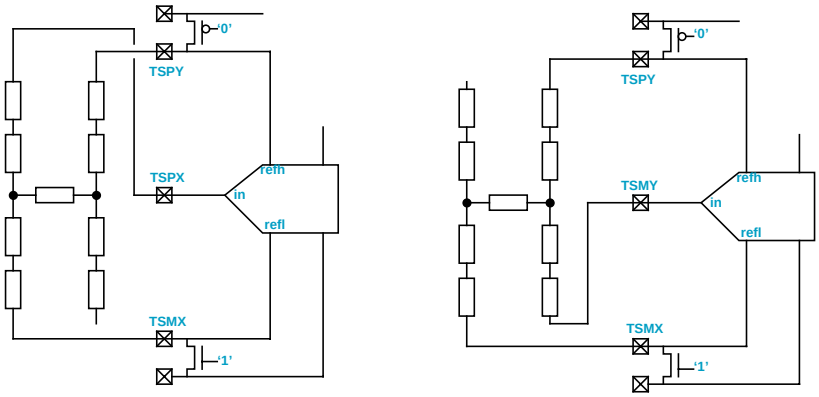


Fig 54. Simplified diagram of a ratiometric touch resistance measurement, left P1 resistance, right P2 resistance

Typically the touch resistance does not need 10 bit resolution, so the 8bit resolution mode can be used during this measurement to improve the conversion speed.

This touch resistance can be calculated from the known plate resistance and the determined touch position (calculation is shown for 10 bits resolution).

$$Rtouch = Rx - plate \times \frac{X - Position}{1024} \times \left(\frac{P1}{P2} - 1\right)$$

Touch screen control:

The touch screen and ADC controller are combined. A touch screen measurement sequence started when the ADCSTART bit is set and one of the touch screen inputs is selected by the ADCMUX control bits. The touch screen conversion can be synchronized to external events (TXON. PWREN1 or PWREN2) using the ADCSYNC mode.

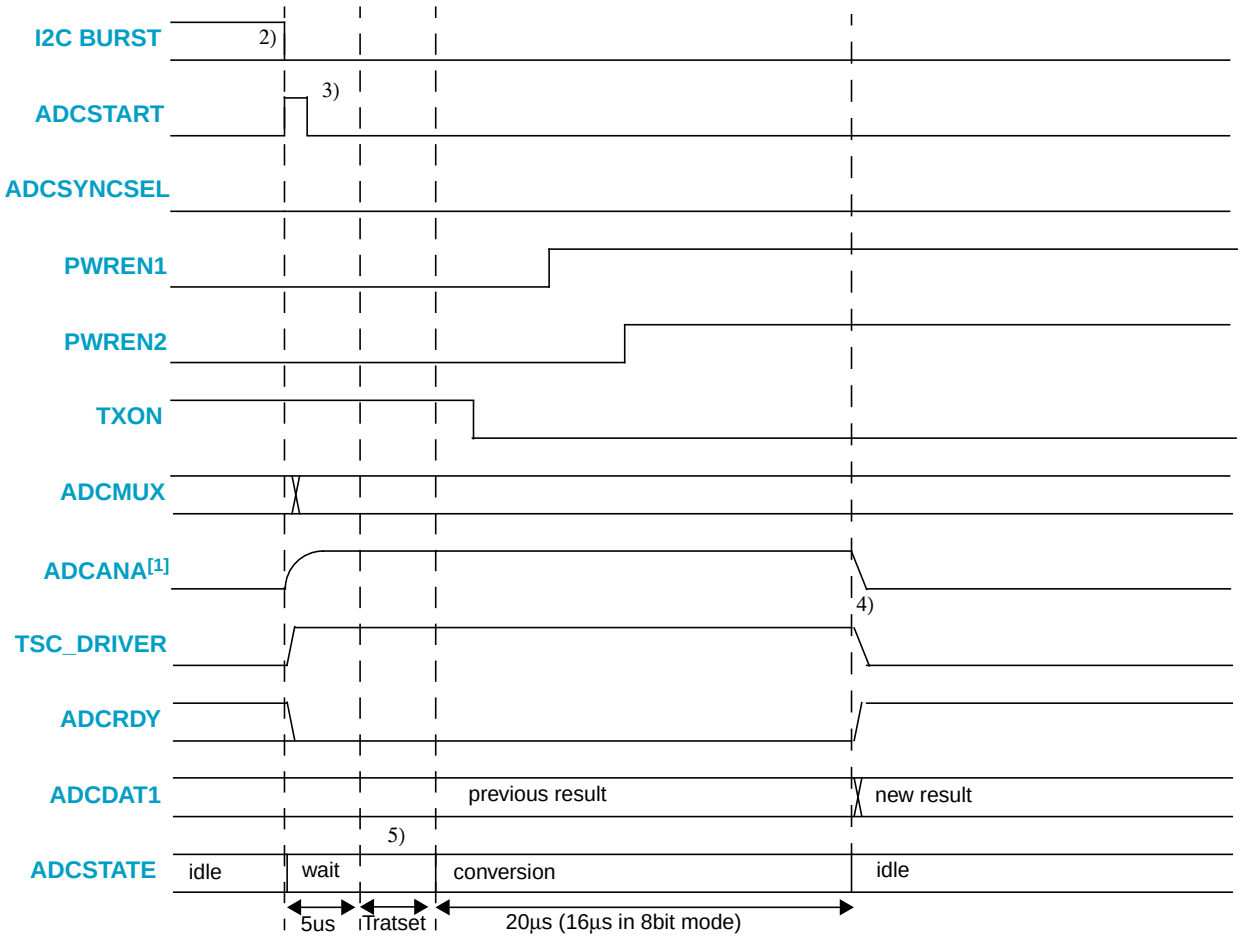
The touch screen and the ADC inputs settings are determined by the combination of the TSCMOD and ADCMUX control bits, as shown in Table 40.

Table 40: Touch screen driver and ADC input selection

TSCMOD	ADCMUX	TSPX	TSMX	TSPY	TSMY	ADC input	ADC vrefh	ADC vrefl
off mode	ADCx input	grounded	grounded	grounded	grounded	[1]	[1]	[1]
interrupt mode	ADCx input	powered AVDD thought resistor	powered AVDD thought resistor	grounded	grounded	[1]	[1]	[1]
X position	don't care	powered AVDD	ground	float	float	TSPY	TSPX internal	TSMX internal
Y position	don't care	float	float	powered AVDD	grounded	TSPX	TSPY internal	TSMY internal
P1 resistance	don't care	float	grounded	powered AVDD	float	TSPX	TSPY internal	TSMX internal
P2 resistance	don't care	float	grounded	powered AVDD	float	TSMY	TSPY internal	TSMX internal

[1] Setting is determined by the selected ADC input and measurement mode, see

The additional waiting time between the ADCSTART bit is set and the start of the actual ADC conversion is also applied for all the touch screen measurements as they are all performed in the ratiometric mode. The ADCTSDEL bit selects again the duration of this waiting timer.



(1) ADCANA represents the state of the ADC analog sub system. It also reflects the operation mode of the input dividers, subtractors and the NTCSW output depending on the selected input.

(2) The ADCC2 register is written last, selecting one of the touch screen inputs.

(3) The ADCSTART bit is cleared by the ADC logic after the ADC sequence is started

(4) The touch screen drivers are activated during the full conversion period.

(5) The ratiometric settling time is included during touch screen measurements.

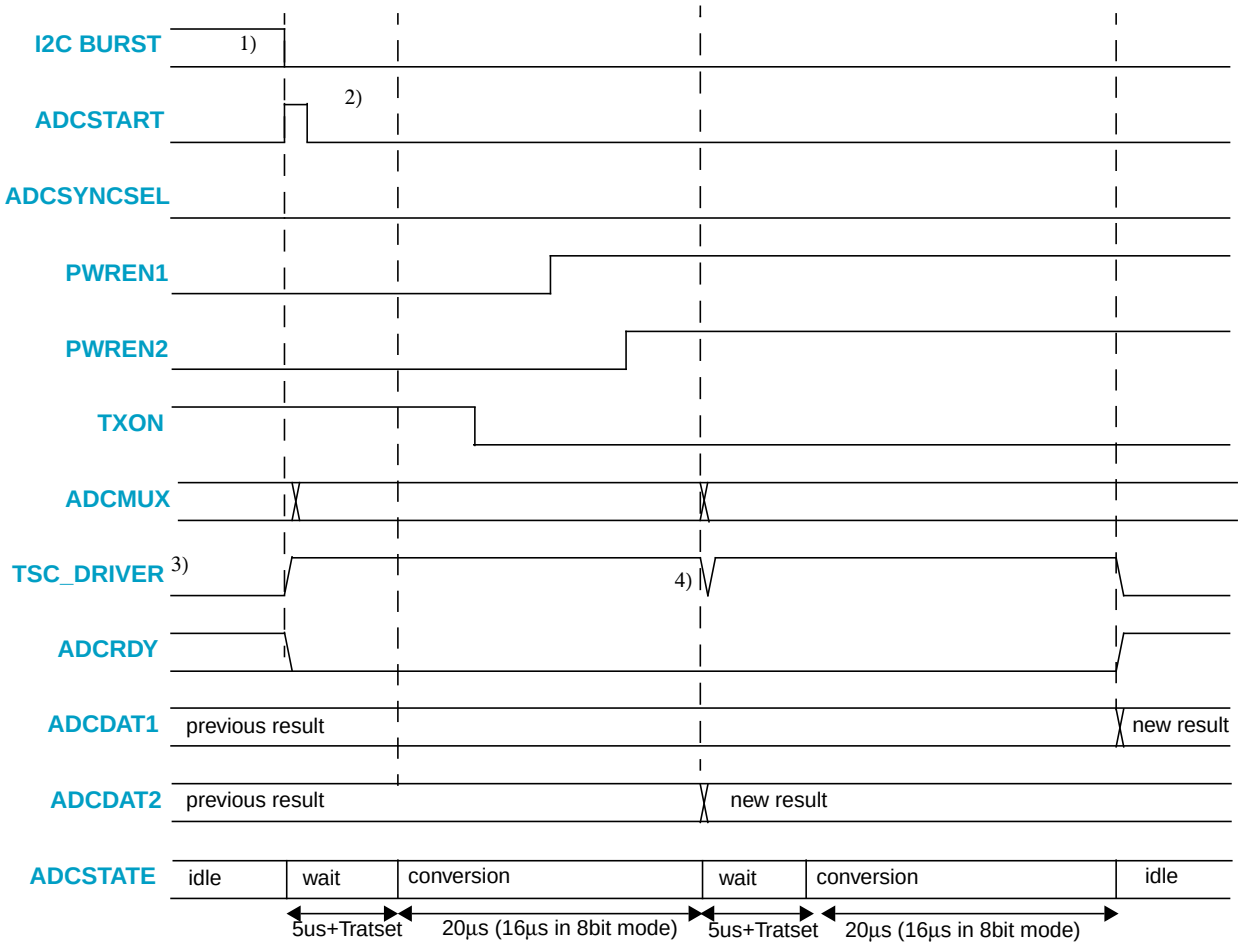
Fig 55. Timing diagram of the touch screen, single measurement no external synchronization.

The TSC module is able to perform single touchscreen measurement (X or Y position) and supports also dual measurement sequences. First a position measurement sequence can be performed, consisting of a X and Y position measurement. Also a dual touch resistance measurement sequence, consisting of a P1 and a P2 resistance measurement is supported.

The results of a single touch screen measurement is stored in the ADCS1 and ADCS2 registers. In case of a dual measurement sequence, the first (X or P1) result is stored in the TSCS1 and TSCS2 registers while the second (Y or P2) result is stored in the ADCS1 and ADCS2 registers.

The ADCRDY interrupt is set after completion of the touch screen measurement to indicate that the touch screen measurement is completed.

The ADCRDY interrupt will be issued after completion the full measurement in case of X+Y or P1+P2 measurement sequences, so after the completion of the Y and P2 measurement.



(1) The ADCC2 register is written last.

(2) The ADCSTART bit is cleared by the ADC logic after the ADC sequence is started

(3) The touch screen drivers are activated during the full conversion period.

(4) The touch screen drivers are changed to the next measurement setting.

Fig 56. Timing diagram of the touch screen, dual measurement sequence without external synchronization.

8.13.3 ADC / Touch screen supply

The analog parts of the ADC and Touch screen module is supplied by the AVDD pin. It is recommended to supply the AVDD pin by the regulator which is used as analog supply in the system (D1, D2, D3 or LP regulator) to prevent coupling between the analog and digital system parts.

Alternatively the AVDD pin can be connected to the internal supply (VINT). However the touch screen circuitry can not be used in this case, since the internal supply is not capable to generate the high supply currents for the touch screen biasing.

8.13.4 Control registers

Table 41: ADCC1 register

BIT	Mode	Symbol	Reset [1]	Description
0	R/W	TSCMODACT	0	Touchscreen mode in ACTIVE state if touch screen is not selected as ADC input 0: Idle mode 1: Interrupt mode
1	R/W	TSCMODSTB	0	Touch screen mode in STANDBY state 0: Idle mode 1: Interrupt mode, with WAKE-UP function
2	R/W	TRATSET	0	Ratiometric settling time 0: 10µs 1: 100µs
3	R/W	NTCSWAPE	0	Enabling of the NTCSW bias 0: off 1: on
4	R/W	NTCSWAOFF	0	Enabling of the NTCSW auto off mode 0: NTCSW bias defined by NTCSWAPE 1: NTCSW bias disabled when the ADC conversion is completed [2]
5	R/W	EXTSYNCBREAK	0	0: allows ADC waiting for external sync 1: stops waiting for an external sync and resets the ADC; No ADC conversion is performed.
6	R/W	reserved	[3]	
7	R	TSCINT	[4]	Touch screen pen status (status from touch screen interrupt comparator) 0: Pen-up (no press/touch on screen) 1: Pen-down (press/touch on screen)

[1] The register is reset at the initial start up of the PCF50606 (register type ‘S’)

[2] The NTCSWAPE bit is also reset when a conversion is completed in this case

[3] Reserved bits should be written ‘0’, the return values are not defined.

[4] This bit represent the status at the moment of the I2C read action.

Table 42: ADCC2 control register

BIT	Mode	Symbol	Reset [1]	Description
0	R/W	ADCSTART	0	ADC start command if ADCSYNSEL=00 the conversion is started when the ADCSTART bit is set If ADCSYNSEL<>00, the ADC is armed to detect the external start command on the selected sync input(s)
4-1	R/W	ADCMUX	0000	ADC input selection 0000: BATVOLT, resistive divider 0001: BATVOLT, subtractor 0010: ADCIN1, resistive divider 0011: ADCIN1, subtractor 0100: BATTEMP, ratiometric 0101: ADCIN2 0110: ADCIN3 0111: ADCIN3, ratiometric 1000: X position measurement 1001: Y position measurement 1010: P1 plate resistance 1011: P2 plate resistance 1100:BATVOLT+ADCIN1 subtractor sequence 1101: reserved 1110: X+Y sequence 1111: P1+P2 plate resistance
6-5	R/W	ADCSYNC	00	ADC synchronization selection 00: no external synchronization 01: falling edge of TXON 10: rising edge of PWREN1 11: rising edge of PWREN2
7	R/W	ADCRES	0	ADC resolution selection 0: 10 bit 1: 8 bit

[1] The register is reset each time the PCF50606 enters the STANDBY state (register type ‘O’)

Table 43: ADCS1 result register

BIT	Mode	Symbol	Reset	Description
7-0	R	ADCDA1TH	[1]	8 most significant bits of the ADC result

[1] These bits represent the status at the moment of the I2C read action.

Table 44: ADCS2 result register

BIT	Mode	Symbol	Reset	Description
1-0	R	ADCDAT1L	[1]	2 least significant bits of the ADC result

Table 44: ADCS2 result register…*continued*

BIT	Mode	Symbol	Reset	Description
3-2	R	ADCDAT2L	[1]	2 least significant bits of the second ADC / TSC conversion of an ADC measurement sequence
6-4	R	reserved	[3]	
7	R	ADCRDY	[1]	ADC status if 1, the conversion is completed if 0, the ADC is waiting for an external sync or the conversion is in progress

[1] These bits represent the status at the moment of the I2C read action.

[2] Reserved bits should be written '0', the return values are not defined.

Table 45: ADCS3 result register

BIT	Mode	Symbol	Reset	Description
7-0	R	ADCDAT2H	[1]	8 most significant bits of the first ADC conversion of an ADC / TSC measurement sequence

[1] These bits represent the status at the moment of the I2C read action.

8.14 Accessory Detection (ACD) (not present on PCF50605)

The accessory detection circuit monitors the voltage on the ADCIN2 input. It indicates the presence of an accessory when the ADCIN2 voltage is lowered below the ACD threshold value. It offers the following features:

- The ACD is enabled through the I2C interface.
- Programmable threshold (V_{VTHACD}) voltage.
- Interrupt generation when accessory is inserted and removed.
- Build in hysteresis and debouncing to prevent system oscillations

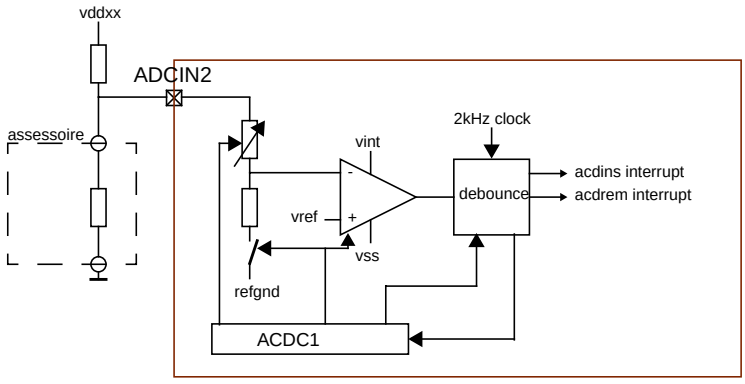


Fig 57. Block diagram of the ACD module

The functional behavior of the ACD module is shown in Figure 58 "Functional ACD behavior"

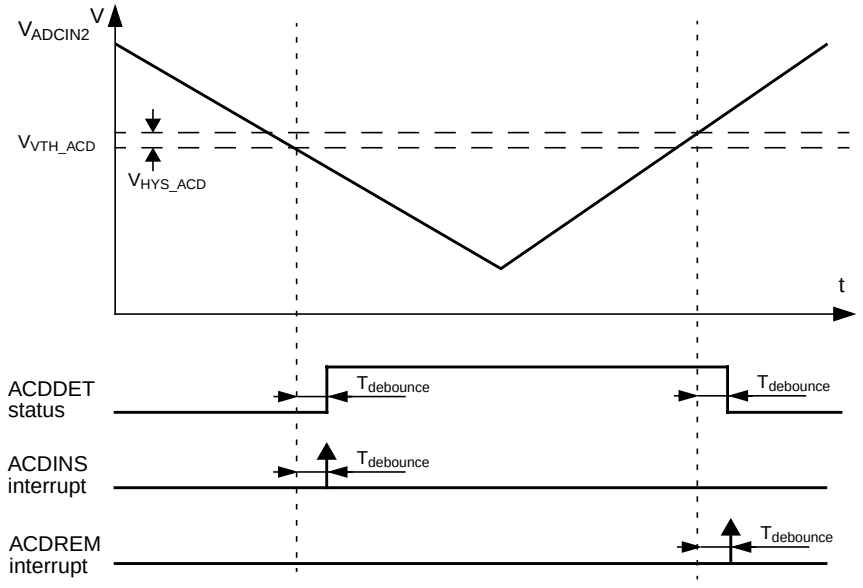


Fig 58. Functional ACD behavior

The ACD module is activated by the ACDAPE bit in the ACDC1 register. The THRSHLD control bits in the ACDC1 register select the threshold voltage (V_{VTHACD}).

The status of the accessory detection can be read through the ACDDET status bit.

8.14.1 Control and status registers

Table 46: ACDC1 register

BIT	Mode	Symbol	Reset[1]	Description
0	R	ACDDET	[2]	ADCIN2 voltage is lower than programmed threshold voltage
3-1	R/W	THRSHLD	000	Threshold voltage: 000: 1.00V 001: 1.20V 010: 1.40V 011: 1.60V 100: 1.80V 101: 2.00V 110: 2.20V 111: 2.40V
4	R/W	DISDB	0	0: Enable 14ms debounce filter 1: Disable 14ms debounce filter
6-5	reserved		[3]	
7	R/W	ACDAPE	0	0: Disable ACD module 1: Enable ACD module

[1] The register is reset at the initial start up of the PCF50606 (register type ‘S’).

[2] This bit represents the status at the moment of the I2C read action.

[3] Reserved bits should be written ‘0’, the return values are not defined.

8.15 Battery voltage monitor (BVM)

The BVM monitors the main battery voltage. It offers the following features:

- The BVM is automatically activated by the On/Off Control logic.
- Programmable low battery threshold (V_{LOWBAT}).
- Interrupt generation when battery voltage drops below the low battery threshold (V_{LOWBAT}).
- Hysteresis and selectable debounce filter built in to prevent system oscillations.

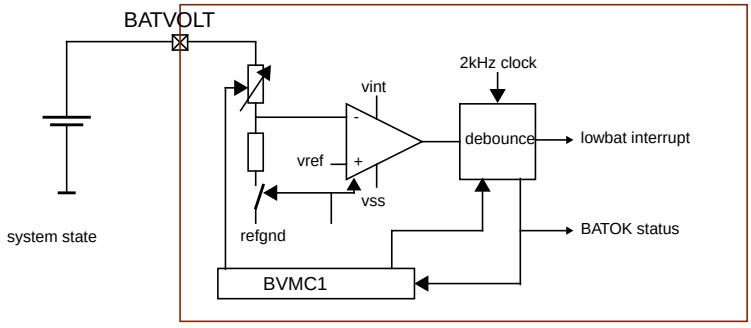


Fig 59. Block diagram of the BVM module

The functional behavior of the BVM is shown in Figure 60 “Functional behavior of the BVM module”

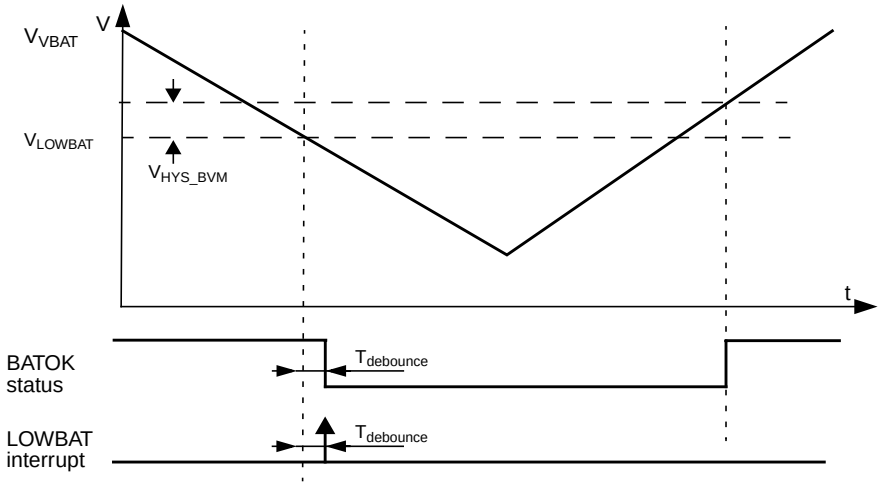


Fig 60. Functional behavior of the BVM module

The battery voltage monitor observes permanently the main battery voltage. The BATOK (one of the functions of the GPO(OD) pins) signal is pulled high as long as the battery voltage is higher than the set V_{LOWBAT} threshold. The BATOK signal is forced low whenever the battery voltage is lower than the V_{LOWBAT} threshold.

A LOWBAT interrupt is generated if the battery voltage drops below the programmed V_{LOWBAT} threshold.

When a low battery situation is detected in ACTIVE state, the host-controller should initiate a transition to STANDBY state. In case the host controller does not initiate a transition to the STANDBY state within 8 seconds after the interrupt occurred, the on/off controller forces the PCF50606 to the STANDBY state in order to prevent a too deep discharge of the battery.

Note that transition to STANDBY on the $\overline{LOWBAT}$ signal is interrupt driven. This means that if a transition to STANDBY has taken place on basis of the LOWBAT interrupt, that at the next activation of the chip, the LOWBAT interrupt must be cleared by reading the corresponding interrupt register. If this is omitted, the deactivation on LOWBAT is not working.

The battery status information of the BVM is also used by the on/off controller to prevent system start up at low battery voltage situations.

A hysteresis and debounce filter is built in to prevent fast cycling. The rising edge of the BVM low battery signal is debounced with a debounce time of 62 ms. The falling edge is not debounced. The debounce filter can be disabled by the DISDB control bit in the BVMC register.

The THRSHLD control bits in the BVMC register select the threshold voltage (V_{LOWBAT}). The status of the low battery condition is available via the LOWBAT status bit.

8.15.1 Control and status registers

Table 47: BVMC register

BIT	Mode	Symbol	Reset[1]	Description
0	R	LOWBAT	[2]	Battery voltage is lower than the programmed threshold
3-1	R/W	THRSHLD	[4]	Threshold voltage: 000: n.a. 100: 3.10 V 001: 2.80 V 101: 3.20 V 010: 2.90 V 110: 3.30 V 011: 3.00V 111: 3.40 V
4	R/W	DISDB	0	0: Enable 62ms debounce filter 1: Disable 62ms debounce filter
7-5	reserved		[3]	

[1] The register is reset at the initial start up of the PCF50606 (register type ‘S’).

[2] This bit represents the status at the moment of the I2C read action.

[3] Reserved bits should be written ‘0’, the return values are not defined.

[4] For reset values, see Section 8.24 “PCF50606 variants”.

8.16 Internal supply and on-chip reference

The Internal Supply (ISM) and on-chip reference (OCR) offer the following features:

- The internal supply generates the supply voltage for the PCF50606 internal circuitry from the applied main battery, backup battery or charger voltage.

- The internal supply generates the supply voltage for the LPREG supply (ECO mode only) from the applied main battery, backup battery or charger voltage (see Section 8.10 “LPREG low drop-out linear regulator”)
- The internal supply module performs the detection of the backup battery, the main battery, and the charger using comparators with fixed threshold levels. The threshold for the main battery and the charger is typically 2.7 V ($V_{VERYLOWBAT}$ and V_{LOWCHG}), for the backup battery it is typically 1.3 V ($V_{LOWBACK}$).
- The on-chip reference generates the reference voltage and bias currents for the PCF50606 internal modules. The voltage at the REFC pin must not be used for other purposes, since the reference source impedance is very high.
- The on-chip reference contains a power-on reset circuit that resets the system at initial power start up.
- The capacitors at the VINT and REFC pins must have the capacitance values as shown in Figure 61. Other values can cause the device to start up in an incorrect way or can result in noisy output voltages, ADC measurements and so on.

Figure 61 shows block diagram of the internal supply module, low-power regulator and on-chip reference.

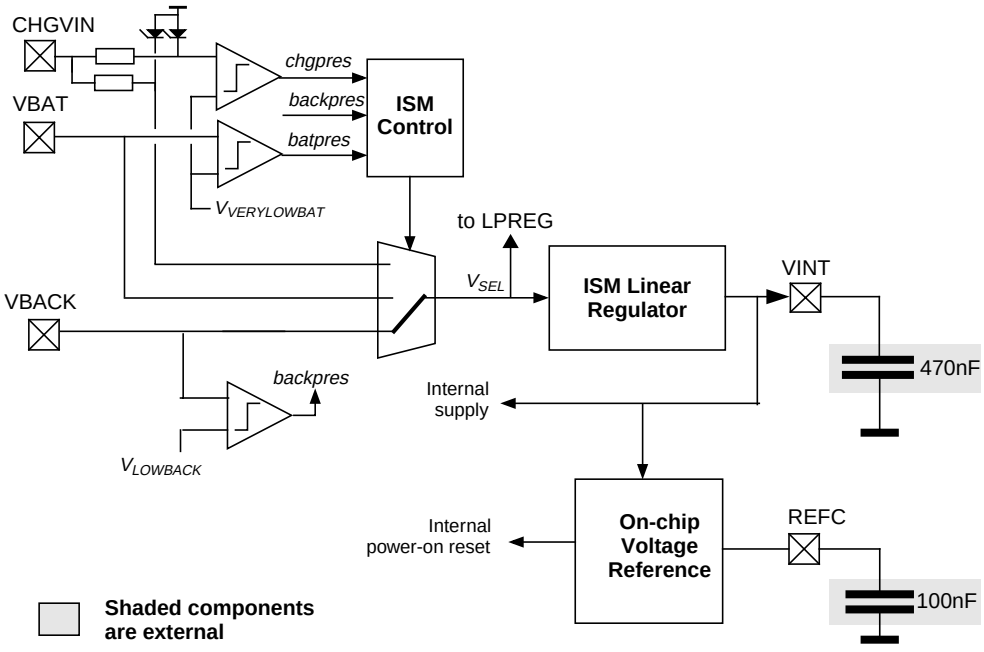


Fig 61. Internal supply and on-chip reference

8.16.1 Generating the internal supply voltage

The internal supply voltage is generated from either the main battery, the charger or the backup battery. If one of these sources is above their threshold level the internal circuitry of the PCF50606 will start up. The following table shows how the supply voltage is selected:

Table 48: Supply voltage selection for internal supply and LPREG

$V_{VBAT} > V_{VERYLOWBAT}$	$V_{VBACK} > V_{LOWBACK}$	$V_{CHGVIN} > V_{LOWCHG}$	Supply for ISM and LPREG
0	0	0	Main battery
0	x	1	Charger
0	1	0	Backup battery
1	x	x	Main battery

The internal supply needs a ceramic decoupling capacitor of at least 330nF to decouple the internal regulator.

The activity state of the PCF50606 (NOPOWER, SAVE, STANDBY or ACTIVE) highly depends on the voltage levels of the main battery, backup battery and charger. For more information about the activity states is referred to Section 8.1 “On/Off control (OOC)”.

When a backup battery is used, the PCF50606 is powered by the backup battery when the main battery is empty, until V_{VBACK} drops below the $V_{LOWBACK}$ threshold. To prevent deep discharge of the battery, the PCF50606 goes into the power saving SAVE mode at low battery conditions.

When no backup battery is used, the pin VBACK should be connected to VSS. In this case the PCF50606 goes to the NOPOWER state if VBAT drops below $V_{VERYLOWBAT}$, and no charger is connected.

The internal supply VINT can be used as a permanent supply for the system. The difference with the LPREG supply is that the VINT has a fixed output voltage, and cannot be switched off by software.

8.16.2 Generating the internal references and power-on reset

The On-Chip Reference circuit generates the 900 mV internal voltage reference from the internal bandgap reference circuit. An external filter capacitor, connected between the REFC pin and ground, is required to reduce the noise on this internal reference voltage. The reference voltage is calibrated during the start up sequence of the PCF50606 to achieve the necessary accuracy.

The internal power-on reset is asserted as long as the internal references are not stable.

8.17 Temperature High Sensor (THS)

The Temperature High Sensor monitors the junction temperature of the PCF50606. It offers the following features:

- Fixed temperature threshold.
- Hysteresis and debounce filter built in to prevent fast cycling.
- The THS is enabled in ACTIVE state. In all other states the THS is disabled.

The behavior of the THS is shown in Figure 62 “THS and HIGHTMP behavior”

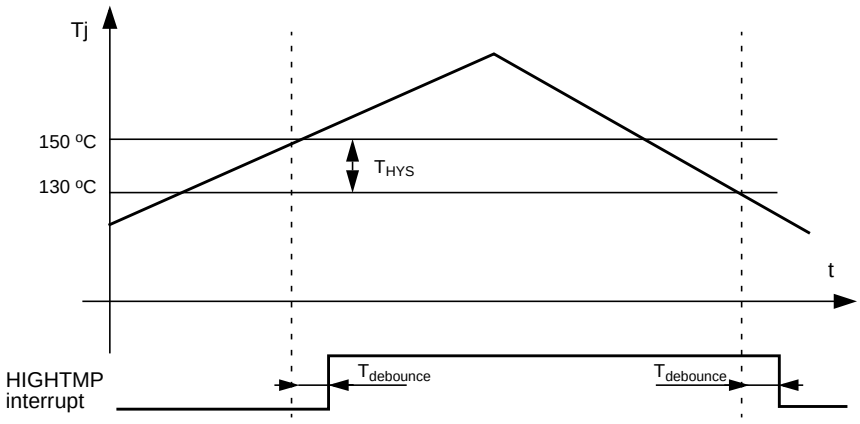


Fig 62. THS and HIGHTMP behavior

A HIGHTMP interrupt is generated when the temperature threshold is passed for more than 62 ms (debouncing time). When a HIGHTMP interrupt is generated the host-controller should initiate a transition to STANDBY state. In case the host controller does not initiate a transition to the STANDBY state within 1 second after the interrupt occurred, the on/off controller forces the PCF50606 to the STANDBY state in order to prevent damage to the circuit.

Note that transition to STANDBY on the HIGHTMP signal is interrupt driven. This means that if a transition to STANDBY has taken place on basis of the HIGHTMP interrupt, that at the next activation of the chip, the HIGHTMP interrupt must be cleared by reading the corresponding interrupt register. If this is omitted, the deactivation on HIGHTMP is not working.

The hysteresis and debounce time have been built in to prevent fast cycling of the HIGHTMP signal.

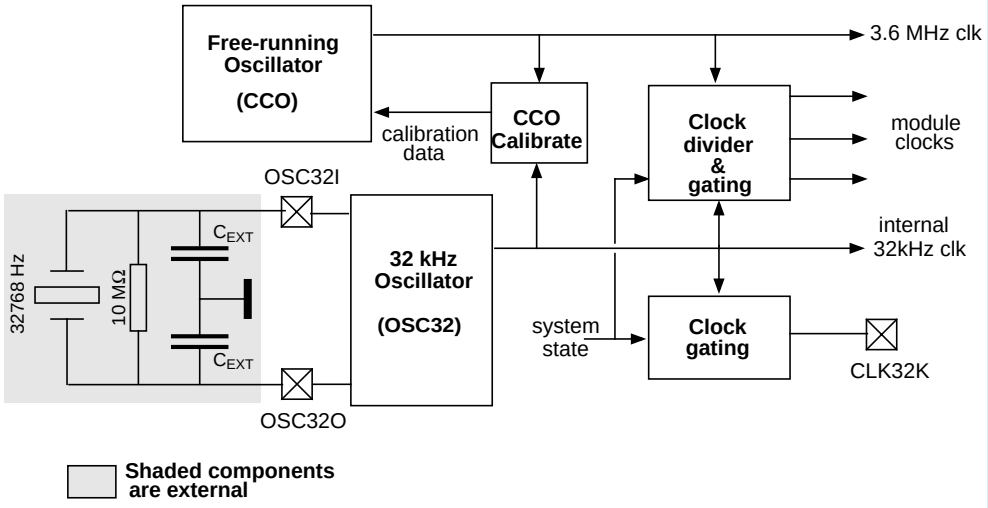
The THS can not be disabled via I2C. The status of the high temperature condition is available via the TEMPOK status bit in the OOCS register (see Table 7 “OOCS register”).

8.18 Clock generator unit (CGU)

The clock generator unit generates all internal and external clocks for the PCF50606. The CGU offers the following features:

- A free-running oscillator generating the internal high clock frequency (clkcco). The typical frequency of the high clock frequency is 3.6 MHz.
- An 32.768 kHz crystal oscillator which provides an accurate low clock frequency for the PCF50606 and external circuitry. The 32 kHz clock is optional.

A block diagram of the CGU is shown in Figure 63. Note that the 2 capacitors and the high ohmic resistor MUST be added to achieve a functional 32 kHz oscillator.



(1) A DC path with 10 MΩ (min. value: 3 MΩ) resistance shall be provided externally (parallel to the quartz crystal).

(2) An additional capacitance to the quartz crystal increases the start up time.

Fig 63. Clock generator unit

8.18.1 Free-running oscillator

The high clock frequency is generated by a current-controlled free-running oscillator (CCO).

The following modules within the PCF50606 require the high clock frequency:

- DCD, DCDE and DCUD DC/DC converters
- I2C interface
- ADC and touchscreen interface

Clock division and clock gating is implemented to optimize the power consumption of the PCF50606. The CCO is disabled when all modules requiring the high clock frequency are disabled. This will reduce the power consumption.

The free-running oscillator is calibrated using the 32.768 kHz clock if available.

8.18.2 32 kHz oscillator

The 32.768 kHz crystal oscillator provides an accurate low clock frequency for the PCF50606 and external circuitry.

The 32 kHz oscillator module can be used without crystal by connecting a 32.768 kHz signal to the OSC32I pin. The OSC32O pin should be left unconnected in this configuration.

The 32 kHz clock is used for the following functions:

- Provide an accurate low frequency clock for the PCF50606.
- Provide the external 32 kHz clock via the CLK32K pin. The CLK32K pad is supplied by the IOREG power supply and becomes active as soon as the PCF50606 has entered the ACTIVE state (see Section 8.1 “On/Off control (OOC)”). The 32 kHz clock is also accessible via the GPO(OD) pins.
- Calibration of the free-running oscillator. This improves the accuracy of the high clock frequency.

The PCF50606 can also be used without 32kHz crystal or external 32 kHz clock input.In this case the 32 kHz clock will be generated internally by dividing the high frequency clock generated by the internal current controlled oscillator (CCO). Note that this will lead to a less accurate 32 kHz clock and an increased power consumption, specially in SAVE and STANDBY states as the internal current controlled oscillator is enabled at all times. Both the OSC32I and OSC32O pins must be grounded when using the PCF50606 without 32kHz crystal or clock.

8.19 Real-time clock (RTC)

The real time clock module provides the time information to the application based on a 1 Hz clock frequency. It contains a calendar function which automatically corrects the date for the different lengths of the months and includes leap year detection.

1. The RTC module is supplied from the internal supply (VINT) and is active whenever the main or backup battery supplies the PCF50606.
2. The RTC unit contains one alarm function that generates an interrupt if the actual (RTC) time equals the content of the alarm register. The alarm registers are preset to all “1” which disables the alarm. It is recommended to mask the ALARM interrupt before a new value is written to the alarm registers, in order to prevent interrupts during the write actions (a new setting may require up to 7 register writes).
3. The RTC timer registers are reset to zero at the first start-up of the PCF50606 when for the first time a backup battery ($V_{VBACK} > V_{LOWBACK}$) or main battery ($V_{VBAT} > V_{VERYLOWBAT}$) is connected. They can be programmed to any start value by programming the RTC time/date registers. It is recommended to mask the RTC interrupts (second/minute) before a new value is written to the time registers to prevent interrupts during the write actions (a new setting may require up to 7 register writes).
4. Only one write access to the RTC time register per second is possible. Write accesses to the alarm register, as well as read accesses to all registers are possible without any restrictions.
5. Values written to the RTC register become effective at the next 1 Hz clock. It can therefore take up to 1 second for new values to become active.
6. To obtain an accurate RTC, a 32 kHz crystal oscillator or an external 32 kHz signal needs to be connected to the PCF50606. When an accurate 32 kHz signal is not available, the clock for the RTC is derived from the integrated free-running oscillator. See Table 92 “Characteristics Free-running Oscillator”.

8.19.1 RTC time registers

All RTC time registers are reset at the initial start-up of the PCF50606, when either a main battery, a backup battery, or a charger is connected to the IC (register type ‘S’).

Table 49: RTCSC register

Bit	Mode	Symbol	Reset [1]	Description
6-0	R/W [2]	SEC	0000000	Current seconds value coded in BCD format; value = 00 to 59. Example: <seconds> = 0001 1001, represents the value 19 s.
7		reserved	[3]	

[1] This register is reset at the initial start up of the PCF50606 (register type ‘S’).

[2] The software shall take into account that after an update of this register counting proceeds and that the complete update (up to 7 registers) must be completed before he seconds counter reaches the 59 seconds. The maximum time for the update is available if the software waits for the one second interrupt and then does the update.

[3] Reserved bits should be written ‘0’, the return values are not defined.

Table 50: RTCMN register

Bit	Mode	Symbol	Reset [1]	Description
6-0	R/W	MIN	0000000	Current minutes value coded in BCD format; value = 00 to 59.
7		reserved	[2]	

[1] This register is reset at the initial start up of the PCF50606 (register type 'S').

[2] Reserved bits should be written '0', the return values are not defined.

Table 51: RTCHR register

Bit	Mode	Symbol	Reset [1]	Description
5-0	R/W	HOUR	000000	Current hours value coded in BCD format; value = 00 to 23.
7-6		reserved	[2]	

[1] This register is reset at the initial start up of the PCF50606 (register type 'S').

[2] Reserved bits should be written '0', the return values are not defined.

8.19.2 RTC date registers

The PCF50606 compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4.

Table 52: RTCWD register

Bit	Mode	Symbol	Reset [1]	Description
2-0	R/W	WKDAY	000	Current weekday value 0 to 6; see Table 53.
7-3	-	reserved	- [2]	

[1] This register is reset at the initial start up of the PCF50606 (register type 'S').

[2] Reserved bits should be written '0', the return values are not defined.

Table 53: Weekday assignments

Day	Bit 2	Bit 1	Bit 0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

Table 54: RTCDT register

Bit	Mode	Symbol	Reset [1]	Description
5-0	R/W	DAY	000001	Current day value coded in BCD format; value = 01 to 31.
7-6		reserved	[2]	

[1] This register is reset at the initial start up of the PCF50606 (register type 'S').

[2] Reserved bits should be written '0', the return values are not defined.

Table 55: RTCMT register

Bit	Mode	Symbol	Reset [1]	Description
4-0	R/W	MONTH	000001	Current month value coded in BCD format; value = 01 to 12; see Table 57.
7-5		reserved	[2]	

[1] This register is reset at the initial start up of the PCF50606 (register type 'S').

[2] Reserved bits should be written '0', the return values are not defined.

Table 56: RTCYR register

Bit	Mode	Symbol	Reset [1]	Description
7-0	R/W	YEAR	00000000	Current year value coded in BCD format; value = 00 to 99.

[1] This register is reset at the initial start up of the PCF50606 (register type 'S').

[2] Reserved bits should be written '0', the return values are not defined.

Table 57: Month assignments

Month	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

8.19.3 RTC alarm registers

When one or more of the alarm registers are loaded with a valid time and/or date, then that information will be compared with the current time and date. When all enabled comparisons match, an interrupt is generated.

When an RTC alarm occurs, the interrupt is captured in the INT module and a state transition from STANDBY to ACTIVE is initiated, as soon as the start-up conditions are met (see Section 8.1.2 “Transitions between activity states”).

Each alarm register can individually be enabled by programming a value different from the reset value.

All RTC alarm registers are reset at the initial start-up of the PCF50606, when either a main battery, a backup battery, or a charger is connected to the IC (register type ‘S’).

Table 58: RTCSCA register

Bit	Mode	Symbol	Reset [1]	Description
6-0	R/W	SECA	1111111	Second alarm information coded in BCD format; value = 00 to 59.
7		reserved	[2]	

[1] This register is reset at the initial start up of the PCF50606 (register type ‘S’).

[2] Reserved bits should be written ‘0’, the return values are not defined.

Table 59: RTCMNA register

Bit	Mode	Symbol	Reset [1]	Description
6-0	R/W	MINA	111111	Minute alarm information coded in BCD format; value = 00 to 59.
7		reserved	[2]	

[1] This register is reset at the initial start up of the PCF50606 (register type ‘S’).

[2] Reserved bits should be written ‘0’, the return values are not defined.

Table 60: RTCHRA register

Bit	Mode	Symbol	Reset [1]	Description
5-0	R/W	HOURA	111111	Hour alarm information coded in BCD format; value = 00 to 23.
7-6		reserved	[2]	

[1] This register is reset at the initial start up of the PCF50606 (register type ‘S’).

[2] Reserved bits should be written ‘0’, the return values are not defined.

Table 61: RTCWDA register

Bit	Mode	Symbol	Reset [1]	Description
2-0	R/W	WKDAYA	111	Weekday alarm information value 0 to 6; see Table 53.
7-3		reserved	[2]	

[1] This register is reset at the initial start up of the PCF50606 (register type ‘S’).

[2] Reserved bits should be written ‘0’, the return values are not defined.

Table 62: RTCDTA register

Bit	Mode	Symbol	Reset [1]	Description
5-0	R/W	DAYA	111111	Day alarm information coded in BCD format; value = 01 to 31.
7-6		reserved	[2]	

[1] This register is reset at the initial start up of the PCF50606 (register type 'S').

[2] Reserved bits should be written '0', the return values are not defined.

Table 63: RTCMTA register

Bit	Mode	Symbol	Reset [1]	Description
4-0	R/W	MONTHA	11111	Month alarm information coded in BCD format; value = 01 to 12; see Table 57.
7-5		reserved	[2]	

[1] This register is reset at the initial start up of the PCF50606 (register type 'S').

[2] Reserved bits should be written '0', the return values are not defined.

Table 64: RTCYRA register

Bit	Mode	Symbol	Reset [1]	Description
7-0	R/W	YEARA	11111111	Year alarm information coded in BCD format; value 00 to 99.

[1] This register is reset at the initial start up of the PCF50606 (register type 'S').

8.20 Pulse-Width Modulator (PWM)

The PCF50606 pulse-width modulator offer the following features:

- Programmable frequency and duty cycle.
- The PWM can be enabled in ACTIVE state. In all other states the PWM is disabled.

The PWM modulator is enabled in ACTIVE state by writing a ‘1’ to the ACTSET control bit in the PWMC1 register. In STANDBY state the ACTSET control bit is automatically cleared.

Figure 64 shows the PWM block diagram.

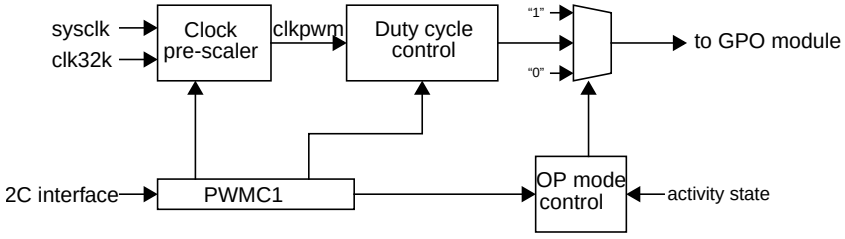


Fig 64. Block diagram of the PWM modulator

The clock for the PWM module (clkpwm) is generated by the pre-scaler. The pre-scaled clock is derived from the system clock. The prescale factor is defined by the PRESCALE control bits in the PWMC1 register.

The duty cycle is programmed though the PWMDC bits in the register PWMC1. During the high period the output of the PWM modulator is high. This corresponds to an high level on the push-pull GPO outputs and with a floating output for the open drain GPO outputs.

The programmed pattern is repeated until either the PWM module is de-activated though the I2C interface or until the module is disabled by writing a ‘0’ to the ACTSET control bit, or by a transition to STANDBY state.

Disabling the PWMx by resetting the ACTSET bits in the PWMxC register or by a transition to STANDBY state has an immediate effect. The module is stopped and set into the OFF mode.

8.20.1 Control registers

Table 65: PWMC1 register

BIT	Mode	Symbol	Reset [1]	Description
0	R/W	ACTSET	0	Defines mode during ACTIVE state: 0: OFF 1: ON This bit is automatically cleared in STANDBY state
4-1	R/W	PWMDC	0	Defines duty cycle of PWM 0000: 0/16 0001: 1/16 0010: 2/16 0011: 3/16 0100: 4/16 0101: 5/16 0110: 6/16 0111: 7/16 1000: 8/16 1001: 9/16 1010: 10/16 1011: 11/16 1100: 12/16 1101: 13/16 1110: 14/16 1111: 15/16
7-5	R/W	PRESCALE	100	Defines PWM clock frequency: 000: 32.768kHz / 64 = 512Hz 001: 32.768kHz / 128 = 256Hz 010: 32.768kHz / 256 = 128Hz 011: 32.768kHz / 512 = 64Hz 100: 3.6MHz / 64 = 56.3kHz 101: 3.6MHz / 128 = 28.1kHz 110: 3.6MHz / 256 = 14.1kHz 111: 3.6MHz / 512 = 7.0kHz

[1] This register is reset at the initial start up of the PCF50606. At each transition to the STANDBY state, the ACTSET bit is cleared (register type 'S/O').

8.21 LED Modulators (LED)

The PCF50606 contains two LED modulators, which can be selected as input for any of the GPO(OD) outputs. The LED modulators of the PCF50606 are used for the control of the indicator LED's. They offer the following features:

- Each LED modulator can select 8 different repetition periods.
- Capable of generating 8 different blinking patterns. The selected pattern is generated once per repetition period.
- Each LED modulator can be used as a status indicator via GPO(OD) outputs during the ACTIVE state, while special patterns can be configured for indication of a charger connected during the SAVE and STANDBY states.

The block diagram of one LED driver is shown in Figure 65.

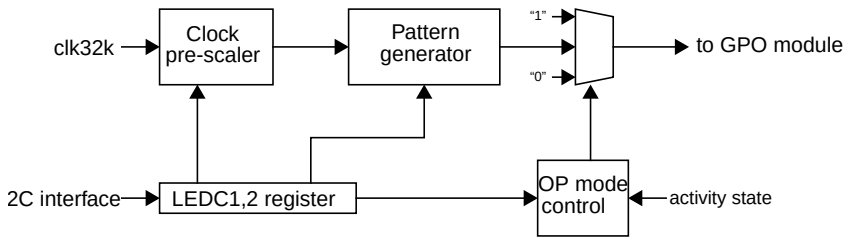


Fig 65. Block diagram of one LED modulator

8.21.1 Selecting the pattern

The LED drivers are capable of generating blinking patterns for indicator LED's. the generated pattern is selected by the PERIOD and PATTERN control bits in the LEDCx control register.

The repetition period for the pattern is selected by the PERIOD bits according to the Table 66.

Table 66: LED repetition periods

PERIOD bits 2-0	repetition period	PERIOD bits 2-0	repetition period
000	0.4 s	100	2.6 s
001	1.0 s	101	4.0 s
010	1.2 s	110	6.0 s
011	2.0 s	111	8.0 s

The blinking pattern is selected by the PATTERN bits according to Table 67. In this table, ON means that the output is pulled-to-ground (LED is burning), OFF means that the output is in tri-state (LED is not burning).

Table 67: LED patterns

PATTERN bits 5-3	Pattern
000	ON = 50 ms, OFF for rest of repetition period
001	ON = 100 ms, OFF for rest of repetition period
010	ON = 200 ms, OFF for rest of repetition period
011	ON= 500 ms, OFF for rest of repetition period
100	ON = 50 ms, OFF = 50 ms, ON = 50 ms, OFF for rest of repetition period
101	ON = 100 ms, OFF = 100 ms, ON = 100 ms, OFF for rest of repetition period
110	ON = 200 ms, OFF = 200 ms, ON = 200 ms, OFF for rest of repetition period
111	LED is continuously ON

The "111" setting of the PATTERN bits is a special case. For this setting the LED is continuously ON.

8.21.2 Operation modes

The operation mode of the LED drivers for the different activity states of the OOC is controlled by the CHGSET, and ACTSET control bits in the LEDCx control register.

The CHGSET control bit defines the operation mode for the LED driver when a charger is connected. Setting this bit allows the generation of a blinking LED when a charger is connected, even when the PCF50606 is in SAVE or STANDBY state.

The ACTSET control bit defines the operation mode for the LED driver when the PCF50606 is in ACTIVE state. The ACTSET control bit is automatically cleared in the STANDBY state.

8.21.3 Control and status registers

Table 68: LEDC1 register

BIT	Mode	Symbol	Reset[1]	Description
2-0	R/W	PERIOD	101	Repetition period: see Table 66
5-3	R/W	PATTERN	001	Blinking pattern: see Table 67
6	R/W	CHGSET	1	Operation mode when charger connected: 0: LED driver is disabled 1: LED driver is enabled
7	R/W	ACTSET	0	Operation mode in ACTIVE state: 0: LED driver is disabled 1: LED driver is enabled This bit is automatically cleared in STANDBY state

[1] This register is reset at the initial start up of the PCF50606. At each transition to the STANDBY state, the ACTSET bit is cleared (register type ‘S/O’).

Table 69: LEDC2 register

BIT	Mode	Symbol	Reset[1]	Description
2-0	R/W	PERIOD	101	Repetition period: see Table 66
5-3	R/W	PATTERN	001	Blinking pattern: see Table 67
6	R/W	CHGSET	1	Operation mode when charger connected: 0: LED driver is disabled 1: LED driver is enabled
7	R/W	ACTSET	0	Operation mode in ACTIVE state: 0: LED driver is disabled 1: LED driver is enabled This bit is automatically cleared in STANDBY state

[1] This register is reset at the initial start up of the PCF50606. At each transition to the STANDBY state, the ACTSET bit is cleared (register type ‘S/O’).

8.22 General purpose outputs (GPO)

The PCF50606 contains six general purpose outputs, divided in 2 CMOS push pull outputs supplied from the IOVDD supply and 4 high current (100mA) open drain outputs They offer the following features:

- Each GPO can be configured as constant low, constant high, as LED modulator output, PWM output, BATOK output, CLK32 output or CHGDET output separately for the ACTIVE state of the PCF50606 for the GPO's and ACTIVE state, STANDBY state and SAVE state for GPOOD's. The BATOK is a signal coming from the BVM, indicating if the battery voltage is above a pre-programmed value. The CHGDET signal is coming from the MBC, indicating if the charger is present. The way the charger presence is detected is determined by the DETMOD bit in register MBCC1 (see table 35).
- The GPOODx outputs allow to sink 100mA from any supply or battery voltage.

The block diagram of a GPO driver is shown in Figure 66.

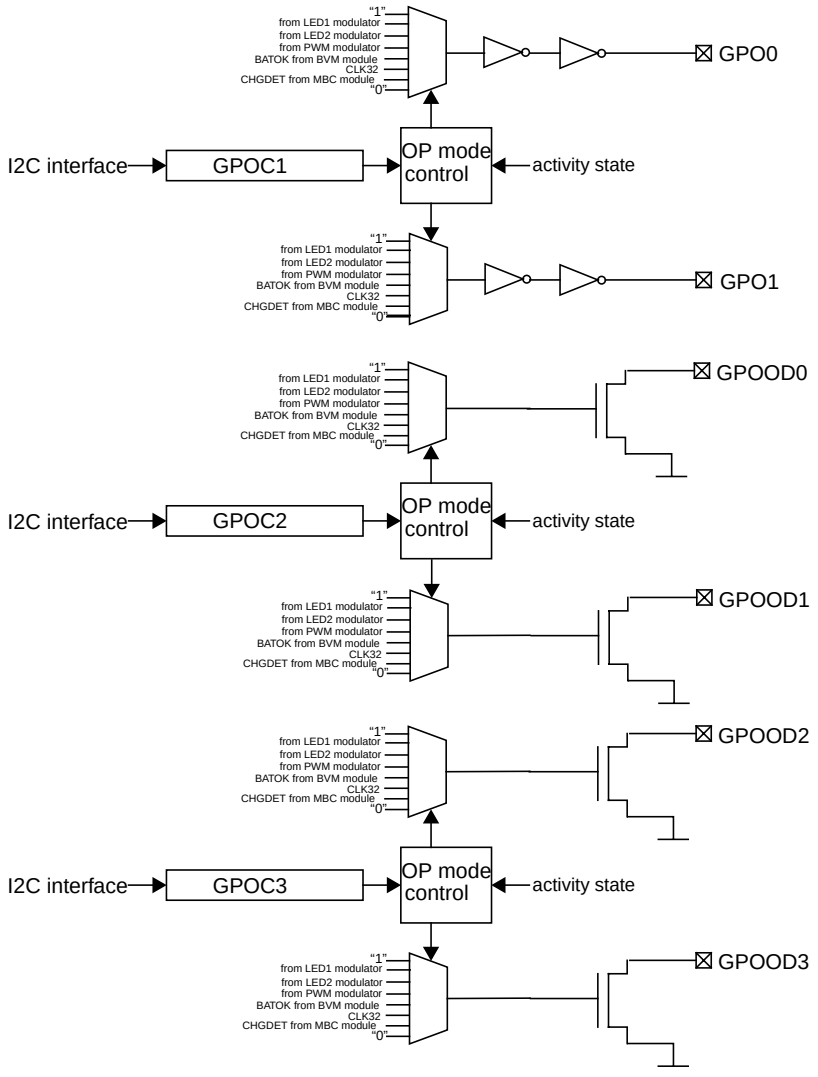


Fig 66. Block diagram of the GPO module

8.22.1 Control and status registers

Table 70: GPOC1 register

BIT	Mode	Symbol	Reset[1]	Description
2-0	R/W	GPO0ACT	100	Functionality GPO0 in ACTIVE state 000: constant low 001: LED1 output 010: LED2 output 011: PWM output 100: BATOK output 101: CLK32 output 110: CHGDET output 111: constant high
3	R/W	GPO0INV	0	If set, inverts the GPO0 output
6-4	R/W	GPO1ACT	000	Functionality GPO1 in ACTIVE state 000: constant low 001: LED1 output 010: LED2 output 011: PWM output 100: BATOK output 101: CLK32 output 110: CHGDET output 111: constant high
7	R/W	GPO1INV	0	If set, inverts the GPO1 output

[1] This register is reset at the initial start up of the PCF50606 (register type 'S').

Table 71: GPOC2 register

BIT	Mode	Symbol	Reset[1]	Description
2-0	R/W	GPOOD0ACT	000	Functionality GPOOD0 in ACTIVE state 000: high Z 001: LED1 output 010: LED2 output 011: PWM output 100: BATOK output 101: CLK32 output 110: CHGDET output 111: constant pulled low
5-3	R/W	GPOOD0STB	000	Functionality GPOOD0 in STANDBY state 000: high Z 001: LED1 output 010: LED2 output 011: PWM output (high Z) 100: BATOK output 101: CLK32 output 110: CHGDET output 111: constant pulled low
6	R/W	GPOOD0INV	0	If set, inverts the GPOOD0 output
7	R/W	reserved	[2]	

[1] This register is reset at the initial start up of the PCF50606 (register type 'S').

[2] Reserved bits should be written ‘0’, the return values are not defined.

Table 72: GPOC3 register

BIT	Mode	Symbol	Reset [1]	Description
2-0	R/W	GPOOD1ACT	000	Functionality GPOOD1 in ACTIVE state 000: high Z 001: LED1 output 010: LED2 output 011: PWM output 100: BATOK output 101: CLK32 output 110: CHGDET output 111: constant pulled low
5-3	R/W	GPOOD1STB	000	Functionality GPOOD1 in STANDBY state 000: high Z 001: LED1 output 010: LED2 output 011: PWM output (high Z) 100: BATOK output 101: CLK32 output 110: CHGDET output 111: constant pulled low
6	R/W	GPOOD1INV	0	If set, inverts the GPOOD1 output
7	R/W	reserved	[2]	

[1] This register is reset at the initial start up of the PCF50606 (register type ‘S’).

[2] Reserved bits should be written ‘0’, the return values are not defined.

Table 73: GPOC4 register

BIT	Mode	Symbol	Reset[1]	Description
2-0	R/W	GPOOD2ACT	000	Functionality GPOOD2 in ACTIVE state 000: high Z 001: LED1 output 010: LED2 output 011: PWM output 100: BATOK output 101: CLK32 output 110: CHGDET output 111: constant pulled low
5-3	R/W	GPOOD2STB	000	Functionality GPOOD2 in STANDBY state 000: high Z 001: LED1 output 010: LED2 output 011: PWM output (high Z) 100: BATOK output 101: CLK32 output 110: CHGDET output 111: constant pulled low
6	R/W	GPOOD2INV	0	If set, inverts the GPOOD2 output
7	R/W	reserved	[2]	

[1] This register is reset at the initial start up of the PCF50606 (register type ‘S’).

[2] Reserved bits should be written ‘0’, the return values are not defined.

Table 74: GPOC5 register

BIT	Mode	Symbol	Reset[1]	Description
2-0	R/W	GPOOD3ACT	000	Functionality GPOOD3 in ACTIVE state 000: high Z 001: LED1 output 010: LED2 output 011: PWM output 100: BATOK output 101: CLK32 output 110: CHGDET output 111: constant pulled low

Table 74: GPOC5 register *…continued*

BIT	Mode	Symbol	Reset [1]	Description
5-3	R/W	GPOOD3STB	000	Functionality GPOOD3 in STANDBY state 000: high Z 001: LED1 output 010: LED2 output 011: PWM output (high Z) 100: BATOK output 101: CLK32 output 110: CHGDET output 111: constant pulled low
6	R/W	GPOOD3INV	0	If set, inverts the GPOOD3 output
7	R/W	reserved	[2]	

[1] This register is reset at the initial start up of the PCF50606 (register type 'S').

[2] Reserved bits should be written '0', the return values are not defined.

8.23 Register map

Table 75: Registers overview

Address	Reset type [2]	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	S	ID	VERSION [7-4]				VARIANT [3-0]			
01H		OOCS	WDTEXP	TEMPOK	CHGOK	BACKOK	BATOK	PWROKRST	EXTON	ONKEY
02H		INT1	ALARM	SECOND	-	EXTONF	EXTONR	ONKEY1S	ONKEYF	ONKEYR
03H		INT2	CHGWDEXP	CHGWD10S	CHGPROT	CHGFRDY	CHGERR	CHGFOK	CHGRM	CHGINS
04H		INT3	HIGHTMP	LOWBAT	-	-	TSCPRES	ACDREM	ACDINS	ADCRDY
05H	S	INT1M	ALARMM	SECONDM	-	EXTONFM	EXTONRM	ONKEY1SM	ONKEYFM	ONKEYRM
06H	S	INT2M	CHGWDEXPM	CHGWD10SM	CHGPROTM	CHGFRDYM	CHGERRM	CHGFOKM	CHGRMM	CHGINSM
07H	S	INT3M	HIGHTMPM	LOWBATM	-	-	TSCPRESM	ACDREMM	ACDINSM	ADCRDYM
08H	S	OOCC1	EXTONWAK		CHGWAK	RTCWAK	WDTRST	CLK32ON	TOTRST	GOSTDBY
09H	S	OOCC2	-	-	-	-	EXTONDB		ONKEYDB	
0AH	S	RTCSC	-	SEC						
0BH	S	RTCMN	-	MIN						
0CH	S	RTCHR	-	-	HOUR					
0DH	S	RTCWD	-	-	-	-	-	WKDAY		
0EH	S	RTCDT	-	-	DAY					
0FH	S	RTCMT	-	-	-	MONTH				
10H	S	RTCYR	YEAR							
11H	S	RTCSCA	-	SECA						
12H	S	RTCMNA	-	MINA						
13H	S	RTCHRA	-	-	HOURSA					
14H	S	RTCWDA	-	-	-	-	-	WKDAYA		
15H	S	RTCDTA	-	-	DAYA					
16H	S	RTCMTA	-	-	-	MONTHA				
17H	S	RTCYRA	YEARA							
18H	S	PSSC	LPPH2	D3PH2	D2PH2	D1PH2	IOPH2	DCUDPH2	DCDEPH2	DCDPH2
19H	S	PWROKM	LPPOKM	D3POKM	D2POKM	D1POKM	IOPOKM	DCUDPOKM	DCDEPOKM	DCDPOKM
1AH		PWROKS	LPOK	D3POK	D2POK	D1POK	IOPOK	DCUDPOK	DCDEPOK	DCDPOK

Table 75: Registers overview…*continued*

Address	Reset type [2]	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1BH	O	DCDC1	OPMOD1			VOUT1				
1CH	O	DCDC2	OPMOD2			VOUT2				
1DH	S	DCDC3	DVMTIM					DVMMOD		
1EH	S	DCDC4	REGSEL	TOGGLEMODE	CURLIM		OFFMOD		PFMMOD / PWMMOD	
1FH	O	DCDEC1	OPMOD			-	VOUT			
20H	S	DCDEC2	-	-	-	-	-	OFFMOD	PFMMOD / PWMMOD	
21H	O	DCUDC1	OPMODE			VOUT				
22H	S	DCUDC2	-	-	CURLIM		-	OFFMOD	PFMMOD / PWMMOD	
23H	O	IOREGC	OPMOD			VOUT				
24H	O	D1REGC1	OPMOD			VOUT				
25H	O	D2REGC1	OPMOD			VOUT				
26H	O	D3REGC1	OPMOD			VOUT				
27H	S/O	LPREGC1	OPMOD			VOUT				
28H	S	LPREGC2	-	-	-	-	-	-	RSTACT	STDBACT
29H	S/C	MBCC1	-	WDRST	DETMOD	CHGMOD			AUTOFST	CHGAPE
2AH	S	MBCC2	-	-	-	WDTIME				
2BH	S	MBCC3	-	WDEXP	CURRAT		VCHGCON			
2CH		MBCS1	CHGCURSTAT		CHGVINSTAT		TBATSTAT		VBATSTAT	
2DH	S	BBCC	-	-	BBCRES	BBCVLIM	BBCCUR		BBCAPESTB	BBCAPEACT
2EH	O	ADCC1	TSCINT	-	EXTSYNCBREAK	NTCSWAOFF	NTCSWAPE	RATSET	TSCMODSTB	TSCMODACT
2FH	O	ADCC2	ADCRES	ADCSYNC		ADCMUX				ADCSTART
30H		ADCS1	ADCDA1TH							
31H		ADCS2	ADCRDY	-	-	-	ADCDAT2L		ADCDAT1L	
32H		ADCS3	ADCDAT2H							
33H	S	ACDC1	ACDAPE	-	-	DISB	THRSHLD			ACDDET
34H	S	BVMC	-	-	-	DISB	THRSHLD			BATOK
35H	S/O	PWMC1	PRESCALE			PWMDC				ACTSET
36H	S	LEDC1	ACTSET	CHGSET	PATTERN			PERIOD		
37H	S	LEDC2	ACTSET	CHGSET	PATTERN			PERIOD		
38H	S	GPOC1	GPO1INV	GPO1ACT			GPO0INV	GPO0ACT		
39H	S	GPOC2	-	GPOOD0INV	GPOOD0STB			GPOOD0ACT		
3AH	S	GPOC3	-	GPOOD1INV	GPOOD1STB			GPOOD1ACT		
3BH	S	GPOC4	-	GPOOD2INV	GPOOD2STB			GPOOD2ACT		
3CH	S	GPOC5	-	GPOOD3INV	GPOOD3STB				GPOOD3ACT	

[1] Bit positions labelled as “-” are reserved. They should be written as ‘0’ and the return value is not defined.

[2] In the reset type column is indicated when the applicable register is reset:

‘S’: only at initial start-up of the PCF50606.

‘O’: each time when the PCF50606 goes to the STANDBY state

‘S/O’: the register is reset at the initial start-up, while the dedicated bits are also reset each time when the PCF50606 goes to the STANDBY state

‘S/C’: the register is reset at the initial start-up of the PCF50606 and each time a charger is connected.

8.24 PCF50606 variants

The reset value of several control bits are mask programmable allowing to optimize the PCF50606 to different applications. These settings define the behavior of the PCF50606 before any control command is given through the serial interface.

Based on this mask programmability feature, different variants of the PCF50606 are available. Table 76 “Reset Settings” lists the reset values of registers that can be programmed.

Contact Philips Semiconductors for a list of available reset values available for the PCF50605HN and PCF50606HN.

Table 76: Reset Settings

Module	Reg Name	Symbol	Options	Reference
ID	ID	VARIANT VERSION	00 to 1F fixed value ‘100’	Table 6 “ID Register”
OOC	OOCC1	CLK32ON	0,1	Table 8 “OOCC1 Register”
IOREG	IOREGC1	OPMOD VOUT	ON / ECO / OFF 1.8V to 3.3 V	Table 29 “IOREGC Register”
D1REG	D1REGC1	OPMOD VOUT	ON / ECO / OFF 0.9V to 3.3 V	Table 30 “D1REGC1 Register”
D2REG	D2REGC1	OPMOD VOUT	ON / ECO / OFF 0.9V to 3.3 V	Table 31 “D2REGC1 Register”
D3REG	D3REGC1	OPMOD VOUT	ON / ECO / OFF 0.9V to 3.3 V	Table 32 “D3REGC1 Register”
LPREG	LPREGC1	OPMOD VOUT	ON / ECO / OFF 0.9V to 3.3 V	Table 33 “LPREGC1 Register”
	LPREGC2	RSTACT STBACT	YES / NO ECO / OFF	Table 34 “LPREGC2 Register”
DCD	DCDC1	OPMOD1 VOUT1	ON / ECO / OFF 0.9V to 3.6 V	Table 21 “DCDC1 Register”
	DCDC2	OPMOD2 VOUT2	ON / ECO / OFF 0.9V to 3.6 V	Table 22 “DCDC2 Register”
DCDE	DCDEC1	OPMOD VOUT	ON / ECO / OFF 0.9V to 3.3 V	Table 25 “DCDEC1 Register”
DCUD	DCUDC1	OPMOD VOUT	ON / ECO / OFF 0.9V to 3.3 V or 4.0V to 5.5V	Table 27 “DCUDC1 Register”
PSS	PSSC	LPPH2 D3PH2 D2PH2 D1PH2 IOPH2 DCUDPH2 DCDEPH2 DCDPH2	PHASE1 / PHASE2 PHASE1 / PHASE2 PHASE1 / PHASE2 PHASE1 / PHASE2 PHASE1 / PHASE2 PHASE1 / PHASE2 PHASE1 / PHASE2 PHASE1 / PHASE2	Table 17 “PSSC Register”
BBC	BBCC	BBCRES BBCVLIM BBCCUR BBCAPESTB BBCAPEAPE	ACTIVE / BYPASSED 3.0V / 2.5V 400µA/200µA/100µA/50µA ON / OFF ON / OFF	Table 39 “BBCC Register”
BVM	BVMC	THRSHLD	3.4V/3.3V/3.2V/3.1V/3.0V/ 2.9V/2.8V	Table 47 “BVMC Register”
MBC	MBCC1	DETMOD AUTOFST	CHARGE DETECT MODE ON / OFF	Table 35 “MBCC1 Register”

9. Limiting values

Table 77: Limiting values

Symbol	Parameter	Conditions		Min	Max	Unit
V_{VBAT}	main battery voltage			–0.5	+6.5	V
V_{VBACK}	backup battery voltage			–0.5	+6.5	V
V_{CHGVIN}	Charger voltage on pin CHGVIN			–0.5	+20	V
V_I	input voltage on any pin with respect to REFGND			–0.5	+6.5	V
P_{tot}	total power dissipation			–	2000	mW
T_{amb}	operating ambient temperature			–40	+85	°C
T_{stg}	storage temperature			–55	+150	°C
V_{esd}	electrostatic discharge voltage					
	pins CHGVIN, VBAT, VBACK, IOVIN, D1VIN, D2VIN, D3VIN, LPVIN, DCDVIN, DCUDVIN, BATVOLT	HBM	[1]	-	±4000	V
		MM	[2]		±200	V
	pin DCDEVIN	HBM	[1]	-	±3200	V
		MM	[2]		±200	V
	pin DCDEPD	HBM	[1]	-	±1200	V
		MM	[2]		±200	V
	all other pins	HBM	[1]	-	±2000	V
		MM	[2]		±200	V

[1] Human Body Model: equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor. The JEDEC class2 limit is ±2000V.

[2] Machine model: equivalent to discharging a 200 pF capacitor via a 0 Ω resistor. The JEDEC class2 limit is ±200V.

10. Thermal characteristics

Table 78: Thermal characteristics

Symbol	Parameter	Package	Typ	Unit
$R_{th\ j\text{-}a}$	Thermal resistance from junction to ambient in free air	HVQFN56	22	K/W

11. Characteristics

11.1 Characteristics OOC

Table 79: Characteristics OOC module

*V_{SS} = REFGND = *GND = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL,ONKEY}$	LOW-level input voltage on $\overline{ONKEY}$ pin		-0.2	-	$0.3V_{INT}$	V
$V_{IH,ONKEY}$	HIGH-level input voltage on $\overline{ONKEY}$ pin		$0.7V_{INT}$	-	V_{INT} + 0.2	V
$R_{PU,ONKEY}$	Pull-Up resistor to VINT on $\overline{ONKEY}$ input		120	185	250	kΩ

Table 79: Characteristics OOC module *…continued…continued*

*V_{SS} = REFGND = *GND = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{LEAKL,ONKEY}$	Input leakage current on $\overline{ONKEY}$ pins when input is low	Low input voltage	-20	-15	-10	µA
$I_{LEAKH,ONKEYN}$	Input leakage current on $\overline{ONKEY}$ pins when input is high	High input voltage	-1	-	1	µA
$V_{IL,EXTON}$	LOW-level input voltage on EXTON pin		-0.2	-	$0.3V_{INT}$	V
$V_{IH,EXTON}$	HIGH-level input voltage on EXTON pin		$0.7V_{INT}$	-	6.0	V
$I_{LEAK,EXTON}$	Input leakage current on EXTON pin		-1	-	+1	µA
$V_{IL,INX}$	LOW-level input voltage on KEEPACT, PWREN1, PWREN2, TXON pins		-0.2	-	$0.3V_{IOVDD}$	V
$V_{IH,INX}$	HIGH-level input voltage on KEEPACT, PWREN1, PWREN2, TXON pins		$0.7V_{IOVDD}$	-	V_{IOVDD} + 0.2	V
$I_{LEAK,INX}$	Input leakage current on KEEPACT, PWREN1, PWREN2, TXON pins		-1	-	+1	µA
$V_{OL,OUTA}$	LOW-level output voltage on $\overline{RST}$, CLK32, PWROK,GPO pins		-0.2	-	$0.1V_{IOVDD}$	V
$V_{OH,OUTA}$	HIGH-level output voltage on CLK32, PWROK,GPO pins		$0.9V_{IOVDD}$	-	V_{IOVDD} + 0.2	V
$I_{OL,OUTA}$	LOW-level output current on $\overline{RST}$, CLK32, PWROK, GPOx pins	V_{IOVDD} > 2.5V V_{IOVDD}> 1.8V	-	2 1	-	mA mA
$I_{OH,OUTA}$	HIGH-level output current on CLK32, PWROK, GPOx pins	V_{IOVDD} > 2.5V V_{IOVDD} > 1.8 V	-	2 1	-	mA
R_{RST}	Pull-Up resistor to IOVDD on $\overline{RST}$ output		120	160	200	kΩ
$T_{D,RSTR}$	duration of reset during state transition from STANDBY to ACTIVE	All supplies activated in phase 1 of Power Supply Sequencer	49	50	51	ms
		At least 1 supply activated in phase 2 of Power Supply Sequencer	99	100	101	ms
$T_{D,RSTF}$	Delay between reset assertion and switching off of power supplies after activity state transition from ACTIVE to STANDBY		1.0		1.5	ms

11.2 Characteristics I2C

Table 80: Characteristics I^2C bus

*V_{SS} = REFGND = *GND = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	LOW-level input voltage for SDA, SCL pins		-0.2	-	$0.3V_{IOVDD}$	V
V_{IH}	HIGH-level input voltage for SDA, SCL pins		$0.7V_{IOVDD}$	-	5.7	V
V_{OL}	LOW-level output voltage for SDA pin		-	-	0.4	V
V_{OH}	HIGH-level output voltage for SDA pin		V_{IOVDD} - 0.4	-	-	V
I_{OL}	LOW-level output current on SDA output	V_{IOVDD} > 1.8 V	-	-	1.5	mA
I_{OH}	HIGH-level output current on SDA output	V_{IOVDD} > 1.8 V	-1.5	-	-	mA
I_{LEAK}	Input leakage current on SDA, SCL pins		-1	-	1	µA
P_{INCAP}	Input capacitance of SDA, SCL pins		-	-	15	pF

11.3 Characteristics INT

Table 81: Characteristics interrupt

*V_{SS} = REFGND = *GND = 0 V; T_{amb} = -40 to +8to +85 °C; unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage for $\overline{IRQ}$ pin		-0.2	-	0.4	V
I_{OL}	LOW-level output current on $\overline{IRQ}$ pin	V_{IOVDD} > 1.8 V	1.5	-	-	mA

[1] The $\overline{IRQ}$ output is implemented as open drain output.

11.4 Characteristics Power supplies

Table 82: Characteristics of the DCD converter

*V_{SS} = REFGND = *GND = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_p	Programmable output voltage		0.9	-	3.30	V
V_S	Programming step size	V_p < 1.2V V_p > 1.2V		25 300		mV mV
V_i	Converter input voltage		2.7 V **and** > $V_p + V_\Delta$	-	5.7	V
V_Δ	Minimum voltage between V_p and V_i for V_o specification				100	mV
V_o	Output voltage	$\Delta I_o / \Delta t$ < 500mA / 10 µs for V_p < V_i $\Delta V_i / \Delta t$ < 0.5 V / 10 µs	-3.5%	V_p [3]	+3.5%	V

Table 82: Characteristics of the DCD converter *...continued*

*V_{SS} = REFGND = *GND = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
I_o	Continuous output current	ON mode, V_p = 1.8V, V_i=3.6V		-	500	mA
		BYP mode, V_i=3.6V		-	250	mA
		PFM-only mode, L_{ext}=10uH V_i=3.6 V, V_p=1.2V V_i=4.2 V , V_p=3.4V			 200 100	 mA mA
V_{PWROK}	Power OK threshold level			0.9 * V_p		V
η	Efficiency [4]	V_i =3.6V, V_p=1.8V I_o = 1mA I_o= 10mA I_o=100mA I_o=500mA	 75 85 85 75			 % % % %
F_{SW}	Switching frequency	PWM mode, 32kHz Xtal connected	488	514	540	kHz
ESR_{COUT}	Internal series resistance of output capacitor		0.07		0.20	Ω
I_{DD}	Total supply current [1][2]	ON or ECO mode; no load	-	75		µA
		OFF mode, ByPass mode	-	-	1	µA
		OFF mode, no ByPass mode	-	-	1	µA

[1] Values are specified at T_{amb} = 25 °C, V_{IN} = 3.6 V and are validated by a product characterization report based on measurements on sample basis.

[2] Sum of the current through the module VBAT pin and the current supplied via the internal supply.

[3] The accuracy of the output voltage is determined by the choice of the external components.

[4] External output capacitor 47uF: with ESR_{COUT} = 0.10Ω, external inductor 15uH with DCR_L = 0.1Ω.

Table 83: Characteristics of the DCDE converter

*V_{SS} = REFGND = *GND = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_p	Programmable output voltage		0.9	-	3.3	V
V_S	Programming step size			300		mV
V_i	Converter input voltage		2.7 V **and** > V_p + V_Δ	-	5.7	V
V_o	Output voltage	$\Delta I_o / \Delta t$ < t.b.f./ 10 µs for V_p < V_i $\Delta V_i / \Delta t$ < 0.5 V / 10 µs	-3.5%	V_p [4]	+3.5%	V
V_{PWROK}	Power OK threshold level			0.9 * V_p		V
F_{SW}	Switching frequency	PWM mode, 32kHz Xtal connected	488	514	540	kHz
I_o	Output current	ON mode, V_p = 1.8V, V_i=3.6V	[3]	-	-	mA
		BYP mode, V_i=3.6V	[3]	-	-	mA
ESR_{COUT}	Internal series resistance of output capacitor		0.07		0.20	Ω
t_{BBM}	Break before make time when swapping state of pins DCDEND and DCDEPD			20		ns

Table 83: Characteristics of the DCDE converter *...continued*

*V_{SS} = REFGND = *GND = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
I_{DRV}	Gate drive current at pins DCDEND and DCDEPD	V_i = 3.6 V	100			mA
η	Efficiency [5]	V_i =3.6V, V_p=3.3 V [3]				
		I_o = 1mA		92		%
		I_o= 10mA		95		%
		I_o=100mA		96		%
		I_o=500mA		94		%
I_{DD}	Total supply current [1] [2] 1nF equivalent load capacity on DCDEND and DCDEPD	ON or ECO mode; no load	-	75		µA
		OFF mode, ByPass mode	-	-	1	µA
		OFF mode, no ByPass mode	-	-	1	µA

[1] Values are specified at T_{amb} = 25 °C, V_{IN} = 3.6 V and are validated by a product characterization report based on measurements on sample basis.

[2] Sum of the current through the module VBAT pin and the current supplied via the internal supply.

[3] These specifications are determined by the external power fets properties

[4] The accuracy of the output voltage is determined by the choice of the external components.

[5] External output capacitor 47uF: with ESR_{COUT} = 0.10Ω, external inductor 15uH with DCR_L = 0.1Ω.

Table 84: Characteristics of the DCUD converter

*V_{SS} = REFGND = *GND = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_p	Programmable output voltage		0.9	-	5.5	V
V_S	Programming step size	V_p < 3.3V		300		mV
		V_p > 4.0V		100		mV
V_i	Converter input voltage		2.7 V **and** > V_p + V_Δ	-	5.7	V
V_Δ	Minimum voltage between V_p and V_i for V_o specification				100	mV
$V_{o(down)}$	Output voltage	$\Delta I_o / \Delta t$ < 500mA / 10 µs for V_p < V_i	-3.5%	V_p [3]	+3.5%	V
		$\Delta V_i / \Delta t$ < 0.5 V / 10 µs				
$V_{o(up)}$	Output voltage	$\Delta I_o / \Delta t$ < 250mA / 10 µs for V_p < V_i	-3.5%	V_p [3]	+3.5%	V
		$\Delta V_i / \Delta t$ < 0.5 V / 10 µs				
$I_{o(DOWN)}$	Continuous output current	ON mode, V_p = 1.8V, V_i=3.6V		-	500	mA
		BYP mode, V_i=3.6V		-	250	mA
		PFM-only mode, L_{ext}=10uH				
		V_i=3.6 V, V_p=1.2V			200	mA
		V_i=4.2 V , V_p=3.4V			100	mA
$I_{o(UP)}$	Continuous output current	ON mode, V_p = 5.0V, V_i=3.6V		-	200	mA
V_{PWROK}	Power OK threshold level			0.9 * V_p		V

Table 84: Characteristics of the DCUD converter *...continued*

*V_{SS} = REFGND = *GND = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$\eta_{(DOWN)}$	Efficiency in down mode [4]	V_i =3.6V, V_p=1.8V				
		I_o = 1mA	75			%
		I_o= 10mA	85			%
		I_o=100mA	85			%
		I_o=500mA	75			%
$\eta_{(UP)}$	Efficiency in UP mode [4]	V_i =5.0V, V_p=1.8V				
		I_o = 1mA	75			%
		I_o= 10mA	85			%
		I_o=100mA	85			%
		I_o=500mA	75			%
ESR_{COUT}	Internal series resistance of output capacitor		0.07		0.20	Ω
F_{SW}	Switching frequency	PWM mode, 32kHz Xtal connected	488	514	540	kHz
I_{DD}	Total supply current [1][2]	ON or ECO mode; no load	-	75		µA
		OFF mode, ByPass mode	-	-	1	µA
		OFF mode, no ByPass mode	-	-	1	µA

[1] Values are specified at T_{amb} = 25 °C, V_{IN} = 3.6 V and are validated by a product characterization report based on measurements on sample basis.

[2] Sum of the current through the module VBAT pin and the current supplied via the internal supply.

[3] The accuracy of the output voltage is determined by the choice of the external components.

[4] External output capacitor 47uF: with ESR_{COUT} = 0.10Ω, external inductor 15uH with DCR_L = 0.1Ω.

Table 85: Characteristics for each of the IO, D1, D2, D3 and LP linear regulators.

*V_{SS} = REFGND = *GND = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.*

External capacitor 470nF: with ESR_{COUT} < 0.05 Ω and ESL_{COUT} < 3 nH for 1 Mhz < f < 50 Mhz.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_p	Programmable output voltage	Steps of 100 mV, IOREG	1.8	-	3.3	V
		Steps of 100 mV, all others	0.9	-	3.3	V
V_i	Regulator input voltage		1.6V **and** > V_p + V_Δ	-	5.7	V
V_Δ	Minimum voltage between V_p and V_{bat} for V_o specification			200	250	mV

Table 85: Characteristics for each of the IO, D1, D2, D3 and LP linear regulators....*continued*

*V_{SS} = REFGND = *GND = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.*
External capacitor 470nF: with ESR_{COUT} < 0.05 Ω and ESL_{COUT} < 3 nH for 1 Mhz < f < 50 Mhz.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_o	Output voltage	V_p < 1.2 V $\Delta I_o / \Delta t < (V_p / 16\ \Omega) / 10\ \mu s$ $\Delta V_i / \Delta t$ < 0.5 V / 10 µs load > 16 Ω	-4.5%	V_p	+4.5%	V
		1.2 V <= V_p < 2.5 V $\Delta I_o / \Delta t < (V_p / 16\ \Omega) / 10\ \mu s$ $\Delta V_i / \Delta t$ < 0.5 V / 10 µs load > 16 Ω	-3.5%	V_p	+3.5%	V
		V_π >= 2.5 V $\Delta I_o / \Delta t$ < 150 mA / 10 µs $\Delta V_i / \Delta t$ < 0.5 V / 10 µs I_o < 150 mA	-3.5%	V_p	+3.5%	V
$V_{o,ECO}$	Output voltage in ECO mode	V_π < 1.2 V $\Delta I_o / \Delta t$ < 100 µA / µs $\Delta V_i / \Delta t$ < 50 mV / µs I_o < 5 mA	-4.5%	V_p	+4.5%	V
		V_p >= 1.2 V $\Delta I_o / \Delta t$ < 100 µA / µs $\Delta V_i / \Delta t$ < 50 mV / µs I_o < 5 mA	-4.0%	V_p	+4.0%	V
V_{PWROK}	Power OK threshold level			0.9 * V_p		V
I_o	Output current	ON mode		-	150	mA
		ECO mode		-	5	mA
C_{dc}	Regulator Output capacitor	R_{ESR} < 50 mΩ and L_{ESL} < 3 nH for 1 Mhz < f < 50 Mhz	400	470		nF
$\Delta V_{o(t)}$	Temperature drift of V_o	V_{bat}=3.6 V		0.07		mV/°*C*
$\Delta V_o / \Delta I_o$	Load regulation	ΔI_o =150 mA, ON mode	-	0.01	0.02	%/mA
$\Delta V_{o(loadstep)}$	Output voltage change after load step	ΔI_o =150 mA, Δt = 10 µs ON mode	-	4	-	%
$\Delta V_o / \Delta V_i$	Line regulation	ON mode	-	1.0	2.0	mV/V
$\Delta V_{o(linestep)}$	Line step response	ΔV_i = 0.5 V, Δt = 10 µs	-	3	-	mV
RR	Input voltage ripple rejection for harmonic signals with amplitude < 50 mV	100 Hz < f < 10 kHz	50	60	-	dB
		f <1 MHz	35	40	-	dB
I_{DD}	Total supply current [1] [2]	ON mode; no load	-	100	120	µA
		ON mode; 150 mA load;		3.1	3.12	mA
		ECO mode; no load	-	15	30	µA
		ECO mode; 5 mA load		30	45	µA
		OFF mode	-	-	1	µA

Table 85: Characteristics for each of the IO, D1, D2, D3 and LP linear regulators....*continued*

*V_{SS} = REFGND = *GND = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.*
External capacitor 470nF: with ESR_{COUT} < 0.05 Ω and ESL_{COUT} < 3 nH for 1 Mhz < f < 50 Mhz.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$I_{DDLPSAVE}$	Total supply current LPREG in SAVE state (supplied by V_{BACK} only, measured values at V_{BACK} input)	ECO mode; no load	-	40		µA
		OFF mode	-	25		µA
t_{on1}	Turn-on time from V_o = 0 to V_o = 90% of nominal value when switching from OFF to ON mode, after debounce of $\overline{ONKEY}$ or RTC alarm interrupt	load > 16 Ω for V_p < 2.5 V I_o <150 mA for V_p > 2.5 V	-	20	60	µs
t_{on2}	Turn-on time from ECO to ON mode. Timing reference is the first falling edge on CLK32 after PWRENx change.	load > 16 Ω for V_p < 2.5 V I_o <150 mA for V_p > 2.5 V	-	20	60	µs
t_{on3}	Turn-on time from OFF to ECO mode. Timing reference is the first falling edge on CLK32 after PWRENx change.	load > 480 Ω for V_p < 2.5 V I_o <5 mA for V_p > 2.5 V	-	100	250	µs

[1] Values are specified at T_{amb} = 25 °C, V_{IN} = 3.6 V and are validated by a product characterization report based on measurements on sample basis.

[2] Sum of the current through the module VBAT pin and the current supplied via the internal supply.

[3] This regulator has no active pull-down circuit to discharge the output capacitor when the regulator is reprogrammed to a lower output voltage. The time to reach the new output voltage is fully determined by the load.

11.5 Characteristics ADC

Table 86: Characteristics of the 10 bit ADC

V_{SS} = 0 V, 2.95 V < V_{bat} < 5.7 V, T_{amb} = -40 to +85 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AVDD}	Voltage range AVDD input		2.5		3.3	V
$V_{BATVOLT}$	Input voltage range BATVOLT input	ADCMUX = 000 ADCMUX = 001	0 3.1		V_{BAT}+0.8 V_{BAT}+0.8	V V
V_{ADCIN1}	Input voltage range ADCIN1 input	ADCMUX = 010 ADCMUX = 011	0 3.1		6.0 5.4	V V
V_{ADCINx}	Input voltage range BATTEMP,ADCIN2/3 inputs		0		2.4	V
RES	Resolution			10		Bit
DNL	Differential non linearity	BATVOLT, ADCIN1 inputs, full scale mode	-0.8	-	0.8	LSB
DNL	Differential non linearity	BATVOLT, ADCIN1 inputs subtractor mode	-1.0	-	1.0	LSB
DNL	Differential non linearity	ADCIN2, ADCIN3, BATTEMP inputs	-0.5	-	0.5	LSB
INL	Integral non linearity	BATVOLT, ADCIN1 inputs full scale mode	-3.0	-	3.0	LSB

Table 86: Characteristics of the 10 bit ADC...*continued*

V_{SS} = 0 V, 2.95 V < V_{bat} < 5.7 V, T_{amb} = -40 to +85 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
INL	Integral non linearity	BATVOLT, ADCIN1 inputs subtractor mode	-4.0	-	4.0	LSB
INL	Integral non linearity	ADCIN2, ADCIN3, BATTEMP inputs	-2.0	-	2.0	LSB
T_{PWRUP}	Power up time			2		µs
T_{SDEL}	Settling time ratiometric measurement mode	ADCSDEL=0 ADCSDEL=1		10 100		µs µs
$T_{SYNCDEL}$	Delay time external synchronization	External synchronization enabled	495		510	µs
T_{CON}	Conversion time			25		µs
$T_{SYNCDEL}$	Delay after detected external synchronization condition		495		510	µs
R_{NTCSW}	Resistance switch between NTCSW and AVDD pins		60	80	120	Ω
$R_{IN(BATV)}$	Input resistance BATVOLT input	ADCMUX=00x	100			kΩ
$R_{IN(ADC1)}$	Input resistance ADCIN1 input	ADCMUX=01x	100			kΩ
$I_{IN(SELNOT)}$	Input leakage none selected ADC inputs				1	µA
$I_{DD(ADC)}$	Current consumption during conversion	V_{bat} = 3.6 Volt			300	µA

11.6 Characteristics TSC

Table 87: Characteristics of the TSC

V_{SS} = 0 V, 2.95 V < V_{bat} < 5.7 V, T_{amb} = -40 to +85 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IN(AVDD)}$	Voltage range AVDD input		2.5		3.0	V
R_{SW}		AVDD=2.7V		10		Ω
I_{SW}		AVDD=2.7V, duration 100ms			50	mA
$C_{IN,TSC}$	Input capacity TSxx pins	AVDD=2.7V			3	pF

11.7 Characteristics ACD

Table 88: Characteristics of the Accessory Detection

V_{SS} = 0 V, 2.95 V < V_{bat} < 5.7 V, T_{amb} = -40 to +85 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{TH(ACD)}$	ACD threshold		-5%	Progr value	+5%	V
$V_{HYS(ACD)}$	Threshold hysteresis			0.04 V_{TH}		V
$t_{DEB(ACD)}$	Debounce time for accessory detection	32 kHz clock available	-5%	62	+5%	ms
		32 kHz clock not available	-10%	62	+10%	ms
$I_{DD(ACD)}$	Total supply current	V_{bat} = 3.6 Volt		3	5	µA

11.8 Characteristics MBC

Table 89: Characteristics of the Main Battery Charger

V_{SS} = 0 V; T_{amb} = −40 to 85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CHG}	Charger wall plug voltage (continuous)		0		15	V
V_{CHGCON}	Programmable “Li-Ion battery fully charged” voltage limit	Steps of 20 mV	4.00	-	4.28	V
V_{BATCHG}	“Battery fully charged” voltage limit	fast charge temperature range (0 to 55ºC), 4.00-4.28V setting	V_{CHGCON} - 0.8%	V_{CHGCON}	V_{CHGCON} + 0.8%	V V
		5.0V setting	4.95	5.0	5.05	V V
$I_{CHGFAST}$	Fast charge current range	adjustable by external resistor	0.25		2.0	A
$I_{CHGSLOW}$	charge current in qualification, pre and trickle charge mode expressed as a ration of $I_{CHGFAST}$	CURRAT=00 CURRAT=01 CURRAT=10 CURRAT=11	0.02 * 0.05 * 0.15* 0.32 *	0.05 * 0.1 * 0.2 * 0.4 *	0.10 * 0.15 * 0.25 * 0.48 *	$I_{CHG, FAST}$
V_{RSENSE}	Voltage drop Rsense resistor	fast charge mode fast charge temperature range	105	111	117	mV
V_{BATMIN}	Minimal battery voltage limit allowing fast charging			2.7		V
$V_{TBATMIN}$	Low battery temperature threshold BATTEMP input		0.695 *	0.740 *	0.785*	V_{NTCSW}
$V_{TBATMAX}$	High battery temperature threshold BATTEMP input		0.244*	0.260 *	0.276 *	V_{NTCSW}
V_{BATOV}	Battery overvoltage, stopping the charging sequence		5.1	5.3	5.5	V
V_{CHGMIN}	Minimal charger voltage, enabling the MBC module		2.3	2.7	3.0	V
$V_{CHGBATMIN}$	Minimal charger battery voltage difference enabling the MBC module	DETMOD = 0	10	25	50	mV
V_{CHGMAX}	Maximum charger voltage, stopping the charging sequence		10.0	10.5	11.0	V
$T_{WD,MAX}$	Maximum time setting watch dog			93		min
$T_{WD,STEP}$	Time step watch dog			3		min
$T_{WD,INT}$	Pre-warning time watch dog expiration interrupt			10		s
V_{CHGDRV}	Output voltage range CHGDRV output	V_{CHGIN}>3.0V	0		2	V
I_{CHGDRV}	Output current range CHGDRV output	V_{CHGIN}>3.0V			25	µA
I_{CHGCUR}	input current CHGCUR input				5	µA
I_{OCP}	over-current protection limit		2.10*	2.25*	2.40*	$I_{CHG, FAST}$

11.9 Characteristics BBC

Table 90: Characteristics of the Backup Battery Charger

*V_{SS} = REFGND = *GND = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_{VBAT}	Main battery input voltage	$V_{VBAT} > V_{LOWBAT}$	V_{VBACK} + 0.2		5.7	V
V_{VBACK}	Backup battery input voltage		0		5.7	V
I_{BBC}	Backup battery charging current	BBCC = '00' and $V_{VBACK}<V_{VBAT}$-0.5V	35	50	65	µA
		BBCC = '01' and $V_{VBACK}<V_{VBAT}$-0.5V	70	100	130	µA
		BBCC = '10' $V_{VBACK}<V_{VBAT}$-0.5V	130	200	270	µA
		BBCC = '11' $V_{VBACK}<V_{VBAT}$-0.5V	250	400	550	µA
V_{LIM}	Backup battery limiting voltage	BBCV = '0'	2.37	2.50	2.63	V
		BBCV = '1'	2.85	3.00	3.15	V
V_{LIM_25}	Backup battery limiting voltage	BBCV = '0' [1]	2.42	2.50	2.58	V
		BBCV = '1' [1]	2.91	3.00	3.09	V
V_{DELTA}	Voltage range where output current is limited	BBCR = '1'	160	220	280	mV

[1] Values are specified at T_{amb} = 25 °C, V_{IN} = 3.6 V and are validated by a product characterization report based on measurements on sample basis.

11.10 Characteristics BVM

Table 91: Characteristics of the Battery Voltage Monitor

*V_{SS} = REFGND = *GND = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$V_{BATVOLT}$	Main battery voltage		2.0	-	5.7	V
V_{LOWBAT}	Low battery threshold		-2%	Progr. value	+2%	V
$V_{HYS(BVM)}$	Low battery hysteresis			0.04 V_{TH}		V
$t_{DEB(BVM)}$	Debounce time for low battery condition (only rising edge)	32 kHz clock available	-5%	62	+5%	ms
		32 kHz clock not available	-10%	62	+10%	ms

[1] Values are specified at T_{amb} = 25 °C, V_{IN} = 3.6 V and are validated by a product characterization report based on measurements on sample basis.

11.11 Characteristics CGU

Table 92: Characteristics Free-running Oscillator

*V_{SS} = REFGND = *GND = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
F_{CLKCCO}	System clock frequency	32 kHz clock is available	3.42	3.6	3.78	MHz
F_{CLKCCO}	System clock frequency	32 kHz clock is not available	3.24	3.6	3.96	MHz

[1] Values are specified at T_{amb} = 25 °C, V_{IN} = 3.6 V and are validated by a product characterization report based on measurements on sample basis.

Table 93: Characteristics 32 kHz oscillator

*V_{SS} = REFGND = *GND = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
I_{osc}	Total supply current from V_{INT} [1]		-	1.2	1.6	µA
GM	Oscillator Transconductance		8	14	20	µS
$T_{OSCSTART}$	Total start up time until CLK32 signal is active	System is forced to go to ACTIVE state when main battery (V_{VBAT} > V_{LOWBAT}) is connected, by $\overline{ONKEY}$	-	400	500	ms
C_{IN}	Input capacitance of pin OSC32I, OSC32O		-	5	-	pF

[1] Values are specified at T_{amb} = 25 °C, V_{IN} = 3.6 V and are validated by a product characterization report based on measurements on sample basis.

11.12 Characteristics ISM and OCR

Table 94: Characteristics internal supply module

*V_{SS} = REFGND = *GND = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_{VBAT}	Main battery input voltage		0	-	5.7	V
V_{VBACK}	Backup battery input voltage		0	-	5.7	V
V_{VINT}	Internal supply voltage	V_{VBAT} > 3.0 V or V_{VBACK} > 3.0 V	2.5	2.7	2.9	V
I_{VINT}	Maximum external load on VINT pin	Resistive loads only	-	-	2	mA
$V_{VERYLOWBAT}$	Main battery presence threshold voltage		-	2.7	-	V
V_{LOWCHG}	Charger presence threshold voltage		-	2.7	-	V
$V_{LOWBACK}$	Backup battery presence threshold voltage		-	1.3	-	V
I_{VBACK}	Backup battery input current (leakage)	V_{VBACK} < V_{VBAT} - 0.5V	-	-	1	µA
C_{dc}	Regulator Output capacitor	R_{ESR} < 50 mΩ and L_{ESL} < 3 nH for 1 MHz < f < 50 MHz	400	470		nF

[1] Values are specified at T_{amb} = 25 °C, V_{IN} = 3.6 V and are validated by a product characterization report based on measurements on sample basis.

11.13 Characteristics THS

Table 95: Characteristics of the Temperature High Sensor

V_{SS} = 0 V, 2.95 V < V_{bat} < 5.7 V, T_{amb} = -40 to +85 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{TH(THS)}$	High temperature threshold		135	150	165	°C
$T_{HYS(THS)}$	Temperature hysteresis		15	20	25	°C
$t_{DEB(THS)}$	Debounce time for high temperature condition	32 kHz clock available	-5%	62	+5%	ms
		32 kHz clock not available	-10%	62	+10%	ms
$I_{DD(THS)}$	Total supply current	V_{bat} = 3.6 Volt		3	5	µA

11.14 Characteristics GPO pins

Table 96: Characteristics for GPOx pins

*V_{SS} = REFGND = *GND = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage on GPO pins		-0.2	-	0.4	V
V_{OH}	HIGH-level output voltage on GPO pins		V_{IOVDD} - 0.4	-	V_{IOVDD} + 0.2	V
I_{OL}	LOW-level output current on GPO pins	V_{IOVDD} > 1.80 V V_{IOVDD} > 2.50 V	- -	- -	1.5 2.0	mA mA
I_{OH}	HIGH-level output current on GPO pins	V_{IOVDD} > 1.80 V V_{IOVDD} > 2.50 V	-1.5 -2.0	- -	- -	mA mA

Table 97: Characteristics for GPOODx pins

*V_{SS} = REFGND = *GND = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INMAX}	Maximum voltage on GPOODx pins		-	-	6	V
I_{SINK}	Sink current through GPOODx pins (active low)	ON mode (switch closed) V_{IOVDD} > 2.5V V_{IOVDD} > 1.6V	 100 50	 -	 -	 mA mA
$I_{LEAKAGE}$	Leakage current through GPOODx pins	Tri-state mode (switch open)	-	-	5	µA
V_{OL}	LOW-level output voltage on GPOODx pins	I_{OL} = I_{SINK}	-0.3	-	0.35	V

12. Quality specification

In accordance with “SNW-FQ-611 part E”. The numbers of the quality specification can be found in the “Quality Reference Handbook”. This handbook can be ordered using the code 9397 750 00192.

13. Package outline

Fig 67. Package outline SOT684-2 (HVQFN56 with 5.20 x 5.20 mm nominal diepad size)

14. Application information

14.1 Power supply concepts

The PCF50606 can generate the supply voltage for a typical multi-media system in different ways:

- 2.7V IO supply
- 2.7V analog supply
- 1.8V memory supply
- 1.0 to 1.8V core supply
- 1.8V permanent supply
- 4.0 to 5.0V white led supply

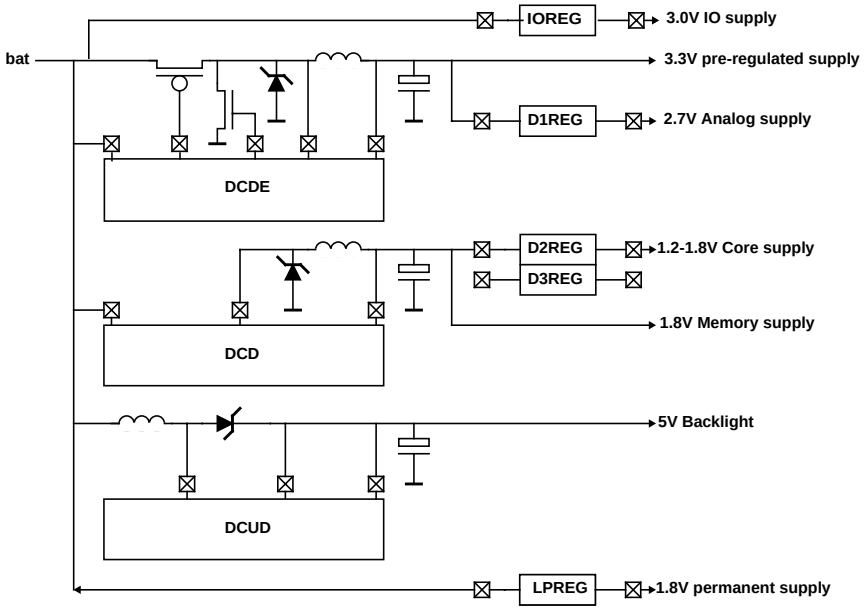


Fig 68. PCF50606HN/xA/N1 PCF50606HN/xB/N1 PCF50605HN/xA/N1 PCF50605HN/xB/N1 in a multi media application with additional high current 3.xV accessory supply, full use of converters offered.

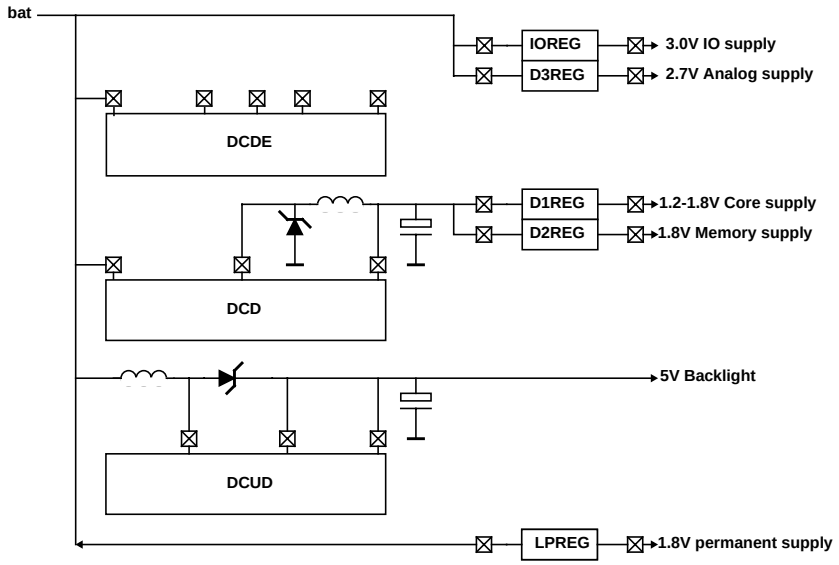


Fig 69. PCF50606HN/xA/N1 PCF50606HN/xB/N1 PCF50605HN/xA/N1 PCF50605HN/xB/N1 in a multi media application, low cost option with optimal use of the offered ECO/BYPASS modes.

In many mobile computing systems three supplies are needed. The PCF50606 can be used to generate these supplies.

The following supply concepts can be used for a system with the following demands

5V supply (<200mA)

3V supply, high current (>0.5A)

core supply 1.0 to 1.8V (<500mA)

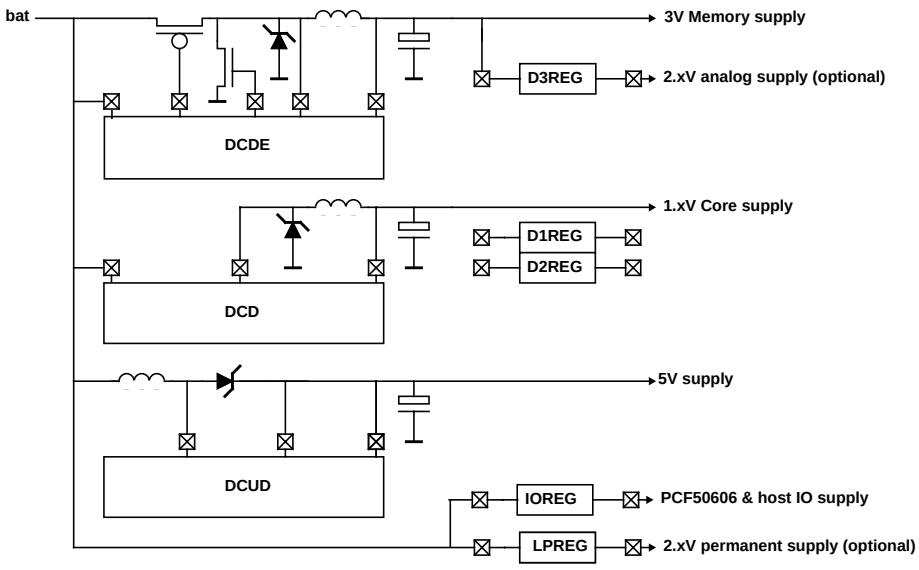


Fig 70. PCF50606HN/xA/N1 PCF50606HN/xB/N1 PCF50605HN/xA/N1 PCF50605HN/xB/N1 in a mobile computing application, minimal use of regulators

In several mobile computing systems the 5V supply is removed. This leads to the following supply architecture. This offers the possibility to split the IO and Memory supplies.

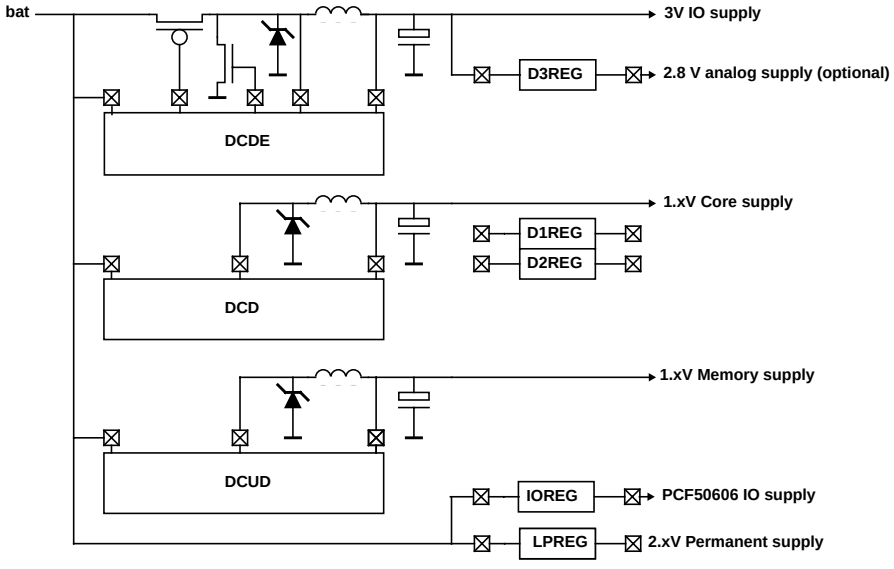
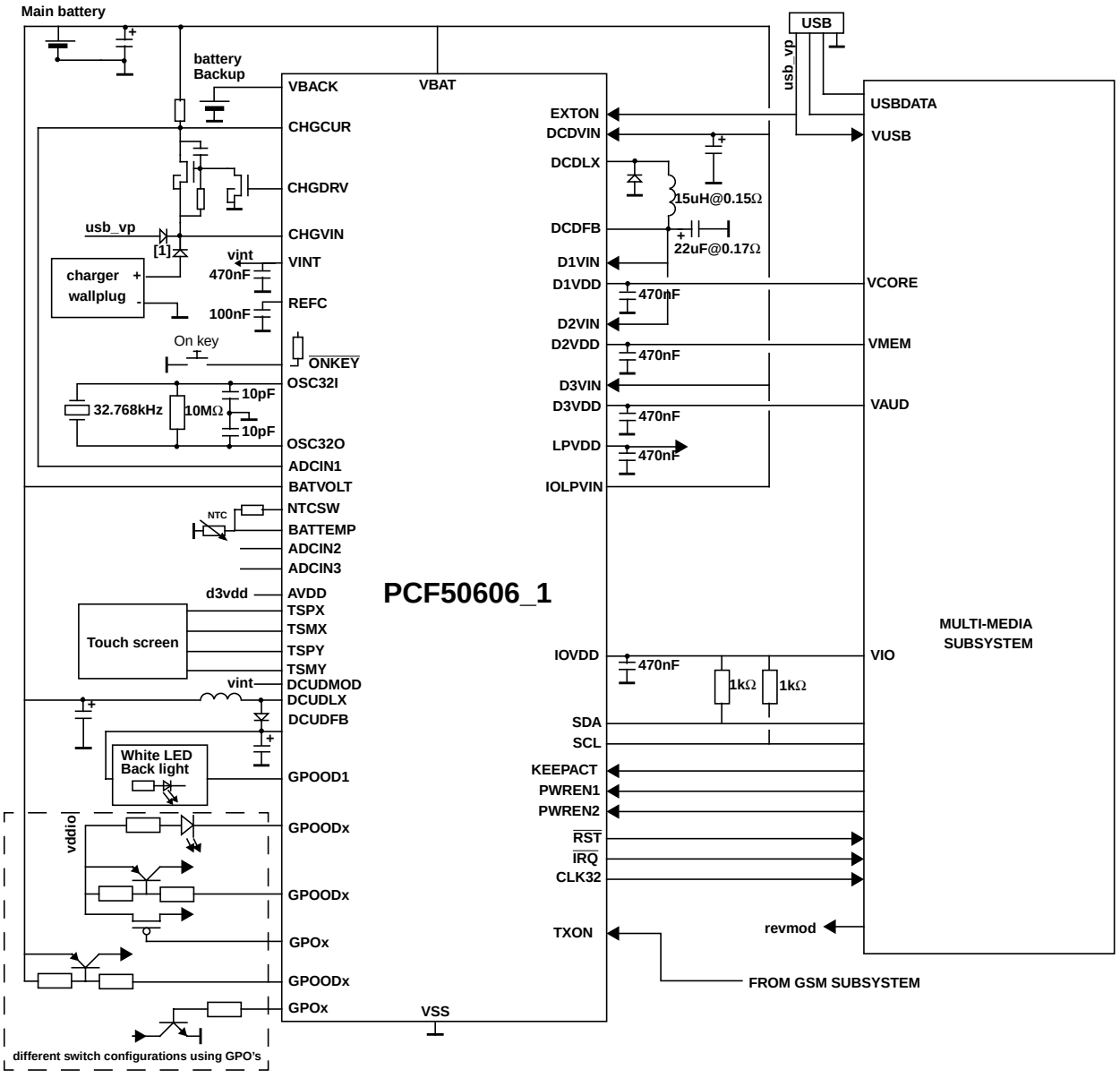


Fig 71. PCF50606HN/xA/N1 PCF50606HN/xB/N1 PCF50605HN/xA/N1 PCF50605HN/xB/N1 in a mobile computing application, minimal use of regulators

14.2 Application diagram



(1) These (schottky) diodes can be removed is no charging from USB is required

Fig 72. PCF50606HN/xA/N1 PCF50606HN/xB/N1 PCF50605HN/xA/N1 PCF50605HN/xB/N1-1 in a multi media application, DCUD used as step up converter for White LED backlight, including battery charging from USB.

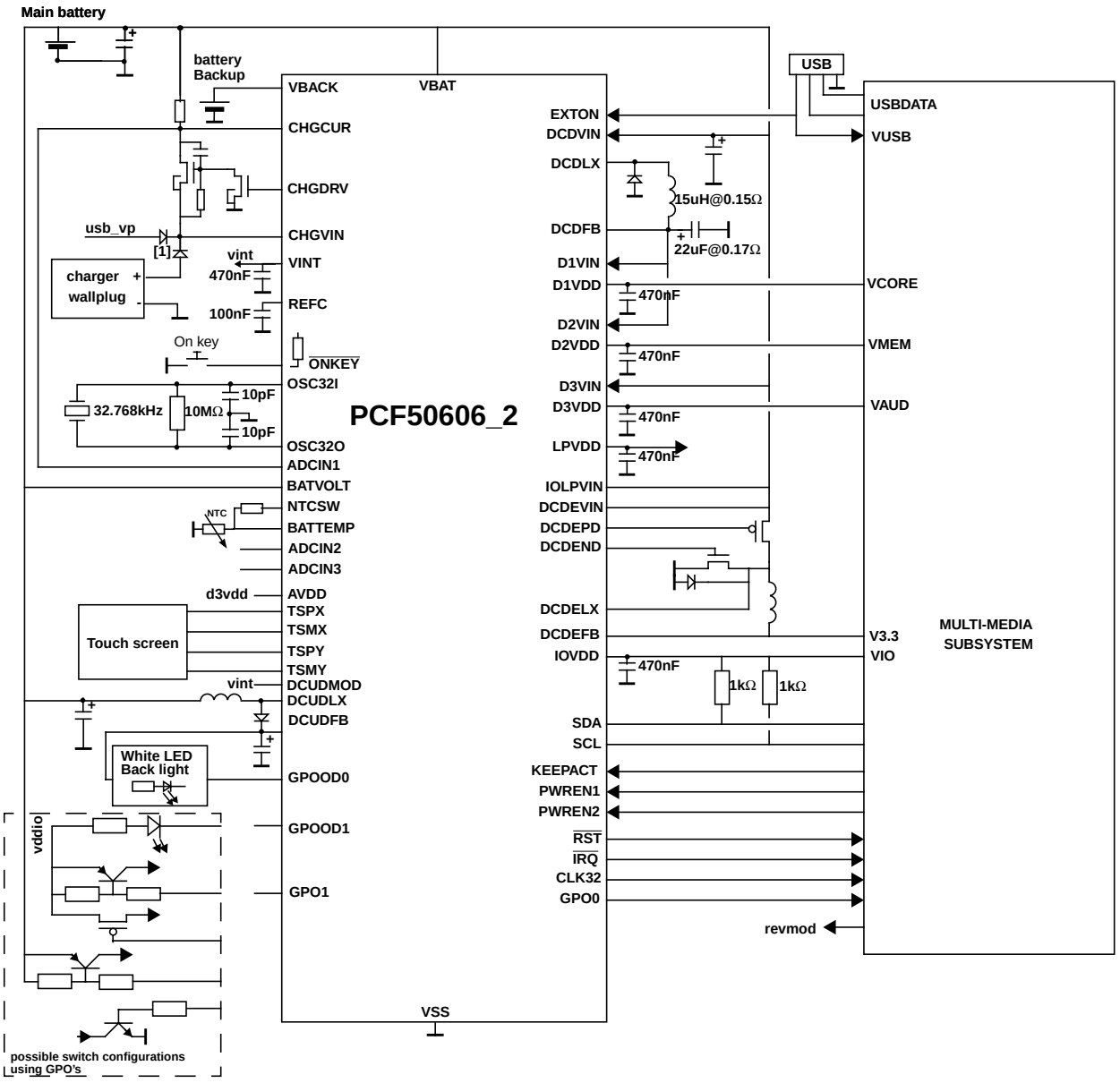


Fig 73. PCF50606HN/xA/N1 PCF50606HN/xB/N1 PCF50605HN/xA/N1 PCF50605HN/xB/N1-2 in a multi media application, DCUD used as step up converter for White LED backlight, DCDE as high current 3.3V supply

15. References

16. Revision history

Table 98: Revision history

Rev	Date	CPCN	Description
0.1	06/10/2001		Initial draft version, not released
0.2	06/18/2001		Added ADC, touch screen and dual PMU operation support
0.3	06/29/2001		Added Charger function, changed to a HVQFP56 package
0.4	08/03/2001		Added the type number PCF50606 Added RTC / BBC / GPO / PWM / LED modules removed the DCDCU1 / USBCHG / Audio modules replaced HCREG by STREG regulators replaced the CCCV charger by a pulse mode charger lowered the output current of the DCDC down converter Updated the pinlist
0.5	08/09/2001		Updated the pulse mode charger pins according the latest PC50604 implementation Added Dynamic Voltage Management for DCD, D1VDD and D2VDD Added Watchdog module Combined LED modulator with GPO module Added drive capability to open drain GPO pins Added a first application diagram
0.6	09/07/2001		Full rework of the spec, changed into an objective datasheet Added DC/DC with external power fets, removed touch screen, removed the USB regulator, made the DCDC up an up or down converter. Added detailed descriptions, spec tables etc.
0.7	10/01/2001		Re-introduced the touch screen interface module Replaced the MBC chapter with the latest PCF50604 main battery charger module Several minor updates in different chapters Version for internal review
1.0	10/05/2001		Processed the feedback on version 0.7 First released version of the objective specification
1.1	10/22/2001		Processed the feedback on version 1.0 Added information for the two bond-out version Update of the current consumption in OFF/SAVE states Extended the $\overline{\text{RST}}$ delay from 10 ms to 50 ms Added supply sequencing possibility Added ECO modes for DC/DC converters Added OFF mode selection for the DC/DC converters Updates in the ADC and touch screen control Added the BATOK as possible output of the GPO0
1.2	10/19/2001		Replaced the MBC module by the CHG module (CCCV fast charging) several minor changes
1.3	12/18/2001		Solved several items in the new charger module
1.4	01/17/2002		Updated the pinning (re-arranging of some pins, adding the DCDELX pin) provide information on the PCF50606/PCF50605 variant2 corrected the error in the charger external circuitry updated the control of the BBC module Added the register map, verified and corrected reset type and mask programmability several minor changes

Table 98: Revision history…*continued*

Rev	Date	CPCN	Description
1.5	08/03/2002		Versions 2 and 3 added. Several small errors corrected.
1.6	10/09/2002		Modifications for the N1D version. Several errors corrected. Introduction new register map. Main changes: Extended GPO(OD) flexibility. Toggle mode DCD-converter. Removing DVM functionality on D1-regulator. Introduction second LED-driver.
1.7	26/05/2003		Major update concerning parameter limits, nomenclature, spelling etc.
2.0	17/07/2003		Note added in general description wrt application notes. JEDEC classes added to ESD specification.
2.1	07/10/2003		Package version adapted PFM/PWM-only behaviour&settings made clear for DC/DC converters ID register setup adapted (more variants possible, no change for current users) Max load PFM-only mode added Stressed level sensitivity of EXTON pin in section 8.1.4 Changed DC/DC inductor & output cap ESR nomenclature Moved DC/DC output cap series resistance from table header to normal table item Added table note for inductor and capacitor properties at specified efficiency ADC header & input section rewritten for more clarity Rntcsw max value increased from 100 to 120 ohms

17. Data sheet status

Datasheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

18. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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