

DATA SHEET

PCF50732

Baseband and audio interface for
GSM

Objective specification
File under Integrated Circuits, IC17

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Baseband and audio interface for GSM**PCF50732**

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1 FEATURES

- Low power and low voltage device in 0.25 micron CMOS technology; supply voltage: analog 2.7 V (typical) and digital 1.5 V (typical)
- Compatible with GSM phase 2 and DCS1800 recommendations
- Complete in-phase and quadrature component interface paths between the Digital Signal Processor (DSP) and RF circuitry
- Complete linear PCM CODEC for audio signal conversion between earphone/microphone and DSP
- Four auxiliary analog inputs for measurement purposes (e.g. battery monitoring)
- Three auxiliary analog outputs for control purposes (i.e. AFC, AGC and power ramping control)
- Separate baseband, audio and control serial interfaces
- Voice band Signal Processor (VSP) for flexible audio data processing.

2 APPLICATIONS

The CMOS integrated circuit PCF50732, Baseband and audio interface for GSM, is dedicated to wireless telephone handsets conforming to the GSM recommendations phases 1 and 2, DCS1800 and PCS1900.

3 GENERAL DESCRIPTION

The baseband CODEC is a complete interface circuit between the RF part in a mobile communication handset and the Digital Signal Processor (DSP). It consists of three parts:

- The **receive path**, which transforms the quadrature signals from the RF (I/Q) to digital signals
- The **transmit path**, which transforms a bitstream to analog quadrature signals for the RF devices

4 ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|-------------|---------|--|----------|
| | NAME | DESCRIPTION | VERSION |
| PCF50732H | LQFP48 | plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm | SOT313-2 |

- The digital **Baseband Serial Interface (BSI)**, which exchanges baseband data between the PCF50732 and the digital signal processor. The interface also includes signals to power-up and power-down the baseband transmit (TX) and receive (RX) paths.

The voice band CODEC is a complete analog front-end circuit. It consists of four parts:

- The **receive path**, which converts a digital signal to an analog signal for an earpiece, an external loudspeaker or a buzzer
- The **transmit path**, which receives the analog external signal from a microphone and converts it into a digital signal
- The **Voice band Signal Processor (VSP)**, which filters the voice band data
- The digital **Audio Serial Interface (ASI)**, which connects the digital linear PCM signals of the receive and transmit paths to an external DSP. The voice band data is coded in 16-bit linear PCM twos complement words.

The **auxiliary Analog-to-Digital Converter (ADC)** section consists of four input channels specified for battery management applications.

The **auxiliary Digital-to-Analog Converter (DAC)** section consists of three DACs for Automatic Gain Control (AGC), for Automatic Frequency Control (AFC) and for power ramping.

The **Control Serial Interface (CSI)** is used to program a set of control registers, to store the power amplifier ramping characteristics into the dedicated RAM and to transmit auxiliary ADC values to the DSP. It also controls switches, modes and power status of the different parts of the IC.

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5 QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------------|-------------------------------|--|------|------|------|--------------|
| V_{DDD} | digital supply voltage | | 1.0 | 1.5 | 2.75 | V |
| V_{DDA} | analog supply voltage | $V_{DDA} \geq V_{DDD}$ | 2.5 | 2.7 | 2.75 | V |
| I_{DDA} | analog supply current | $V_{DDD} = 1.5$ V; $V_{DDA} = 2.7$ V; RXON active | – | 3.5 | – | mA |
| P_{av} | average power consumption | $V_{DDD} = 1.5$ V; $V_{DDA} = 2.7$ V; note 1 | – | 15 | – | mW |
| $I_{stb(tot)}$ | total standby current | | – | 10 | – | μ A |
| f_{clk} | master clock frequency | | – | 13.0 | – | MHz |
| T_{amb} | operating ambient temperature | | –40 | +27 | +85 | $^{\circ}$ C |

Note

1. Without load on audio outputs EARP, EARN, AUXSP and BUZ.

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6 BLOCK DIAGRAM

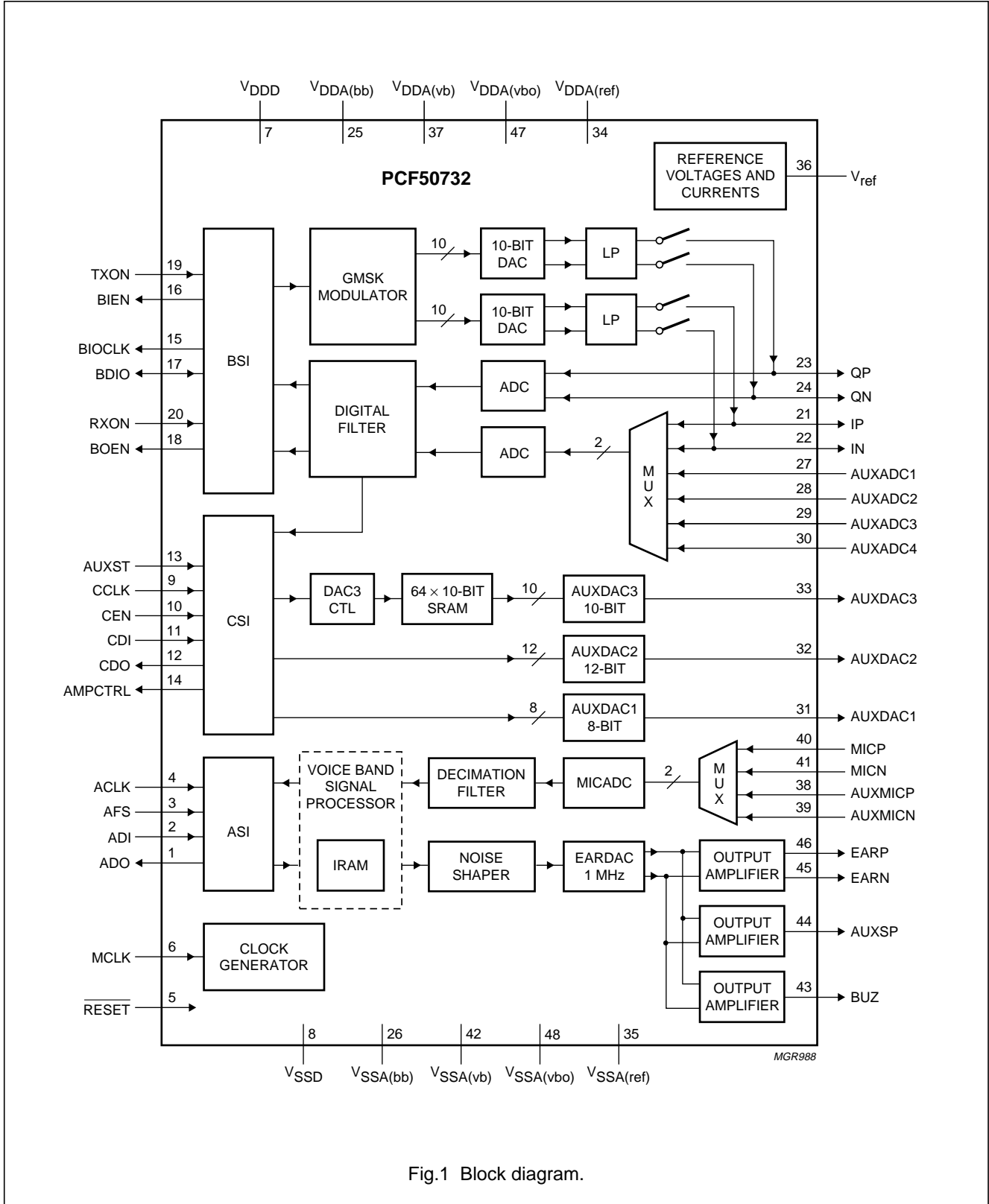


Fig.1 Block diagram.

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7 PINNING

| SYMBOL | PIN | | | | | DESCRIPTION |
|----------------------|-----|---------------------|--------------|-------------|-----------------|---|
| | NR. | TYPE ⁽¹⁾ | ACTIVE LEVEL | ACTIVE EDGE | I _{DD} | |
| ADO | 1 | O/TS | – | – | 1.5 mA | audio digital interface PCM data output to DSP |
| ADI | 2 | I | – | – | – | audio digital interface PCM data input from DSP |
| AFS | 3 | I | – | rising | – | audio digital interface PCM frame synchronization signal from DSP |
| ACLK | 4 | I | – | rising | – | audio digital interface PCM clock signal from DSP |
| RESET | 5 | I | LOW | – | – | asynchronous reset input |
| MCLK | 6 | I | – | rising | – | low-swing master clock input; f _{clk} = 13 MHz; integrated capacitive coupling |
| V _{DDD} | 7 | P | – | – | – | digital power supply |
| V _{SSD} | 8 | G | – | – | – | digital ground |
| CCLK | 9 | I | – | falling | – | control bus clock input from DSP |
| CEN | 10 | I | LOW | – | – | control bus data enable from DSP |
| CDI | 11 | I | – | – | – | control bus data input from DSP |
| CDO | 12 | O/TS | – | – | 1.5 mA | control bus data output to DSP |
| AUXST | 13 | I | HIGH | – | – | status control signal for activation of AUXDAC1, AUXDAC2 and MCLK input |
| AMPCTRL | 14 | O | – | – | 1.5 mA | general purpose output pin |
| BIOCLK | 15 | O/TS | – | – | 3 mA | baseband interface data clock |
| BIEN | 16 | O | LOW | – | 1.5 mA | baseband transmit interface data enable signal |
| BDIO | 17 | I/O | – | – | 1.5 mA | baseband interface data I/O from/to DSP |
| BOEN | 18 | O | LOW | – | 1.5 mA | baseband receive interface data enable signal |
| TXON | 19 | I | HIGH | – | – | baseband transmit path activation signal |
| RXON | 20 | I | HIGH | – | – | baseband receive path activation signal |
| IP | 21 | I/O | – | – | – | (I) baseband differential positive input/output to IF circuit |
| IN | 22 | I/O | – | – | – | (I) baseband differential negative input/output to IF circuit |
| QP | 23 | I/O | – | – | – | (Q) baseband differential positive input/output to IF circuit |
| QN | 24 | I/O | – | – | – | (Q) baseband differential negative input/output to IF circuit |
| V _{DDA(bb)} | 25 | P | – | – | – | baseband power supply (analog) |
| V _{SSA(bb)} | 26 | G | – | – | – | baseband ground (analog) |
| AUXADC1 | 27 | I | – | – | – | auxiliary ADC input 1 for battery voltage measurement |
| AUXADC2 | 28 | I | – | – | – | auxiliary ADC input 2 |
| AUXADC3 | 29 | I | – | – | – | auxiliary ADC input 3 |
| AUXADC4 | 30 | I | – | – | – | auxiliary ADC input 4 |
| AUXDAC1 | 31 | O | – | – | – | auxiliary DAC output for AGC; max. load 50 pF // 2 kΩ |
| AUXDAC2 | 32 | O | – | – | – | auxiliary DAC output for AFC; max. load 50 pF // 10 kΩ |

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| SYMBOL | PIN | | | | | DESCRIPTION |
|-----------------------|-----|---------------------|--------------|-------------|-----------------|---|
| | NR. | TYPE ⁽¹⁾ | ACTIVE LEVEL | ACTIVE EDGE | I _{DD} | |
| AUXDAC3 | 33 | O | – | – | – | auxiliary DAC output for power ramping; maximum load 50 pF, ±600 µA |
| V _{DDA(ref)} | 34 | P | – | – | – | reference voltage power supply (analog) |
| V _{SSA(ref)} | 35 | G | – | – | – | reference voltage ground (analog) |
| V _{ref} | 36 | I/O | – | – | – | band gap reference voltage noise decoupling |
| V _{DDA(vb)} | 37 | P | – | – | – | voice band voltage power supply |
| AUXMICP | 38 | I | – | – | – | auxiliary microphone differential positive input |
| AUXMICN | 39 | I | – | – | – | auxiliary microphone differential negative input |
| MICP | 40 | I | – | – | – | microphone differential positive input |
| MICN | 41 | I | – | – | – | microphone differential negative input |
| V _{SSA(vb)} | 42 | G | – | – | – | voice band ground |
| BUZ | 43 | O | – | – | – | buzzer output |
| AUXSP | 44 | O | – | – | – | auxiliary speaker output |
| EARN | 45 | O | – | – | – | earphone differential negative output |
| EARP | 46 | O | – | – | – | earphone differential positive output |
| V _{DDA(vbo)} | 47 | P | – | – | – | voice band output buffer voltage power supply (analog) |
| V _{SSA(vbo)} | 48 | G | – | – | – | voice band output buffer ground (analog) |

Note

1. O/TS = 3-state output.

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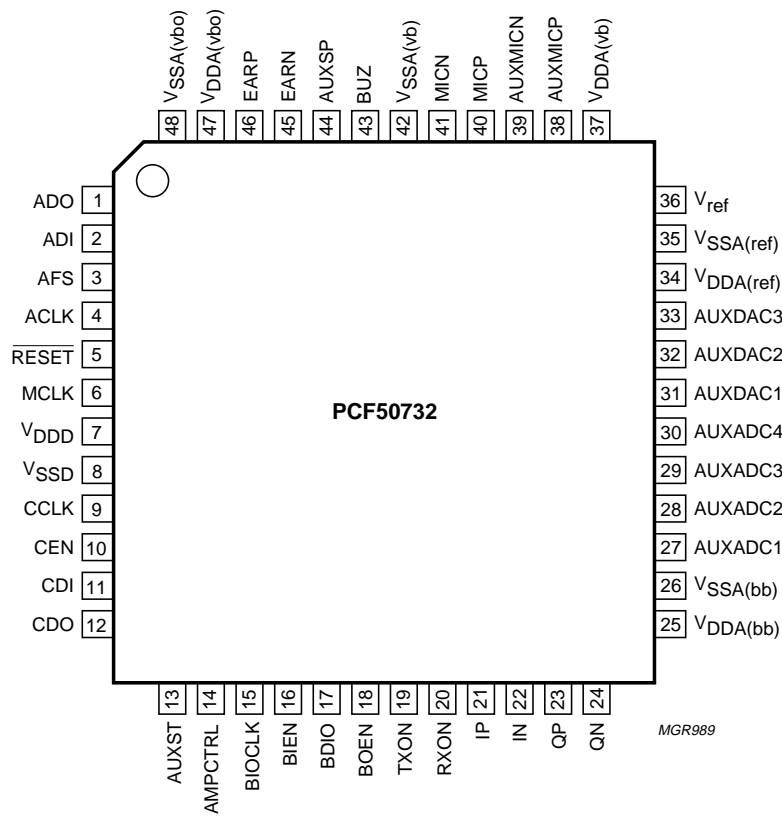


Fig.2 Pin configuration.

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8 FUNCTIONAL DESCRIPTION

This chapter gives a brief overview of the device. The detailed functional description can be found in the following chapters:

- Chapter 9 “Baseband CODEC”
- Chapter 10 “Voice band CODEC”
- Chapter 11 “Auxiliary functions”
- Chapter 12 “Control Serial Interface (CSI)”
- Chapter 13 “Voice band Signal Processor (VSP)”.

8.1 General

As low power consumption in mobile telephones is a very important issue, all the circuit parts in the PCF50732 can be powered-on/off either by means of the external signals AUXST, TXON or RXON, or by programming the respective register bits in the Control Serial Interface (CSI).

The most important signal for the digital and analog circuit functions in the PCF50732 is the DAC enable signal AUXST, which allows to activate AUXDAC1 (AGC) and AUXDAC2 (AFC), as well as the low-swing master clock input MCLK. AUXST must be active (HIGH) and **V_{DDA} must be stable** (see also Section 18.1) to allow the master clock to access different circuit parts after a reset ($\overline{\text{RESET}}$ active). AUXDAC1 and AUXDAC2 are only activated if their related power-on bit is set. AUXDAC1 is default off, AUXDAC2 is default on.

$\overline{\text{RESET}}$ must be active during at least 3 MCLK cycles, with AUXST active, to ensure a correct initialisation of all the digital circuitry of the PCF50732. Since $\overline{\text{RESET}}$ is asynchronous even small spikes of a few nanoseconds can cause partial resets.

For power supply noise interference reduction, a pair of power supply and ground pins are provided for the:

- Baseband analog: $V_{\text{DDA}(\text{bb})}/V_{\text{SSA}(\text{bb})}$
- Voice band analog: $V_{\text{DDA}(\text{vb})}/V_{\text{SSA}(\text{vb})}$
- Voice band output drivers: $V_{\text{DDA}(\text{vbo})}/V_{\text{SSA}(\text{vbo})}$
- DC reference voltages and currents: $V_{\text{DDA}(\text{ref})}/V_{\text{SSA}(\text{ref})}$
- Digital circuitry: $V_{\text{DDD}}/V_{\text{SSD}}$.

All V_{SS} pins are connected internally. V_{DDD} is the digital supply. $V_{\text{DDA}(\text{bb})}$, $V_{\text{DDA}(\text{vb})}$, $V_{\text{DDA}(\text{vbo})}$, and $V_{\text{DDA}(\text{ref})}$ are analog supplies, and are referred to as V_{DDA} throughout this document. These analog supplies must be connected externally.

8.2 Baseband and voice band reference voltages

The reference voltage V_{ref} is generated on-chip by a band gap voltage reference circuit and is available at pin V_{ref} .

As V_{ref} is used as reference for most of the internal analog circuitry, noise must be kept as low as possible by connecting an external decoupling capacitor at this pin.

The voltage at V_{ref} is buffered to generate the baseband and voice band reference voltage V_{ref} as well as internal references for the different functions, such as the auxiliary and the transmit DACs.

9 BASEBAND CODEC

The baseband CODEC is a complete interface circuit between the RF part in a mobile communication handset and the digital signal processor. It consists of three parts:

- The **transmit path**, which converts a bitstream to analog quadrature signals for the RF devices
- The **receive path**, which transforms the quadrature signals of the IF chip (I/Q) to digital signals
- The digital **baseband serial interface**, which exchanges baseband data between the PCF50732 and the DSP. The interface also includes signals to power-up and power-down the baseband transmit (TX) and receive (RX) paths.

9.1 Baseband transmit path

The baseband transmit path consists of three parts:

- **GMSK modulator**: generation of a Gaussian Minimum Shift Keying (GMSK) signal
- **10-bit DACs**: digital-to-analog converters for the I and Q components of the GMSK signal
- **Low-pass filters**: analog reconstruction low-pass filters for the output of the DACs.

The requirements of the transmit path of a GSM terminal are given by “*GSM recommendation 05.05*”:

- Phase RMS error $<5^\circ$
- Phase peak error $<20^\circ$
- Amplitude error $< \pm 1$ dB.

Nevertheless the performance of the PCF50732 is far better than these figures indicate; see Section 18.1.

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9.1.1 GMSK MODULATOR

The input signal of the GMSK modulator is a bitstream coming from the baseband serial interface, with a sampling frequency of 270.833 kHz. Typically 148 bits are modulated during a normal burst, and 88 bits during an access burst. Using this bitstream, the GMSK modulator generates digital I and Q components as described in "GSM recommendation 05.04".

This is done in three steps:

1. First the incoming bitstream is differentially encoded by an EXOR operation on the actual bit and the previous bit
2. The instantaneous phase (φ) is calculated using a gaussian filter with an impulse response of 4 taps
3. A look-up table provides the cosine (I component) and the sine values (Q component) of the phase (φ).

The look-up table also interpolates the signal to a 16 times higher frequency (4.333 MHz).

9.1.2 10-BIT DACs

The two 10-bit DACs are working at a sampling rate of 4.3333 MHz. They convert the digital I and Q components of the GMSK modulator to differential analog I and Q signals.

9.1.3 LOW-PASS FILTER

The analog output signals of the DACs are filtered by analog reconstruction low-pass filters.

These filters remove high frequency components of the DAC output signals and attenuate components around the 4.3333 MHz sampling frequency. The low-pass filters have a cut-off frequency of approximately 300 kHz, with very linear phase behaviour in the pass band.

9.2 Baseband receive path

The baseband receive path consists of two parts:

- **Receive ADC:** $\Sigma\Delta$ analog-to-digital converters
- **Decimation filter:** digital decimation filters for I and Q.

The baseband receive section can be switched between two modes of operation:

- **ZIF (zero IF) mode** for radio sections, which convert the receive signal down to baseband. In this mode the ADC is sampled at 6.5 MHz, the decimation filter samples down by a factor of 24 with a pass band as specified in Fig.3. The serial interface output BDIO delivers 2×12 -bit values for I and Q components at 270.833 kHz.
- **NZIF (near zero IF) mode** for radio sections, which converts the receive signal down to a centre frequency of 100 kHz. In this mode the ADC is sampled at 13 MHz, the decimation filter samples down by a factor of 24 with a pass band as specified in Fig.3. The serial interface output BDIO delivers 2×12 -bit values for I and Q components at 541.667 kHz.

9.2.1 RECEIVE ADC

The receive ADCs are $\Sigma\Delta$ analog-to-digital converters that convert differential input signals into 1-bit data streams with a sampling frequency of 6.5 or 13 MHz.

9.2.2 DIGITAL DECIMATION FILTER

Digital filtering is required for:

- Suppression of out-of-band noise produced by the $\Sigma\Delta$ ADC
- Decimation of the sampling rate (6.5 or 13 MHz) by 24
- System level filtering.

The digital filtering is performed by a digital FIR filter with a group delay for this running average filter of approximately 23 or 11.5 μ s respectively. The filter uses twos complement arithmetic.

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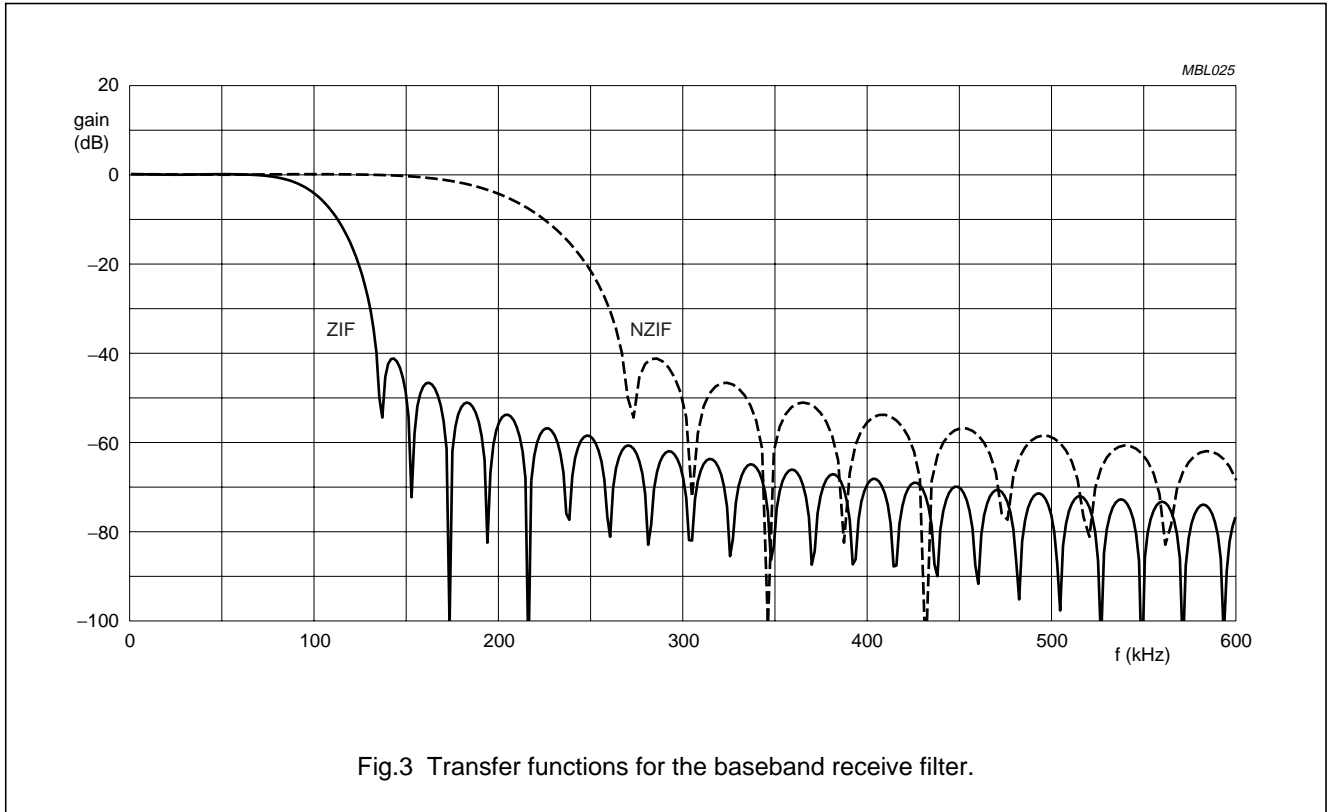


Fig.3 Transfer functions for the baseband receive filter.

9.3 Baseband Serial Interface (BSI)

9.3.1 OVERVIEW

The digital part of the baseband consists of a receive section and a transmit section. The receive section is a FIR filter that reduces the 6.5 MHz (13 MHz for NZIF mode) bitstream from the sigma-delta converters into 2 × 12-bit values at 270.833 kHz (541.667 kHz for NZIF mode).

The transmit section converts the 270.833 kHz data stream from the DSP into a GMSK signal sampled at 4.333 MHz. The 10-bit I and Q signals are then fed into two 10-bit DACs. The power ramping signal is also generated by the transmit section with the 10-bit AUXDAC3 block.

9.3.2 TRANSMIT PATH BLOCK DESCRIPTION

9.3.2.1 Transmit serial interface

The power-up of the BSI transmit path is controlled via the TXON pin. When TXON is pulled HIGH, the transmit path recovers from power-down. The $MCLK/48 = 270.833$ kHz output signal BIOCLK is activated. When the BIEN0 period has elapsed the output signal BIEN goes LOW and the bits to be transmitted are clocked out of the DSP.

BIEN0 must be at least 10 quarterbits long to allow settling of the analog filters. Bits are clocked out of the DSP by the falling edge and clocked into the PCF50732 by the rising edge of BIOCLK. After the BIEN1 period has elapsed, BIEN is set HIGH again and transmission from the DSP ends. Logic 1s are modulated whenever BIEN is HIGH and the baseband transmit (BBTX) block is active. Values for BIEN0 and BIEN1 can be set in the Burst control register.

Figure 5 shows the timing for the BSI data transmission. In power-down the de-asserted value of BIOCLK is high-Z and BIEN is HIGH. Typical connection to the system DSP is defined in Table 1.

Table 1 Connection of BSI transmit signals to PCF5087X

| PCF50732 | | PCF5087X | |
|----------|-----|----------|-----|
| PIN | I/O | PIN | I/O |
| TXON | I | RFSIG[y] | O |
| BDIO | I/O | SIOXD | I/O |
| BIEN | O | SOXEN_N | I |
| BIOCLK | O | SIOXCLK | I |

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9.3.2.2 Power ramping controller

The PCF50732 fully supports all multislot modes which do not require full duplex operation or more than two consecutive transmit bursts. In this specification double burst mode is used for all supported multislot modes while single burst mode supports the normal GSM modes.

The power ramping controller drives the power amplifier output envelope.

In each transmit (TX) burst one ramp-up and one ramp-down will be carried out. In multislot mode one intermediate ramp will be carried out in addition to ramp-up and ramp-down. Each ramp consists of 16 discrete step values that are sent to the DAC3. Each step's duration is 2 quarterbits which translates into 8-bit long ramps. The DAC3 output is in 3-state whenever it is powered down. The ramping step values are stored in a 64×10 -bit RAM as shown in Table 2.

In order to initialize AUXDAC3 it is necessary to write into the RAM all 32 (or 48 in multislot mode) DAC3 output values. Filling the RAM is normally done by writing a logic 0 to the address sub-register of the Burst control register, after which 32 or 48 values, depending on multislot mode, can be written into the data sub-register of the Burst control register. Writing to the DAC3 RAM is only possible when the DAC3 is powered off.

Total number of CSI-accesses is therefore 33 for a normal burst and 49 for a double burst.

An autoincrement feature will store these data into the correct RAM positions.

The value after power-up of DAC3 will always be equal to the value of RAM location 47.

AUXDAC3 timing is controlled by the Burst control register. This contains the following sub-registers:

- The **RU register** containing the delay in number of quarterbit cycles from the assertion of TXON to the start of the power-up ramping; default value is 0
- The **RM register** containing the delay in number of quarterbit cycles from the assertion of TXON to the start of the intermediate power ramp; default value is 0. RM is only used in case of multislot mode
- The **RD register** containing the delay in number of quarterbit cycles from the assertion of TXON to the start of the power-down ramping; default value is 0
- DAC3 burst RAM address register
- DAC3 burst RAM data register
- Single/double burst mode register: normal mode or multislot mode selection flag.

After TXON goes HIGH and a time equal to RU quarterbit periods has elapsed, power ramp-up is done.

After a time period equal to RD quarterbits has elapsed power ramp-down is initiated.

The AUXDAC3 output is also shown in Fig.4.

Values for RU (ramp-up) and RD (ramp-down) can be set in the Burst control register of the control serial interface. RD must be greater than RU + 32. RU and RD range from 0 to 4000 QB (quarterbit). The register offers the possibility to enter codes up to 4095.

The GMSK modulator is active for a period of 2 clock cycles after the ramp-down or for the length of the TXON burst, whichever is longer.

Multislot (high speed switched data mode) can be selected by setting the appropriate bit in the Burst control register. In multislot mode an intermediate ramping step is done. This intermediate step is started after a time period equal to RM quarterbits has elapsed. A value for RM (intermediate ramp) is also set using the Burst control register. The following conditions must be true:

$$RU + 32 < RM \text{ and } RM + 32 < RD.$$

Table 2 AUXDAC3 RAM contents

| RAM ADDRESS | DATA |
|-------------|------------------------|
| 0 to 15 | ramp-up data |
| 16 to 31 | intermediate ramp data |
| 32 to 47 | ramp-down data |
| 48 to 64 | not used |

Table 3 Power ramping timing characteristics

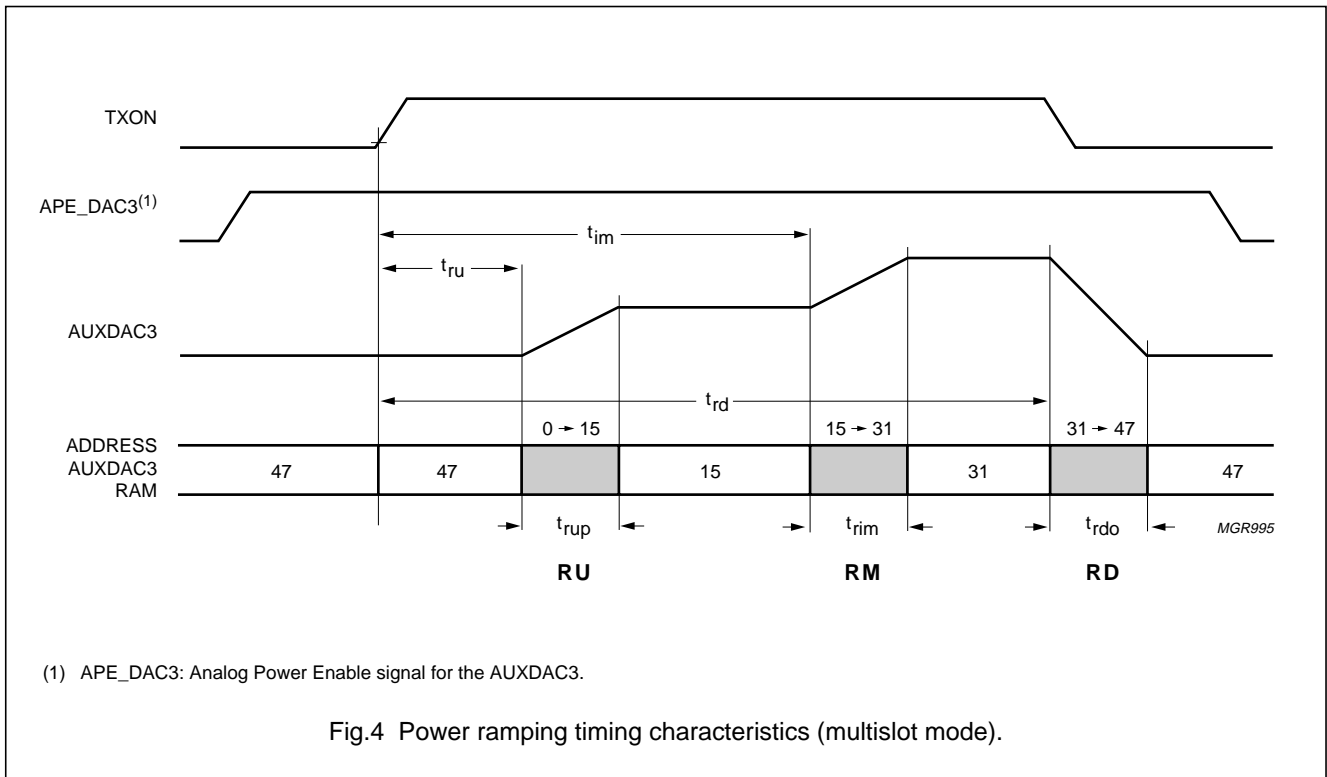
| SYMBOL | VALUE | COMMENTS ⁽¹⁾ |
|-----------------------------|-------------|-------------------------|
| t_0 | $12t_1$ | one quarterbit (QB) |
| t_{ru} | RU register | 0 to 4000 QB |
| t_{im} | RM register | RU + 32 to 4000 QB |
| t_{rd} | RD register | RM + 32 to 4000 QB |
| $t_{rup}, t_{rim}, t_{rdo}$ | $32t_0$ | 8 bits; 32 QB |

Note

1. QB: Quarterbit, usually referred to the time needed for one quarter of a GSM baseband bit, i.e. a frequency of $\frac{1}{12} \times 13$ MHz.

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9.3.3 RECEIVER PATH BLOCK DESCRIPTION

9.3.3.1 Receive serial interface

The baseband serial interface sends the digital signal of the receive path to a digital signal processor. It also takes the digital bitstream from the digital signal processor and transmits it via the baseband CODEC.

The baseband reception and transmission are active in bursts. A normal burst has a length of 548 μ s. The frame rate of bursts is 4.615 ms. Using a normal traffic channel, one burst for each frame is transmitted and two bursts are received. To save as much power as possible, the transmit path and the receive path of the PCF50732 are in power-up mode only during the transmission or reception bursts respectively.

The power-up of the receive section is controlled via the RXON pin or RXON bit. When RXON is driven HIGH, the receive section recovers from power-down and the output clock BIOCLK is activated. After a settling delay of 52 μ s (ZIF mode, analog circuitry + decimation filter settling time), BOEN goes LOW to transfer the first 12-bit I and Q words. The settling time is only 26 μ s in NZIF mode.

Bits are clocked out of the PCF50732 by the falling edge, and clocked into the DSP by the rising edge of BIOCLK. In normal bursts 148 I/Q pairs are read from the PCF50732.

When RXON goes LOW, the last pair of I and Q values will be sampled and transferred to the baseband processor (both I and Q components). BIOCLK stops after additional 16 BIOCLK cycles. The receive path is powered down again. In power-down the BIOCLK output is put in 3-state and the BOEN output is HIGH.

The output format is 2 \times 12-bit I/Q (twos complement). Transmission occurs MSB first, I followed by Q. The serial clock signal BIOCLK will run at 6.5 MHz, or 13 MHz in the NZIF mode. Figure 6 shows the timing of the BSI data reception.

An automatic offset compensation mechanism is provided in order to achieve the required performance. This mechanism will short the receive (RX) inputs internally and measure the resulting offset value. This offset value will be subtracted from all subsequent I/Q output words. The offset inherent to the device can thereby be reduced to a few millivolts. Default value for both I- and Q-offset is zero.

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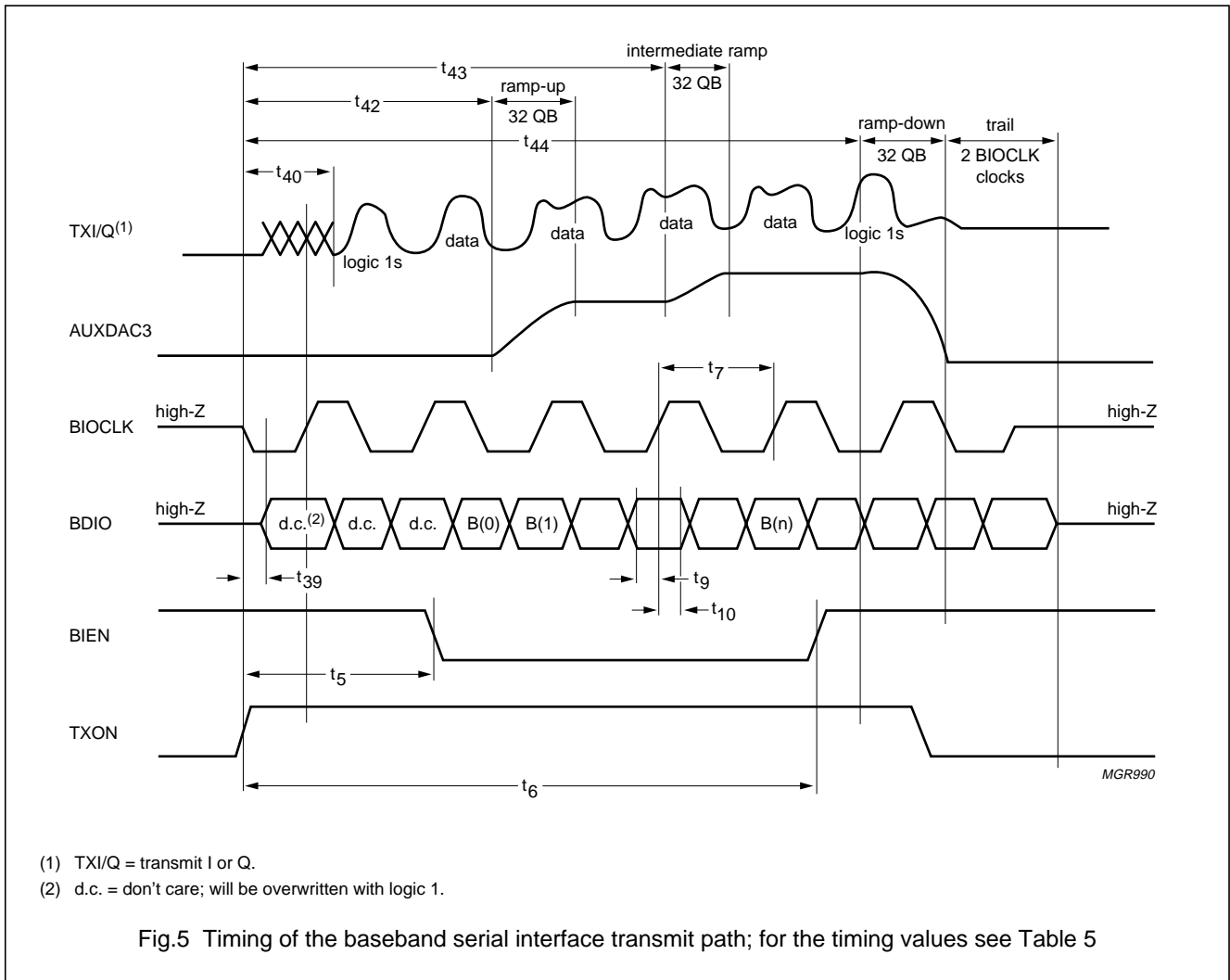
Offset compensation measurement can be done on three channels separately: baseband receive I channel, baseband receive Q channel and AUXADC channel. All AUXADC channels use the same offset compensation value. Starting an offset measurement is done by writing a logic 1 into the offset trigger register for each channel that needs calibration. If the value '7' (decimal) is written into the offset trigger register offsets will be measured for I, Q and AUXADC channels.

Offsets can also be read or written directly. Each offset measurement is implemented internally as an AUXADC measurement and takes approximately 100 μ s. Offsets from -256 up to 255 can be compensated.

Table 4 Connection of BSI receive signals to the PCF5087X

| PCF50732 | | PCF5087X | |
|----------|-----|----------|-----|
| PIN | I/O | PIN | I/O |
| RXON | I | RFSIG[z] | O |
| BDIO | I/O | SIOXD | I/O |
| BOEN | O | SIXEN_N | I |
| BIOCLK | O | SIOXCLK | I |

9.3.4 BASEBAND SERIAL INTERFACE (BSI) TIMING CHARACTERISTICS



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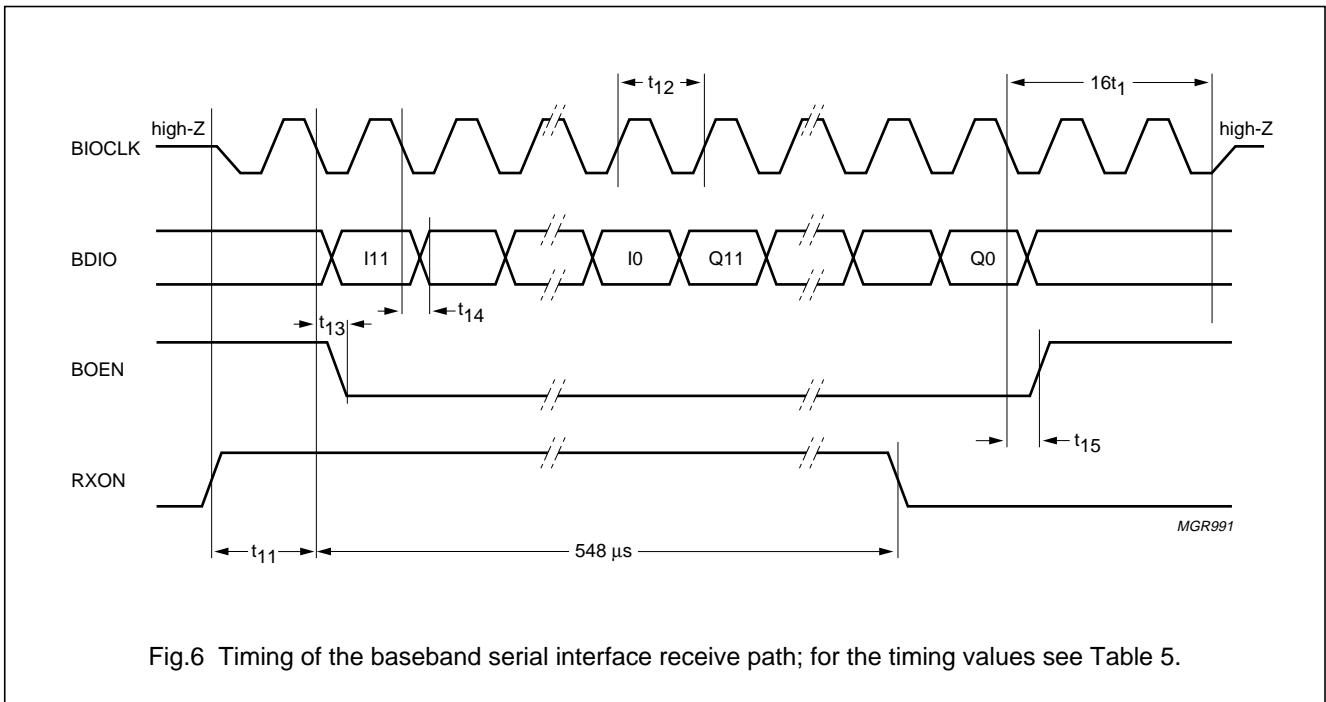


Table 5 BSI timing characteristics

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|--|--------------------------------------|---------------|------------------|-------|------|
| Master clock | | | | | |
| t_1 | MCLK cycle time | – | 76.9 | – | ns |
| t_2 | MCLK LOW time | 30 | $\frac{1}{2}t_1$ | – | ns |
| t_3 | MCLK HIGH time | 30 | $\frac{1}{2}t_1$ | – | ns |
| t_4 | RESET LOW time | $3t_1$ | – | – | ns |
| Baseband Serial Interface (BSI) transmit path (see Fig.5) | | | | | |
| t_5 | BIEN0 value | 10 | – | 511 | QB |
| t_6 | BIEN1 value | t_5 | – | 4000 | QB |
| t_7 | BIOCLK cycle time | – | $48t_1$ | – | ns |
| t_9 | data set-up time | 20 | – | – | ns |
| t_{10} | data hold time | 20 | – | – | ns |
| t_{39} | BIOCLK active after TXON rising edge | – | – | t_1 | ns |
| t_{40} | analog TX and GMSK power-up time | – | – | 17.4 | QB |
| t_{42} | ramp-up value | 0 | – | 3940 | QB |
| t_{43} | intermediate ramp value | $32 + t_{42}$ | – | 3980 | QB |
| t_{44} | ramp-down value | | | | |
| | normal mode | $32 + t_{42}$ | – | 4020 | QB |
| | double burst mode | $32 + t_{43}$ | – | 4020 | QB |

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| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|--|------|-----------------|------|------|
| Baseband Serial Interface (BSI) receive path (see Fig.6) | | | | | |
| t ₁₁ | analog power-up and filter settling time | | | | |
| | ZIF mode | – | 52 | – | μs |
| | NZIF mode | – | 26 | – | μs |
| t ₁₂ | BIOCLK cycle time | | | | |
| | ZIF mode | – | 2t ₁ | – | ns |
| | NZIF mode | – | t ₁ | – | ns |
| t ₁₃ | BOEN LOW after falling clock edge | – | – | 15 | ns |
| t ₁₄ | BIOCLK falling edge to data valid | – | – | 15 | ns |
| t ₁₅ | BOEN HIGH after falling clock edge | – | – | 15 | ns |

10 VOICE BAND CODEC

The voice band CODEC is a complete analog front-end circuit. It consists of three parts:

- The **receive path**, which converts a digital linear PCM signal to an analog signal for an earpiece, an external loudspeaker or a buzzer
- The **transmit path**, which receives an analog signal from a microphone or an auxiliary input and converts it into a digital linear PCM signal
- The digital **Audio Serial Interface (ASI)**, which connects the digital linear PCM signals of the receive and transmit paths to a digital signal processor.

Various functions and characteristics of the voice band CODEC can be selected by programming the corresponding control registers in the Control register block (see also Tables 11, 22, 23, 24 and 25).

10.1 Voice band receive path

The voice band receive path consists of the following parts:

- The receive part of the voice band signal processor
- **NOISE SHAPER**: 3rd order digital $\Sigma\Delta$ modulator, generates a bit stream at 1 MHz to drive the EARDAC
- **EARDAC**: digital-to-analog converter including low-pass filter for high frequency noise content of noise shaper
- **EARAMP**: amplifier for an earpiece
- **AUXAMP**: amplifier for an auxiliary loudspeaker
- **BUZAMP**: amplifier for a buzzer output.

Linearity of receiver equipment (to earpiece) at EARPGA = 0 dB and a volume control (VOLPGA and EARAMP or AUXAMP) of –12 dB, signal-to-total harmonic distortion ratio according to “GSM recommendation II.11.10 V.4.16.1”.

10.1.1 RXVOL

RXVOL controls the volume of the voice band receive path. In conjunction with EARAMP, AUXAMP and BUZAMP it allows a gain variation from +6 to –30 dB in 64 steps; see Table 25. RXVOL also provides a mute selection of the three outputs EARP/EARN, AUXSP and BUZ respectively. At RESET the volume is automatically set to –12 dB.

10.1.2 RXPGA

RXPGA controls the gain of the voice band receive path within a range of –24 to +12 dB in 64 steps for calibration purposes.

10.1.3 RXFILTER

RXFILTER is a digital band-pass filter with a pass band from 300 to 3400 Hz. It is realized by a programmable structure (voice band signal processor).

10.1.4 EARDAC

EARDAC is a DAC operating at a sampling frequency of 1 MHz. It converts the bitstream input to a sampled differential analog signal and low-pass filters the output signal at the same time.

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10.1.5 EARAMP

EARAMP is an amplifier, capable of driving a standard earpiece with a minimum impedance of 8 Ω in single-ended mode or 16 Ω in differential mode.

10.1.6 AUXAMP

AUXAMP is an amplifier for connection to an external loudspeaker amplifier of minimum 8 Ω (hands-free car kit).

An 'auxiliary speaker external amplifier control' output pin (AMPCTRL) can be used to switch on/off an external amplifier (hands-free car kit). The status of AMPCTRL is programmable via the Control Serial Interface; its default value is on.

10.1.7 BUZAMP

BUZAMP is an amplifier for connection to an external buzzer of minimum 8 Ω . It has the same output characteristics as the AUXAMP and can hence be used as a second auxiliary output amplifier. It is switched on/off by a dedicated control bit in the Control register block.

10.2 Voice band transmit path

The voice band transmit path consists of the following parts:

- **MICMUX**: microphone input multiplexer
- **MICADC**: $\Sigma\Delta$ analog-to-digital converter
- **DECIMATOR**: decimates the incoming bit stream from 1 MHz to 40 kHz
- **TXFILTER**: band-pass filter for the digital transmit signal and down-sampling
- **TXPGA/LIM**: fine-programmable gain for calibration, limiter
- **SidePGA**: voice band sidetone programmable gain amplifier.

Linearity of transmitter equipment, signal-to-total harmonic distortion ratio according to "GSM recommendation II.11.10 V.4.16.1".

10.2.1 MICMUX

MICMUX is used to select between a differential signal at pins MICP/MICN and a differential signal at pins AUXMICP/AUXMICN.

Values are specified for a standard electret microphone with a sensitivity of -64 ± 3 dB for high gain or for an external microphone with an amplifier sensitivity of -26 ± 3 dB (0 dB \equiv 1 V/0.1 Pa = 1 V/ μ bar; at 1 kHz).

10.2.2 MICADC

MICADC is a $\Sigma\Delta$ A/D converter which generates a 1 MHz bitstream.

10.2.3 DECIMATOR AND TXFILTER

The DECIMATOR is a digital filter, which performs a signal processing to a lower sampling rate at the output compared to the input.

The bitstream with a sampling frequency of 1 MHz is low-pass filtered and down-sampled to 40 kHz by a FIR filter.

A digital high-pass filter and a digital low-pass filter (both IIR filters) process the 14-bit input samples to achieve a band-pass with a pass band from 300 to 3400 Hz. These filters run on the on-chip voice band signal processor (see Fig.7). It's program is down-loaded into the instruction memory (IRAM) via the CSI (see Table 26).

The output of the TXFILTER is down-sampled to a sampling frequency of 8 kHz with a word length of 16 bits.

10.2.4 TXPGA

TXPGA adapts the analog signals coming from MICMUX within a range of -30 to $+6$ dB. It is designed for calibration purposes.

10.2.5 SidePGA

SidePGA loops part of the voice band transmit signal back into the receive path. There are 64 gain steps from mute to $+6$ dB.

10.3 Voice band digital circuitry

The voice band digital circuitry is responsible for converting a 16-bit PCM signal at 8 kHz sample rate to and from a 1-bit 1 MHz signal. It also contains a band-pass filter for 300 to 3400 Hz and a sidetone engine. Various volume settings are calculated inside this block. Figure 7 shows the block diagram of the voice band signal processor.

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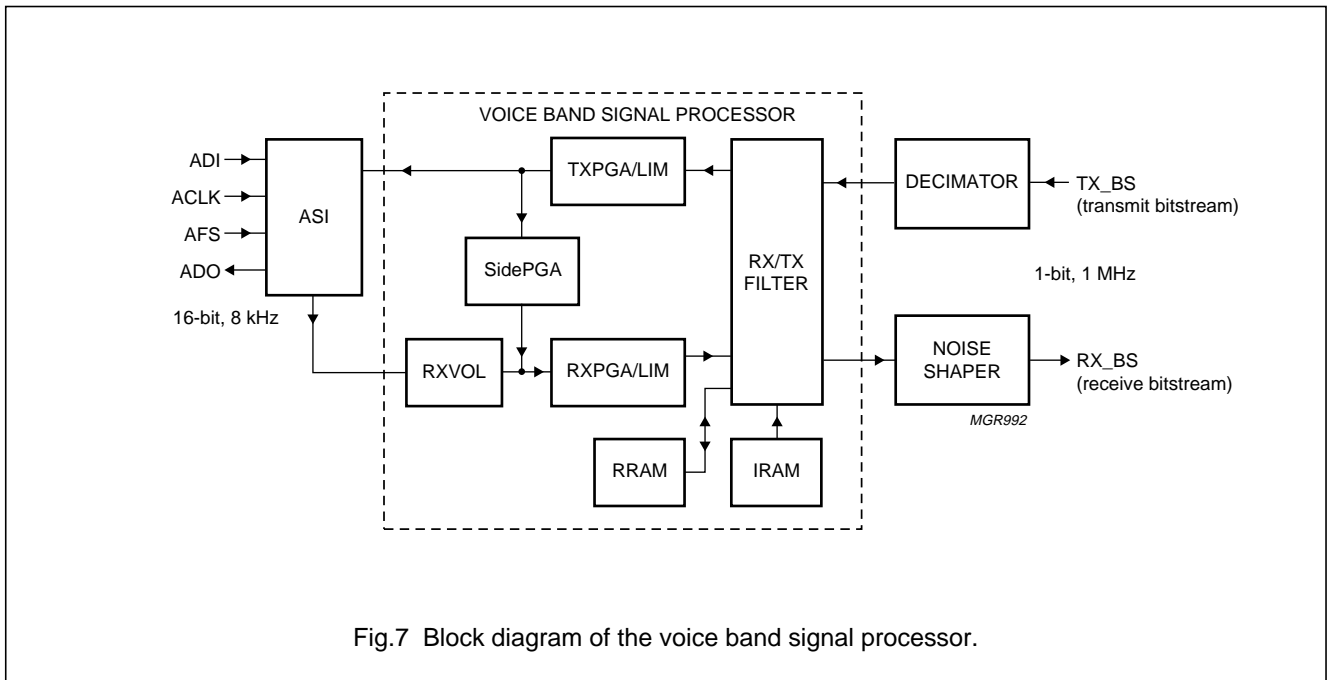


Fig.7 Block diagram of the voice band signal processor.

10.3.1 VOLUME CONTROL BLOCK

The volume control block contains the RXPGA, SidePGA, TXPGA and both limiter blocks. The possible settings can be found in the description of the CSI block. All digital volume control blocks, i.e. RXPGA, SidePGA, and TXPGA, will allow settings from +6 to -30 dB and mute in 64 steps. However, not all combinations of settings for these blocks will be meaningful. The limiter will always clip signals with overflow to the maximum or minimum allowable value.

10.3.2 AUDIO SERIAL INTERFACE (ASI) BLOCK

The ASI is the voice band serial interface which provides the connection for the exchange of PCM data in both receive and transmit directions, between the baseband digital signal processor and the PCF50732. The data is coded in 16-bit linear PCM twos complement words.

A frame start is defined by the first falling edge of ACLK after a rising AFS. This first falling edge is used to clock in the first data bit on both the baseband and the DSP device.

Data on pin ADI is clocked in (MSB first) on the falling edge of the ACLK clock. Data is clocked out (MSB first) on pin ADO on the rising edge of the ACLK clock.

Pin ADO is put in 3-state after the LSB of the transmit word, independent of the length of the AFS pulse. If the channel position 0 (see Section 10.3.2.1) is selected, then the MSB must be output directly after AFS becomes a logic 1, even if no rising edge on ACLK has been given yet.

The following modes of operation are programmable: channel position and ACLK clock mode.

10.3.2.1 Channel position mode

Depending on a programmable register value n (n = 0 to 15) one of 16 channels can be selected (see Table 22). The ASI can add a delay of 16 × n-bit clocks between the assertion of AFS and the start of the MSB of the PCM values. This delay is independently programmable for transmit and receive mode.

10.3.2.2 ACLK clock mode

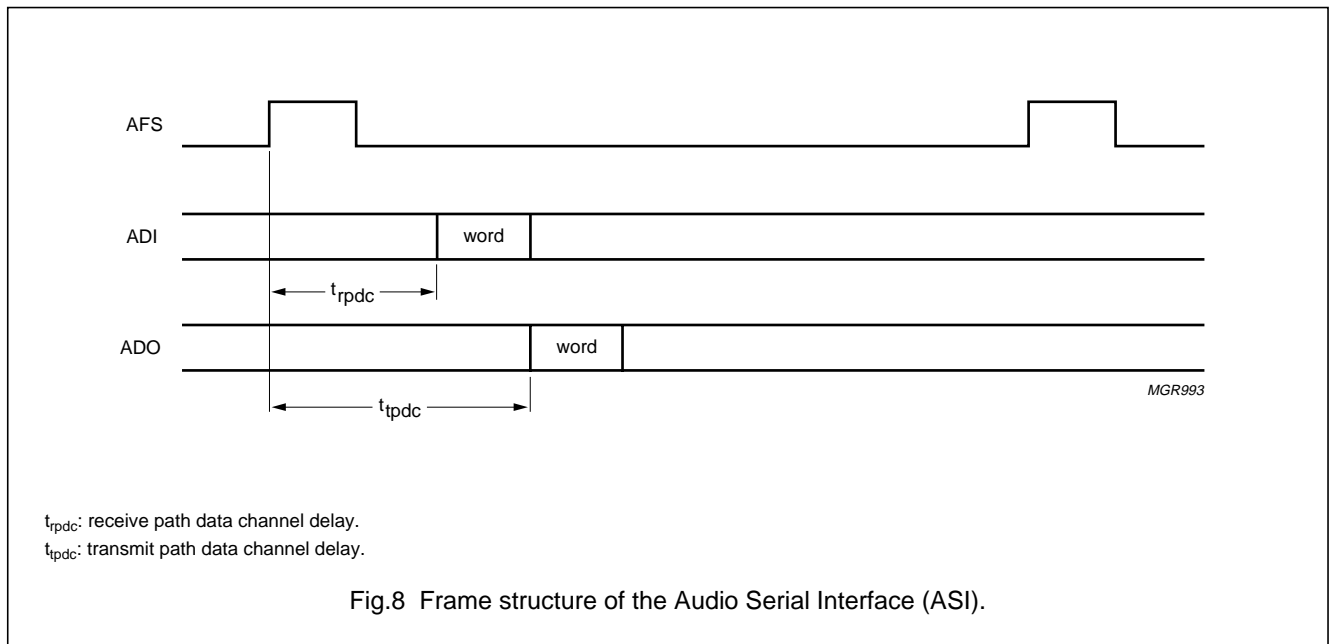
Single or double clock mode can be selected. Double clock mode implies two clock pulses per data bit and is used for communication with IOM2 compatible devices. In double clock mode data must be output on the first rising edge and be read on the last falling edge.

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Table 6 Pin connection of the audio serial interface to the PCF5087X

| PCF50732 | | PCF5087X | |
|----------|-----|----------|-----|
| PIN | I/O | PIN | I/O |
| ADI | I | DD | O |
| ADO | O | DU | I |
| ACLK | I | DCL | O |
| AFS | I | FSC | O |



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10.3.2.3 Audio Serial Interface (ASI) timing characteristics

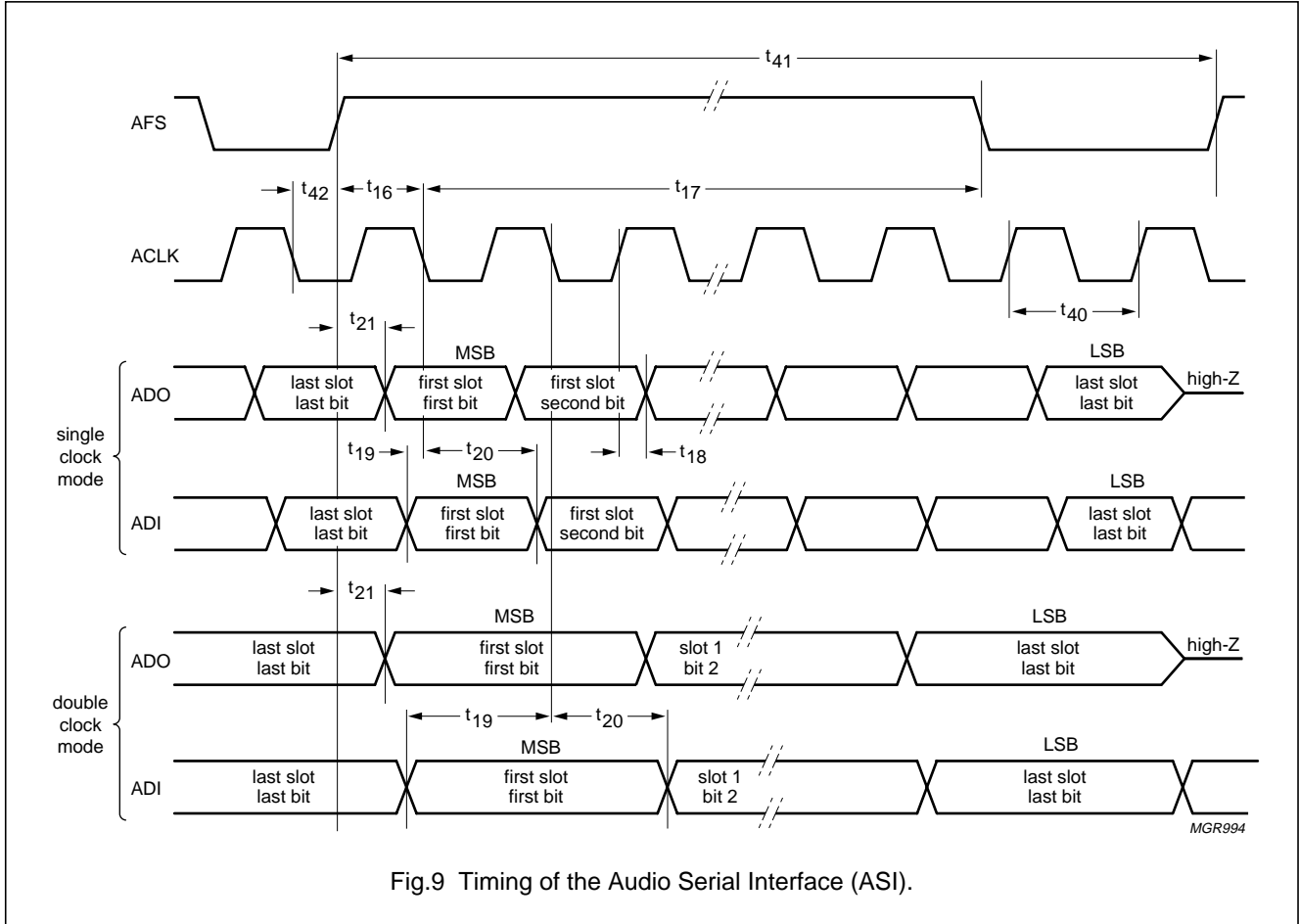


Fig.9 Timing of the Audio Serial Interface (ASI).

Table 7 ASI timing characteristics

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|----------|--|------|------|------|---------|
| t_{16} | frame sync (AFS) set-up time to falling edge of ACLK | 70 | – | – | ns |
| t_{17} | frame sync (AFS) hold time from falling edge of ACLK | 40 | – | – | ns |
| t_{18} | ACLK rising edge to data (ADO) valid | –30 | – | +30 | ns |
| t_{19} | data (ADI) set-up time to falling edge of ACLK | 50 | – | – | ns |
| t_{20} | data (ADI) hold time from falling edge of ACLK | 80 | – | – | ns |
| t_{21} | first data valid (ADO) after AFS rising edge | 0 | – | 60 | ns |
| t_{40} | ACLK period | | | | |
| | single clock mode | 0.5 | – | 7.8 | μ s |
| | double clock mode | 0.5 | – | 3.9 | μ s |
| t_{41} | AFS period | – | 125 | – | μ s |
| t_{42} | ACLK LOW before AFS rising edge | 40 | – | – | ns |

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11 AUXILIARY FUNCTIONS

The auxiliary functions part consists of three digital-to-analog converters (DACs) and a 4 input analog-to-digital converter (ADC) with a 12-bit range. The DACs are for:

- Automatic Gain Control (AGC): AUXDAC1
- Automatic Frequency Control (AFC): AUXDAC2
- Power ramping: AUXDAC3.

11.1 Automatic Gain Control (AGC): AUXDAC1

The AUXDAC1 is an 8-bit binary coded, guaranteed monotonic digital-to-analog converter.

The status of AUXDAC1 is controlled by the signal AUXST and a power-up bit in the Power control register. The signal that switches the external VCXO can also be used to control the AUXST pin of the PCF50732. The AUXDAC1 output is floating in Power-down mode (AUXST = LOW). The input MCLK is then deactivated.

When AUXST goes HIGH, AUXDAC1 is powered-up and the converted value of the corresponding register in the control register block is available at the AUXDAC1 output pin.

If a write access to the AUXDAC1 register occurs, the DAC is activated with the new content of the DAC register (see Table 14 and 15). The AUXDAC1 must be powered-up by setting the correct bit in the Power control register. At reset AUXDAC1 is powered-down.

11.2 Automatic Frequency Control (AFC): AUXDAC2

The AUXDAC2 is a 12-bit binary coded, guaranteed monotonic digital-to-analog converter. This DAC is used to control the frequency of an external master clock VCXO.

The status of AUXDAC2 is controlled by the signal AUXST and a power-up bit in the Power control register. The signal that switches the external VCXO can also be used to control the AUXST pin of the PCF50732. The AUXDAC2 output is floating in Power-down mode (AUXST = LOW). When AUXST goes HIGH, AUXDAC2 is powered-up and the converted value of the corresponding register in the control register block is available at the AUXDAC2 output pin.

The default value for AUXDAC2 is 1.1 V which corresponds to a 800H code in the AUXDAC2 register. At reset AUXDAC2 is powered on.

11.3 Power ramping: AUXDAC3

AUXDAC3 is a 10-bit binary coded digital-to-analog converter designed for power ramping purposes. AUXDAC3 is default off. The power ramping behaviour is described in Section 9.3.2.2.

11.4 Auxiliary analog-to-digital converter (AUXADC)

The AUXADC is specified for voltage and temperature measurements. It contains 4 input channels required for ΔT and ΔV measurements, as well as battery type recognition:

- ΔT : battery temperature, ambient temperature (measured across sensor)
- ΔV : peak battery voltage, battery voltage during transmit burst.

Five 12-bit registers are available in which results of auxiliary analog-to-digital conversions can be stored. Two registers are dedicated to the input AUXADC1 and one to each of AUXADC2, AUXADC3 and AUXADC4.

The AUXADC1 input can be used for battery voltage measurement. In the AUXADC1A register the voltage during a transmit time slot can be stored. The AUXADC1B register can store the voltage during other time slots. If a read request to one of these registers is executed by loading its address into the Read request register, the actual contents of the addressed register are given to the control interface and a new measurement is performed in the next appropriate time slot.

A multiplexer connects each of the AUXADC inputs to a channel of the receive ADC depending on read access to the corresponding register.

Thus an auxiliary analog-to-digital conversion is only possible, if the baseband receive section is not in use (RXON is LOW). At each read request to one of the AUXADC registers, a flag is set in the AUXADC flag register indicating that an analog-to-digital conversion is to be performed. When one of the registers AUXADC1B, AUXADC2, AUXADC3, or AUXADC4 is being read, the baseband interface verifies that RXON is LOW, indicating that no receive burst is currently active. The baseband receive path is then powered up. After the ADC settling time has elapsed (see $POST_{AUXADC}$ in Chapter 18), valid data is available and stored in the corresponding register.

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After conversion the corresponding bit in the AUXADC flag register is reset (see Table 18). If RXON is activated during an auxiliary analog-to-digital conversion cycle, the auxiliary conversion is interrupted and restarted when RXON returns LOW, indicating no receive burst activity.

The PCF50732 waits for a rising edge of TXON, and powers up the receive path. After the settling time of the ADC added to the programmed AUXADC conversion delay (in 48 MCLK cycles) has elapsed, valid data is available and stored in the AUXADC1A register.

When register AUXADC1A is read, a battery voltage measurement during a transmission burst is executed.

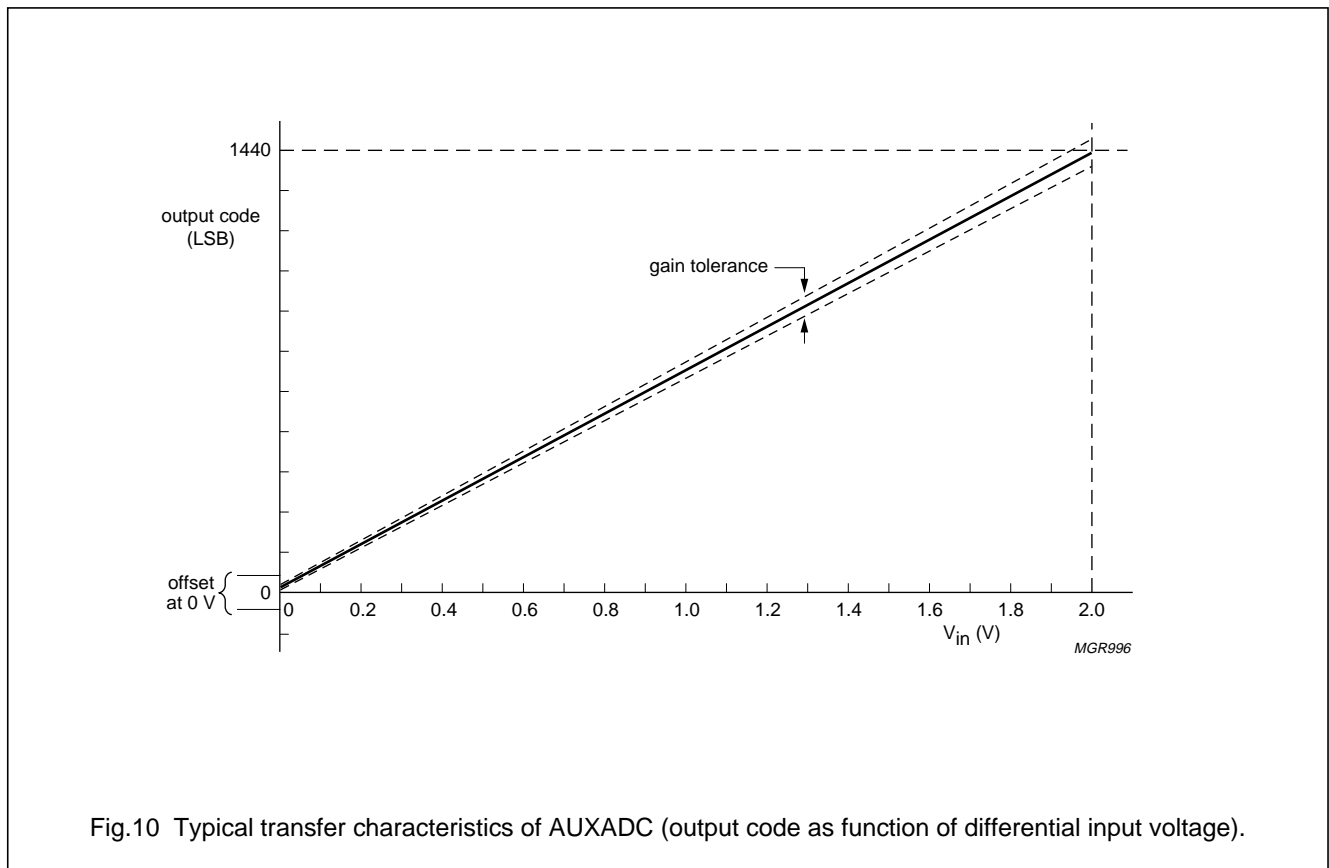


Fig.10 Typical transfer characteristics of AUXADC (output code as function of differential input voltage).

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12 CONTROL SERIAL INTERFACE (CSI)

The Control Serial Interface block is used to set and read the status bits inside the PCF50732. It is also used to read data from the auxiliary ADCs and to write data into the auxiliary DACs. Finally, the block is used to write the power ramping curve into a 64×10 -bit static RAM. It should be noted that only 48 of the 64 addresses can be accessed; see Table 2.

12.1 The serial interface

A 4-line bidirectional serial interface is used to control the circuit. It allows access to each register of the control register block (read and/or write). The 4 lines are:

- Data in (CDI)
- Data out (CDO)
- Clock (CCLK)
- Enable (CEN).

Table 8 lists the normal connections to the PCF5087X.

The data sent to or from the device is loaded in bursts framed by CEN. Clock edges and data bits are ignored until CEN goes active (LOW). Each data word consists of 21 bits that comprises a 4-bit device address, a 4-bit register address, a 12-bit data word and a dummy bit; see Table 9. The 21 bits are transmitted with MSB first.

Figure 5 shows the valid timing for data transmission on the control interface.

Data is read in from the CDI pin on the rising edge of the CCLK clock and output on CDO on the falling edge of the CCLK clock. Data is written into the registers on the rising edge of CEN.

If the device address is equal to the chip address, the programmed information on CDI (DB11 to DB00) is loaded into the addressed register (RA3 to RA0) when CEN returns inactive HIGH.

The dummy bit in front is needed for compatibility with older baseband devices.

Reading a register is accomplished by writing the address of the required register into the read request register. The next time CEN goes LOW, the requested data will be shifted out, together with the register and device address.

Table 8 Pin connection of the CSI to the PCF5087X

| PCF50732 | | PCF5087X | |
|----------|-----|----------|-----|
| PIN | I/O | PIN | I/O |
| CDI | I | RFDO | O |
| CDO | O | RFDI | I |
| CCLK | I | RFCLK | O |
| CEN | I | RFE_N2 | O |

Table 9 Bit mapping of the 21-bit words

| BIT | CONTENT | DESCRIPTION |
|----------|--------------|---|
| 00 to 03 | ADD0 to ADD3 | device address; for the PCF50732 this is '1001' (= 9 decimal) |
| 04 to 07 | RA0 to RA3 | register address |
| 08 to 19 | DB00 to DB11 | data value |
| 20 | dummy | don't care |

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12.2 Control Serial Interface (CSI) timing characteristics

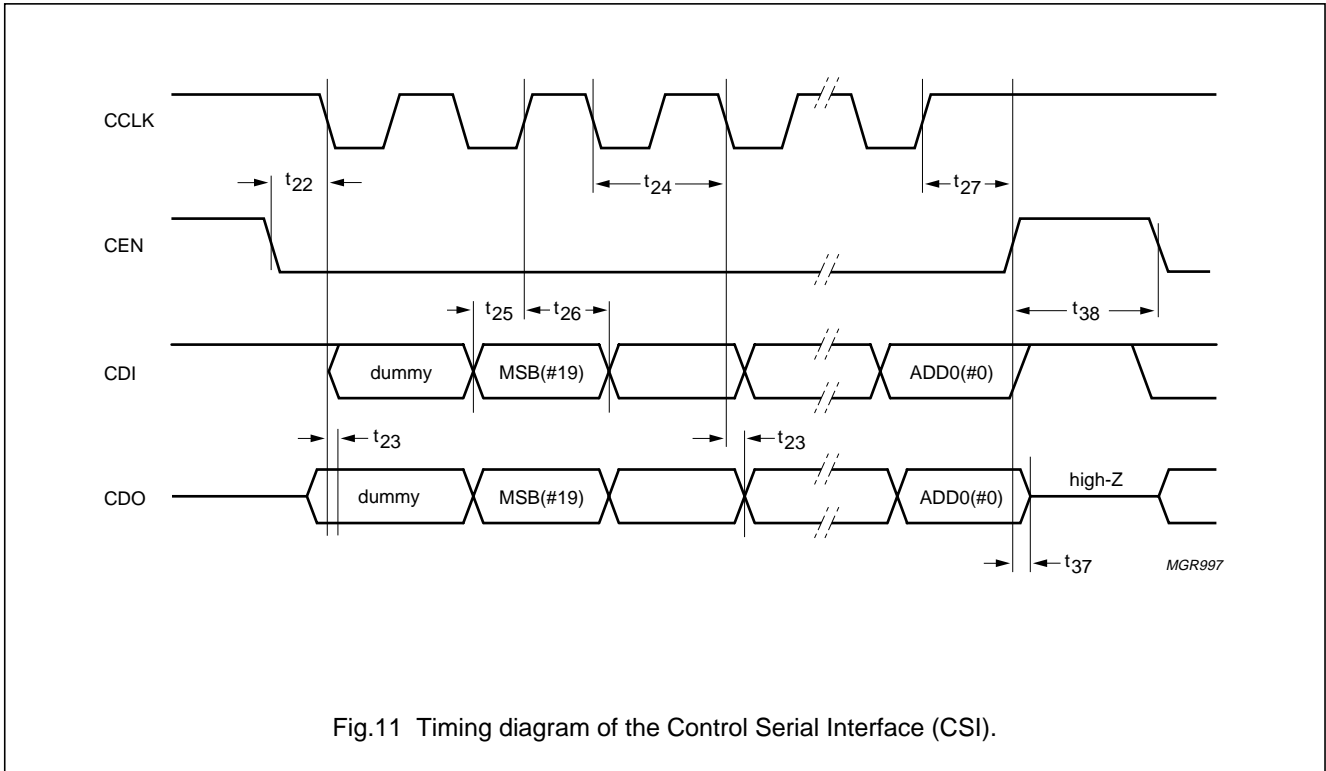


Fig.11 Timing diagram of the Control Serial Interface (CSI).

Table 10 CSI timing characteristics

For the timing diagram see Fig.11.

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|----------|---|------|------|------|
| t_{22} | CEN set-up time | 20 | – | ns |
| t_{23} | CDO data valid after falling clock edge | – | 50 | ns |
| t_{24} | CCLK cycle time | 100 | – | ns |
| t_{25} | data set-up time to rising edge of CCLK | 20 | – | ns |
| t_{26} | data hold time from rising edge of CCLK | 30 | – | ns |
| t_{27} | CEN hold time | 30 | – | ns |
| t_{37} | CDO 3-state after CEN HIGH | – | 30 | ns |
| t_{38} | CEN HIGH time | 50 | – | ns |

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12.3 Control register block

This section describes the different registers that are implemented in the PCF50732. An overview is given in Table 11. Tables 12 to 29 describe all the registers of the PCF50732.

Table 11 Control register block overview

| ADDRESS | ACCESS | REGISTER NAME |
|---------|--------|--|
| 0000 | W | Read request register |
| 0001 | R/W | AUXDAC1 (AGC) value register |
| 0010 | R/W | AUXDAC2 (AFC) value register |
| 0011 | R/W | Burst control register |
| 0100 | R/W | AUXADC control register |
| 0101 | R | AUXADC channel 1 register A (AUXADC1A); note 1 |
| 0110 | R | AUXADC channel 1 register B (AUXADC1B); note 1 |
| 0111 | R | AUXADC channel 2 register (AUXADC2); note 1 |
| 1000 | R | AUXADC channel 3 register (AUXADC3); note 1 |
| 1001 | R | AUXADC channel 4 register (AUXADC4); note 1 |
| 1010 | R/W | Voice band control register |
| 1011 | R/W | Voice band volume register |
| 1100 | R/W | Power control register |
| 1101 | R/W | RAM interface register |
| 1110 | R/W | Baseband receive control register |
| 1111 | R/W | Test mode register; note 2 |

Notes

1. See description in Section 11.4.
2. Do not use this register.

12.3.1 READ REQUEST REGISTER

Table 12 Read request register

X = don't care during a read/or write access.

| ADDRESS | REGISTER NAME | VALUE | | | | | | | | | | | |
|---------|-----------------------|-------|----|---|---|----|----|----|----|----|----|----|----|
| | | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0000 | Read request register | X | X | X | X | r3 | r2 | r1 | r0 | s3 | s2 | s1 | s0 |

Table 13 Read request registers value description

| VALUE OF | SYMBOL | DESCRIPTION |
|-----------------------|----------|---|
| Read request register | r3 to r0 | Address of the register to be read. |
| | s3 to s0 | Subaddress that might be needed. The subaddress bits are right aligned, meaning that the subaddress always starts with bit 's0' (LSB); e.g. in case of two subaddress bits, 's1' and 's0' are used. |

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12.3.2 AUXDAC1 (AGC) VALUE AND AUXDAC2 (AFC) VALUE REGISTERS

Table 14 Registers overview

X = don't care during a read/or write access.

| ADDR. | REGISTER NAME | VALUE | | | | | | | | | | | |
|-------|------------------------------|-------|-----|----|----|----|----|----|----|----|----|----|----|
| | | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0001 | AUXDAC1 (AGC) value register | X | X | X | X | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| 0010 | AUXDAC2 (AFC) value register | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |

Table 15 AUXDAC1 (AGC) value and AUXDAC2 (AFC) value registers value description

| VALUE OF | SYMBOL | DESCRIPTION |
|------------------------------|-----------|---|
| AUXDAC1 (AGC) value register | b7 to b0 | input value to the 8-bit AUXDAC1 (fed directly into the DAC); the default value is 85H |
| AUXDAC2 (AFC) value register | b11 to b0 | input value to the 8-bit AUXDAC2 (fed directly into the DAC); the default value is 800H |

12.3.3 BURST CONTROL REGISTER

The Burst control register controls the timing of the transmit burst (TX-burst). The 'lo'-registers contain the lower 8 bits, the 'hi'-registers the upper 4 bits of a 12-bit delay value. Therefore, each register has a programmable range from 0 to 4095. Not all combinations of values might make sense e.g. ramp-down before ramp-up.

Table 16 Burst control register (address 001 and subaddresses)

X = don't care during a read/or write access.

| FUNCTION | SUBADDRESS | | | | VALUE | | | | | | | |
|---|------------|------------|-------------------|-------------------|-------|----|----|----|-----|-----|----|----|
| | 11 (s3) | 10 (s2) | 9 (s1) | 8 (s0) | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RU-lo | 0 | 0 | 0 | 0 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| RU-hi | 0 | 0 | 0 | 1 | X | X | X | X | b11 | b10 | b9 | b8 |
| RM-lo | 0 | 0 | 1 | 0 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| RM-hi | 0 | 0 | 1 | 1 | X | X | X | X | b11 | b10 | b9 | b8 |
| RD-lo | 0 | 1 | 0 | 0 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| RD-hi | 0 | 1 | 0 | 1 | X | X | X | X | b11 | b10 | b9 | b8 |
| BIEN0-lo | 0 | 1 | 1 | 0 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| BIEN0-hi | 0 | 1 | 1 | 1 | X | X | X | X | b11 | b10 | b9 | b8 |
| BIEN1-lo | 1 | 0 | 0 | 0 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| BIEN1-hi | 1 | 0 | 0 | 1 | X | X | X | X | b11 | b10 | b9 | b8 |
| Single/double burst mode ⁽¹⁾ | 1 | 0 | 1 | 0 | X | X | X | X | X | X | X | b0 |
| DAC3 burst RAM address ⁽¹⁾ | 1 | 0 | 1 | 1 | X | X | a5 | a4 | a3 | a2 | a1 | a0 |
| DAC3 burst RAM data ⁽¹⁾ | 1 | 1 | d9 ⁽²⁾ | d8 ⁽²⁾ | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |

Notes

1. The programming is described in Section 9.3.2.2.
2. The subaddress positions bit 9 (s1) and bit 8 (s0) do not apply to the DAC3 burst RAM data register.

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Table 17 Burst control registers value description

| VALUE OF | DESCRIPTION |
|----------|---|
| RU | Value RU, consisting of RU-lo (least significant byte) and RU-hi (most significant byte), is the delay measured in quarterbits ($\frac{1}{12}$ MCLK) between the rising edge of TXON and the start of the ramp-up on AUXDAC3. After this delay, the first 16 values of the AUXDAC3 RAM are sent to AUXDAC3. Shifting out is done at $\frac{1}{24}$ MCLK. |
| RM | Value RM, consisting of RM-lo (least significant byte) and RM-hi (most significant byte), is the delay measured in quarterbits between the rising edge of TXON and the start of the intermediate ramp in a double burst ramp. The RM value is only used in multislot mode. RM must be greater than RU + 32. |
| RD | Value RD, consisting of RD-lo (least significant byte) and RD-hi (most significant byte), is the delay measured in quarterbits between the rising edge of TXON and the start of the ramp-down on AUXDAC3. RD must be greater than RU + 32, or in case of multislot mode, greater than RM + 32. |
| BIEN0 | Value BIEN0, consisting of BIEN0-lo (least significant byte) and BIEN0-hi (most significant byte), is the delay measured in quarterbits between the rising edge of TXON and the falling edge of BIEN. |
| BIEN1 | Value BIEN1, consisting of BIEN1-lo (least significant byte) and BIEN1-hi (most significant byte), is the delay measured in quarterbits between the rising edge of TXON and the rising edge of BIEN. BIEN1 must be greater than BIEN0. |

12.3.4 AUXADC CONTROL REGISTER

Table 18 AUXADC control register (address 0100 and subaddresses)

X = don't care during a read/or write access.

| FUNCTION | SUBADDRESS | | | VALUE | | | | | | | | |
|--|------------|------------|-----------|--|------|------|--------|--------|--------|--------|---------|---------|
| | 11 (s2) | 10 (s1) | 9 (s0) | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AUXADC conversion delay value register | 0 | 0 | 0 | X | X | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| AUXADC flag register | 0 | 0 | 1 | X | Qoff | loff | auxoff | flag 4 | flag 3 | flag 2 | flag 1B | flag 1A |
| AUXADC offset value register | 1 | 0 | 0 | 9-bit signed offset compensation value | | | | | | | | |
| I channel offset value register | 1 | 0 | 1 | 9-bit signed offset compensation value | | | | | | | | |
| Q channel offset value register | 1 | 1 | 0 | 9-bit signed offset compensation value | | | | | | | | |
| Offset trigger register | 1 | 1 | 1 | X | X | X | X | X | X | Q-off | I-off | Aux |

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Table 19 AUXADC control registers value description

| VALUE OF | DESCRIPTION |
|--|--|
| AUXADC conversion delay value register | The 7-bit value (b6 to b0) denotes the delay measured in 48MCLK units between the rising edge of TXON and the conversion on AUXADC1A. The normal power-on settling time is added to this delay. Default value is 0. |
| AUXADC flag register | The AUXADC flag register returns the status of the AUXADC converters. If an auxiliary A/D conversion is pending, the flag of the corresponding AUXADC will be set. The flag register is read only. |
| AUXADC offset value register | <p>The offset value registers contain signed 9-bit offset compensation values. These values are subtracted automatically from all baseband receive (BBRX) and AUXADC measurements to compensate for offset errors. The compensation values can be read and written and have a default value of 0. It can also be measured by the device itself.</p> <p>A write to the Offset trigger register will trigger an offset measurement for each of the channels (Q-off, I-off or AUXADC) selected.</p> <p>Offset measurements are special cases of AUXADC measurements and are done sequentially. Each calibration measurement takes approximately 100 μs. The Offset trigger register is write only.</p> |
| I channel offset value register | |
| Q channel offset value register | |
| Offset trigger register | |

12.3.5 AUXADC REGISTERS

Table 20 AUXADC registers overview

| ADDR. | REGISTER NAME | VALUE | | | | | | | | | | | |
|-------|--|-------|-----|----|----|----|----|----|----|----|----|----|----|
| | | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0101 | AUXADC channel 1 register A (AUXADC1A) | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| 0110 | AUXADC channel 1 register B (AUXADC1B) | | | | | | | | | | | | |
| 0111 | AUXADC channel 2 register (AUXADC2) | | | | | | | | | | | | |
| 1000 | AUXADC channel 3 register (AUXADC3) | | | | | | | | | | | | |
| 1001 | AUXADC channel 4 register (AUXADC4) | | | | | | | | | | | | |

Table 21 AUXADC registers value description

| VALUE OF | DESCRIPTION |
|----------|--|
| AUXADC1A | 12-bit result of the A/D conversion on AUXADC channel 1, measured during a transmission burst |
| AUXADC1B | 12-bit result of the A/D conversion on AUXADC channel 1, measured outside a transmission burst |
| AUXADC2 | 12-bit result of the A/D conversion on AUXADC channel 2 |
| AUXADC3 | 12-bit result of the A/D conversion on AUXADC channel 3 |
| AUXADC4 | 12-bit result of the A/D conversion on AUXADC channel 4 |

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12.3.6 VOICE BAND CONTROL REGISTER

The Voice band control register is used to control the following functionality of the voice band CODEC:

- Analog input source: microphone (MICAMP) or auxiliary (AUXMIC) input
- Analog output device: earphone (EARAMP), auxiliary (AUXAMP) or buzzer (BUZAMP) output; this register allows individual control of all three output amplifiers
- EARAMP output mode: single-ended (EARP) or differential (EARN/EARP). This selects the input source for the EARAMP-N amplifier. In single-ended mode EARAMP-N will be at V_{ref} , in differential mode it will carry the output signal
- General purpose output pin: AMPCTRL
- Receive and transmit path delay values
- ASI clock mode
- TX gain boost (MICHI).

Table 22 Voice band control register (address 1010 and subaddresses)

X = don't care during a read/or write access.

| FUNCTION | SUBADDRESS | | | VALUE | | | | | | | | FUNCTION SETTING | | | | |
|----------------------------|------------|------------|-----------|------------|---|---|---|---|---|---|---|---------------------------------|------------------------|---|---|-----------------------|
| | 11 (s2) | 10 (s1) | 9 (s0) | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | | 0 | | | |
| Select input source | 0 | 0 | 0 | don't care | | | | | | | | 0 | MICAMP (default) | | | |
| | | | | | | | | | | | | 1 | AUXMIC | | | |
| Select output amplifier | 0 | 0 | 1 | don't care | | | | | | | | X | X | X | 0 | EARAMP-P off |
| | | | | | | | | | | | | X | X | X | 1 | EARAMP-P on (default) |
| | | | | | | | | | | | | X | X | 0 | X | EARAMP-N off |
| | | | | | | | | | | | | X | X | 1 | X | EARAMP-N on (default) |
| | | | | | | | | | | | | X | 0 | X | X | AUXAMP off (default) |
| | | | | | | | | | | | | X | 1 | X | X | AUXAMP on |
| | | | | | | | | | | | | 0 | X | X | X | BUZAMP off (default) |
| | | | | | | | | | | | | 1 | X | X | X | BUZAMP on |
| EARAMP output mode | 0 | 1 | 0 | don't care | | | | | | | | 0 | single-ended | | | |
| | | | | | | | | | | | | 1 | differential (default) | | | |
| AMPCTRL pin polarity | 0 | 1 | 1 | don't care | | | | | | | | 0 | active LOW | | | |
| | | | | | | | | | | | | 1 | active HIGH (default) | | | |
| Receive path data channel | 1 | 0 | 0 | don't care | | | | d | c | b | a | 4-bit delay value (default = 0) | | | | |
| Transmit path data channel | 1 | 0 | 1 | | | | | d | c | b | a | | | | | |
| ASI clock mode | 1 | 1 | 0 | don't care | | | | | | | | 0 | single clock (default) | | | |
| | | | | | | | | | | | | 1 | double clock | | | |
| TX gain boost (MICHI) | 1 | 1 | 1 | don't care | | | | | | | | 0 | 7 dB | | | |
| | | | | | | | | | | | | 1 | 35 dB (default) | | | |

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12.3.7 VOICE BAND VOLUME REGISTER

Voice band gain settings can be independently programmed for: TXPGA, RXPGA, RXVOL and SidePGA.

Table 23 Voice band volume register (address 1011 and subaddresses)

X = don't care during a read/or write access.

| FUNCTION | SUBADDRESS | | | VALUE | | | | | | | | | SELECTED RANGE | DEFAULT SETTING |
|------------------------|------------|---------|--------|-------|---|---|-----|-----|----|------|------|-----|----------------|------------------------|
| | 11 (s2) | 10 (s1) | 9 (s0) | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| TXPGA gain | 0 | 0 | 0 | X | X | X | a | b | c | d | e | f | -24 to +12 dB | 0 dB |
| RXPGA gain | 0 | 0 | 1 | X | X | X | a | b | c | d | e | f | | |
| RXVOL gain | 0 | 1 | 0 | X | X | X | a | b | c | d | e | f | -30 to +6 dB | -12 dB |
| SidePGA gain | 0 | 1 | 1 | X | X | X | a | b | c | d | e | f | | mute |
| Band gap setting level | 1 | 0 | 0 | X | X | X | a | b | c | X | X | X | -100 to +75 mV | 0 mV offset |
| Experimental bits | 1 | 0 | 1 | X | X | X | dir | pll | dc | vbch | hclk | bgb | - | pll on, all others off |

Table 24 Voice band volume registers value description

| VALUE | REMARKS | DESCRIPTION |
|------------------------|-------------------------|---|
| TXPGA gain | microphone calibration | TXPGA and RXPGA settings use the 6-bit binary fixed point value 'ab.cdef' as a multiplier for each PCM-sample. This results in a control range of +12 to -24 dB. See note 1a. |
| RXPGA gain | earphone calibration | |
| RXVOL gain | customer volume control | RXVOL and SidePGA settings use the 6-bit binary fixed point value 'a.bcdef' as a multiplier for each PCM-sample. This results in a control range of +6 to -30 dB (and mute). See note 1b. |
| SidePGA gain | - | |
| Experimental bits | - | <ul style="list-style-type: none"> • dir: bypass clock buffer • pll: clock optimizer • dc: bypass clock capacitor • vbch: voice band chopping • hclk: 26 MHz master clock input • bgb: band gap boost |
| Band gap setting level | | do not use |

Note

- Possible gain settings are listed in Table 25 or can be calculated using the following formulae ('n' is an integer that represents the value that is written into the register; n = 0 to 63):

a) RXPGA and TXPGA: $\text{gain} = 20 \times \log \frac{n}{16}$; add 6.02 dB to each gain for RXPGA and TXPGA settings.

b) RXVOL and SidePGA: $\text{gain} = 20 \times \log \frac{n}{32}$

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12.3.7.1 Possible gain selections for voice band blocks: RXPGA, TXPGA, RXVOL and SidePGA

Table 25 shows the possible gain selections for the voice band blocks RXPGA, TXPGA, RXVOL and SidePGA. It should be noted that not all possible combinations of these volume settings are meaningful; setting RXPGA, SidePGA and RXVOL to maximum will result in clipping of the output signal.

Table 25 Gain selections

| BINARY CODE | GAIN (dB) | | BINARY CODE | GAIN (dB) | |
|-------------|-------------|---------------|-------------|-------------|---------------|
| | RXPGA/TXPGA | RXVOL/SidePGA | | RXPGA/TXPGA | RXVOL/SidePGA |
| 111111 | 11.88 | 5.88 | 011111 | 5.72 | -0.28 |
| 111110 | 11.74 | 5.74 | 011110 | 5.44 | -0.56 |
| 111101 | 11.60 | 5.60 | 011101 | 5.14 | -0.86 |
| 111100 | 11.46 | 5.46 | 011100 | 4.84 | -1.16 |
| 111011 | 11.31 | 5.31 | 011011 | 4.52 | -1.48 |
| 111010 | 11.17 | 5.17 | 011010 | 4.20 | -1.80 |
| 111001 | 11.01 | 5.01 | 011001 | 3.86 | -2.14 |
| 111000 | 10.86 | 4.86 | 011000 | 3.50 | -2.50 |
| 110111 | 10.70 | 4.70 | 010111 | 3.13 | -2.87 |
| 110110 | 10.54 | 4.54 | 010110 | 2.75 | -3.25 |
| 110101 | 10.38 | 4.38 | 010101 | 2.34 | -3.66 |
| 110100 | 10.22 | 4.22 | 010100 | 1.92 | -4.08 |
| 110011 | 10.05 | 4.05 | 010011 | 1.47 | -4.53 |
| 110010 | 9.88 | 3.88 | 010010 | 1.00 | -5.00 |
| 110001 | 9.70 | 3.70 | 010001 | 0.51 | -5.49 |
| 110000 | 9.52 | 3.52 | 010000 | 0.00 | -6.02 |
| 101111 | 9.34 | 3.34 | 001111 | -0.58 | -6.58 |
| 101110 | 9.15 | 3.15 | 001110 | -1.18 | -7.18 |
| 101101 | 8.96 | 2.96 | 001101 | -1.82 | -7.82 |
| 101100 | 8.77 | 2.77 | 001100 | -2.52 | -8.52 |
| 101011 | 8.57 | 2.57 | 001011 | -3.28 | -9.28 |
| 101010 | 8.36 | 2.36 | 001010 | -4.10 | -10.10 |
| 101001 | 8.15 | 2.15 | 001001 | -5.02 | -11.02 |
| 101000 | 7.94 | 1.94 | 001000 | -6.04 | -12.04 |
| 100111 | 7.72 | 1.72 | 000111 | -7.20 | -13.20 |
| 100110 | 7.49 | 1.49 | 000110 | -8.54 | -14.54 |
| 100101 | 7.26 | 1.26 | 000101 | -10.12 | -16.12 |
| 100100 | 7.02 | 1.02 | 000100 | -12.06 | -18.06 |
| 100011 | 6.78 | 0.78 | 000011 | -14.56 | -20.56 |
| 100010 | 6.53 | 0.53 | 000010 | -18.08 | -24.08 |
| 100001 | 6.27 | 0.27 | 000001 | -24.10 | -30.10 |
| 100000 | 6.00 | 0.00 | 000000 | off | off |

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12.3.8 POWER CONTROL REGISTER

The Power control register is used to control power-up and power-down of the different sections of the device. Changing the power status is accomplished by addressing the device as shown in Table 26 and setting bit 0 (= a) according to the required state:

a = 0 → power-down

a = 1 → power-up.

Setting the baseband RX or TX flag is functionally equivalent to setting RXON or TXON respectively (logical OR function). The CSI is also accessible when the band gap is powered down. Therefore no reset is required to power-up after total power-down.

Table 26 Power control register (address 1100 and subaddresses)

| FUNCTION | SUBADDRESS | | | | VALUE | | | | | | | | DEFAULT | | |
|---------------------|------------|---------|--------|--------|------------|---|---|---|---|---|---|---|---------|--------|-----|
| | 11 (s3) | 10 (s2) | 9 (s1) | 8 (s0) | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | VALUE | STATUS | |
| AUXDAC1 | 0 | 0 | 0 | 1 | don't care | | | | | | | | a | 0 | off |
| AUXDAC2 | 0 | 0 | 1 | 0 | | | | | | | | | a | 1 | on |
| AUXDAC3 | 0 | 0 | 1 | 1 | | | | | | | | | a | 0 | off |
| Voice band transmit | 0 | 1 | 0 | 0 | | | | | | | | | a | 0 | off |
| Voice band receive | 0 | 1 | 0 | 1 | | | | | | | | | a | 0 | off |
| V _{ref} | 0 | 1 | 1 | 0 | | | | | | | | | a | 1 | on |
| Baseband receive | 1 | 0 | 0 | 0 | | | | | | | | | a | 0 | off |
| Baseband transmit | 1 | 0 | 0 | 1 | | | | | | | | | a | 0 | off |
| Complete device | 1 | 1 | 1 | 1 | | | | | | | | | a | 1 | on |

12.3.9 RAM INTERFACE REGISTER

The RAM interface register is a general purpose communication channel between the serial interface CSI and the voice band signal processor. None of the processor registers have default values.

The Voice band control register is used to communicate with the voice band signal processor. Register functions with subaddress '00' to '11' can be used to program the Instruction RAM (IRAM) when the voice band processor is not running, i.e. when voice band receive and transmit sections are both powered down.

The IRAM registers are used to write into the voice band instruction RAM.

Normal operation is to write an address into the VSP instruction RAM program counter and write low and high bytes of the 16-bit instructions into their respective locations. No auto-increment is foreseen, i.e. the address register must be updated by the user. Writing to the IRAM is only possible when voice band transmit and receive sections are both powered off. If this is not the case write actions are ignored.

Reading back from the IRAM is not straightforward due to the need for an extra clock pulse when accessing RAMs; when reading back the contents of RAM locations 1, 2, 3 and 4 actual output is 'undefined' as 1, 2, 3, etc.

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Table 27 RAM interface register (address 1101 and subaddresses)

X = don't care during a read/or write access.

| FUNCTION | SUBADDRESS | | VALUE | | | | | | | | | |
|-------------------------------------|------------|---------|-------|----|----|----|----|----|----|----|----|----|
| | 11 (s1) | 10 (s0) | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VSP instruction RAM data low-byte | 0 | 0 | X | X | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| VSP instruction RAM data high-byte | 0 | 1 | X | X | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| VSP instruction RAM program counter | 1 | 0 | X | a8 | a7 | a6 | a5 | a4 | a3 | a2 | a1 | a0 |
| VSP interface register | 1 | 1 | x9 | x8 | x7 | x6 | x5 | x4 | x3 | x2 | x1 | x0 |

12.3.10 BASEBAND RECEIVE CONTROL REGISTER

Normal bandwidth refers to an input signal bandwidth of 100 kHz used for ZIF operation, double bandwidth is 200 kHz used for NZIF operation. Normal sampling refers to a sampling rate of 1/2MCLK, double sampling refers to sampling at MCLK.

Table 28 Baseband receive control register (address 1110)

| FUNCTION | VALUE | | | | | | | | | | | OUTPUT RATE | |
|---|-------|----|------------|---|---|---|---|---|---|---|---|-------------|------------------------|
| | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | | 0 |
| Normal bandwidth; normal sampling (ZIF) double sampling; note 2 | 0 | 0 | don't care | | | | | | | | 0 | 0 | 271 kHz ⁽¹⁾ |
| | 0 | 0 | don't care | | | | | | | | 0 | 1 | 135 kHz |
| Double bandwidth; normal sampling (NZIF) double sampling | 0 | 0 | don't care | | | | | | | | 1 | 0 | 542 kHz |
| | 0 | 0 | don't care | | | | | | | | 1 | 1 | 271 kHz |

Notes

- 1. Default value.
- 2. Do not use this function.

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12.3.11 TEST MODE REGISTER

Only test mode 8 (TM8) is available to the end user. It is used to mark baseband-I (BB-I) samples with a logic 0 and baseband-Q (BB-Q) samples with a logic 1 on the LSB of the 12-bit value.

Table 29 Test mode register (address 1111)

| TEST MODE | FUNCTION | VALUE | | | | | | | | | | | |
|-----------|---|------------|----|---|---|---|---|---|---|---|---|---|---|
| | | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NM | normal mode (default) | | | | | | | | | 0 | 0 | 0 | 0 |
| TM1 | baseband transmit (BBTX) I digital | | | | | | | | | 0 | 0 | 0 | 1 |
| TM2 | baseband receive (BBRX) digital | | | | | | | | | 0 | 0 | 1 | 0 |
| TM3 | voice band (VB) loop digital | | | | | | | | | 0 | 0 | 1 | 1 |
| TM4 | voice band transmit/receive (VBTX/RX) digital | | | | | | | | | 0 | 1 | 0 | 0 |
| TM5 | CSI | | | | | | | | | 0 | 1 | 0 | 1 |
| TM6 | baseband (BB) DACs | don't care | | | | | | | | 0 | 1 | 1 | 0 |
| TM7 | voice band receive (VBRX) DAC current sources | | | | | | | | | 0 | 1 | 1 | 1 |
| TM8 | I/Q marking test | | | | | | | | | 1 | 0 | 0 | 0 |
| TM9 | voice band signal processor test mode | | | | | | | | | 1 | 0 | 0 | 1 |
| TM10 | VSP signature output mode | | | | | | | | | 1 | 0 | 1 | 0 |
| TM11 | MCLK input reflected on BDIO | | | | | | | | | 1 | 0 | 1 | 1 |
| TM12 | baseband bitstream output | | | | | | | | | 1 | 1 | 0 | 0 |

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13 VOICE BAND SIGNAL PROCESSOR (VSP)

13.1 Hardware description

The VSP used in the PCF50732 is a 30-bit fixed point VSP with separate data and instruction areas. The data path consists of two guard bits, 16 data bits before and 12 data bits behind the binary point for a total of 30 bits. Twos complement notation is used inside the data path. Intermediate results from calculations are stored in a 64×30 -bit wide data RAM. Data and Programmable Gain Amplifier (PGA) settings are read in via 7 input ports and written back into 3 output ports.

The instruction path uses a 16-bit format with the 4 MSBs designating the opcode and the trailing 12 bits used to describe the operand. The VSP has 12 major instructions; some instructions use two opcodes (operation codes). The addressing range is 9 bits wide, allowing for a total of 512 instructions, which is more than adequate for the filter types it is intended to calculate. Some room is available for Built-In Self Test (BIST). The ALU consists of a 30-bit subtractor, a 30-bit adder and a 30×16 -bit 'modified booth'-type parallel multiplier.

The VSP's accumulator has built-in overrange checking and will limit values to their minimum (in case of underflow) or maximum (in case of overflow) value.

The VSP engine is designed to operate at 4 MIPS on a 8 kHz PCM signal.

All instructions take one clock-cycle to complete. It should be noted that since the noise shaper operates at a sample rate of 32 kHz and the voice band filter operates at a sample rate of 40 kHz it is necessary to transfer 4 samples to the receive output and to read 5 samples from transmit input for each frame.

No buffering is foreseen for these samples, which means that the VSP program is responsible for proper spacing in time of the input- and output samples. Failure to ensure proper spacing will result in heavily distorted signals.

Synchronization to the 8 kHz frame-sync signals AFS is also done under program control. The VSP program must ensure that noise shaper and FIR filter are properly reset before actual operation is started.

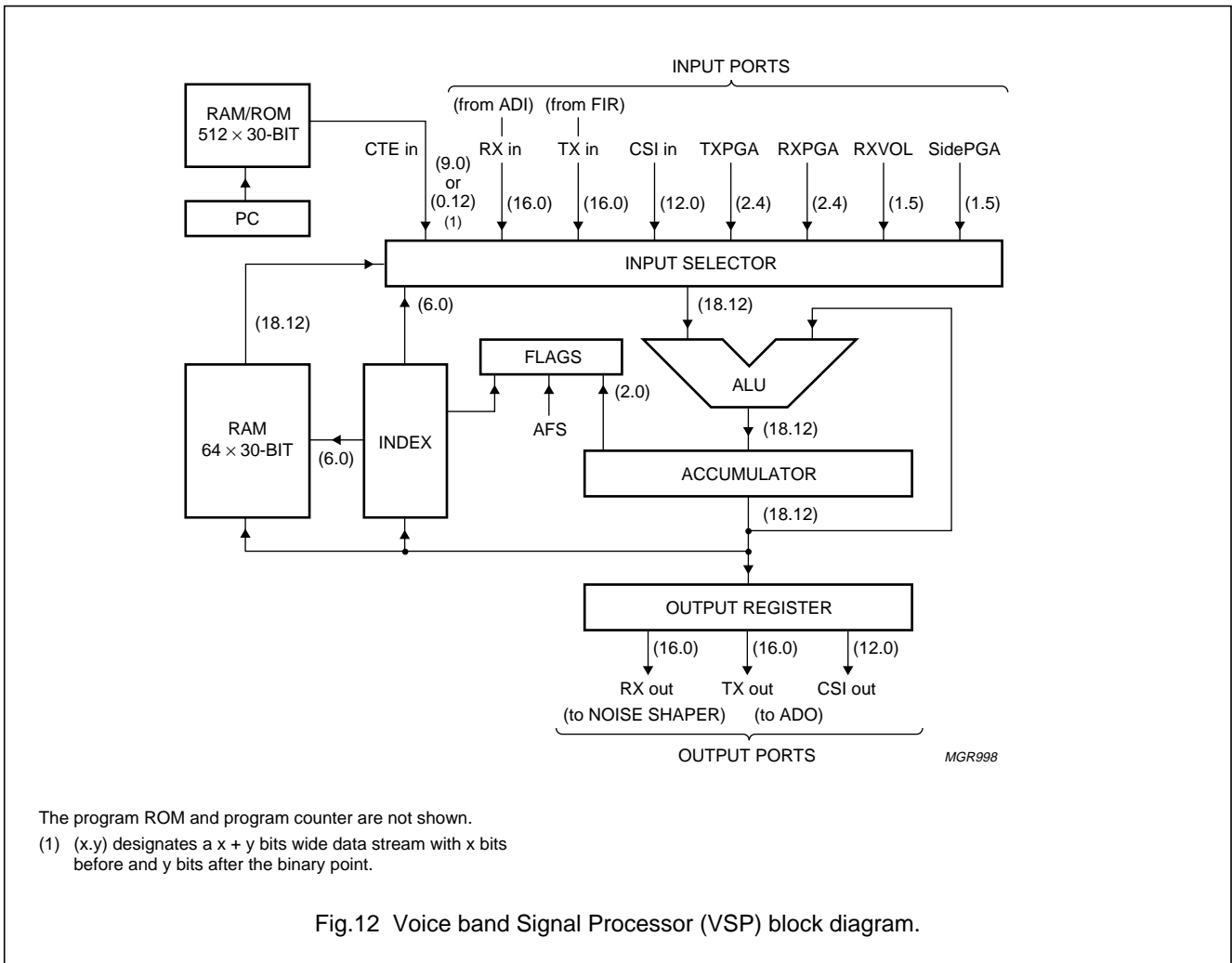
A VSP-emulator and a VSP-assembler have been written in order to facilitate program development. The assembler generates a stream of 16-bit words that need to be loaded into the instruction RAM. This is done by repeated writes to the VSP control register. The sequence would be as follows:

1. Write address into the VSP instruction RAM program counter register
2. Write the upper 8 bits into the VSP instruction RAM data high-byte register
3. Write the lower 8 bits into the VSP instruction RAM data low-byte register.

This sequence should be repeated until the VSP is fully programmed. Programming can only be done when the VSP is not active. The VSP program counter will be set to location 0 and operation starts after enabling voice band transmit or voice band receive. See also the CSI description in Chapter 12.

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13.2 VSP assembler language

The stack for return addresses is only one entry deep which means that nesting of subroutines is not possible.

Table 30 VSP instruction set

X = don't care during a read/or write access. For the description of the bit symbols see notes 1 to 8.

| MNEMONIC | INSTRUCTION | I3 | I2 | I1 | I0 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|-------------------------------|----|----|----|----|-----|-----|-----|----|----|----|----|----|----|----|----|----|
| LDA | Load accumulator | 0 | 0 | 0 | m3 | c11 | c10 | c9 | c8 | c7 | c6 | c5 | c4 | c3 | c2 | c1 | c0 |
| | | | | | m3 | m2 | m1 | m0 | d8 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| STO | Store accumulator | 0 | 0 | 1 | 0 | m2 | m1 | m0 | X | X | X | d5 | d4 | d3 | d2 | d1 | d0 |
| RTN | Return from subroutine | 0 | 0 | 1 | 1 | X | X | X | X | X | X | X | X | X | X | X | X |
| ADD | Add to accumulator | 0 | 1 | 0 | m3 | c11 | c10 | c9 | c8 | c7 | c6 | c5 | c4 | c3 | c2 | c1 | c0 |
| | | | | | m3 | m2 | m1 | m0 | d8 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| SUB | Subtract from accumulator | 0 | 1 | 1 | m3 | c11 | c10 | c9 | c8 | c7 | c6 | c5 | c4 | c3 | c2 | c1 | c0 |
| | | | | | m3 | m2 | m1 | m0 | d8 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| MUL | Multiply with accumulator | 1 | 0 | 0 | m3 | c11 | c10 | c9 | c8 | c7 | c6 | c5 | c4 | c3 | c2 | c1 | c0 |
| | | | | | m3 | m2 | m1 | m0 | d8 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| JMFS | Jump if flag set | 1 | 0 | 1 | 0 | f2 | f1 | f0 | a8 | a7 | a6 | a5 | a4 | a3 | a2 | a1 | a0 |
| JMFC | Jump if flag clear | 1 | 0 | 1 | 1 | f2 | f1 | f0 | a8 | a7 | a6 | a5 | a4 | a3 | a2 | a1 | a0 |
| JSFS | Jump subroutine if flag set | 1 | 1 | 0 | 0 | f2 | f1 | f0 | a8 | a7 | a6 | a5 | a4 | a3 | a2 | a1 | a0 |
| JSFC | Jump subroutine if flag clear | 1 | 1 | 0 | 1 | f2 | f1 | f0 | a8 | a7 | a6 | a5 | a4 | a3 | a2 | a1 | a0 |
| STF | Set/clear flag | 1 | 1 | 1 | 0 | f2 | f1 | f0 | X | X | X | X | X | X | X | X | d0 |
| IDX | Index operations | 1 | 1 | 1 | 1 | im2 | im1 | im0 | X | X | X | i5 | i4 | i3 | i2 | i1 | i0 |

Notes

1. c11 to c0 denotes a 12-bit twos complement coefficient between -1 and +1.
2. m3 to m0 denotes a 4-bit instruction mode descriptor.
3. f2 to f0 denotes a 3-bit flag descriptor.
4. a8 to a0 denotes a 9-bit address.
5. i5 to i0 denotes a 6-bit index register value.
6. a8 to a0 denotes a 9-bit address.
7. X is a don't care bit.
8. im2 to im0 denotes a 3-bit instruction mode descriptor for the IDX operator.

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Table 31 Mode descriptions

| m3 | m2 | m1 | m0 | MODE NAME | OPERAND | RANGE | ASSEMBLER SHORT HAND |
|----|--|----|----|------------------|-----------------------|----------------------|----------------------|
| 0 | 0 | 0 | 0 | register | R(d5 to d0) | register 0 to 63 | r |
| 0 | 0 | 0 | 1 | register indexed | R((d5 to d0) + index) | register 0 to 63 | i |
| 0 | 0 | 1 | 0 | port | P(d2 to d0) | ports 0 to 7 | p |
| 0 | 0 | 1 | 1 | small integer | d8 to d0 | -256 to +255; note 1 | s |
| 0 | 1 | 0 | 0 | index | index | 0 to 63; note 1 | i |
| 1 | bits 11 to 0 form a 12-bit twos complement coefficient between -1 and +1 | | | | | | c |

Note

- Value range in increments of 1.

Table 32 Index mode descriptions

| im2 | im1 | im0 | NAME | OPERAND |
|-----|-----|-----|-----------|----------------------------|
| 0 | 0 | 0 | store | index = d5 to d0 |
| 0 | 0 | 1 | increment | index = (d5 to d0) + index |
| 1 | 0 | 0 | accu | index = accu |

Table 33 Flag descriptions

| f2 | f1 | f0 | NAME | DESCRIPTION | REMARKS | TYPE |
|----|----|----|------|-----------------------|---|--------|
| 0 | 0 | 0 | ALW | always set | flag is clear in VSP test mode; used to initiate BIST | system |
| 0 | 0 | 1 | INZ | set if index not zero | used to implement loops | |
| 0 | 1 | 0 | EQ0 | set if accu is all 0 | | |
| 0 | 1 | 1 | EQ1 | set if accu is all 1 | | |
| 1 | 0 | 0 | SYNC | PCM sync signal | used to sync VSP to external PCM signal | |
| 1 | 0 | 1 | A | user flag A | | user |
| 1 | 1 | 0 | B | user flag B | | |
| 1 | 1 | 1 | C | user flag C | used to reset noise shaper and FIR filter | |

Table 34 Port descriptions

| P2 | P1 | P0 | NAME | DIRECTION | RANGE |
|----|----|----|---------------|------------|----------------------------|
| 0 | 0 | 0 | Receive (RX) | read/write | -32768 to +32767 (16 bits) |
| 0 | 0 | 1 | Transmit (TX) | read/write | -32768 to +32767 (16 bits) |
| 0 | 1 | 0 | CSI | read/write | -2048 to +2047 (12 bits) |
| 0 | 1 | 1 | ZERO | read | fixed 0 |
| 1 | 0 | 0 | TXPGA | read | 0 to 63 (-24 to +12 dB) |
| 1 | 0 | 1 | RXPGA | read | 0 to 63 (-24 to +12 dB) |
| 1 | 1 | 0 | RXVOL | read | 0 to 63 (-20 to +6 dB) |
| 1 | 1 | 1 | SidePGA | read | 0 to 63 (-20 to +6 dB) |

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13.3 Descriptions of the VSP instruction set

13.3.1 CONVENTIONS

In the descriptions of the VSP instruction set:

- A = the 30-bit accumulator
- I = the 6-bit index register
- r.a. = a 6-bit register address
- p.n. = a 3-bit port number (address)
- coeff = a 12-bit coefficient

- f.l. = a 3-bit flag descriptor
- addr = a 9-bit address
- stack = a one entry deep return address stack
- PC = a 9-bit program counter
- o.a. = the 9-bit old address
- s.i. = small integer
- X = don't care during a read/or write access.

13.3.2 LDA INSTRUCTION

The LDA (Load accumulator) instruction is used to load data into the VSP's accumulator. Flags affected are EQ0 and EQ1.

Table 35 LDA instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER | NAME |
|----|----|----|----|-------------|----|---|---------------|---|---|------------------|---|---|-------------|---|-----------|-----------------|------------------|-----------------------|
| 0 | 0 | 0 | 1 | coefficient | | | | | | | | | | | coeff → A | LDA c <coeff> | load coefficient | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | register address | | | | | | R(r.a.) → A | LDA r <r.a.> | load register |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | X | register address | | | | | | R(r.a. + I) → A | LDA i <r.a.> | load register indexed |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | X | X | X | X | X | X | port number | | | P(p.n.) → A | LDA p <p.n.> | load port |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | small integer | | | | | | | | | s.i. → A | LDA s <s.i.> | load integer |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | I → A | LDA x | load index |

13.3.3 STO INSTRUCTION

The STO (Store accumulator) instruction is used to store data into register RAM or output ports. No flags are affected.

Table 36 STO instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER | NAME |
|----|----|----|----|----|----|---|---|---|---|------------------|---|---|-------------|---|---|-----------------|--------------|------------------------|
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | X | X | X | register address | | | | | | A → R(r.a.) | STO r <r.a.> | store register |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | X | X | X | register address | | | | | | A → R(r.a. + I) | STO i <r.a.> | store register indexed |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | X | X | X | X | X | X | port number | | | A → P(p.n.) | STO p <p.n.> | store port |

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13.3.4 ADD INSTRUCTION

The ADD (Add to accumulator) instruction is used to add data to the VSP's accumulator. Flags affected are EQ0 and EQ1.

Table 37 ADD instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER | NAME |
|----|----|----|----|-------------|----|---|---------------|---|---|------------------|---|---|-------------|---|----------------------------------|--|-----------------|----------------------|
| 0 | 1 | 0 | 1 | coefficient | | | | | | | | | | | $A + \text{coeff} \rightarrow A$ | ADD c <coeff> | add coefficient | |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | X | X | X | register address | | | | | | $A + R(\text{r.a.}) \rightarrow A$ | ADD r <r.a.> | add register |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | X | X | X | register address | | | | | | $A + R(\text{r.a.} + I) \rightarrow A$ | ADD i <r.a.> | add register indexed |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | X | X | X | X | X | X | port number | | | $A + P(\text{p.n.}) \rightarrow A$ | ADD p <p.n.> | add port |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | small integer | | | | | | | | | $A + \text{s.i.} \rightarrow A$ | ADD s <s.i.> | add integer |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | $A + I \rightarrow A$ | ADD x | add index |

13.3.5 SUB INSTRUCTION

The SUB (Subtract from accumulator) instruction is used to subtract data from the VSP's accumulator. Flags affected are EQ0 and EQ1.

Table 38 SUB instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER | NAME |
|----|----|----|----|-------------|----|---|---------------|---|---|------------------|---|---|-------------|---|----------------------------------|--|----------------------|---------------------------|
| 0 | 1 | 1 | 1 | coefficient | | | | | | | | | | | $A - \text{coeff} \rightarrow A$ | SUB c <coeff> | subtract coefficient | |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | X | X | X | register address | | | | | | $A - R(\text{r.a.}) \rightarrow A$ | SUB r <r.a.> | subtract register |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | X | X | X | register address | | | | | | $A - R(\text{r.a.} + I) \rightarrow A$ | SUB i <r.a.> | subtract register indexed |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | X | X | X | X | X | X | port number | | | $A - P(\text{p.n.}) \rightarrow A$ | SUB p <p.n.> | subtract port |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | small integer | | | | | | | | | $A - \text{s.i.} \rightarrow A$ | SUB s <s.i.> | subtract integer |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | $A - I \rightarrow A$ | SUB x | subtract index |

13.3.6 MUL INSTRUCTION

The MUL (Multiply with accumulator) instruction is used to multiply data with the VSP's accumulator. Flags affected are EQ0 and EQ1. The second operand of the multiplication is restricted to 16-bit; e.g. R(r.a.).

Table 39 MUL instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER | NAME |
|----|----|----|----|-------------|----|---|---------------|---|---|------------------|---|---|-------------|---|---------------------------------------|---|----------------------|---------------------------|
| 1 | 0 | 0 | 1 | coefficient | | | | | | | | | | | $A \times \text{coeff} \rightarrow A$ | MUL c <coeff> | multiply coefficient | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | register address | | | | | | $A \times R(\text{r.a.}) \rightarrow A$ | MUL r <r.a.> | multiply register |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | X | register address | | | | | | $A \times R(\text{r.a.} + I) \rightarrow A$ | MUL i <r.a.> | multiply register indexed |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | X | X | X | X | X | X | port number | | | $A \times P(\text{p.n.}) \rightarrow A$ | MUL p <p.n.> | multiply port |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | small integer | | | | | | | | | $A \times \text{s.i.} \rightarrow A$ | MUL s <s.i.> | multiply integer |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | $A \times I \rightarrow A$ | MUL x | multiply index |

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13.3.7 JMFS INSTRUCTION

The JMFS (Jump if flag set) is used for conditional jumps. The jump is carried out when the flag is set, otherwise the PC is simply incremented.

Table 40 JMFS instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER |
|----|----|----|----|------|----|---|---------|---|---|---|---|---|---|---|-------------|--------------------|-----------|
| 1 | 0 | 1 | 0 | flag | | | address | | | | | | | | <addr> → PC | JMFS <f.l.> <addr> | |

13.3.8 JMFC INSTRUCTION

The JMFC (Jump if flag clear) is used for conditional jumps. The jump is carried out when the flag is clear, otherwise the PC is incremented.

Table 41 JMFC instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER |
|----|----|----|----|------|----|---|---------|---|---|---|---|---|---|---|-------------|--------------------|-----------|
| 1 | 0 | 1 | 1 | flag | | | address | | | | | | | | <addr> → PC | JMFC <f.l.> <addr> | |

13.3.9 JSFS INSTRUCTION

The JSFS (Jump subroutine if flag set) is used for conditional call to a subroutine. The jump is carried out when the flag is set, otherwise the PC is incremented. Note that the return stack is just one entry deep, so nesting of subroutines is not allowed.

Table 42 JSFS instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER |
|----|----|----|----|------|----|---|---------|---|---|---|---|---|---|---|------------------------------|--------------------|-----------|
| 1 | 1 | 1 | 0 | flag | | | address | | | | | | | | <o.a> → stack <addr> → PC | JSFS <f.l.> <addr> | |

13.3.10 JSFC INSTRUCTION

The JSFC (Jump subroutine if flag clear) is used for conditional jumps to a subroutine. The jump is carried out when the flag is clear, otherwise the PC is incremented. It should be noted that the return stack is just one entry deep, so nesting of subroutines is not allowed.

Table 43 JSFC instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER |
|----|----|----|----|------|----|---|---------|---|---|---|---|---|---|---|------------------------------|--------------------|-----------|
| 1 | 1 | 1 | 1 | flag | | | address | | | | | | | | <o.a> → stack <addr> → PC | JSFC <f.l.> <addr> | |

13.3.11 RTN INSTRUCTION

The RTN (Return from subroutine) is used to return from a subroutine.

Table 44 RTN instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|------------|-----------|
| 0 | 0 | 1 | 1 | X | X | X | X | X | X | X | X | X | X | X | X | stack → PC | RTN |

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13.3.12 STF INSTRUCTION

The STF (Set/clear flag) instruction is used to set or clear the user flags A, B or C. System flags cannot be set or reset under program control.

Table 45 STF instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER |
|----|----|----|----|------|----|---|---|---|---|---|---|---|---|---|-------|------------------|--------------------|
| 1 | 1 | 0 | 0 | flag | | | X | X | X | X | X | X | X | X | value | <value> → <f.l.> | STF <f.l.> <value> |

13.3.13 IDX INSTRUCTION

The IDX (Index operations) instruction is used to store and increment/decrement index values. It should be noted that additions to the index register is done in modulo 64. A 'decrement index register by one' could therefore be programmed as 'IDX + 63'. The 'IDX A' instruction loads the 6 bits to the left of the binary point into the index register, i.e. it stores the integer part modulo 64 into I.

Table 46 IDX instruction

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OPERATION | ASSEMBLER |
|----|----|----|----|----|----|---|---|---|---|-------|---|---|---|---|-----------------|---------------|-----------|
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | X | X | X | value | | | | | <value> → I | IDX = <value> | |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | X | X | X | value | | | | | I + <value> → I | IDX + <value> | |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | A → I | IDX A |

13.4 The assembler/emulator

A 2-pass assembler and an emulator was made to assist with the development of VSP programs. The software programs are written in 'C' and currently run under NT, HPUNIX and LINUX operating systems. The assembler reads assembler source files and produces a log file, sets of VHDL or Verilog stimuli and an output file containing CSI instructions that, when loaded, will load the executable into the VSP RAM.

Requirements for the assembler source code are:

- One instruction or pseudo instruction (see Table 47) per line
- No empty lines
- A maximum of 512 instructions
- Operation always starts at instruction 0.

Table 47 Assembler pseudo instructions

| MNEMONIC | INSTRUCTION | DEFINITION |
|----------|---------------------------------|---|
| . label | {<.>< ><label>} | Defines a location inside the source code. Is usually used as an argument to JMF/JSF instructions. |
| define | {<define>< ><label> < ><value>} | Defines a variable and assigns a value to it. These variables can then be referenced in the assembler instructions. |
| include | {<include>< ><file name>} | Reads in another source code file and then continues with the current file. |
| -- | {<-->< ><comment>} | Defines a comment; the rest of the line is skipped. |

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14 LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|-----------|--|------|----------------|------|
| V_{DD} | supply voltage | -0.5 | +3.3 | V |
| I_{DD} | supply current | - | 30 | mA |
| I_{I1} | DC current into any pin; except EARP/EARN, AUXSP and BUZ | -10 | +10 | mA |
| I_{I2} | DC current into pins EARP/EARN, AUXSP and BUZ | -100 | +100 | mA |
| V_I | input voltages on all inputs | -0.5 | $V_{DD} + 0.5$ | V |
| P_{tot} | total power dissipation | - | 800 | mW |
| T_{amb} | operating ambient temperature | -40 | +85 | °C |
| T_{stg} | storage temperature | -65 | +150 | °C |

15 THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|---------------|---|-------------|-------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 80 | K/W |

16 DC CHARACTERISTICS $T_{amb} = -40$ to $+85$ °C; $V_{SS} = 0$ V (ground pins must be interconnected externally); $V_{DDA} \geq V_{DDD}$; $V_{DDA(bb)} = V_{DDA(vb)} = V_{DDA(vbo)} = V_{DDA(ref)} = V_{DDA} = 2.5$ to 2.75 V (supply pins must be interconnected externally); all voltages with respect to V_{SS} unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|---------------------------|--|--------------|---------|--------------|---------|
| $I_{stb(tot)}$ | total standby current | | - | 10 | - | μ A |
| P_{av} | average power consumption | $V_{DDD} = 1.5$ V; $V_{DDA} = 2.7$ V; without load on audio outputs EARP, EARN, AUXSP and BUZ | - | 15 | - | mW |
| Digital power supply: V_{DDD} | | | | | | |
| V_{DDD} | digital supply voltage | | 1.0 | 1.5 | 2.75 | V |
| Digital inputs: CCLK, CEN, CDI, TXON, RXON, AUXST, ADI, AFS, ACLK and RESET | | | | | | |
| V_{IL} | LOW-level input voltage | | 0.0 | - | $0.3V_{DDD}$ | V |
| V_{IH} | HIGH-level input voltage | | $0.7V_{DDD}$ | - | V_{DDD} | V |
| I_{LI} | input leakage current | | - | ± 1 | - | μ A |
| Digital outputs: BIEN, BOEN, ADO and AMPCTRL | | | | | | |
| V_{OL} | LOW-level output voltage | $I_{sink} = 1.5$ mA | - | - | $0.2V_{DDD}$ | V |
| V_{OH} | HIGH-level output voltage | $I_{source} = 1.5$ mA | $0.7V_{DDD}$ | - | - | V |
| Digital output: BIOCLK | | | | | | |
| V_{OL} | LOW-level output voltage | $I_{sink} = 1.5$ mA | - | - | $0.2V_{DDD}$ | V |
| V_{OH} | HIGH-level output voltage | $I_{source} = 1.5$ mA | $0.7V_{DDD}$ | - | - | V |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---------------------------|---|--------------|--------------|--------------|---------------|
| Digital bidirectional pins: CDO and BDIO | | | | | | |
| V_{IL} | LOW-level input voltage | | 0.0 | – | $0.3V_{DDD}$ | V |
| V_{IH} | HIGH-level input voltage | | $0.7V_{DDD}$ | – | V_{DDD} | V |
| I_{LI} | input leakage current | | – | ± 1 | – | μA |
| V_{OL} | LOW-level output voltage | $I_{\text{sink}} = 1.5 \text{ mA}$ | – | – | $0.2V_{DDD}$ | V |
| V_{OH} | HIGH-level output voltage | $I_{\text{source}} = 1.5 \text{ mA}$ | $0.7V_{DDD}$ | – | – | V |
| Low-swing clock input: MCLK | | | | | | |
| I_{LI} | input leakage current | | – | ± 1 | – | μA |
| Analog power supplies: $V_{DDA(bb)}$, $V_{DDA(vb)}$, $V_{DDA(vbo)}$ and $V_{DDA(ref)}$ | | | | | | |
| V_{DDA} | analog supply voltage | | 2.5 | 2.7 | 2.75 | V |
| I_{DDA} | analog supply current | $V_{DDD} = 1.5 \text{ V};$ $V_{DDA} = 2.7 \text{ V};$ RXON active | – | 3.5 | – | mA |
| Analog reference pin: V_{ref} | | | | | | |
| V_{ref} | DC reference level | no external load | – | 1.25 | – | V |
| $I_{I(ref)}$ | input source/sink current | | – | 0.1 | – | μA |
| Analog output pins: IP, IN, QP and QN | | | | | | |
| $V_{bias(TXIQ)}$ | DC bias level | | 1.175 | 1.25 | 1.325 | V |
| Analog input pins: MICP and MICN | | | | | | |
| $V_{ref(MIC)}$ | DC input reference level | | – | $0.5V_{ref}$ | – | V |
| Analog input pins: AUXMICP and AUXMICN | | | | | | |
| $V_{ref(AUXMIC)}$ | DC input reference level | | – | $0.5V_{ref}$ | – | V |
| Analog output pins: EARP and EARN | | | | | | |
| $V_{bias(EAR)}$ | DC bias level | | – | V_{ref} | – | V |
| Analog output pin: AUXSP | | | | | | |
| $V_{bias(AUX)}$ | DC bias level | | – | V_{ref} | – | V |
| Analog output pin: BUZ | | | | | | |
| $V_{bias(BUZ)}$ | DC bias level | | – | V_{ref} | – | V |

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17 AC CHARACTERISTICS

$V_{DD} = 1.0$ to 2.75 V; $V_{DDA} = 2.5$ to 2.75 V; $T_{amb} = -40$ to $+85$ °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|-----------------------------|--|------|------|-------------|------------|
| f_{clk} | master clock frequency | | – | 13.0 | – | MHz |
| Digital input pins: CCLK, CEN, CDI, TXON, RXON, AUXST, ADI, AFS, ACLK and RESET | | | | | | |
| C_i | input capacitance | | – | 5.0 | – | pF |
| Digital output pins: BIOCLK, BIEN, BOEN, ADO and AMPCTRL | | | | | | |
| t_{dLHO} | output rise time | output load = 10 pF | – | 10 | – | ns |
| t_{dHLO} | output fall delay | output load = 10 pF | – | 10 | – | ns |
| Digital bidirectional pins: CDO and BDIO | | | | | | |
| C_i | input capacitance | | – | 5.0 | – | pF |
| t_{dLHO} | output rise time | output load = 20 pF | – | 10 | – | ns |
| t_{dHLO} | output fall delay | output load = 20 pF | – | 10 | – | ns |
| Low-swing clock input: MCLK | | | | | | |
| V_{MCLK} | input amplitude | note 1 | 0.1 | – | $0.5V_{DD}$ | V |
| δ_{MCLK} | duty cycle | | 40 | – | 60 | % |
| Analog output pins: IP, IN, QP and QN | | | | | | |
| $t_{st(TXIQ)}$ | output settling time | output load = 10 pF // 10 k Ω , to 1 LSB, for 0.8 to 2.2 V | – | 9.6 | – | μ s |
| $R_{o(TXIQ)}$ | output resistance | $f < 100$ kHz | – | 105 | – | Ω |
| Analog input pins: IP, IN, QP and QN | | | | | | |
| $R_{i(RXIQ)}$ | input resistance | differential | 200 | – | – | k Ω |
| $C_{i(RXIQ)}$ | input capacitance | | – | 5 | – | pF |
| Analog input pins: AUXADC1, AUXADC2, AUXADC3 and AUXADC4 | | | | | | |
| $R_{i(AUXADC)}$ | input resistance | | – | 1 | – | M Ω |
| Analog input pins: MICP and MICN | | | | | | |
| $R_{i(eq)(MIC)}$ | equivalent input resistance | differential | 200 | 220 | 320 | k Ω |
| Analog input pin: AUXMICP and AUXMICN | | | | | | |
| $R_{i(eq)(AUXMIC)}$ | equivalent input resistance | | 200 | 220 | – | k Ω |
| Analog output pins: EARP and EARN | | | | | | |
| $R_{o(EARAMP)}$ | output resistance | $f = 1$ kHz | 0 | – | 1 | Ω |
| Analog output pin: AUXSP | | | | | | |
| $R_{o(AUXAMP)}$ | output resistance | $f = 1$ kHz | 0 | – | 1 | Ω |
| Analog output pin: BUZ | | | | | | |
| $R_{o(BUZ)}$ | output resistance | $f = 1$ kHz | 0 | – | 1 | Ω |

Note

1. Input MCLK is internally AC coupled; the signal must not go below V_{SS} or above V_{DD} .

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18 FUNCTIONAL CHARACTERISTICS**18.1 Baseband transmit (BSI to TXI/Q)**

$V_{DDA} = 2.5$ to 2.75 V; $T_{amb} = -40$ to $+85$ °C.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---------------------------|---|--|----------------|---------|----------------|---------|
| RES _{TXIQ} | resolution of TX DACs | | – | 10 | – | bit |
| S/N _{TXIQ} | signal-to-noise TX DACs | | – | 55 | – | dB |
| FSIN _{TXIQ} | input sampling frequency | | – | 270.833 | – | kHz |
| V _{O(TXIQ)(p-p)} | output signal amplitude (peak-to-peak value) | note 1 | 0.9 | 1.0 | 1.1 | V |
| V _{DC(TXIQ)} | output DC level | | 1.15 | 1.25 | 1.35 | V |
| AMAT _{TXIQ} | output amplitude matching between I and Q TX paths | note 1 | –1.75 –0.15 | – | +1.75 +0.15 | % dB |
| VOFS _{TXIQ} | differential DC offset voltage between IP/IN or QP/QN | note 1 | –4.5 | – | +4.5 | mV |
| FRESP _{TXIQ} | frequency response of random output signal | f = 0 to 100 kHz | –3 | – | – | dB |
| | | f = 200 kHz | – | – | –30 | dB |
| | | f = 250 kHz | – | – | –33 | dB |
| | | f = 400 kHz | – | – | –60 | dB |
| | | f = 600 kHz | – | – | –70 | dB |
| | | f = 1200 kHz | – | – | –70 | dB |
| | | f > 1800 kHz | – | – | –70 | dB |
| MPEI _{TXIQ} | maximum phase effect instance | note 2 | – | 22 | – | µs |
| AGD _{TXIQ} | absolute group delay | note 1 | – | 10 | – | µs |
| GDL _{TXIQ} | group delay linearity | measured at full-scale; 10 kHz < f < 100 kHz; load: 10 pF // 10 kΩ | – | 100 | – | ns |
| GDMAT _{TXIQ} | group delay matching of I and Q TX paths | | – | – | 40 | ns |
| PMAT _{TXIQ} | phase matching of I and Q TX paths | note 1 | – | 0.5 | – | deg |
| PTERMS _{TXIQ} | RMS phase trajectory error | random input pattern; notes 1 and 3 | – | 0.5 | 0.8 | deg |
| PTEPEAK _{TXIQ} | peak phase trajectory error | | – | 1.5 | 3.0 | deg |

Notes

1. Measured at full-scale; load: 10 pF // 10 kΩ; f = 67 kHz.
2. Not tested. Defined between the rising edge of BIOCLK which latches a data bit at BDIO to its corresponding maximum phase change on the analog outputs ITX and QTX.
3. Not tested.

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18.2 Baseband receive (RXI/Q to BSI)

$V_{DDA} = 2.5$ to 2.75 V; $T_{amb} = -40$ to $+85$ °C; all values valid for ZIF and NZIF modes.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|--|--|-------|---------|-------|------|
| RES _{RXIQ} | resolution | I and Q word length at BSI | – | 12 | – | bit |
| S/N _{RXIQ} | signal to noise ratio | | – | 66 | – | dB |
| V _{ICM(RXIQ)} | input common mode voltage | (IP + IN)/2; (QP + QN)/2; referred to V _{SS} | 1.0 | 1.25 | 1.5 | V |
| V _{IDM(RXIQ)} | input differential voltage | (IP – IN); (QP – QN) | –1.5 | – | 1.5 | V |
| FSIN _{RXIQ} | input sampling frequency | Baseband receive control register = 0X | – | 6.5 | – | MHz |
| | | Baseband receive control register = 1X | – | 13 | – | MHz |
| FSOUT _{RXIQ} | output sample rate | Baseband receive control register = 00 or 11 | – | 270.833 | – | kHz |
| | | Baseband receive control register = 10 | – | 541.667 | – | kHz |
| FRESP _{RXIQ} | frequency response | Baseband receive control register = 0X; note 1 | | | | |
| | | f = 0 to 70 kHz; V _{IDM(RXIQ)} = 150 mV (p-p) | –0.8 | 0 | +0.3 | dB |
| | | f = 90 kHz; V _{IDM(RXIQ)} = 150 mV (p-p) | – | –3.5 | – | dB |
| | | f = 100 kHz; V _{IDM(RXIQ)} = 150 mV (p-p) | – | –5.5 | – | dB |
| | | f = 200 kHz; V _{IDM(RXIQ)} = 150 mV (p-p) | – | – | –35 | dB |
| | | f > 220 kHz; V _{IDM(RXIQ)} = 150 mV (p-p) | – | – | –45 | dB |
| | | Baseband receive control register = 1X; note 1 and 2 | | | | |
| | | f = 0 to 140 kHz; V _{IDM(RXIQ)} = 150 mV (p-p) | –0.8 | 0 | +0.3 | dB |
| | | f = 180 kHz; V _{IDM(RXIQ)} = 150 mV (p-p) | – | –3.5 | – | dB |
| | | f = 200 kHz; V _{IDM(RXIQ)} = 150 mV (p-p) | – | –5.5 | – | dB |
| f = 400 kHz; V _{IDM(RXIQ)} = 150 mV (p-p) | – | – | –35 | dB | | |
| f > 440 kHz; V _{IDM(RXIQ)} = 150 mV (p-p) | – | – | –45 | dB | | |
| DYN _{RXIQ} | dynamic signal range ZIF mode | f = 20 Hz to 135 kHz | 60 | 68 | – | dB |
| | NZIF mode | f = 20 Hz to 270 kHz | 60 | 68 | – | dB |
| SINAD _{RXIQ} | signal to noise and distortion ratio | f = 20.0 kHz; V _{IDM(RXIQ)} = 2 V (p-p) | 40 | – | – | dB |
| | | f = 67.7 kHz; V _{IDM(RXIQ)} = 2 V (p-p) | – | 65 | – | dB |
| | | f = 20 kHz; V _{IDM(RXIQ)} = 150 mV (p-p) | – | 40 | – | dB |
| | | f = 67.7 kHz; V _{IDM(RXIQ)} = 150 mV (p-p) | – | 40 | – | dB |
| OPC | output code in BDIO | for maximum input amplitude | – | ±1440 | – | LSB |
| PSRR _{RXIQ} | power supply ripple rejection | applying a 100 mV (p-p)/217 Hz sine wave on top of the analog power supply | – | 70 | – | dB |
| GERR _{RXIQ} | gain error | referenced to maximum amplitude | –6 | – | +6 | % |
| | | | –0.5 | – | +0.5 | dB |
| GMAT _{RXIQ} | gain matching error | at maximum input level | –3 | – | +3 | % |
| | | | –0.25 | – | +0.25 | dB |
| GDMAT _{RXIQ} | group delay matching of I and Q RX paths | measured at full-scale; 10 kHz < f < 100 kHz; output load = 10 pF // 10 kΩ | – | – | 5 | ns |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------------------|---|-----------------------------|------|------|------|------|
| OFFS _{RXIQ} | offset error | before compensation | -40 | - | +40 | mV |
| | | after compensation | -5 | - | +5 | mV |
| POST _{RXIQ} | power-on settling time ZIF mode NZIF mode | including decimation filter | - | 52 | - | μs |
| | | | - | 26 | - | μs |
| FGD _{RXIQ} | filter group delay ZIF mode NZIF mode | - | 23 | - | μs | |
| | | - | 11.5 | - | μs | |

Notes

1. Reference level is full-scale input at 67 kHz.
2. This will not be tested.

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18.3 Voice band transmit (microphone to ASI)
 $V_{DDA} = 2.5$ to 2.75 V; $T_{amb} = -40$ to $+85$ °C.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|--|------|------|------|----------------------|
| RES _{MICADC} | resolution of ADC | | – | 13 | – | bit |
| FSIN _{MICADC} | internal sampling frequency | | – | 1000 | – | kHz |
| GRAN _{TXPGA} | calibration gain range | | –24 | 0 | +12 | dB |
| GSTP _{TXPGA} | calibration gain step size | see Table 25 | – | 64 | – | steps |
| GTOL _{VBTX} | gain tolerance of coder | at TXPGA = 0 dB | –1.5 | – | +1.0 | dB |
| FRESP _{VBTX} | digital filter frequency response of implemented standard VSP software (version: vb5_all) | f < 100 Hz | – | – | –20 | dB |
| | | 100 Hz < f < 200 Hz | – | – | –10 | dB |
| | | f = 300 Hz to 3.3 kHz | –1 | – | +1 | dB |
| | | f = 3.3 to 3.4 kHz | –1.5 | – | 0 | dB |
| | | f ≥ 4 kHz | – | – | –20 | dB |
| FREJ _{VBTX} | out-of-band rejection | f = 4.6 kHz | 40 | 45 | – | dB |
| | | f = 6 to 30 kHz | 45 | 50 | – | dB |
| Microphone/auxiliary signal path | | | | | | |
| V _{IN(rms)} | nominal input level (RMS value) | TXPGA = 0 dB, MICH1 = 1 | – | –35 | – | dBm |
| | | TXPGA = 0 dB, MICH1 = 0 | – | –7 | – | dBm |
| N _{IDLE} | idle noise level (pin ADO) | psophometrically weighted ⁽¹⁾ ; T _{amb} = 25 °C | – | – | –75 | dBm0p ⁽²⁾ |
| THD | total harmonic distortion | f = 1 kHz; PGA = –4 dB; ADO = +2 dBm0 | – | – | 1 | % |
| SINAD | signal-to-noise and distortion | ADO = 3 dBm0 | 30 | – | – | dB |
| | | ADO = 0 dBm0 | 40 | – | – | dB |
| | | ADO = –10 dBm0 | 45 | – | – | dB |
| | | ADO = –20 dBm0 | 45 | – | – | dB |
| | | ADO = –30 dBm0 | 40 | – | – | dB |
| | | ADO = –40 dBm0 | 30 | – | – | dB |
| | | ADO = –45 dBm0 | 25 | – | – | dB |
| PSCT _{VBTX} | power supply crosstalk | applying a 100 mV (p-p)/217 Hz sine wave on top of the analog power supply | – | – | 2 | LSB |
| Audio Serial Interface (ASI) | | | | | | |
| FASOUT | PCM output bit rate | | 128 | – | 2048 | kbits/s |
| FSYNC _{AFS} | PCM frame synchronization frequency at pin AFS | | – | 8 | – | kHz |

Notes

1. Psophometrical weighting: a frequency weighting curve described in "ITU recommendation O.41".
2. The unit dBm0p: 0 dBm0p is generally defined as –3.14 dBFS, where dBFS denotes dB full scale, i.e. a signal with an amplitude covering the complete range of digital values. The suffix 'p' refers to psophometrical weighting.

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18.4 Voice band receive (ASI to earphone)

 $V_{DDA} = 2.5$ to 2.75 V; $T_{amb} = -40$ to $+85$ °C

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---------------------------------------|---|--|------|------------------|------|---------------------|
| RES _{EARDAC} | resolution of DAC | | – | 13 | – | bit |
| FSIN _{EARDAC} | internal sampling frequency | | – | 1000 | – | kHz |
| GRAN _{VOL} | gain step range | | –30 | –12 | +6 | dB |
| GSTP _{VOL} | gain step size | digital steps; see Table 25 | – | 64 | – | steps |
| GRAN _{PGA} | calibration PGA range | | –24 | – | +12 | dB |
| GSTP _{PGA} | gain step size | digital steps; see Table 25 | – | 64 | – | steps |
| GTOL _{VBRX} | gain tolerance of decoder | | –1 | – | +1 | dB |
| GMUTE _{VBRX} | mute attenuation of decoder | | 40 | – | – | dB |
| FRESP _{VBRX} | digital filter frequency response of implemented standard VSP software (version: vb5_all) | f = 0 to 100 Hz | – | – | –20 | dB |
| | | f = 300 to 3300 Hz | –1.0 | – | +1.0 | dB |
| | | f = 3300 to 3400 Hz | –2.0 | – | +1.0 | dB |
| | | f = 4000 Hz | – | – | –18 | dB |
| FREJ _{VBRX} | out-of-band rejection | f = 4600 Hz | 38 | – | – | dB |
| | | f = 28.6 kHz | 40 | – | – | dB |
| Audio Serial Interface (ASI) | | | | | | |
| FASIN | PCM input bit rate | | 128 | – | 2048 | kbits/s |
| FSYNC _{AFS} | PCM frame synchronization frequency at pin AFS | | – | 8 | – | kHz |
| Earphone output: EARP and EARN | | | | | | |
| V _{ref(EAR)} | DC reference level | | – | V _{ref} | – | V |
| V _{o(EAR)(p-p)} | output voltage (peak-to-peak value) | load: 16 Ω differential | – | 2 | – | V |
| | | load: 8 Ω single-ended | – | 1.5 | – | V |
| I _{o(EAR)peak} | output source/sink current | load: 8 Ω single-ended | – | 100 | – | mA |
| GAIN _{EARVOL} | nominal gain from ASI to EARP/EARN | GRAN _{VOL} = –12 dB; load 32 Ω differential | –13 | –12 | –11 | dB |
| | | single-ended | –19 | –18 | –17 | dB |
| GRAN _{SIDVOL} | total sidetone gain (from MICP/MICN to EARP/EARN) | | +5 | – | +41 | dB |
| THD _{EAR} | total harmonic distortion | GRAN _{EARVOL} = –12 dB | – | – | 1 | % |
| IDLN _{EAR} | idle noise at EARP/EARN | psophometrically weighted ⁽¹⁾ ; GRAN _{EARPGA} = 0 dB | – | – | –72 | dBmp ⁽²⁾ |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--------------------------------|---|--|------|-------------------------|------|------|
| SINAD _{EAR} | signal-to-noise and distortion ratio from ASI to earphone | psophometrically weighted ⁽¹⁾ | | | | |
| | | at 3 dBm ₀ input signal level | 30 | – | – | dB |
| | | at 0 dBm ₀ input signal level | 35 | – | – | dB |
| | | at –10 dBm output signal level | 45 | – | – | dB |
| | | at –20 dBm output signal level | 42 | – | – | dB |
| | | at –30 dBm output signal level | 40 | – | – | dB |
| | | at –40 dBm output signal level | 30 | – | – | dB |
| PSRR _{EAR} | power supply ripple rejection at EARP/EARN | at –45 dBm output signal level | 25 | – | – | dB |
| | | applying a 100 mV (p-p)/217 Hz sine wave on top of the analog power supply | 70 | – | – | dB |
| Auxiliary output: AUXSP | | | | | | |
| V _{ref(AUXSP)} | DC reference level | | – | V _{ref} | – | V |
| V _{o(AUXSP)} | output voltage | load: 16 Ω with 47 μF in series to ground | – | V _{ref} ±1 | – | V |
| | | load: 8 Ω with 100 μF in series to ground | – | V _{ref} ±0.77 | – | V |
| I _{o(AUXSP)peak} | output source/sink current | load: 16 Ω with 47 μF in series to ground | – | 62.5 | – | mA |
| GAIN _{AUXSP} | nominal gain from ASI to AUXSP | load: 16 Ω with 47 μF in series to ground; GRAN _{VOL} = –12 dB | –19 | –18 | –17 | dB |
| Buzzer output: BUZ | | | | | | |
| V _{ref(BUZ)} | DC reference level | | – | V _{ref} | – | V |
| V _{o(BUZ)} | output voltage | load: 8 Ω with 100 μF in series to ground | – | V _{ref} – 0.77 | – | V |
| I _{o(BUZ)peak} | output source/sink current | | – | 100 | – | mA |
| GAIN _{BUZ} | nominal gain from ASI to BUZ | load: 8 Ω with 100 μF in series to ground; GRAN _{VOL} = –12 dB | –19 | –18 | –17 | dB |

Notes

1. Psophometrical weighting: a frequency weighting curve described in “ITU recommendation O.41”.
2. The unit dBmp: 0 dBmp refers to a voltage of a signal of 1 mW across a 600 Ω load. The suffix ‘p’ refers to psophometrical weighting.

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18.5 Auxiliary digital-to-analog converters

 $V_{DDA} = 2.5$ to 2.75 V; $T_{amb} = -40$ to $+85$ °C.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------------|---|---|------|-------|------|------|
| AUXDAC1 | | | | | | |
| RES _{DAC1} | resolution | | – | 8 | – | bit |
| VOMIN _{DAC1} | minimum output voltage | register value: 000H | 0 | – | 0.15 | V |
| VOMAX _{DAC1} | maximum output voltage | register value: 0FFH | 2.1 | 2.2 | 2.3 | V |
| VDEF _{DAC1} | output voltage after reset | register value: 085H | – | 1.147 | – | V |
| MON _{DAC1} | monotonicity range | | – | 8 | – | bit |
| INL _{DAC1} | integral non-linearity ⁽¹⁾ | | –5.0 | – | +5.0 | LSB |
| DNL _{DAC1} | differential non-linearity ⁽²⁾ | | –1.0 | – | +1.0 | LSB |
| OFFS _{DAC1} | offset error | | –80 | – | +80 | mV |
| FSST _{DAC1} | full-scale settling time | load: 50 pF // 2 kΩ, to V _{SS} ; | – | 40 | – | μs |
| LSBST _{DAC1} | one LSB settling time | see Fig.13a | – | 8 | – | μs |
| AUXDAC2 | | | | | | |
| RES _{DAC2} | resolution | | – | 12 | – | bit |
| VOMIN _{DAC2} | minimum output voltage | register value: 000H | 0 | – | 0.15 | V |
| VOMAX _{DAC2} | maximum output voltage | register value: FFFH | 2.1 | 2.2 | 2.32 | V |
| VDEF _{DAC2} | output voltage after reset | register value: 800H | – | 1.1 | – | V |
| MON _{DAC2} | monotonicity range | | – | 12 | – | bit |
| INL _{DAC2} | integral non-linearity ⁽¹⁾ | | – | ±10 | – | LSB |
| DNL _{DAC2} | differential non-linearity ⁽²⁾ | | –1.0 | – | +2.0 | LSB |
| OFFS _{DAC2} | offset error | | –25 | – | +25 | mV |
| FSST _{DAC2} | full-scale settling time | load: 50 pF // 10 kΩ, to | – | 40 | – | μs |
| LSBST _{DAC2} | one LSB settling time | V _{SS} ; see Fig.13b | – | 8 | – | μs |
| POST _{DAC2} | power-on settling time | see Section 18.1 | – | – | 4 | ms |
| AUXDAC3 | | | | | | |
| RES _{DAC3} | resolution | | – | 10 | – | bit |
| VOMIN _{DAC3} | minimum output voltage | register value: 000H | 0 | – | 0.15 | V |
| VOMAX _{DAC3} | maximum output voltage | register value: 3FFH | 2.1 | 2.2 | 2.3 | V |
| MON _{DAC3} | monotonicity range | | – | 10 | – | bit |
| INL _{DAC3} | integral non-linearity ⁽¹⁾ | | –5.0 | – | +5.0 | LSB |
| DNL _{DAC3} | differential non-linearity ⁽²⁾ | | –1.0 | – | +1.0 | LSB |
| OFFS _{DAC3} | offset error | | –40 | – | +40 | mV |
| FSST _{DAC3} | full-scale settling time | load: 50 pF // 1 kΩ, to V _{SS} ; | 1 | 10 | 15 | μs |
| LSBST _{DAC3} | one LSB settling time | see Fig.13c | – | 2.5 | – | μs |
| SSC _{DAC3} | output source/sink current | | – | – | 2.5 | mA |

Notes

- INL: the difference of the output to the best fit line. $INL_{(i)} = [V_{(i)} - (a + i \times b)]/1$ LSB; $INL = (INL_{(i)(max)} - INL_{(i)(min)})/2$.
- DNL is the difference between individual code width and average code width (1 LSB); maximum and minimum specified. $DNL_{(i)} = [(V_{(i+1)} - V_{(i)} - 1 \text{ LSB})/1 \text{ LSB}]$; $DNL_{(min)} > -1$ is equivalent to monotonicity $V_{(i+1)} > V_{(i)}$.

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18.6 Auxiliary analog-to-digital converters: AUXADC1, AUXADC2, AUXADC3 and AUXADC4

$V_{DDA} = 2.5$ to 2.75 V; $T_{amb} = -40$ to $+85$ °C.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---------------------------|---------------------------------------|-----------------------------------|------|------|-------|------|
| RES _{AUXADC} | resolution | coded in 12 bits | – | 1440 | – | LSB |
| VIN _{AUXADC} | input voltage | | 0.0 | – | 2.0 | V |
| VIN _{AUXADC} MIN | V _{in} for output code 0 | | –20 | – | 20 | mV |
| VIN _{AUXADC} MAX | V _{in} for output code +1820 | after offset compensation | – | 2.0 | – | V |
| R _{i(AUXADC)} | input resistance | | – | 1.0 | – | MΩ |
| INL _{AUXADC} | integral non-linearity | | – | 2.5 | – | mV |
| DNL _{AUXADC} | differential non-linearity | | – | 2.5 | – | mV |
| GERR _{AUXADC} | gain error | V _i = V _{ref} | –0.5 | – | + 0.5 | dB |
| OFFS _{AUXADC} | offset error after compensation | | –3 | – | 3 | LSB |
| POST _{AUXADC} | power-on settling time | | – | 170 | – | μs |

18.7 Typical total current consumption

The typical total current consumption values for the chip in different modes; $T_{amb} = 25$ °C.

| ACTIVITY | TOTAL CURRENT (mA) | | REMARKS |
|--|--------------------|--------|--|
| | NOTE 1 | NOTE 2 | |
| Baseband transmit | 3.96 | 4.04 | baseband transmit + references + MCLK + BSI |
| receive | 5.14 | 5.41 | baseband receive + references + MCLK + BSI |
| Voice band transmit and receive | 4.79 | 4.94 | voice band transmit and receive + references + 13 MHz + auxiliary DAC2; note 3 |
| Voice band transmit and receive baseband transmit | 7.32 | 7.51 | voice band transmit and receive + baseband transmit + references + 13 MHz + CSI + auxiliary DACs 2 and 3 |
| baseband receive | 8.52 | 8.91 | voice band transmit and receive + baseband receive + references + 13 MHz + auxiliary DAC 2 |
| Auxiliary ADC function | 2.75 | 2.86 | auxiliary ADC + CSI + references + 13 MHz + auxiliary DAC2 |
| Auxiliary DAC1 | 2.35 | 2.49 | auxiliary DACs 1 and 2 + references + 13 MHz |
| Auxiliary DAC2 | 1.55 | 1.59 | auxiliary DAC2 + references + 13 MHz |
| Auxiliary DAC3 | 4.35 | 4.56 | auxiliary DACs 3 and 2 + CSI + baseband transmit + references + 13 MHz |
| Idle with MCLK running | 0.23 | 0.24 | references + 13 MHz clock |
| Idle no MCLK; references on | 0.18 | 0.19 | references; see Section 19.1.1 "Possibility 1" |
| Idle | 0.01 | 0.01 | all blocks in power-down, no 13 MHz clock |

Notes

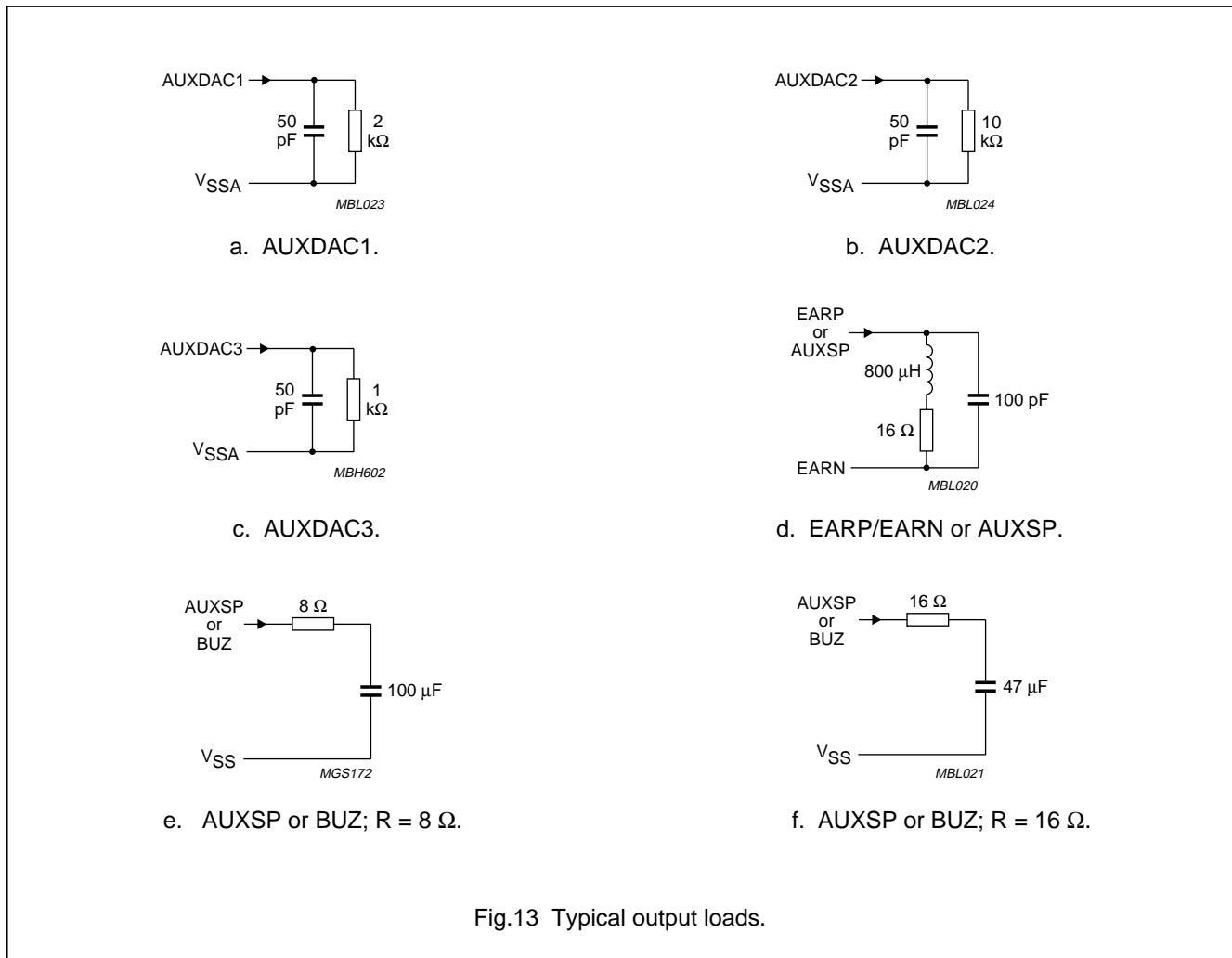
- $V_{DDD} = 2.3$ V; $V_{DDA} = 2.65$ V; external interface current is not included.
- $V_{DDD} = 2.6$ V; $V_{DDA} = 2.65$ V; external interface current is not included.
- For a signal at the earpiece differential output of amplitude 'A' across a load resistance of 'R', the current 'I' must be added, where: $I = \frac{4}{\pi} \cdot \frac{A}{R}$.

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18.8 Typical output loads

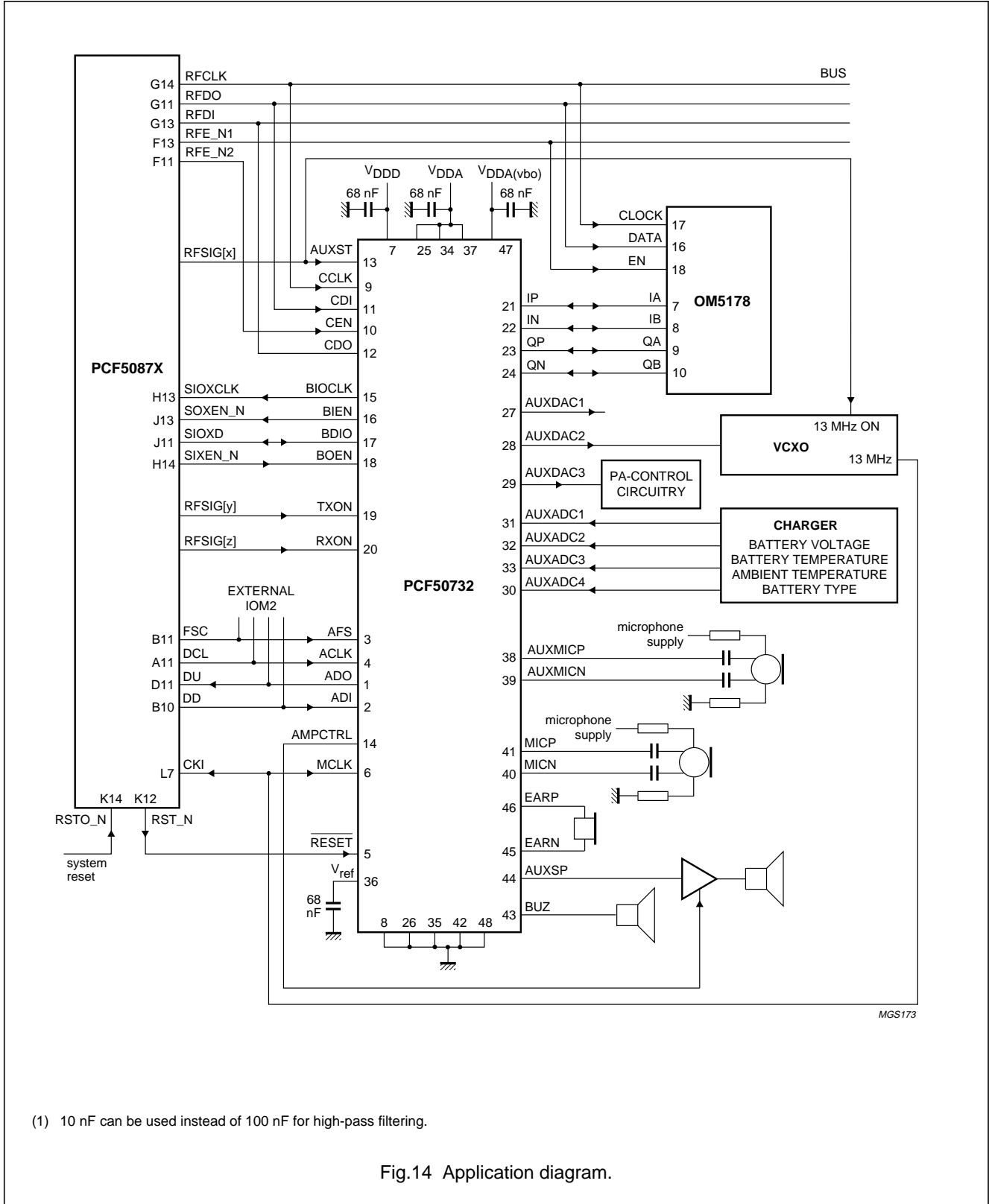
Figure 13 illustrates the typical loads for the outputs: AUXDAC1, AUXDAC2, AUXDAC3, EARP, EARN, AUXSP and BUZ.



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19 APPLICATION INFORMATION



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19.1 Wake-up procedure from Sleep mode

Apart from being the status control signal of AUXDAC1, AUXDAC2 and the MCLK input, AUXST also starts a down-counter at each rising edge which controls the output drive capability of pin V_{ref} . This is important for the following considerations. For current consumption reduction during Sleep mode there are **two** possibilities as shown in Section 19.1.1 and 19.1.2.

19.1.1 POSSIBILITY 1

Program every block into power-down via CSI except for the band gap, then pull AUXST LOW to switch off the clock internally. This results in a $I_{DD(total)} = 60 \mu A$ (typical). Since the band gap hasn't been programmed into power-down, the only active reference is V_{ref} . After a rising edge of AUXST, $POST_{DAC}$ is in the order of 1.5 ms.

19.1.2 POSSIBILITY 2

If AUXST is also used to switch off the analog power supply, all references are shut down. The power-up time in this case is measured from the point where the MCLK clock input has valid levels or V_{DDA} has settled to its final value (the latter of the two signals sets the reference point).

A down-counter increases the band gap output drive capability for 32768 MCLK cycles which equals approximately 2.5 ms. After that time the voltage at V_{ref} has reached ± 0.5 mV of its final value. The timing diagram illustrates the situation (see Fig.15). Other points to note for this possibility:

- As long as V_{DDD} is not switched off, all registers keep their values.
- As long as $V_{DDA(bb)}$ is not stable, the internal master clock is not running, because the first stage of the clock generator is supplied by V_{DDA} .
- All digital signals **MUST** remain stable for t_{MCLK} after AUXST has gone HIGH. This is necessary to avoid any timing violations in the digital part of the PCF50732 caused by an unstable MCLK clock input.
- The previously mentioned 2.5 ms for t_{BG} are only valid for $C_{Vref} = 68 \text{ nF} \pm 10\%$ or less. The maximum of value 68 nF is highly recommended for good noise and power supply rejection figures.

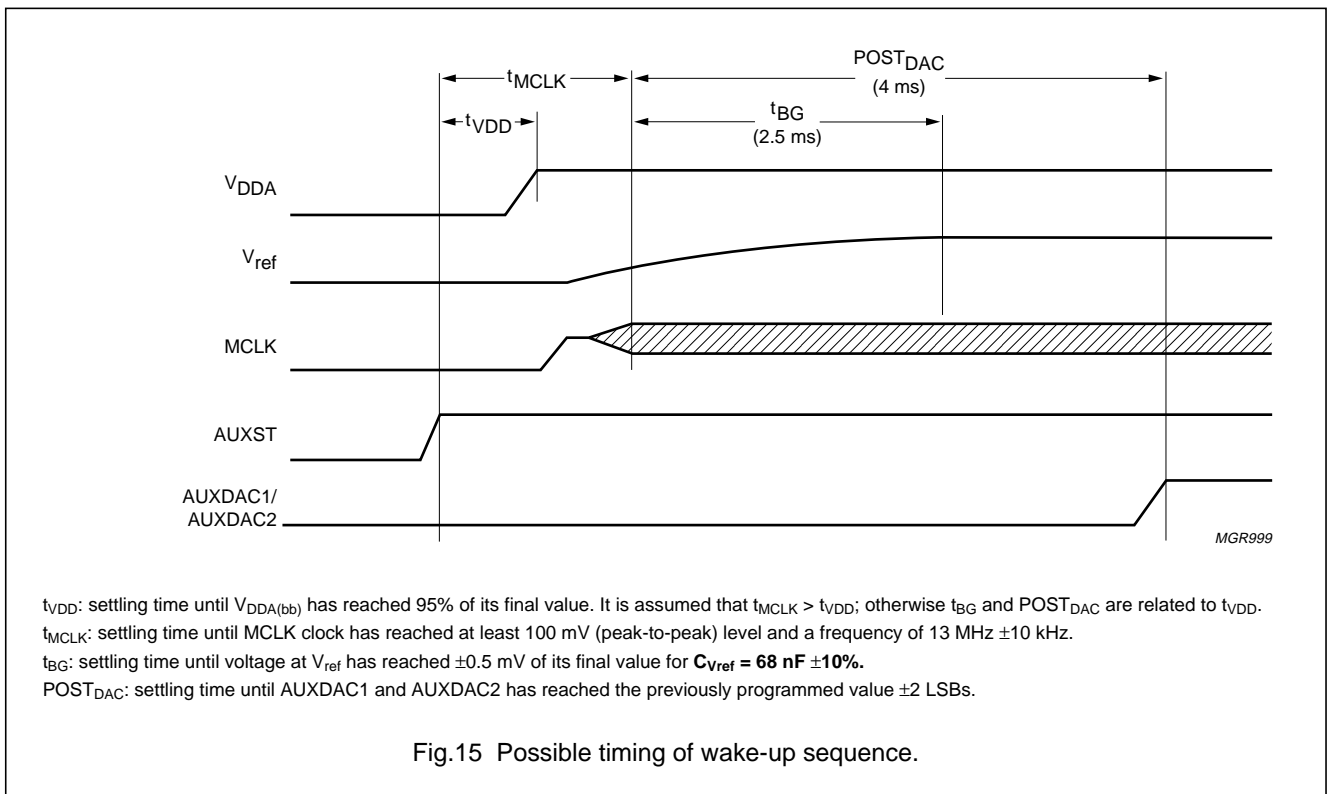
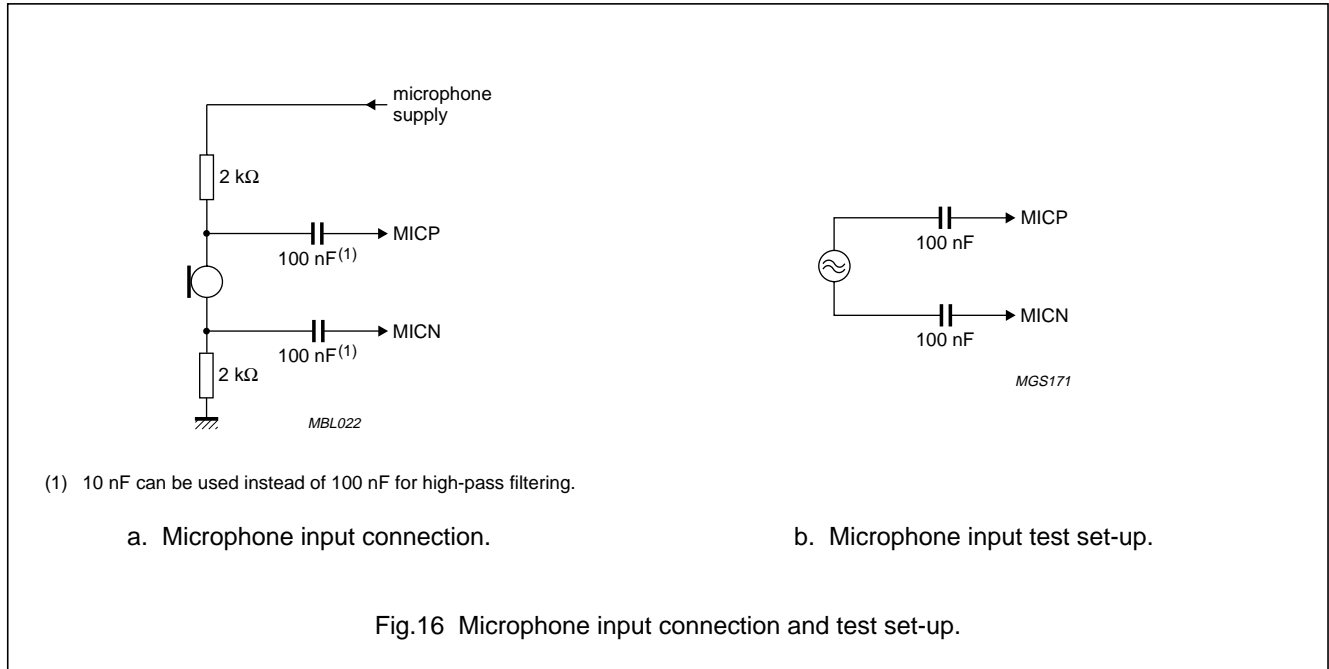


Fig.15 Possible timing of wake-up sequence.

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19.2 Microphone input connection and test set-up



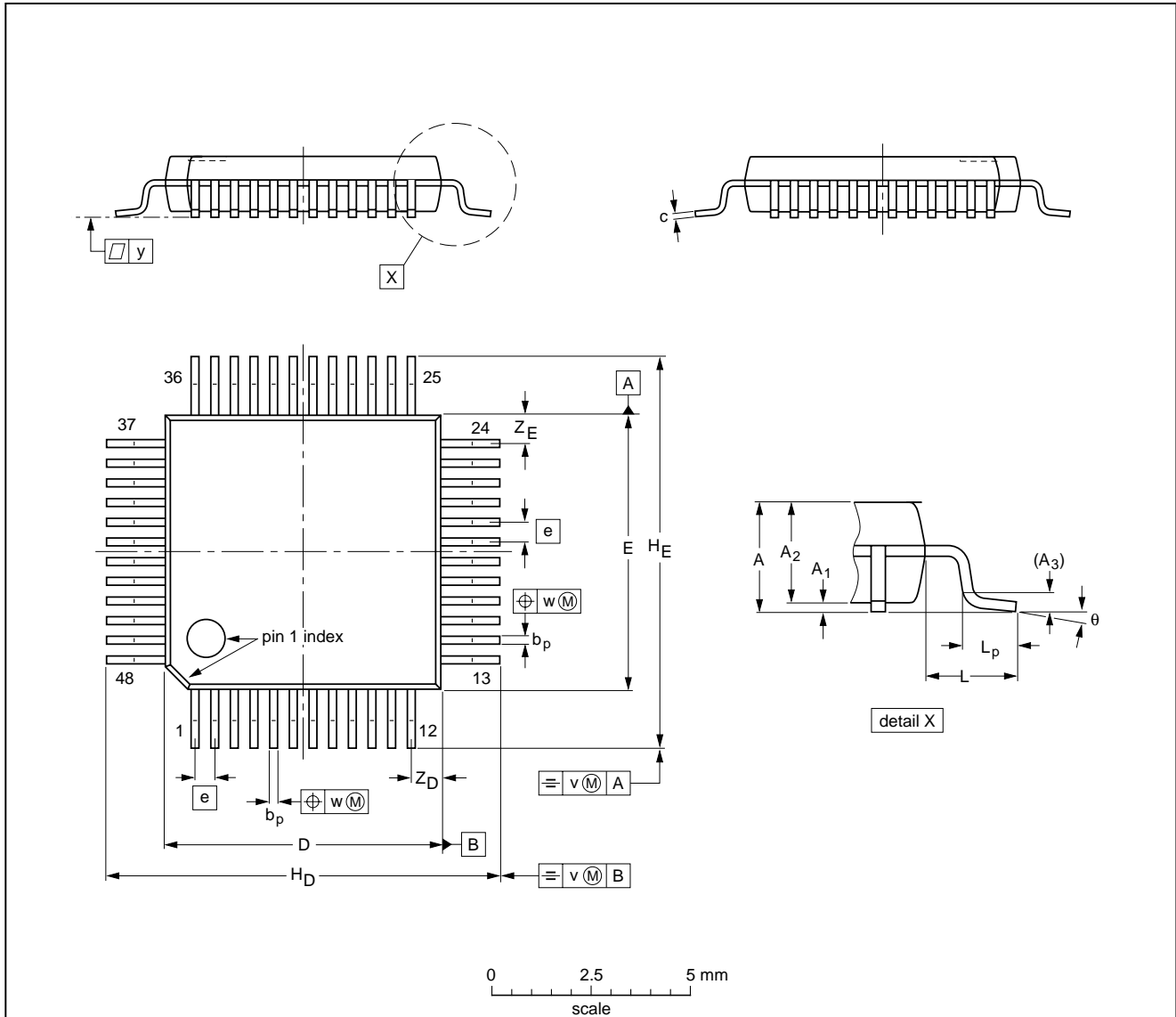
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20 PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm

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DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _D | H _E | L | L _p | v | w | y | Z _D ⁽¹⁾ | Z _E ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|-----|----------------|----------------|-----|----------------|-----|------|-----|-------------------------------|-------------------------------|----------|
| mm | 1.60 | 0.20 0.05 | 1.45 1.35 | 0.25 | 0.27 0.17 | 0.18 0.12 | 7.1 6.9 | 7.1 6.9 | 0.5 | 9.15 8.85 | 9.15 8.85 | 1.0 | 0.75 0.45 | 0.2 | 0.12 | 0.1 | 0.95 0.55 | 0.95 0.55 | 7° 0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT313-2 | | | | | | 94-12-19 97-08-01 |

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21 SOLDERING

21.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

21.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

21.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

21.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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21.5 Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE | SOLDERING METHOD | |
|---------------------------------|-----------------------------------|-----------------------|
| | WAVE | REFLOW ⁽¹⁾ |
| BGA, SQFP | not suitable | suitable |
| HLQFP, HSQFP, HSOP, HTSSOP, SMS | not suitable ⁽²⁾ | suitable |
| PLCC ⁽³⁾ , SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended ⁽³⁾⁽⁴⁾ | suitable |
| SSOP, TSSOP, VSO | not recommended ⁽⁵⁾ | suitable |

Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

22 DEFINITIONS

| Data sheet status | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

23 LIFE SUPPORT APPLICATIONS

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