256 × 8-bit STATIC CMOS EEPROM WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8582A is a 2 Kbits 5 Volt electrically erasable programmable read only memory (EEPROM) organized as 256 by 8-bits. It is designed in a floating gate CMOS technology.

As data bytes are received and transmitted via the serial I²C-bus, an eight pin DIL package is sufficient. Up to eight PCF8582A devices may be connected to the I²C-bus.

Chip select is accomplished by three address inputs.

Timing of the Erase/Write cycle can be done in two different ways; either by connecting an external clock to the "Programming Timing Control", pin (7 or 13), or by using an internal oscillator. If the latter is used an RC time constant must be connected to pin 7 or 13.

Features

- Non-volatile storage of 2 Kbits organized as 256 x 8
- Only one power supply required (5 V)
- On chip voltage multiplier for erase/write
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Low power consumption
- One point erase/write timer
- Power on reset
- 10,000 erase/write cycles per byte
- 10 years non-volatile data retention
- Infinite number of read cycles
- Pin and address compatible to PCF8570, PCF8571, PCF8582 and PCD8572
- External clock signal possible.

A version with automotive temperature range −40 to + 125 °C (PCF8582B) and a version with extended temperature range −40 to + 85 °C (PCF8582C) are in preparation.

PACKAGE OUTLINE

PCF8582AP; 8-lead dual in line; plastic (SOT97).
PCF8582AT; 16-lead mini-pack; plastic (SO16L; SOT162A).

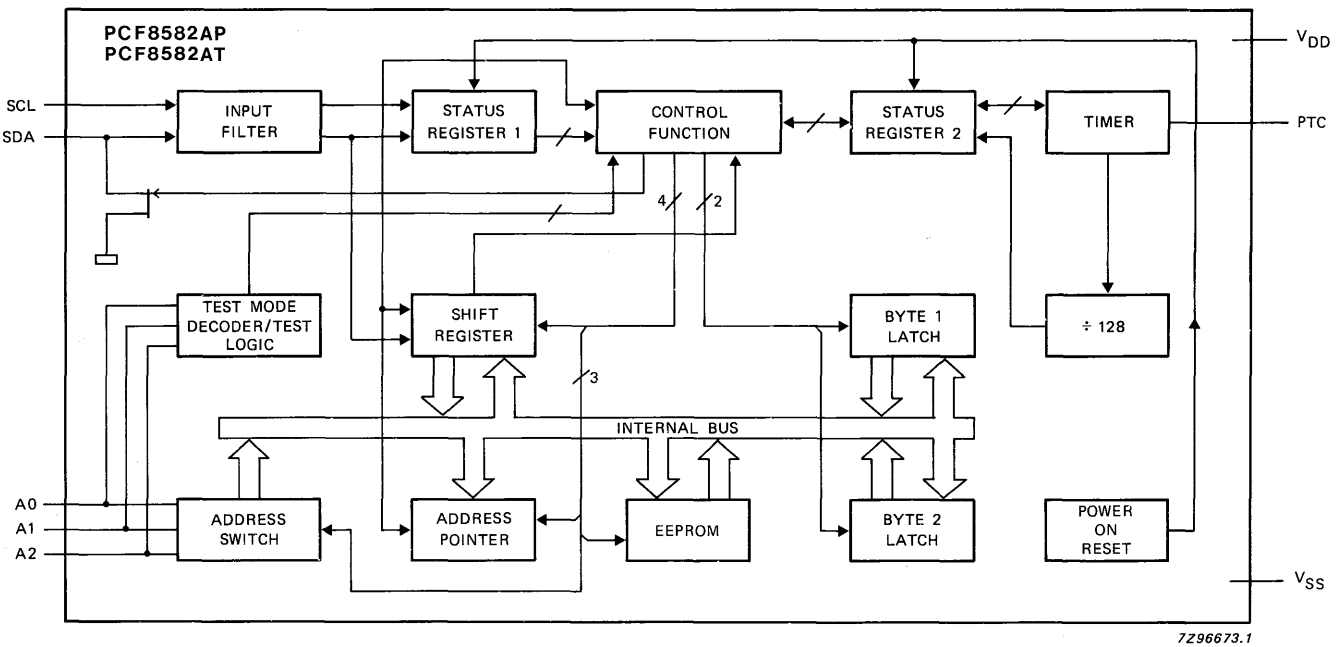
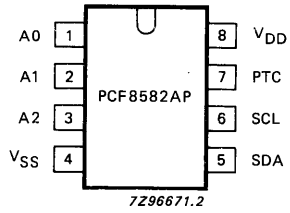
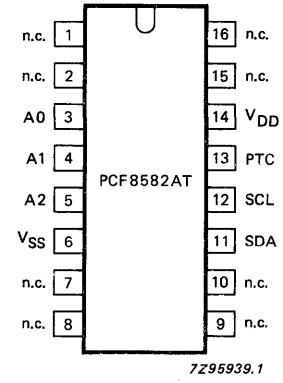


Fig. 1 Block diagram.



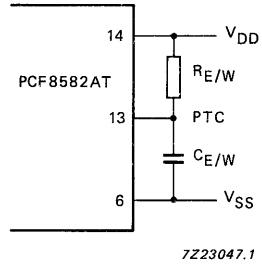
1	A0	address inputs/test mode select
2	A1	
3	A2	
4	V_{SS}	ground
5	SDA	I^2C-bus lines
6	SCL	
7	PTC	programming time control
8	V_{DD}	positive supply

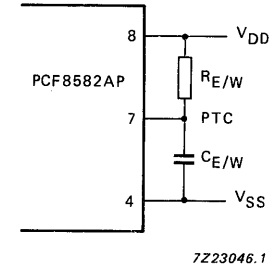
Fig. 2 (a) Pinning diagram.



1	n.c.	
2	n.c.	
3	A0	address inputs/test mode select
4	A1	
5	A2	
6	V_{SS}	ground
7	n.c.	
8	n.c.	
9	n.c.	
10	n.c.	
11	SDA	I^2C-bus lines
12	SCL	
13	PTC	programming time control
14	V_{DD}	positive supply
15	n.c.	
16	n.c.	

Fig. 2 (b) Pinning diagram.





Figs. 3 (a) and (b) RC circuit connections to PCF8582AP and PCF8582AT when using the internal oscillator

FUNCTIONAL DESCRIPTION

Characteristics of the I²C-bus

The I²C-bus is intended for communication between different ICs. The serial bus consists of two bi-directional lines, one for data signals (SDA), and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

Data transfer may be initiated only when the bus is not busy.
During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The following bus conditions have been defined:

Bus not busy; both data and clock lines remain HIGH.
Start data transfer; a change in the state of the data line, from HIGH to LOW,
while the clock is HIGH defines the start condition. Stop data transfer; a change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the stop condition.
Data valid; the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to two bytes in the ERASE/WRITE mode and unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications a low speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined. The PCF8582A operates in both modes.

By definition a device that sends a signal is called a "transmitter", and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

Each word of eight bits is followed by one acknowledge bit. This acknowledge bit is a HIGH level put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse.
The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.
The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse in clock pulse.
Set-up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this condition the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

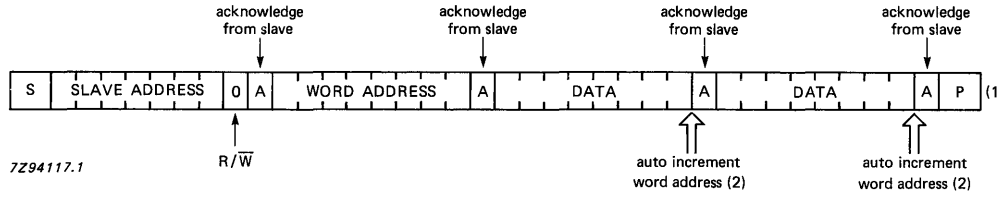
Note

Detailed specifications of the I²C-bus are available on request.

DEVELOPMENT DATA

I²C-Bus Protocol

The I²C-bus configurations for different READ and WRITE cycles of the PCF8582A are shown in Fig. 4, (a), (b) and (c).



(1) After this stop condition the erase/write cycle starts and the bus is free for another transmission. The duration of the erase/write cycle is approximately 30 ms if only one byte is written and 60 ms if two bytes are written. During the erase/write cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

(2) The second data byte is voluntary. It is not allowed to erase/write more than two types.

Fig. 4(a) Master transmitter transmits to PCF8582A slave receiver (ERASE/WRITE mode).

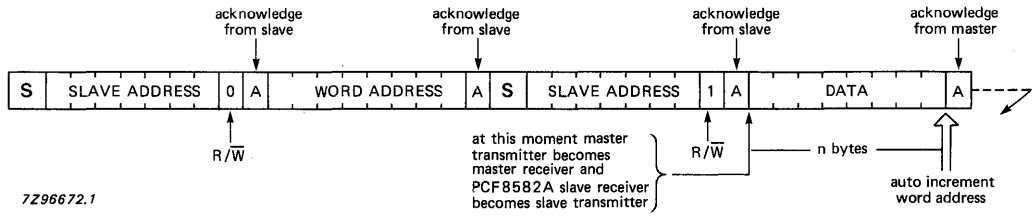
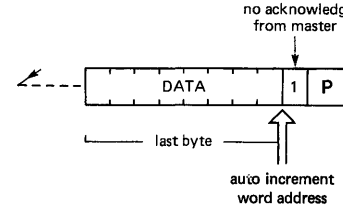


Fig. 4(b) Master reads PCF8582A slave after setting word address (write word address; READ data).



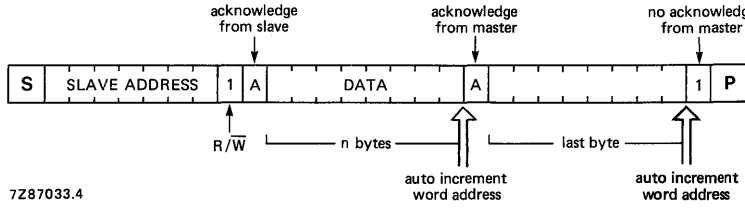


Fig. 4(c) Master reads PCF8582A slave immediately after first byte (READ mode).*

Note: the slave address is defined in accordance with the I²C-bus specification as:

1	0	1	0	A2	A1	A0	R/W

* The device can be used as read only without the programming clock.

I²C-bus timing

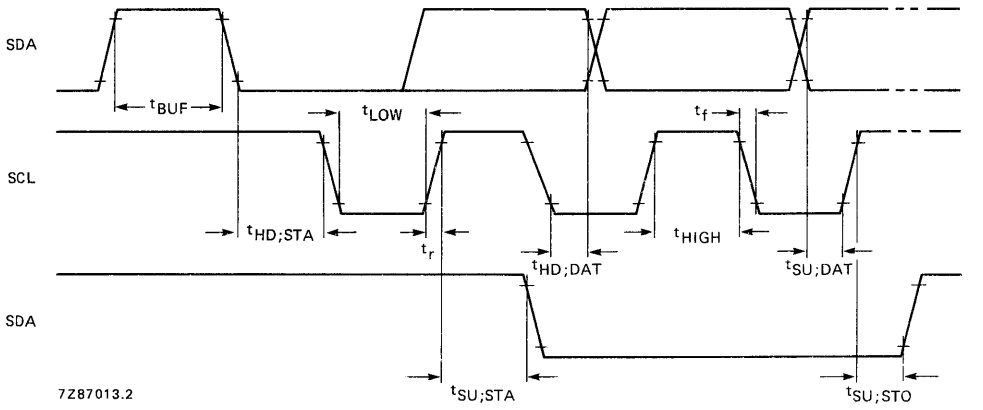
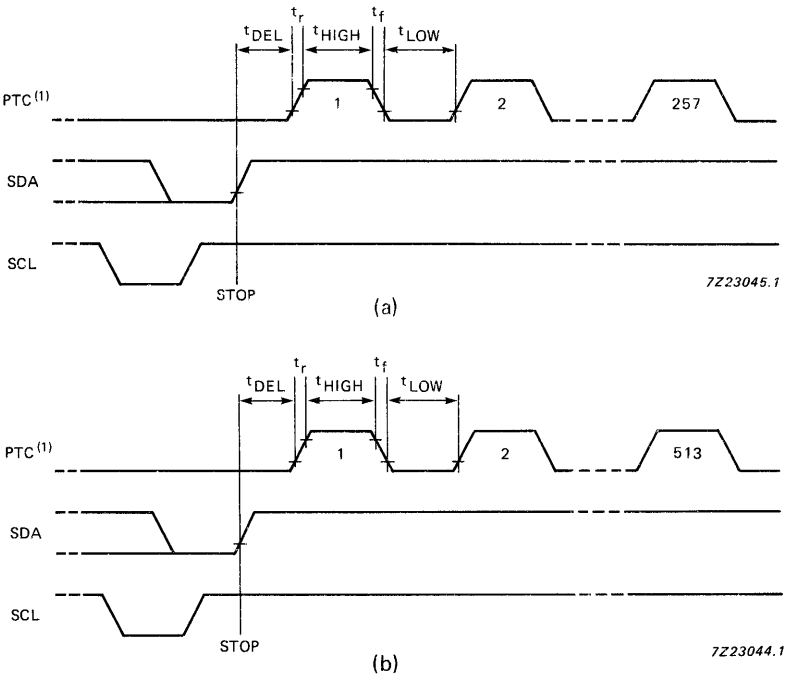


Fig. 5 I²C-bus timing.



(1) If external clock for PTC is chosen, this information is latched internally by leaving pin 7 LOW after transmission of the eight bit of the word address (negative edge of SCL). The state of PTC then, may be previously undefined.

Fig. 6 (a) One-byte ERASE/WRITE cycle; (b) two-byte ERASE/WRITE cycle.

Ratings

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{DD}	−0.3	+7	V
Voltage on any input pin input impedance 500 Ω	V_I	$V_{SS} - 0.8$	$V_{DD} + 0.8$	V
Operating temperature range	T_{amb}	−40	+85	°C
Storage temperature range	T_{stg}	−65	+150	°C
Current into any input pin	$\|I_I\|$	−	1	mA
Output current	$\|I_O\|$	−	10	mA

DEVELOPMENT DATA

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage		V_{DD}	4.5	5.0	5.5	V
Operating supply current READ	V_{DD} max. f_{SCL} = 100 kHz	I_{DD}	–	–	0.4	mA
Operating supply current WRITE/ERASE	V_{DD} max.	I_{DDW}	–	–	2.0	mA
Standby supply current	V_{DD} max.	I_{DDO}	–	–	10	μA
Input PTC						
Input voltage HIGH			V_{DD} − 0.3	–	–	V
Input voltage LOW			–	–	V_{SS} + 0.3	V
Input SCL and input/output SDA						
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	V_{DD} + 0.8	V
Output voltage LOW	I_{OL} = 3 mA V_{DD} = 4.5 V	V_{OL}	–	–	0.4	V
Output leakage current HIGH	$V_{OH} = V_{DD}$	I_{LO}	–	–	1	μA
Input leakage current (SCL)	$V_I = V_{DD}$ or V_{SS}	I_{LI}	–	–	1	μA
Clock frequency		f_{SCL}	0	–	100	kHz
Input capacitance (SCL; SDA)		C_I	–	–	7	pF
Time the bus must be free before new transmission can start		t_{BUF}	4.7	–	–	μs
Start condition hold time after which first clock pulse is generated		$T_{HD;STA}$	4	–	–	μs

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
The LOW period of the clock		t_{LOW}	4.7	–	–	μs
The HIGH period of the clock		t_{HIGH}	4.0	–	–	μs
Set-up time for start condition	repeated start only	$t_{SU;STA}$	4.7	–	–	μs
Data hold time for I²C-bus compatible masters		$t_{HD;DAT}$	5.0	–	–	μs
Data hold time for I²C devices	note 1	$t_{HD;DAT}$	0	–	–	ns
Date set up time		$t_{SU;DAT}$	250	–	–	ns
Rise time for SDA and SCL lines		t_r	–	–	1	μs
Fall time for SDA and SCL lines		t_f	–	–	300	ns
Set-up time for stop condition		$T_{SU;STO}$	4.7	–	–	μs
Programming time control						
Erase/write cycle time		$t_{E/W}$	5	–	40	ms
Capacitor used for E/W cycle of 30 ms	max. tolerance ±10%; using internal oscillator (Fig. 3)	$C_{E/W}$	–	3.3	–	nF
Resistor used for E/W cycle of 30 ms	max. tolerance ±5%; using internal oscillator (Fig. 3)	$R_{E/W}$	–	56.0	–	kΩ
Programming frequency using external clock						
Frequency		f_p	10	–	50	kHz
Period LOW		t_{LOW}	10.0	–	–	μs
Period HIGH		t_{HIGH}	10.0	–	–	μs
Rise-time		t_r	–	–	300	ns
Fall-time		t_f	–	–	300	ns
Delay-time		t_d	0	–		ns
Data retention time	T_{amb} = 55 °C	t_S	10	–	–	years

Note to the characteristics

1. The hold time required to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter. It is not greater than 300 ns.

CHARACTERISTICS (continued)

E/W programming time control

A. Using external resistor $R_{E/W}$ and capacitor $C_{E/W}$ (see Table 1)

Table 1 Recommended R, C combinations

$R_{E/W}$ (kΩ) note 1	$C_{E/W}$ (nF) note 2	$t_{E/W}$ (typ.) (ms) note 3
56	3.3	34
56	2.2	21
22	3.3	13
22	2.2	7.5 (note 4)

Notes to Table 1

1. Maximum tolerance is 10%.
2. Maximum tolerance is 5%.
3. Actual E/W lines are mainly influenced by the tolerances in values of R and C.
4. Minimum allowed $t_{E/W}$ is 5 ms (see CHARACTERISTICS).

B. Using an external clock (see Table 2 and Fig.6)

Table 2 E/W programming time control using an external clock

parameters	symbol	min.	max.	unit
frequency	f_p	10.0	50.0	kHz
period LOW	t_{LOW}	10.0	–	s
period HIGH	t_{HIGH}	10.0	–	s
rise time	t_r	–	300	ns
fall time	t_f	–	300	ns
delay time	t_d	0	–	ns