512 × 8-bit static CMOS EEPROM with I²C-bus interface

PCF8594

FEATURES

- Low Power CMOS
  maximum active current 2.5 mA
  maximum standby current 10 µA
- Non-volatile storage of 4-Kbits organized as two pages
  each 256 x 8-bits
- Only one power supply required
- On-chip voltage multiplier
- Serial input/output bus (I²C)
- Write operations
  byte write mode
  8-byte page write mode (minimizes total write time per byte)
- Write-protection input
- Read operations
  sequential read
  random read
- Extended supply voltage range (2.5 to 6.0 V)
- Internal timer for writing (no external components)
- Power-on reset
- High reliability by using a redundant storage code
  (single bit error correction)
- Endurance
  100 k; $T_{amb} = 85$ °C
- 10 years non-volatile data retention time
- Pin and Address compatible to
  PCF8570, PCF8571, PCF8572, PCF8581, PCF8582A, PCA8582B and PCF8582C

GENERAL DESCRIPTION

The PCF8594 is a 4-Kbit (512 x 8-bit) floating gate electrically erasable programmable read only memory (EEPROM). By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability compared to conventional EEPROM memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on chip, using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to four PCF8594 devices may be connected to the I²C-bus. Chip select is accomplished by two address inputs.

Timing of the Erase/Write cycle is done internally, thus no external components are required. Pin 7 must be connected to either V_{DD} or left open-circuit.

There is an option of using an external clock for timing the length of an Erase/Write cycle.

A write protection input (pin 1) allows disable of write-commands from the master by a hardware signal. When pin 1 is HIGH and one of the upper 256 EEPROM cells is addressed, then the data bytes will not be acknowledged by the PCF8594 and the EEPROM-contents are not changed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		2.5	6.0	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz			
		V_{DD} = 3 V	-	0.1	mA
		V_{DD} = 6 V	-	0.4	mA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz			
		V_{DD} = 3 V	-	0.35	mA
		V_{DD} = 6 V	-	2.5	mA
I_{DDO}	supply current STANDBY				
		V_{DD} = 3 V	-	3.5	µA
		V_{DD} = 6 V	-	10	µA

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8594P	8	DIL	plastic	SOT97
PCF8594T	8	mini-pack	plastic	SO8; SOT96A

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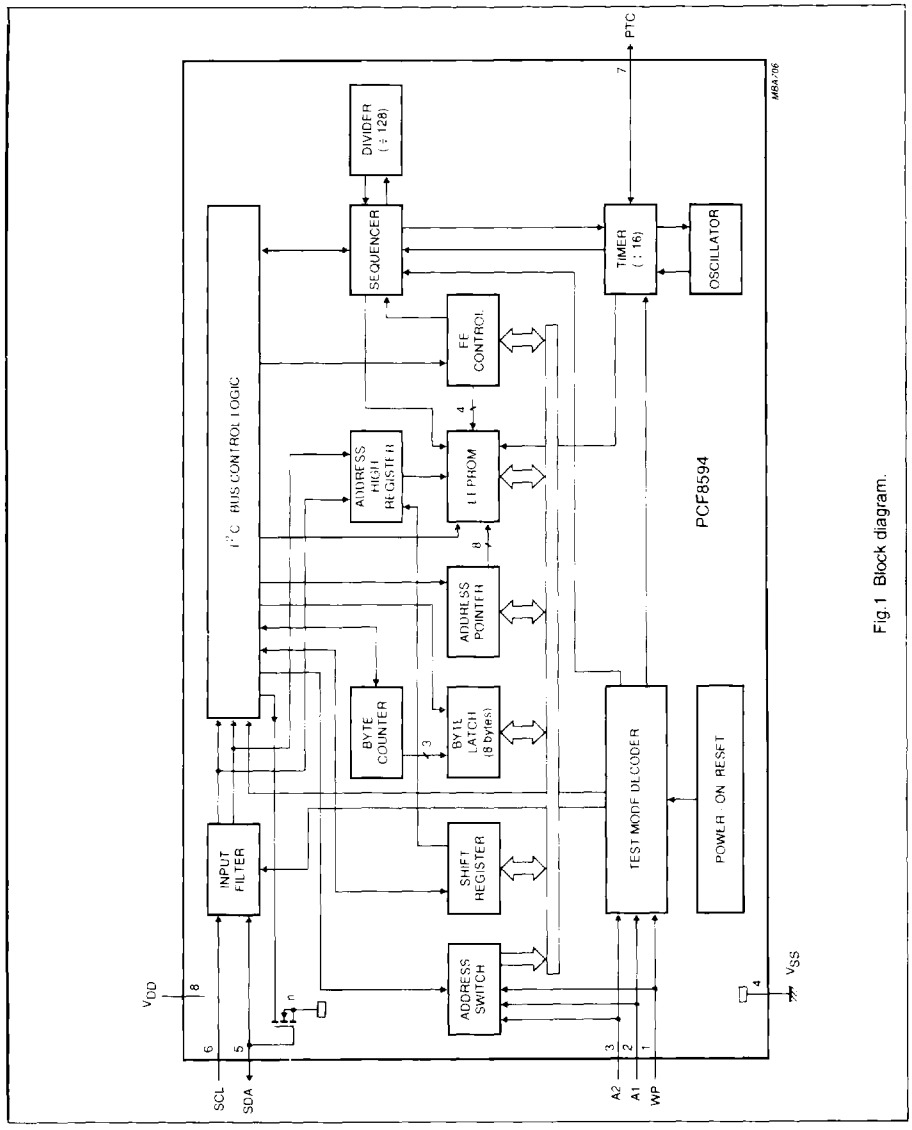


Fig.1 Block diagram.

512 × 8-bit static CMOS EEPROM with I²C-bus interface

PCF8594

PIN CONFIGURATION

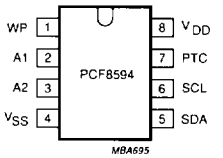


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
WP	1	write-protect
A1	2	address input
A2	3	address input
V_{SS}	4	negative supply voltage
SDA	5	serial data line I²C-bus
SCL	6	serial clock line I²C-bus
PTC	7	programming time control
V_{DD}	8	positive supply voltage

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.3	+7.0	V
V_I	voltage on any input pin	$\|Z_I\| > 500\ \Omega$	V_{SS} −0.8	V_{DD} +0.8	V
I_I	current on any input pin		-	1	mA
I_O	output current		-	10	mA
T_{stg}	storage temperature range		−65	+150	°C
T_{amb}	operating ambient temperature range		−40	+85	°C

CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supplies					
V_{DD}	supply voltage		2.5	6.0	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz			
		V_{DD} = 3 V	-	0.1	mA
		V_{DD} = 6 V	-	0.4	mA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz			
		V_{DD} = 3 V	-	0.35	mA
		V_{DD} = 6 V	-	2.5	mA
I_{DDO}	supply current STANDBY				
		V_{DD} = 3 V	-	3.5	µA
		V_{DD} = 6 V	-	10	µA
PTC input					
V_{IL}	input voltage LOW		−0.8	0.1 V_{DD}	V
V_{IH}	input voltage HIGH		0.9 V_{DD}	V_{DD} +0.8	V
SCL input					
V_{IL}	input voltage LOW		−0.8	0.3 V_{DD}	V
V_{IH}	input voltage HIGH		0.7 V_{DD}	V_{DD} +0.8	V
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}	-	± 1	µA
f_{SCL}	clock frequency		0	100	kHz
C_I	input capacitance	V_I = V_{SS}	-	7	pF
SDA input/output					
V_{IL}	input voltage LOW		−0.8	0.3 V_{DD}	V
V_{IH}	input voltage HIGH		0.7 V_{DD}	V_{DD} +0.8	V
V_{OL}	output voltage LOW	I_{OL} = 3 mA; V_{DD} = 2.5 V	-	0.4	V
I_{LO}	output leakage current	V_{OH} = V_{DD}	-	1	µA
C_I	input capacitance	V_I = V_{SS}	-	7	pF
Data retention time					
t_S	data retention time	T_{amb} = 55 °C	10	-	yrs

WRITE CYCLE LIMITS

The power-on reset circuit resets the I²C-bus logic with a set-up time ≤ 10 µs.

Selection of the chip address is achieved by connecting the A1 and A2 inputs to either V_{SS} or V_{DD}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{EW}	ERASE/WRITE cycle time					
		internal oscillator	5	10	25	ms
		external clock	5	-	25	ms
Endurance						
$N_{E/W}$	ERASE/WRITE cycles per byte	T_{amb} = 85 °C; $t_{E/W}$ = 5 to 25 ms	-	-	100 000	
Programming						
f_p	programming frequency		10	-	50	kHz
t_{LOW}	LOW time		5	-	-	µs
t_{HIGH}	HIGH time		5	-	-	µs
t_r	rise time		-	-	300	ns
t_f	fall time		-	-	300	ns
t_d	delay time		0	-	t_{LOW}	µs

I²C-bus PROTOCOL

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The serial bus consists of two bidirectional lines: one for data signals (SDA), and one for clock signals (SCL).
Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The following bus conditions have been defined:

Bus not busy: both data and clock lines remain HIGH.

Start data transfer: a change in the state of the data line, from HIGH-to-LOW, while the clock is HIGH defines the start condition.

Stop data transfer: a change in the state of the data line, from LOW-to-HIGH, while the clock is HIGH defines the stop condition.

Data valid: the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes transferred between the start and stop conditions is limited to seven bytes in the ERASE/WRITE mode and eight bytes in the PAGE ERASE/WRITE mode. Data transfer is unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications a low-speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined.
The PCF8594 operates in both modes.

By definition a device that sends a signal is called a "transmitter", and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

Each byte is followed by one acknowledge bit. This acknowledge bit is a HIGH level, put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse. The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.

The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse.

Set-up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

DEVICE ADDRESSING

Following a start condition the bus master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Fig. 3). For the PCF8594 this is fixed as 1010.

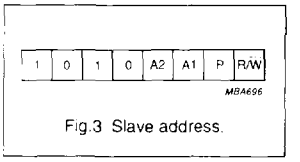


Fig.3 Slave address.

The next two significant bits address a particular device. A system could have up to four PCF8594 devices on the bus. The four addresses are defined by the state of the A1 and A2 inputs.

The next bit (bit 1) of the slave address field is the page selection bit. It is used by the host to select the upper/lower 256 bytes of memory. This is, in effect, the most significant bit for the word address.

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read operation is selected.

WRITE OPERATIONS

Byte/word write

For a write operation the PCF8594 requires a second address field. This address field is a word address providing access to any one of the 256 words of memory. Upon receipt of the word address the PCF8594 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. Word address is automatically incremented. The master can now terminate the transfer by generating a stop condition or transmit up to six more bytes of data and then terminate by generating a stop condition.

After this stop condition the ERASE/WRITE cycle starts and the bus is free for another transmission. Its duration is 10 ms per byte. During the ERASE/WRITE cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

PAGE WRITE

The PCF8594 is capable of a eight-byte page write operation. It is initiated in the same manner as the byte write operation. The master can transmit eight data bytes within one transmission. After receipt of each byte the PCF8594 will respond with an acknowledge.

After the receipt of each data byte the three low order bits of the word address are internally incremented. The high order five bits of the address remain unchanged. If the master transmits more than eight bytes prior to generating the stop condition, no acknowledge will be given on the ninth (and following) data bytes and the whole transmission will be ignored. As in the byte write operation, all inputs are disabled until completion of the internal write cycles. The typical duration of a page write is 45 ms.

Note

A write to the EEPROM is always performed if the pin WP is LOW. If WP is HIGH, then the upper half of the EEPROM is write-protected and no acknowledge will be given by the PCF8594 when one of the upper 256 EEPROM cells is addressed. However, an acknowledge will be given after the slave address and the word address.

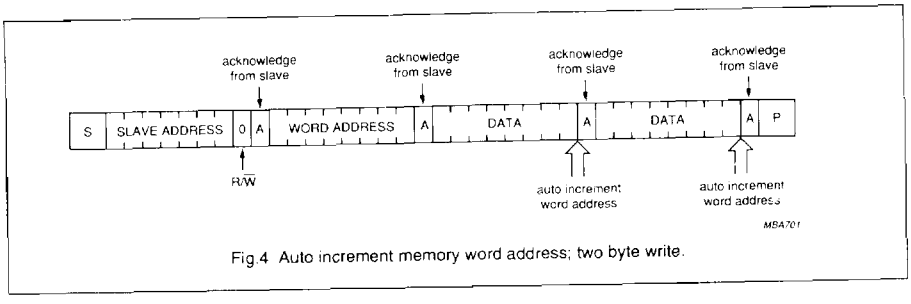


Fig.4 Auto increment memory word address; two byte write.

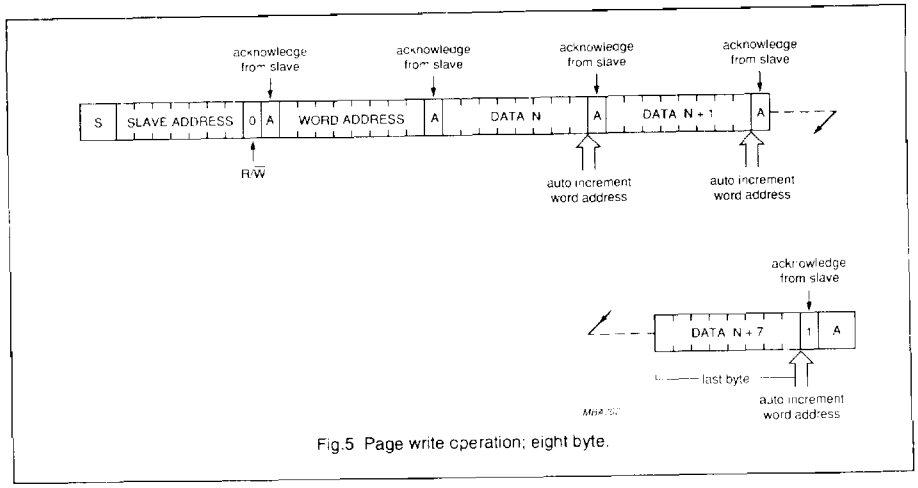


Fig.5 Page write operation; eight byte.

READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the LSB of the slave address is set to logic 1. There are three basic read operations; current address read, random read and sequential read.

Note

The lower 8-bits of the word address are incremented after each transmission of a data byte (read or write). The MSB of the word address, which is defined in the slave address, is not changed when the word address count overflows. Thus, the word address overflows from 255 to 0 and from 511 to 256.

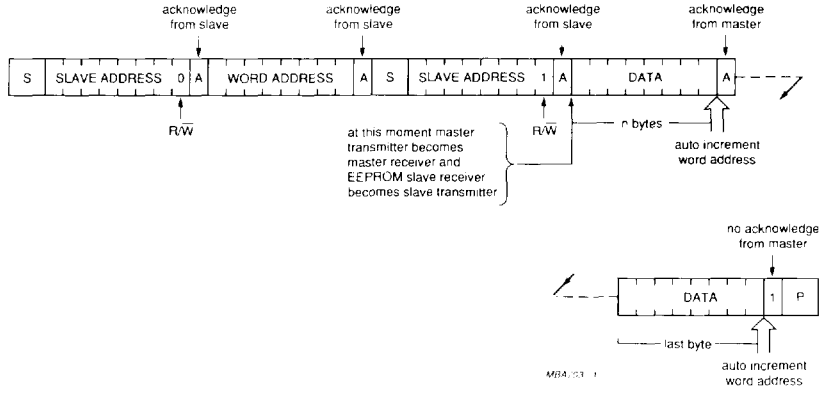


Fig.6 Master reads PCF8594 slave after setting word address (WRITE word address; READ data).

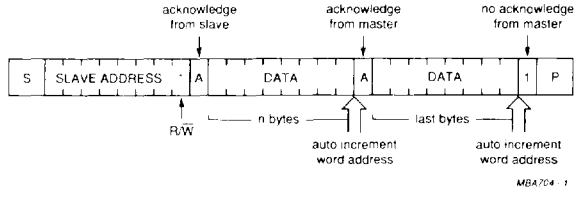


Fig.7 Master reads PCF8594 immediately after first byte (READ mode).

I²C-bus TIMING

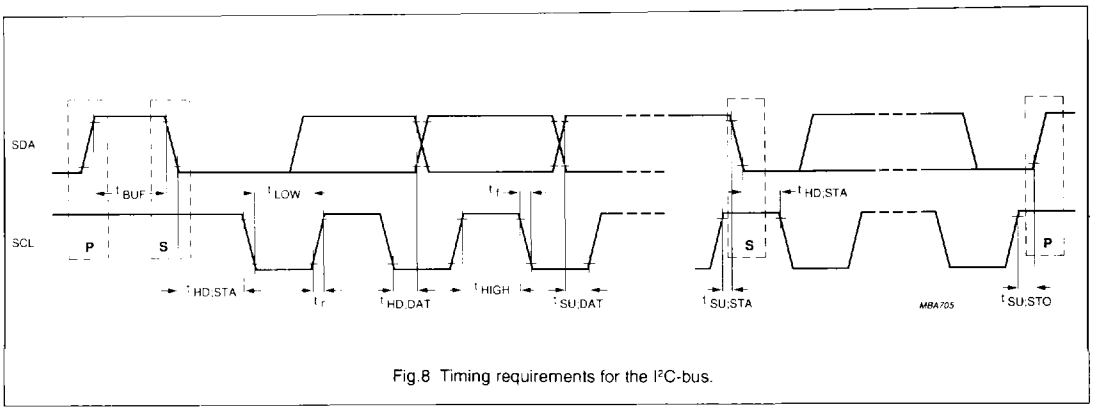


Fig.8 Timing requirements for the I²C-bus.

I²C-bus CHARACTERISTICS

(note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{SCL}	clock frequency		0	100	kHz
t_{BUF}	time the bus must be free before a new transmission can start		4.7	-	µs
$t_{HD;STA}$	start condition hold time after which first clock pulse is generated		4.0	-	µs
t_{LOW}	clock period LOW		4.7	-	µs
t_{HIGH}	clock period HIGH		4.0	-	µs
$t_{SU;STA}$	set-up time for start condition	repeated start	4.7	-	µs
$t_{HD;DAT}$	data hold time for bus compatible masters		5	-	µs
$t_{HD;DAT}$	data hold time for bus devices	note 2	0	-	ns
$t_{SU;DAT}$	data set-up time		250	-	ns
t_r	SDA and SCL rise time		-	1	µs
t_f	SDA and SCL fall time		-	300	ns
$t_{SU;STO}$	set-up time for stop condition		4.7	-	µs

Notes to the I²C-bus characteristics

1. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
2. The hold time required to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter. It is not greater than 300 ns.

EXTERNAL CLOCK TIMING

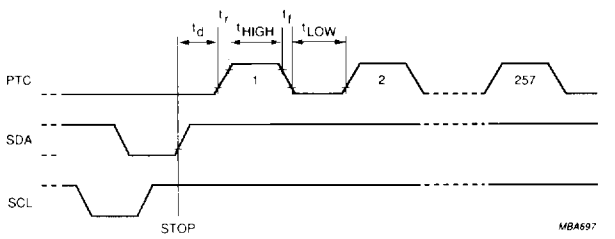


Fig.9 One byte ERASE/WRITE cycle.

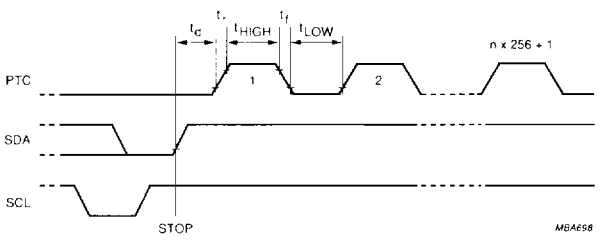


Fig.10 n byte ERASE/WRITE cycle (n = 2 to 7).

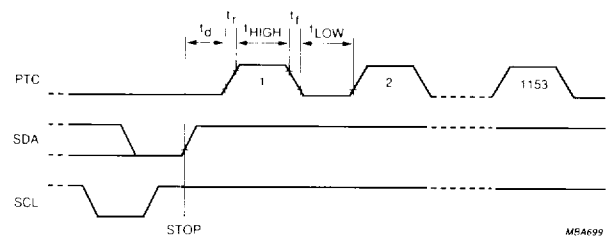
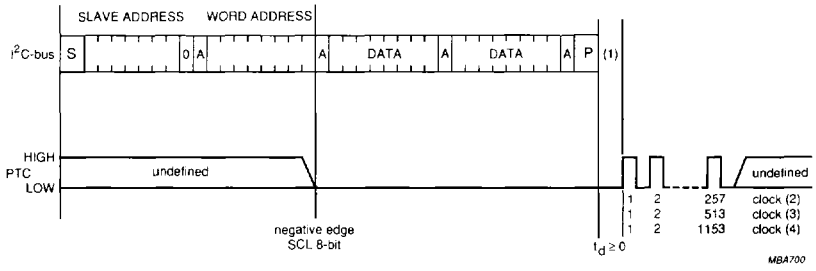


Fig.11 Page mode.



(1) If an external clock is chosen, this information is latched internally by setting pin 7 (PTC) LOW after transmission of the eight bit of the word address (negative edge of SCL). Thus the state of pin 7 may be previously undefined. Leaving pin 7 LOW causes a higher standby current.

(2) 1-byte programming.

(3) 2-byte programming.

(4) One page (8 byte) programming.

Fig.12 External clock.