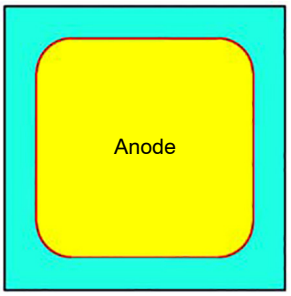
Silicon Carbide (SiC) Schottky Diode – EliteSiC, 10 A, 1200 V, D1, Die

PCFFS10120AF



Description

Silicon Carbide (SiC) Schottky Diode has no switching loss, provides improved system efficiency against Si diodes by utilizing new semiconductor material – Silicon Carbide, enables higher operating frequency, and helps increasing power density and reduction of system size/cost. Its high reliability ensures robust operation during surge or over−voltage conditions.

Features

- Max Junction Temperature 175°C
- Avalanche Rated 105 mJ
- High Surge Current Capacity
- Positive Temperature Coefficient
- Ease of Paralleling
- No Reverse Recovery / No Forward Recovery

Applications

- General Purpose
- SMPS, Solar Inverter, UPS
- Power Switching Circuits

Die Information

- Wafer Diameter: 6 inch
- Die Size: 2,280 × 2,280 μm (Include Scribe Lane)
- Metallization
  - Top: Ti / TiN / Al 4 μm
  - Back: Ti/ NiV / Ag
- Die Thickness: Typ. 200 μm
- Bonding Pad Size
  - Anode: 1700 × 1700 μm
- Recommended Wire Bond (Note 1)
  - Anode: 15 mil × 1

NOTE:
1. Based on TO−247 package of **onsemi**

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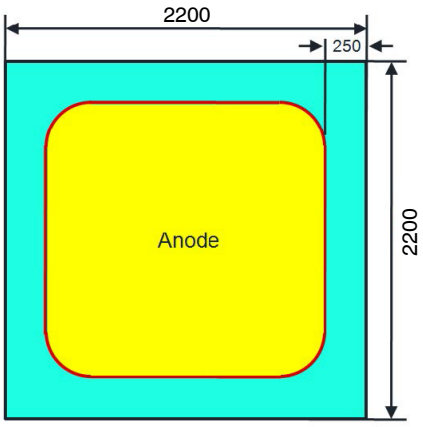
DIE LAYOUT

(Dimension: μm, Except Scribe Lane)

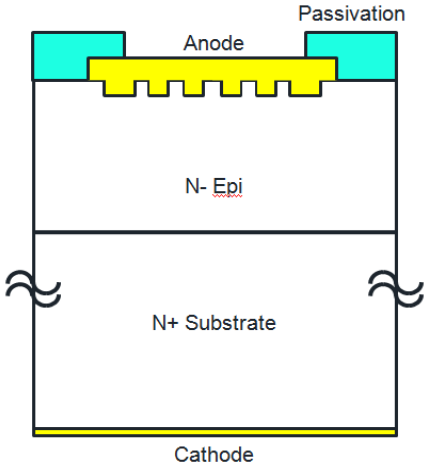


Passivation Area

Passivation Information

- Passivation Material: Polymide (PSPI)
- Passivation Type: Local Passivation
- Passivation Thickness: 90KA

CROSS SECTION



ORDERING INFORMATION

Part Number	Package	Die Size
PCFFS10120AF	N/A	2,280 × 2,280 μm (Include Scribe Lane)

ELECTRICAL CHARACTERISTICS ON WAFER (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_R	Reverse Blocking Voltage	I_R = 200 μA, T_C = 25°C	1230	–	–	V
V_F	Forward Voltage	I_F = 10 A, T_C = 25°C	1.22	–	1.723	V
I_R	Reverse Current	V_R = 1230 V, T_C = 25°C	–	–	200	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
2. Tested 100% on wafer
3. –F: sawn−on−film frame packing based on wafer tested

For Additional Product Information and Electrical Characteristics on Package

Refer to the FFSH20120ADN−F155 product datasheet.

The Configuration of Chips (Based on 6 Inch Wafer)

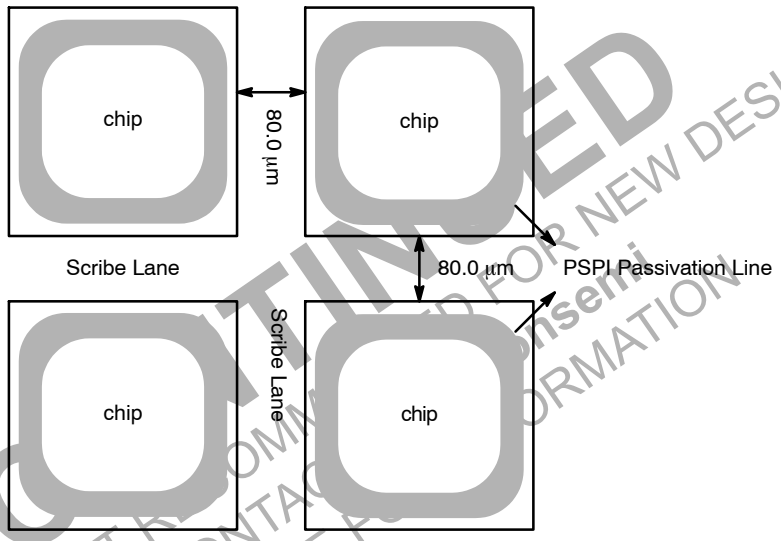


Figure 1. The Configuration of Chips (Based on 6 Inch Wafer)

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