PCGA200T65NF8M1

650 V, 200 A Field Stop Trench IGBT with Solderable Top Metal



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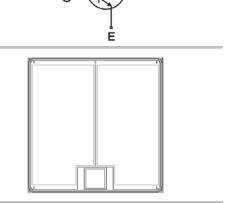
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Features

- AEC–Q101 Qualified
- Maximum Junction Temperature 175°C
- Positive Temperature Coefficient
- Easy Paralleling
- Short Circuit Rated
- Very Low Saturation Voltage: $V_{CE(SAT)} = 1.53 V(Typ.) @ I_C = 200 A$
- Optimized for Motor Control Applications
- Emitter Pad Covered with Solderable Metal Layer

Applications

- Automotive Traction Modules
- General Power Modules



ORDERING INFORMATION

| Part Number | PCGA200T65NF8M1 | | | | |
|-------------------------------|---------------------------------------|-----------------------|--|--|--|
| Packing | Water (sawn on foil) | | | | |
| | mils | μm | | | |
| Die Size | 394 × 394 | 10,000 × 10,000 | | | |
| Emitter Attach Area | 2 × (177 × 348) | 2 × (4,493.5 × 8,832) | | | |
| Gate / Sensor Pad Attach Area | 55 × 55 | 1,408 × 1,406 | | | |
| Die Thickness | 3 | 79 | | | |
| Top Metal | 5 μm AlSiCu + 1.15 μm Ti/NiV/Ag (STM) | | | | |
| Back Metal | 0.95 µm NiV/Ag | | | | |
| Topside Passivation | Silicon Nitride plus Polyimide | | | | |
| Wafer Diameter | 200 mm | | | | |
| Max Possible Die Per Wafer | 234 | | | | |

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ABSOLUTE MAXIMUM RATINGS (T_J = 25° C unless otherwise noted)

| Parameter | Symbol | Ratings | Units | |
|--|------------------|-------------|-------|--|
| Collector-Emitter Voltage | V _{CES} | 650 | V | |
| Gate-Emitter Voltage | V _{GES} | ±20 | V | |
| DC Collector Current, limited by T_J max | Ι _C | (Note 1) | А | |
| Pulsed Collector Current, V_{GE} =15 V, t_p limited by T_J max (Note 2) | I _{CM} | 600 | А | |
| Short Circuit Withstand Time, V_{GE} = 15 V, V_{CE} \le 400 V, T_J $\le 150^\circ C$ | t _{sc} | 5 | μs | |
| Operating Junction Temperature | TJ | -40 to +175 | °C | |
| Storage Temperature Range | T _{stg} | +17 to +25 | °C | |

Depends on the thermal properties of assembly
Not subject to production test – verified by design/characterization

ELECTRICAL CHARACTERISTICS (T_J = 25° C unless otherwise noted)

| Parameter | Symbol | Test Condition | | Min. | Тур. | Max. | Units |
|---|-----------------------|---|------------------------|------|------|------|-------|
| Static Characteristics (Tested on wafers) | | · | | | | | |
| Collector–Emitter Breakdown Voltage | BV _{CES} | $V_{GE} = 0 V, I_C = 1 mA$ | | 650 | - | - | V |
| Collector–Emitter Saturation Voltage | V _{CE(SAT)} | I _C = 100 A, V _{GE} = 15 V | | _ | 1.25 | 1.75 | V |
| Gate-Emitter Threshold Voltage | V _{GE(th)} | $V_{GE} = V_{CE}$, $I_C = 200 \text{ mA}$ | | 4.5 | 5.5 | 6.5 | V |
| Collector Cut–Off Current | ICES | $V_{CE} = V_{CES}, V_{GE} = 0 V$ | | - | - | 40 | μΑ |
| Gate Leakage Current | I _{GES} | $V_{GE} = V_{GES}, V_{CE} = 0 V$ | | _ | - | ±400 | nA |
| Electrical Characteristics (Not subjected | to production test – | verified by design/ | characterization) | | | | |
| Collector to Emitter Saturation Voltage | V _{CE(SAT)} | I _C = 200 A, | $T_J = 25^{\circ}C$ | - | 1.53 | 1.9 | V |
| | | V _{GE} = 15 V | T _J = 175°C | _ | 2.04 | - | V |
| Input Capacitance | CIES | V _{CE} = 30 V, V _{GE} = 0 V f = 1 MHz | | _ | 9.6 | - | nF |
| Output Capacitance | C _{OES} | | | - | 445 | - | pF |
| Reverse Transfer Capacitance | C _{RES} | | | - | 78 | - | pF |
| Internal Gate Resistance | R _G | f = 1 MHz | | - | 2.0 | - | Ω |
| Total Gate Charge | Q _{G(Total)} | V _{CE} = 400 V, I _C = 200 A V _{GE} = 15 V | | - | 229 | - | nC |
| Gate-to-Emitter Charge | Q _{GE} | | | - | 66 | - | nC |
| Gate-to-Collector Charge | Q _{GC} | | | - | 64 | - | nC |
| Turn–On Delay Time | t _{d(on)} | $V_{CE} = 400 \text{ V}, I_{C} = 200 \text{ A} \\ R_{G} = 15 \Omega \\ V_{GE} = 15 \text{ V} \\ \text{Inductive Load} \\ T_{J} = 25^{\circ}\text{C}$ | | - | 67 | - | ns |
| Rise Time | t _r | | | - | 233 | - | ns |
| Turn–Off Delay Time | t _{d(off)} | | | _ | 118 | - | ns |
| Fall Time | t _f | | | - | 177 | - | ns |
| Turn–On Delay Time | t _{d(on)} | $V_{CE} = 400 \text{ V}, \text{ I}_{C} = 200 \text{ A}$ $R_{G} = 15 \Omega$ $V_{GE} = 15 \text{ V}$ Inductive Load $T_{J} = 175^{\circ}\text{C}$ | | - | 64 | - | ns |
| Rise Time | t _r | | | _ | 236 | - | ns |
| Turn–Off Delay Time | t _{d(off)} | | | _ | 124 | - | ns |
| Fall Time | t _f | | | _ | 208 | - | ns |

3. For ordering, technique and other information on Onsemi automotive bare die products, please contact automotivebaredie@onsemi.com

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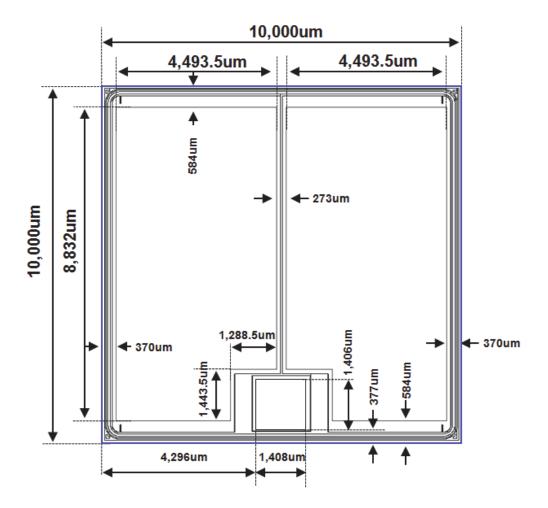


Figure 1. Dimensional Outline and Pad Layout

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