DATA SHEET

PCF7900

PCH7900

Fractional-N Transmitter IC (FraNTIC)

Product Specification

2007 Dec 13

Confidential

CONTENTS

1 GENERAL INFORMATION

1.1 Features

- Fully integrated fractional-N PLL frequency synthesizer
- Integrated VCO without external components
- Independent Power down modes for oscillator and PLL
- Operating frequency: 315/434/869/915 MHz ISM/SRD bands
- OOK / ASK / FSK modulation
- Software programmable output power
- Software programmable modulation index for ASK
- Software programmable frequency deviation for FSK
- Software programmable multi channel capability
- Software programmable crystal trimming capability
- Low power operation
- Very low external component count
- Low pin-count
- Very small package

1.2 General Description

The UHF ASK/FSK Fractional-N Transmitter IC (FraNTIC) is intended for future integration with the NXP MRKII micro-controller. For this purpose, FRANTIC is implemented in sophisticated SI CMOS technology. The device provides a fully integrated fractional-N phase locked loop (PLL) frequency synthesizer and a power amplifier to drive an external antenna.

FRANTIC is especially designed for use in the ISM frequency bands (315/434/868/915 MHz). Fine-tuning of the reference oscillator by means of fractional-N synthesis allows the compensation of manufacturing tolerances of the crystal. The device also includes an adjustable output power capability.

FRANTIC can be used for both ASK and FSK modulation with data rates up to 40 kBit/s. Due to the high level of integration, only few external components are needed to build up a complete transmitter.

2 ORDERING INFORMATION

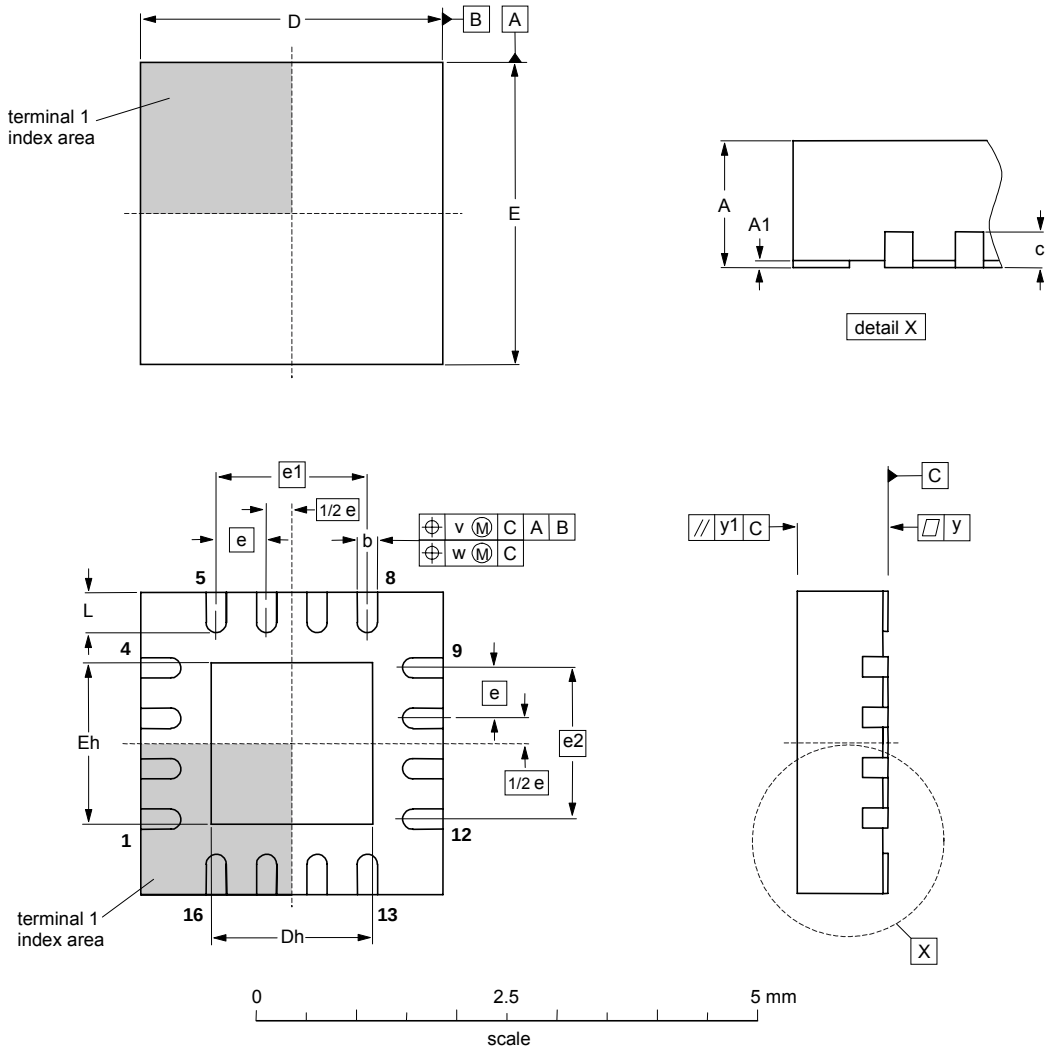
EXTENDED TYPE NUMBER	DESCRIPTION	PACKAGE		TEMPERATURE RANGE (°C)
		NAME	OUTLINE VERSION	
PCF 7900NHN	PA Capacitor 0pF	HVQFN16	SOT758-1	-40°C to +85°C
PCF 7900VHN	PA Capacitor Range 0 to 5pF			
PCH 7900NTT	PA Capacitor 0pF	TSSOP16	SOT403-1	-40°C to +125°C
PCH 7900VTT	PA Capacitor Range 0 to 5pF			

Note

1. Due to package constraints, the TSSOP16 type is suited for operation up to 460 MHz only.
2. The HVQFN package features an exposed die attach pad and shall be connected to GND in case it is being connected or shall not be connected at all.

3 PACKAGE OUTLINE

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.85 mm **SOT758-1**



DIMENSIONS (mm are the original

UNIT	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.75 1.45	3.1 2.9	1.75 1.45	0.5	1.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

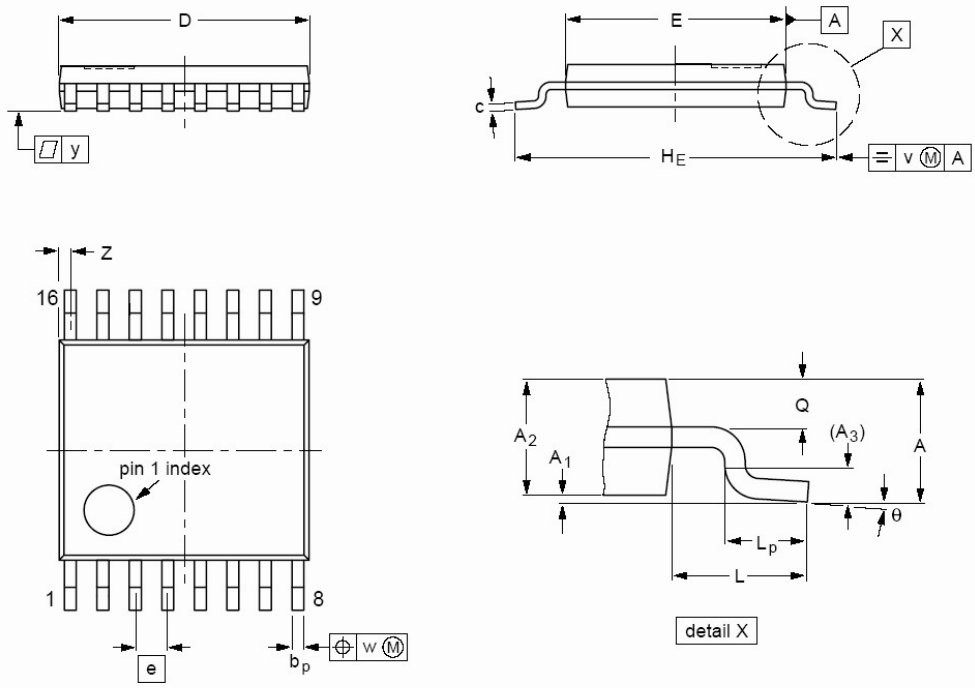
Note

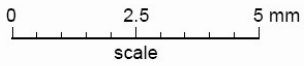
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT758-1	- - -	MO-220	- - -			~~02-03-25~~ 02-10-21

Figure 1. Package Outline HVQFN16

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Figure 2. Package Outline TSSOP16

4 PNNING INFORMATION

4.1 Pin Assignment

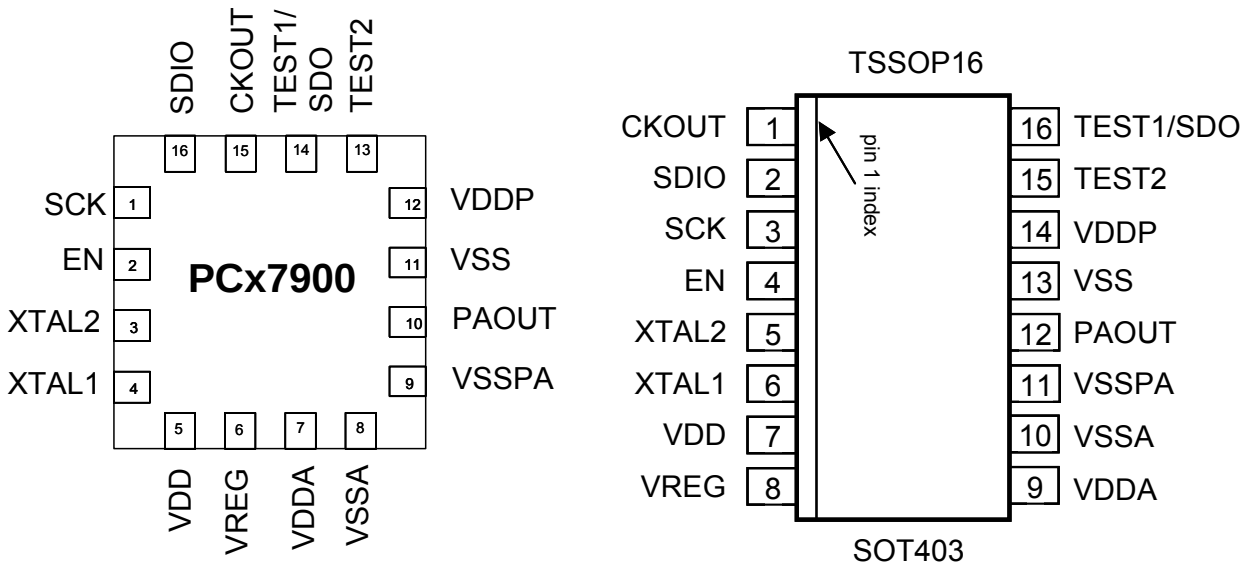


Figure 3. Pin Assignment (Top View)

4.2 Pin Description

Table 1 Pin Description

SYMBOL	PIN		FUNCTION	NOTE
	HVQFN	TSSOP		
SCK	1	3	Serial interface clock input	
EN	2	4	Enable input	
XTAL2	3	5	Crystal oscillator 2	
XTAL1	4	6	Crystal oscillator 1	
VDD	5	7	Positive supply	
VREG	6	8	Voltage regulator output	
VDDA	7	9	Analogue PLL supply	
VSSA	8	10	Analogue ground	
VSSPA	9	11	Power amplifier ground	
PAOUT	10	12	Power amplifier output	
VSS	11	13	Digital ground	
VDDP	12	14	Digital PLL supply	
TEST2	13	15	Test output	
TEST1/ SDO	14	16	Test output or Serial Data Output	
CKOUT	15	1	Clock output	
SDIO	16	2	Serial interface data input-output	

Note

1. The HVQFN package features an exposed die attach pad that must be connected to GND in case it is being connected or shall not be connected at all.

5 FUNCTIONAL DESCRIPTION

5.1 Functional Block Diagram

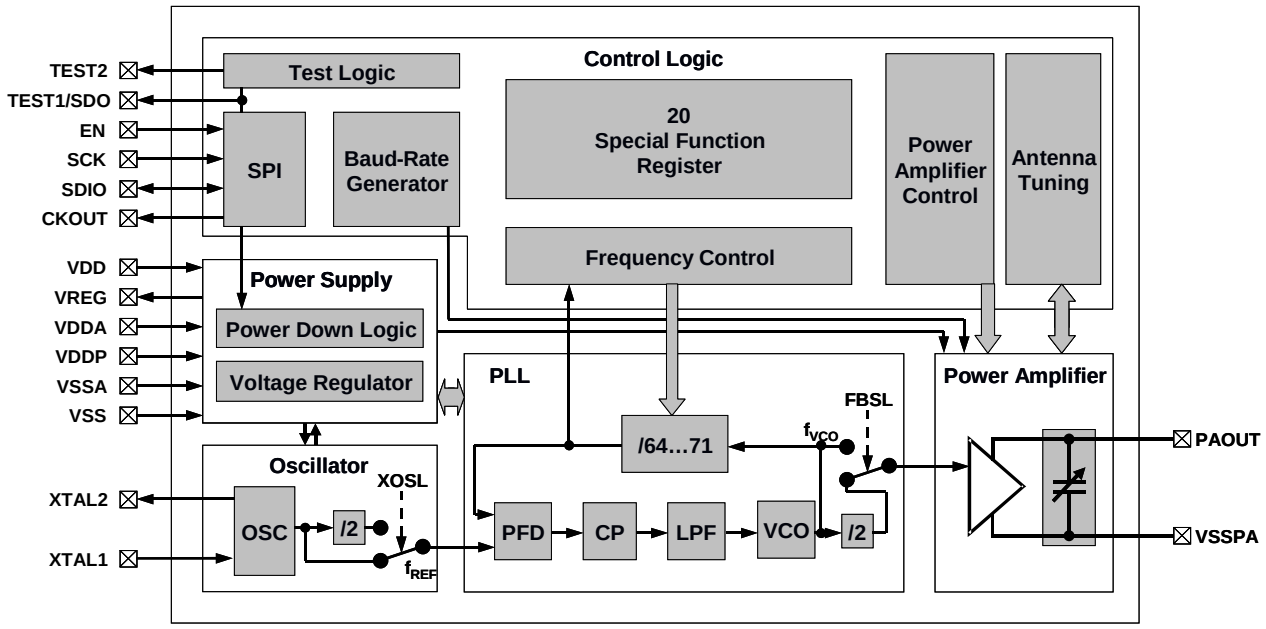


Figure 4. Functional block diagram

5.2 Functional Blocks Overview

5.2.1 Power Management, Voltage Regulator

The supply voltage source is connected between the VDD and the VSS, VSSA and VSSPA pins.

An integrated low-dropout voltage-regulator is used to supply the PLL and the PA-driver with a reduced, regulated voltage. This helps keeping the current consumption and the supply voltage dependencies of the PLL as low as possible. The output of this regulator is the VREG pin. This pin has to be connected to an external blocking capacitor in order to guarantee stability of the regulator. A recommended set-up is shown in Figure 29.

Two different regulator modes are available, for a detailed description see section 5.6

Pin VDDA is the positive supply voltage of the analogue part of the PLL, pin VDDP is the positive supply of the PLL prescaler and the PA-driver stage. Both pins should be connected to VREG.

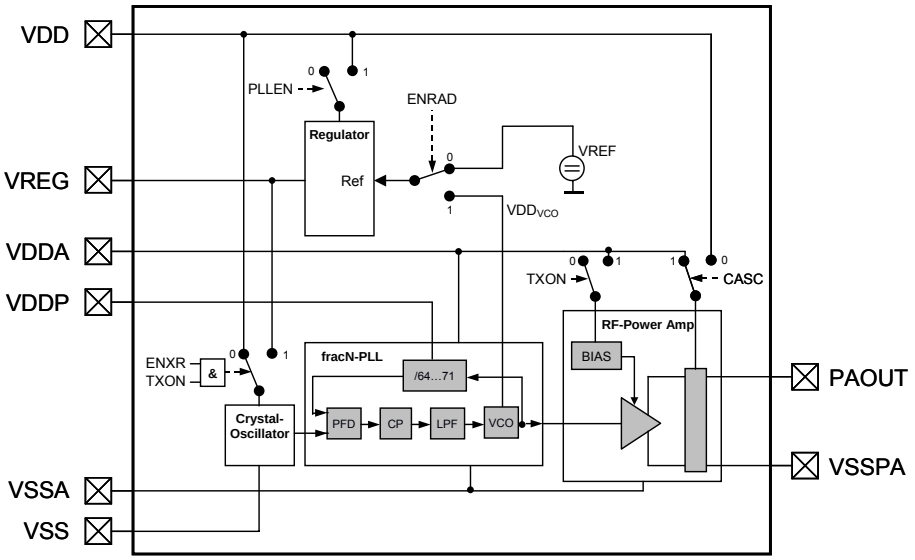


Figure 5. Power management

5.2.2 Interface and Control Logic

5.2.2.1 configurable 3 or 4 wire interface

The PCx7900 can be configured via a simple SPI interface. The interface itself can be configured for 3 or 4 wire mode, the latter one uses pin TEST1 as serial data output SDO where the SDIO is used as input (see Figure 4. Peripheral connection diagram)

EN

The EN pin has to be set to enable communication via the 3 or 4-wire serial interface. If the EN pin is kept low for at least 2^{16} XTAL clocks, the transmitter device will be reset, the bit-counter implemented inside the SPI counting the already transferred bits shall be set to zero, SCK and SDIO are disabled and the device will enter the power down mode (also the crystal oscillator is switched off). If the 4-wire interface has been used, a reset would also deactivate the SDO pin (set to tristate, ENSDO is not influenced).

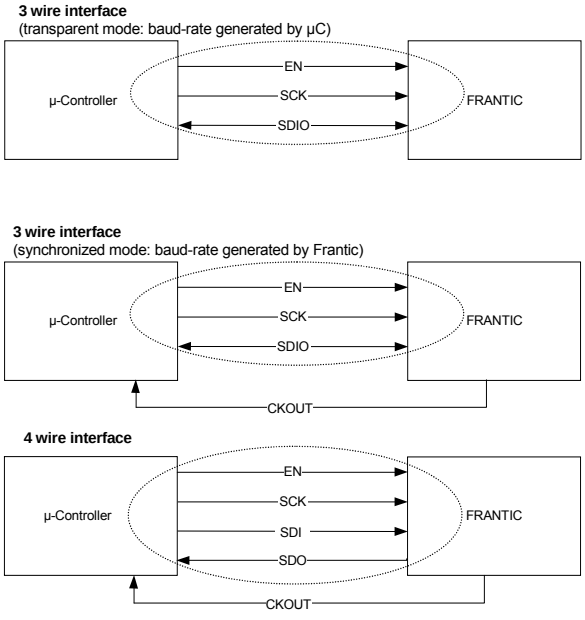


Figure 6. Peripheral connection diagram

After a transmit command the EN pin has an additional function: At the falling edge of the EN pin the level of the SDIO pin is latched and directly connected to the modulator input. In this case it is possible to intercept the RF-data transmission without deactivating the PA and to loop the last transmitted bit while the SDIO interface is used for SFR configuration. But notice, EN must not be low for more than 2^{16} XTAL clocks otherwise the device will be reset.

SCK

SCK is the clock input for the serial interface. Depending on the start-up condition of SCK at the rising edge of EN (see 5.9.2) each rising/falling edge of SCK shifts data into or gets data from the SPI register-set. During RF data transmission SCK is don't care (signal on SCK has no influence on interface).

SDIO

SDIO is the configurable bi-directional data input/output pin of the serial interface. By default, the bi-directional mode is configured, so SDIO is used for both input and output data transmission. If ENSDO in register ACON2 is set, SDIO is used as input only and TEST1 is configured as data output SDO (4 wire interface) . The SDO pin is high ohmic until data is written.

Table 2 serial data output / TEST1 control (ENSDO)

ENSDO	SDO/TEST1 control state
0	pin TEST1 not used (only for test purposes)
1	pin TEST1 used as SDO (serial data output)

Data In or Data Out operation is adapted automatically during SPI communication sequences.

Command Overview:

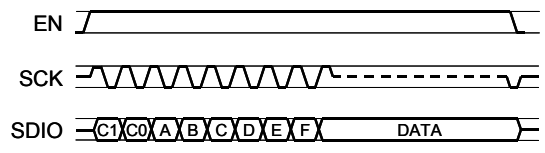


Figure 7. Command Overview

C1	C0	Command	A-F
0	0	write SFR	Start address A5..A0
0	1	read SFR	Start address A5..A0
1	0	transmit	transmit options
1	1	antenna tune	transmit options

5.2.3 Reference Oscillator

The reference oscillator is of Pierce type with automatic amplitude regulation and gain control to reduce the total current consumption. The device pins XTAL1 and XTAL2 connect the internal circuitry to the external reference crystal resonator and the load capacitances. To get oscillation on the specified crystal frequency the input capacitances of the two XTAL pins and PCB parasitics have to be considered. The oscillator typically operates at frequencies ranging from 9 MHz to 19 MHz to achieve the allowed transmit frequencies.

5.2.4 Baud Rate Generator

The output-pin of the integrated baud-rate generator, CKOUT, will provide a clock, which is derived from the XTAL clock frequency. The baud rate is programmable by a special function register-set (BDSEL, SCSEL). CKOUT is not always active. (see chapter 0)

5.2.5 Power Amplifier

The Power Amplifier is driven from the PLL synthesizer and operates in single ended fashion, according to

Figure 11.

The Power Amplifier output (pin PAOUT) requires an external DC path to pin VBAT, established by the antenna loop or a dedicated bias coil. A dedicated ground pin (VSSPA) is provided to improve the RF properties of the circuitry. Pin VSSPA must be connected with pin VSS. Best efficiency is achieved, if the output voltage swing at pin PAOUT yields one volt less than two times the supply voltage: $V_{PAOUT\ PP} \sim 2\ (V_{VDDA} - 0.5V)$.

Three special-function-registers ACON0, ACON1 and ACON2 are available to control the output power of the 4 binary weighted output stages.

The Power Amplifier also features three regulated and one unregulated (high power) output power modes, as selected by the control bits PAM1 and PAM0 located in the TXCON register. In regulated mode the input drive level of the amplifier is derived from an internal reference voltage and so the output power is stabilized against supply voltage and temperature variations over a large degree.

5.3 Transmitter operating modes

Power down mode

If the EN pin is kept low for at least 2^{16} XTAL clocks (~5ms at 13.08MHz crystal frequency), the transmitter (PLL, power amplifier and crystal oscillator) will be reset, the bit-counter inside the SPI counting the already transferred bits is set to zero, SCK and SDIO are disabled (also SDO, if used) and the device will enter the power down mode. In this state the TXCON bit PLLEN is cleared. The total current consumption is almost zero.

Another possibility to enter the power down mode is to set the PD bit in the TXCON register.

When the Power down mode is left (by rising edge of EN) the PD bit is cleared.

XTAL Active mode

With rising edge of EN the Power down mode is left and the crystal oscillator is activated. The XTAL clock will be stable after $t_{XTAL,SET}$. The SPI is activated, so the SFR's can be programmed. The XTAL Active mode can be left by either activating the PLL (set PLLEN in TXCON) or by entering the Power down mode.

PLL Active mode

If the XTAL Active mode is active and the crystal oscillator is settled, the PLL can be switched on (after $t_{XTAL,SET}$). Setting the bit PLLEN in the register TXCON directly powers on the PLL. The VCO output frequency will be stable after t_{ACQ}. This mode stays active as long as EN is kept 1 or as long EN is kept 0 for a period shorter than 2^{16} XTAL clock cycles. If EN is kept 0 for a longer period or the PD bit in TXCON is set, the device returns to Power down mode. By resetting the PLLEN bit in TXCON the PLL is turned off and XTAL Active mode is entered again. Another possibility to leave the PLL active mode is to send a dedicated SPI command (antenna tune or transmit command).

Antenna Tune mode

To enter the Antenna Tune mode a dedicated SPI command, the antenna tune command, has to be sent when the device is in PLL Active mode. It is also possible to send the antenna tune command when in Transmitter Active mode. The Antenna Tune mode will then be kept while EN remains high. During the antenna tune command the SPI output (either SDIO or SDO, depending on the configuration of the SPI interface – see Table 2) has to be checked for a negative edge indicating the tuned state. By setting EN to 0 the antenna tune command is finished and the PLL active mode (or Transmitter Active mode – depending on the configuration settings) is entered again.

Transmitter Active mode

The Transmitter Active mode can only be entered upon a SPI command. This only is possible if the PLLEN bit is set (with a previous SPI command). Dependent of the configuration coded into the transmit command, the Transmitter Active mode can be left when either EN set low directly, or when EN is set low in a synchronized way with the edge of the last data-bit (in both cases the PLL Active mode is entered) or upon direct SPI register setting (then XTAL Active mode is entered). If a POR or power fail condition occurs during a transmit sequence, the XTAL Active mode is entered.

By setting the PD bit in TXCON the transmitter is turned off and the device enters the Power down mode. This also happens if EN is kept 0 for a period longer than 2^{16} XTAL clocks.

When the device is in the Transmitter Active mode SPI communication (change of register contents) is possible (depending on the configuration settings), if it is done within one bit (or during a constant bit stream).

For this feature EN has to be set low right after the beginning of one transmitted bit and set high again. Then SPI communication is enabled for commands. Afterwards transmitting new data can be activated again with another dedicated transmit command. During the SPI communication the transmitted data will keep unchanged. It is also allowed to send an antenna tune command when the device is in Transmitter Active mode.

With the first transmitted string the power amplifier is activated and (only here!) the baud rate generator is reset. When the transmit-phase is interrupted with an SPI communication and the transmit-phase is re-started, the baud rate generator will keep synchronized with the previous string. No jitter will occur, when switching from the previous to the next string.

After the transmission of data-bits the PLLEN bit can be read. The brown out detection monitors the actual regulated supply voltage and indicates proper supply-condition during the whole transmission phase. If PLLEN is cleared the supply voltage has dropped below the minimum required voltage level and the transmission will be interrupted. To restart a transmission a new transmit command has be sent after the PLL is enabled again.

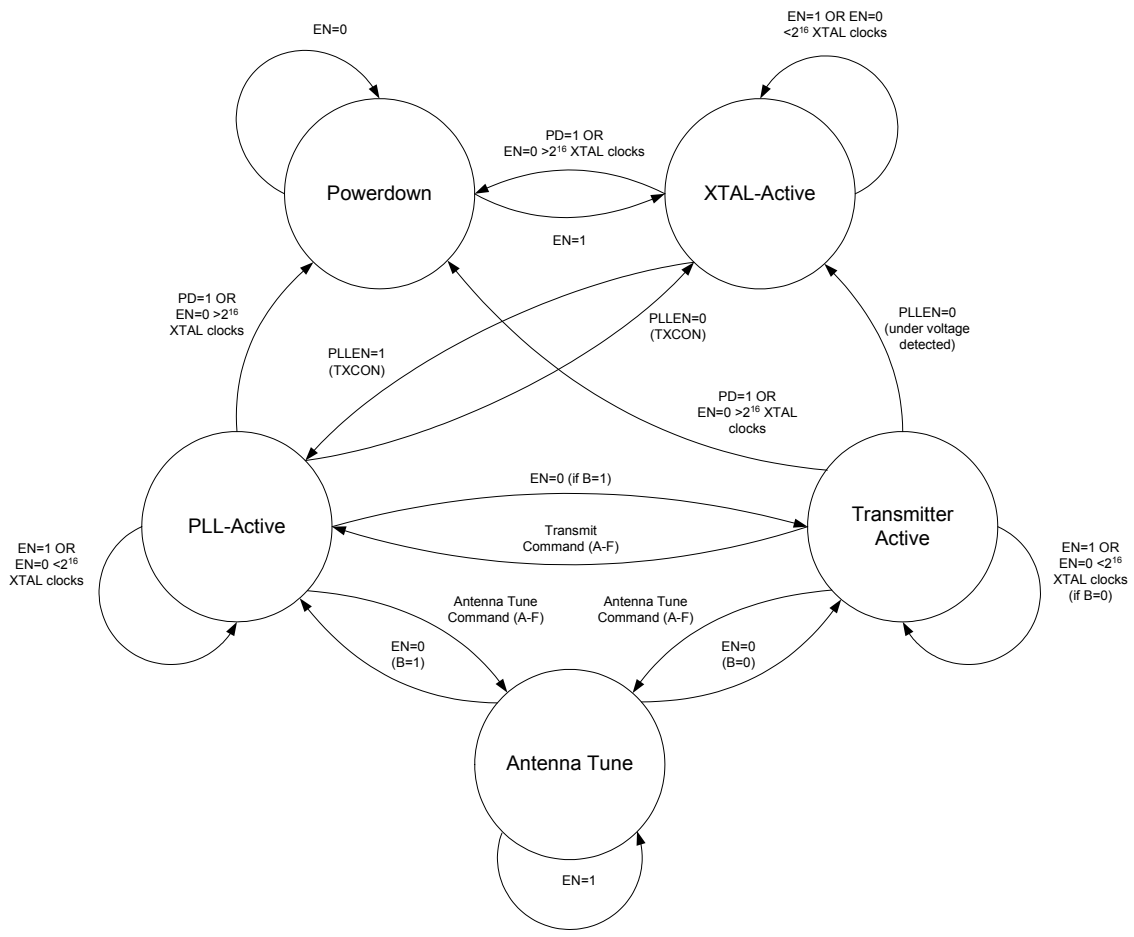


Figure 8. State Diagram

5.4 Reference Clock generation

The crystal frequency is used as reference for the fractional-N PLL as well as for baud-rate generation.

The oscillator is designed to work in parallel resonance mode of the crystal. In addition two external load capacitances are required to operate the crystal at the specified nominal frequency. For a calculation of the required capacitances the pin capacitors at XTAL1 and XTAL2 and the parasitic PCB stray capacitances have to be considered. The total load capacitance C_{LOAD} is given by:

$$C_{load} = \frac{1}{\frac{1}{C_{load1} + C_{XTAL1}} + \frac{1}{C_{load2} + C_{XTAL2}}} + C_{par,PCB}$$

Table 3 load capacitance calculation parameters

Variable	Description	Note
C_{load1}	load capacitor at XTAL1	
C_{load2}	load capacitor at XTAL2	
C_{XTAL1}	pin capacitor at XTAL1	
C_{XTAL2}	pin capacitor at XTAL2	
$C_{par,PCB}$	parasitic PCB capacitance	

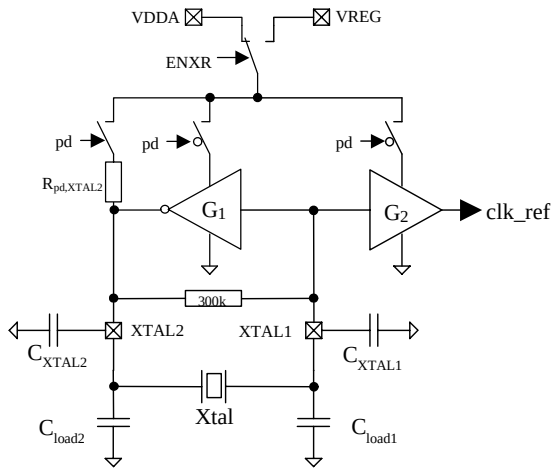


Figure 9. Crystal Oscillator Implementation

The oscillator is build by an inverting gain stage between the two XTAL-pins and a clock buffer stage in series. The feedback resistor between XTAL1 and XTAL2 is used to define the DC operating point to keep the amplifier working in linear region.

The gain stage G1 features an automatic amplitude regulation. Maximum gain is required only during oscillator start-up where a short start-up time and also a high start-up margin are needed. If the amplitude exceeds V_{supply} - 0.5V the gain is reduced to keep the current consumption as low as possible.

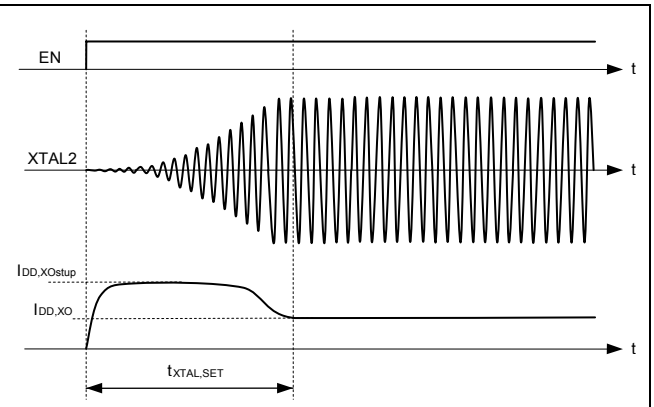


Figure 10. Crystal Oscillator Start-up

To additionally reduce the total current consumption the power supply of the crystal oscillator can be switched from VDDA to the regulated supply voltage VREG by setting the control bit ENXR in the special function register TXCON.

Table 4 oscillator supply switch (ENXR)

ENXR	selected XTAL oscillator power supply
0	VDDA, unregulated supply mode
1	VREG, regulated supply mode

If ENXR is set, the oscillator supply automatically is changed to a regulated supply when the transmit-state is entered. The XTAL supply is switched back to the unregulated supply when the transmit-state is left again.

In power down mode both gain stages are switched off and XTAL2 is defined by an internal pull-up-resistor $R_{pd,XTAL2}$.

Table 5 TXCON, Transmitter Control

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	Bit 0
PD	PDCK	XOSL	FBSL	PAM1	PAM0	ENXR	PLLEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 0EH

Drive Level:

A typical calculation of the approximate power dissipated in a crystal is:

$$P_{\max} = ESR_{\max} * \frac{(2\pi f \cdot C_{load} \cdot V_{dd})^2}{2}$$

Example:

10MHz crystal, C_{load} ~ 6pF, ESR ~ 20Ω (ESR_{max} ~ 200Ω) at V_{DD} = 3V: P_{max} = 128µW

5.5 Power Amplifier Control and ASK Modulation

For control of the output power and the modulation characteristics some special function register bits (ACON, PAM, CASC) are available.

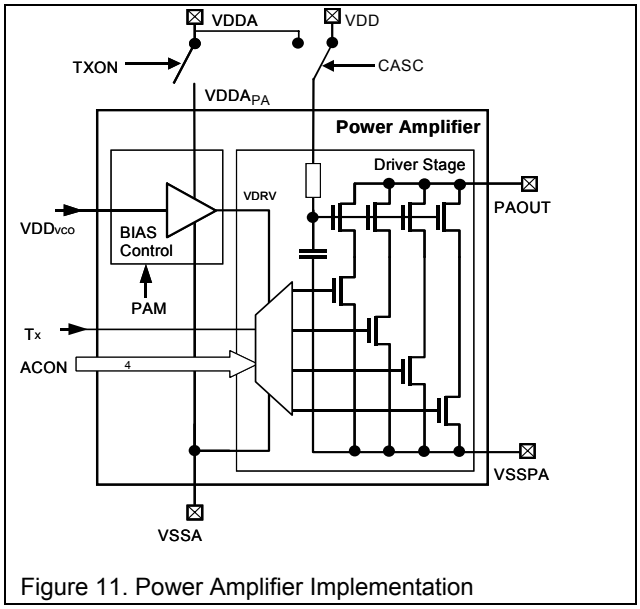


Figure 11. Power Amplifier Implementation

5.5.1 PAM0,PAM1 Power Amplifier Modes

The two bits PAM0 and PAM1 located in the special function register TXCON can be used to choose between 3 regulated und one unregulated power modes. The regulated modes should be used for applications where the output power should be independent from changes of the supply voltage and ambient temperature.

Table 6 TXCON, Transmitter Control

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	Bit 0
PD	PDCK	XOSL	FBSL	PAM1	PAM0	ENXR	PLLEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 0EH

For very high power applications the regulation mechanisms can be deactivated by using power mode 3 (see Table 7)

The lowest power mode provides the best regulation characteristics. Hence, select the lowest power mode acceptable for the application and eventually control the exact output power by means of the control signal ACON0-ACON2.

Table 7 Power Amplifier Modes

PAM1	PAM0	Power Mode	Comment	Note
0	0	0	Low power Highest stability	1
0	1	1	Medium power Medium stability	
1	0	2	High power Low stability	
1	1	3	Maximum power Stabilization OFF	

Note1: the lowest supply voltage and temperature dependency is achievable with power mode 0.

Further, the available output power is a function of the actual VCO frequency. The higher the VCO frequency, hence its supply voltage (VDD_{VCO}) is, the higher the output power becomes. To select a low VCO frequency is desirable for Japan, due to the limitation in place regarding the radiated output power.

5.5.2 ACON Power Amplifier Amplitude Control

The control registers ACON0-ACON2 control the power amplifier driver stage in all 4 power modes for either amplitude fine-tuning or ASK modulation means.

The actual output power is set by three 4-bit values in the ASK modulation control registers ACON[2..0]. Two different HIGH (AMH) levels and one LOW (AML) level are configurable.

5.5.3 ASK Settings

Amplitude modulation is achieved by switching between one of the HIGH levels (selected by the control bit “D” of the transmit-command) and the LOW level in accordance to the control signal AMOUT, which is derived from the TX-Data, see figure Figure 17 and Figure 12.

Table 8 amplitude control for ASK, FSK

ASK1	ASK0	D	Mode	Amplitude control by
x	0	0	FSK	ACON0
x	1	0	ASK	ACON0
0	x	1	FSK	ACON1
1	x	1	ASK	ACON1

ASK0 located in ACON0 and ASK1 located in ACON1 determine ASK or FSK operation.

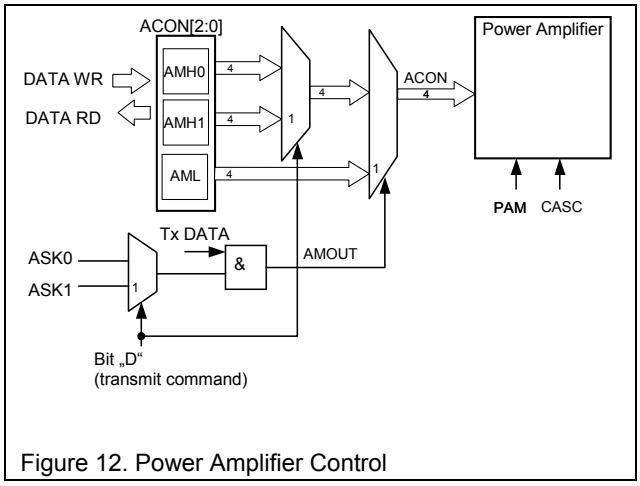


Figure 12. Power Amplifier Control

If TxDATA is low then AMOUT is low and the amplitude is determined by the value of bit “D” of the transmit command. If the bit is set, the actual high level is controlled by the 4 bits of AMH1[3:0] located in ACON1 otherwise AMH0[3:0] from ACON0 would be used if “D” is cleared.

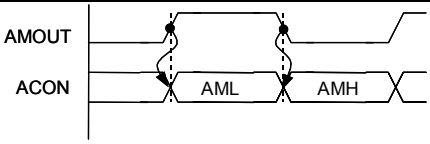


Figure 13. ASK Modulation Timing

If TxDATA is high then AMOUT is set and the amplitude is given by the content AML[3:0] in register ACON2 and the settings of ASK0 and ASK1. If “D” is cleared ASK0 located in register ACON0 determines between ASK and FSK operation otherwise if “D” is set ASK1 is used. In both cases the selected ASK bit has to be set to achieve amplitude modulation. If the selected ASK bit is cleared AMOUT is kept low and the carrier remains unmodulated (used for FSK with continuous wave operation).

Table 9 ACON0, ASK Modulation Control 0

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ASK0	X	X	X	AMH03	AMH02	AMH01	AMH00
R/W				R/W	R/W	R/W	R/W

Address = 0AH

Table 10 ACON1, ASK Modulation Control 1

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	Bit 0
ASK1	X	X	X	AMH13	AMH12	AMH11	AMH10
R/W				R/W	R/W	R/W	R/W

Address = 0BH

Table 11 ACON2, ASK Modulation Control 2

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CASC	ENRAD	ENPF	ENSDO	AML3	AML2	AML1	AML0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 0CH

5.5.4 SASK, Soft ASK mode

To reduce the ASK modulation bandwidth a “soft” modulation scheme is implemented. The soft ASK shape is modelled by a linear interpolation approach.

The switching between the selected AMH and AML value is done in a linear way. The output power is changed by switching the 4 binary weighted PA output stages with a programmable timing configured with the bits RMP[6..0] of register MRCON (modulation ramp control).

The value of RMP[6..0] specifies the number of reference clocks (derived from the crystal frequency) between two consecutive power steps. Setting the bits RMP[6..0] to 0x0h results in immediate change between the values AMH and AML (normal ASK mode).

Rem: If bit XOSL in register TXCON is set, the reference clock applied to the SASK ramp control is the crystal clock divided by a factor of 2 and the ramp time is doubled.

Table 12 MRCON, Modulation Ramp Control

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	Bit 0
x	RMP6	RMP5	RMP4	RMP3	RMP2	RMP1	RMP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 0DH

Note: MRCON is also used for soft-FSK

The configured ramp time also defines the maximum possible data rate for ASK operation. The ramp time can be calculated by:

$$t_{SASK} = (AMH - AML) * \frac{1}{f_{ref}} * MRCON[6:0]$$

For RMP[6..0] ≠ 0 the maximum baud rate is given by:

$$f_{DATA\max,SASK} = \frac{1}{2 * t_{SASK}}$$

For RMP[6..0] = 0 (normal ASK mode) the maximum baud rate is only limited by the baud rate generator (see section 11) and the maximum channel bandwidth.

5.5.5 CASC, cascode control signal

For a further improvement of the supply voltage stability also for high power modes, the cascode stage can be switched to the regulated power supply by setting the bit CASC located in register ACON2. But one should notice that the maximum output power is reduced compared to the maximum available power in power mode 3.

Table 13 cascode control flag (CASC)

CASC	cascode control state
0	cascode stage switched to VDD
1	cascode stage switched to VDDA (regulated)

5.6 Voltage regulation and power fail detection

The integrated line-regulator supports two different operation modes. The default mode is called “fixed low” mode where the regulated supply voltage is derived from an internal, transistor threshold voltage based reference**.** After start-up of the PLL the second mode called adaptive mode can be entered by setting the SFR bit ENRAD.

5.6.1 ENRAD, enable regulator adaptive mode

If set, the line regulator is switched to adaptive mode where the output voltage at VREG is directly derived from the VCO’s power supply.

Important: ENRAD must not be set until the PLL start-up has finished. It is strongly recommended to use the fixed mode during PLL start-up.

Table 14 voltage regulator control (ENRAD)

ENRAD	voltage regulator state
0	fixed output voltage, derived from internal reference
1	adaptive mode: regulated supply derived from VCO supply voltage

5.6.2 ENPF, enable power fail detection

If set, the built in power fail detection (brown out detection) is enabled. In this case the PLL and the PA are switched off if the supply voltage at VDD is not sufficiently high to guarantee proper operation of the line regulator. This also includes the proper function of the PLL circuit.

Table 15 power fail enable signal (ENPF)

ENPF	power fail control state
0	power fail detection disabled
1	power fail detection enabled

The power fail detection can be selected for fixed and adaptive mode. The detection circuit is only active if transmission is active (the power amplifier must be enabled). It is recommended to set ENPF before the power amplifier is activated to ensure that the PLL is working properly but it is also possible to set ENPF if a transmission has already been started. In the latter case there is no guarantee that the PLL runs at the right frequency when the power amplifier is enabled.

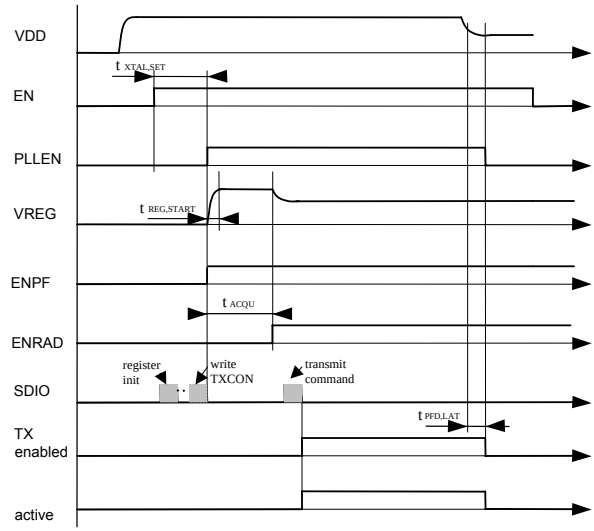


Figure 14. TX start-up timing

Once the power fail detection has detected a voltage drop at VDD during transmission so that the remaining supply voltage is not sufficient to keep the PLL in save operation the PLLEN is immediately cleared, the power amplifier will be disabled and the transmission will be stopped. The two control signals ENPF and ENRAD (if adaptive mode is used) will stay enabled. The user has to disable ENRAD before the next PLL activation otherwise a proper start-up of the PLL cannot be guaranteed.

If ENXR was set to operate the crystal oscillator with the regulated supply and the adaptive mode was active (ENRAD =1) then a power fail (and also wanted deactivation of the PA) will change the supply of the crystal oscillator from regulated to unregulated mode. If the fixed mode was used a power-fail does not influence the supply of the oscillator.

5.7 Frequency Control and FSK Operation

FSK modulation is applied if the ASK control bit of the selected ACON register is cleared. Dependent of the setting of the control-bit "D" of the transmit-command ACON0 or ACON1 are then selected for amplitude setting of the FSK transmission.(see Table 8 amplitude control)

5.7.1 Frequency Control registers

The operation frequency is set by the content of the frequency control registers FC1 to FC4, which each have a width of 18 bits. The two MSB's of all four frequency control registers are located in the register FCA. The two corresponding 'low' bytes are located in FCxH and FCxL registers. The selection of the 'active' frequency control register is done directly with the transmit command (bits "E" and "F" see section 5.9.3). Example of the complete frequency- setting for frequency configuration 1:

SFR	FCA		FC1H							
Bit	F1C17	F1C16	F1C15	F1C14	F1C13	F1C12	F1C11	F1C10	F1C9	F1C8
FCON	17	16	15	14	13	12	11	10	9	8

SFR	FC1L							
Bit	F1C7	F1C6	F1C5	F1C4	F1C3	F1C2	F1C1	F1C0
FCON	7	6	5	4	3	2	1	0

Figure 15. frequency control bits

5.7.2 PLL operation frequency f_{VCO}

The PLL operation frequency is calculated by the following equations:

$$F_{VCO} = F_{ref} \times \left(\frac{FC + 0.5}{32768} + 65 \right)$$

frequency step width:

$$F_{VCOstep} = \frac{F_{ref}}{32768}$$

Table 16 PLL operation frequency calculation parameters

Variable	Description	Note
F_{VCO}	VCO frequency	
F_{REF}	PLL reference frequency	1
$F_{VCOstep}$	minimum VCO frequency step	
F_{XTAL}	XTAL oscillator frequency	
F_{RF}	RF frequency on PAOUT	
FC	Frequency control value (FCx register)	2

Note:

1. F_{REF} can be set to F_{XTAL} / 2 by a test-mode bit
2. in order to avoid fractional-N overflow don't use values above 163839

$F_{REF} = F_{XTAL}$
$F_{RF} = F_{VCO}$ for 868/915 MHz bands (FBSL set to 1)
$F_{RF} = F_{VCO}$ / 2 for 315/434 MHz bands (FBSL set to 0)
FC = 0…163839

5.7.3 PLL frequency deviation (FSK)

The FSK frequency deviation is set as part of the FCON (FSK modulation control) register and has a width of 8 bits.

Table 17 FCON, Modulation Control

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	Bit 0
FSK7	FSK 6	FSK 5	FSK 4	FSK 3	FSK 2	FSK 1	FSK 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 09H

FSK deviation is calculated by:

$$F_{DEV} = \pm F_{ref} \times \frac{FSK_{DEV}}{16384}$$

Table 18 PLL frequency deviation calculation parameters

Variable	Description	Note
F_{DEV}	FSK frequency deviation	
FSK_{DEV}	FSK deviation value (FCON register)	
F_{REF}	PLL reference frequency	1

Note:

1. F_{REF} can be set to F_{XTAL} / 2 by a test-mode bit

$F_{REF} = F_{XTAL}$
FSK_{DEV} = 0..255

Table 19 Frequency selection limits

ISM-Band [MHz]	F_{XTAL} [MHz]	$F_{RF,min}$ [MHz]	$F_{RF,max}$ [MHz]	$F_{RF,step}$ [Hz]	$F_{DEV,min}$ [+/-kHz]	$F_{DEV.max}$ [+/-kHz]	$F_{DEV,step}$ [Hz]
315	9.185183	298.51852	321.48127	140.15	0,560	143	560
434	13.08148	425.14815	457.85155	199.61	0,800	204	800
868	12.85185	835.37038	899.62903	392.21	0,785	200	785
915	13.55555	881.11112	948.88826	413.68	0,827	211	827

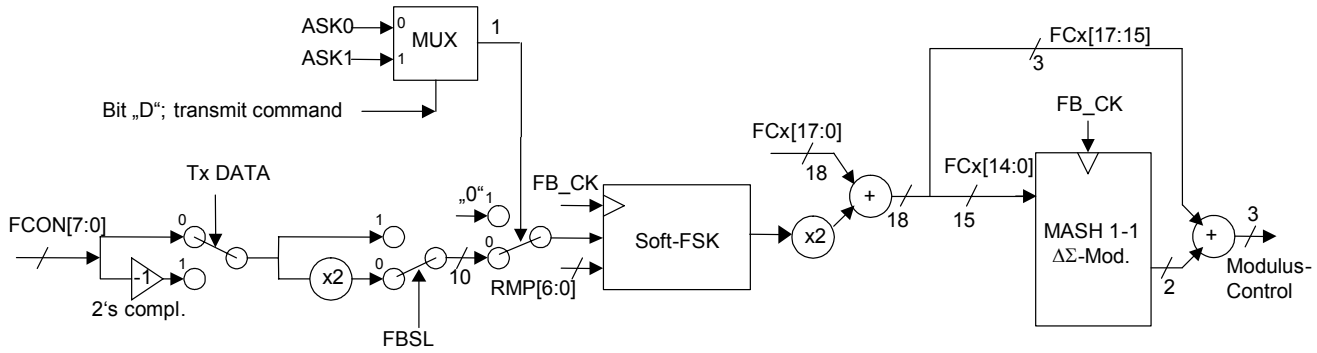


Figure 16. FSK-Circuitry and Delta-Sigma Modulator

5.7.4 oscillator and feedback divider settings

In order to allow operation for all ISM bands different oscillator divider and PLL divider settings can be selected with the special function register bits XOSL and FBSL located in register TXCON. See also Figure 4.

Table 20 TXCON, Transmitter Control

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	Bit 0
PD	PDCK	XOSL	FBSL	PAM1	PAM0	ENXR	PLLEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 0EH

Setting the bit XOSL enables the XTAL clock divider that lowers the reference clock frequency of the PLL by a factor of 2. This allows for example the use of an 18MHz crystal for the 315MHz ISM band.

If the bit FBSL is set, the power amplifier is driven by the VCO frequency. FBSL has to be set to one if the 868MHz band or the 915MHz band is selected, otherwise it has to be cleared. In the latter case the PA is driven by the VCO frequency divided by two.

F_{XTAL} [MHz]	XOSL	FBSL	F_{PLL} [MHz]	F_{RF} [MHz]
13.08	0	0	868	434
13.08	0	1	868	868
13.08	1	0	434	217 (note1)
13.08	1	1	434	434

note1: not a valid ISM band

5.7.5 FSK mode selection

In order to achieve a narrower signal bandwidth of the FSK spectrum a GFSK like modulation, further called Soft-FSK scheme is implemented. The Soft-FSK shape is modelled by a linear interpolation approach.

The FSK frequency shifting is done in a linear way between $F_{RF} - F_{DEV}$ and $F_{RF} + F_{DEV}$.

Table 21 MRCON, Modulation Ramp Control

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	Bit 0
x	RMP6	RMP5	RMP4	RMP3	RMP2	RMP1	RMP0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 0DH

The frequency is changed with the clock of F_{REF} in a configurable number of steps stored in the register MRCON (modulation ramp control). Setting the register MRCON to 00h results in normal FSK operation.

The Soft-FSK ramp time is calculated by:

$$t_{SFSK} = (2 - FBSL)\frac{2 \cdot FSK_{DEV} \cdot RMP}{f_{REF}}$$

Example:

F_{REF} = 13.08 MHz, FCON = 0x0Fh --> F_{DEV} = ±11,975 kHz

for MRCON = 0x2Ah the frequency step width will result in:

F_{STEP} = 2 * 11,975 kHz / 42 = 570.24 Hz

5.8 Baudrate Generation

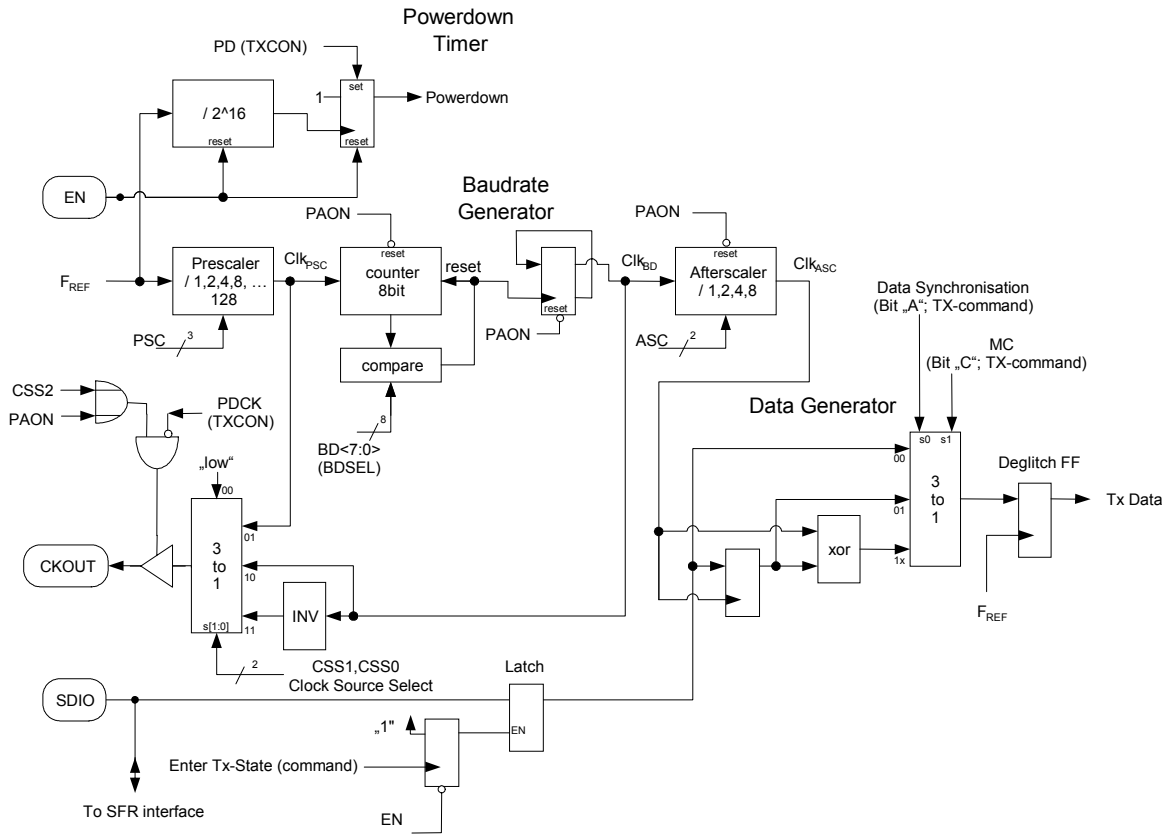


Figure 17. Serial configuration interface block diagram of baud rate and data generation

5.8.1 Baud-rate setting

Dependent on the setting of register BDSEL (baud rate selection) different baud rates for the internal transmit data stream generation can be chosen.

Table 22 BDSEL, baud rate selection

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	Bit 0
BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 0FH

The bits BD[7..0] set the division ratio of a programmable frequency divider. The input clock of this divider is influenced by prescaler ratio PSC[2:0] defined in register SCSEL. The output of this divider is fed to the baud-rate generator. See Figure 17.

The prescaler output clock is derived from the reference frequency F_{REF} divided by the prescaler ratio PSC[2:0]. The prescaler clock then is divided by (N+1) (N is the baud rate setting in the BDSEL register) and again divided by a factor of 2. (See Figure 17 and Table 23).

The Baud rate division ratio is:

$$CLK_{BD} = \frac{CLK_{PSC}}{2 \times (N+1)}$$

Note: For synchronization reasons both baud-rate counter and afterscaler are kept in reset state while the power amplifier is turned off. The prescaler will be clocked continuously whenever the XTAL oscillator is running.

Table 23 baud rate division ratio values

BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	baud rate division ratio: N
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
								….
1	1	1	1	1	1	1	1	255

5.8.2 Clock generation / selection

The special function register SCSEL contains the configuration bits CSS[2:0] for the clock source selection, the bits PSC[2:0] for the prescaler control and ASC[2:0] for the afterscaler control.

Table 24 SCSEL, Scaler selection

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	Bit 0
CSS2	CSS1	CSS0	PSC2	PSC1	PSC0	ASC1	ASC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 10H

The bit PDCK in the TXCON register determines the activity of the CKOUT signal. If PDCK is cleared, CKOUT will be active.

Table 25 TXCON, Transmitter Control

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	Bit 0
PD	PDCK	XOSL	FBSL	PAM1	PAM0	ENXR	PLLEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 0EH

CKOUT is defined with the settings of CSS[2:0] from register SCSEL and can be configured as prescaler output or baud rate output. (see table 26 Clock source selections).

If CSS2 is cleared then CKOUT is set to baud rate, prescaler or static high or low dependent on the settings of CSS1 and CSS0 if transmit state is active and set to tristate if transmission is not active.

If CSS2 is set then CKOUT is set according to the configuration of CSS1 and CSS0 and tristate mode is not entered during transmission .

Table 27 Clock source selection (CSS)

CSS2	CSS1	CSS0	CKOUT	Note
0	0	0	tristate if TX disabled; ”low” if TX enabled	
0	0	1	tristate if TX disabled; prescaler clock if TX enabled	
0	1	0	tristate if TX disabled; baud rate clock if TX enabled	
0	1	1	tristate if TX disabled; inverted baud rate if TX enabled	
1	0	0	“low”	
1	0	1	prescaler clock	1
1	1	0	“low” if TX disabled; baud rate clock if TX enabled	
1	1	1	“high” if TX disabled; inverted baud rate clock if TX enabled	

If the bit PDCK in register TXCON is set, CKOUT is set tristate (independent from the CSS[2:0] settings).

5.8.3 Prescaler

The Prescaler clock is the reference clock divided by 1,2,4,8 to 128. The division ratio is set in the PSC[2..0] bits, See Table 28 Prescaler Control

Table 28 Prescaler Control (PSC)

PSC2	PSC1	PSC0	Division ratio ($Clk_{PSC}=F_{REF}/2^N$)	Note
0	0	0	1	
0	0	1	2	
0	1	0	4	
0	1	1	8	
1	0	0	16	1
1	0	1	32	
1	1	0	64	
1	1	1	128	

Note

1. reset / power on state, if SDIO is low at the rising edge of EN, a division ratio of 16 will be applied, else the division ratio will remain unchanged.

5.8.4 After-scaler

The after-scaler clock is the baud rate clock divided by 1,2,4 and 8. The division ratio is set in the ASC[2:0] bits. (see Table 29.)

Table 29 After-Scaler Control (ASC)

ASC1	ASC0	Division ratio ($Clk_{ASC}=Clk_{BD}/2^N$)	Note
0	0	1	
0	1	2	
1	0	4	
1	1	8	

Note: The afterscaler is only active in transmit mode when the power amplifier is switched on.

5.8.5 TxData Output

The TxDATA output is synchronized with the reference clock even in transparent transmission mode where the data is selected from SDIO and directly fed to the power amplifier control stage (see Figure 12. Power Amplifier Control).

5.9 General SPI Information

The chip is configured via the serial SPI interface, consisting of an 8-bit shift register and 20 8-bit registers holding the configuration data.

Data can be exchanged with multiple 8-bit frames (auto-increment) or in portions of 8 bits (1 byte), which could be of advantage if a hardware SPI-Interface is used. Data in the shift register is loaded into the addressed register with the last edge of SCK within the last bit of the transferred byte.

SPI Special Function Register-Set

All registers are read/write-able via the SPI communication. Therefore these registers are arranged as block with 20 addressable bytes.

Some of the bits of the registers indicate the state of the implemented TX state-machine and can alter without SPI transmission. (e.g. the "PD-bit" can be automatically set, if EN is kept low for a number of XTAL clocks or via dedicated SPI communication). Other bits only can be altered via SPI communication. (e.g. the frequency setting for the Baud-rate generator BD[7:0] or the configuration-bits for the TX state-machine).

In order change the operating mode of the transmitter, the special function register bits PD or PLLEN of register TXCON have to be accessed. To get from one state to another via SPI communication without intermediate states, these state describing bits are arranged in one byte. The byte will be written after completion of the byte transfer.

All the registers keep the stored information in Power Down state but if a dynamic power on reset occurs (can be evaluated by checking the PLLEN bit after transmission) the registers content may change. Only register TXCON is reset to a default state. All other registers have to be set again to ensure proper function after a dynamic reset.

5.9.1 SFR summary

Table 30 Special Function Register Summary

NAME	DESCRIPTION	ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	Reset Value Note 2
FC1H	Freq. Config. 1 High Byte	00h	F1C15	F1C14	F1C13	F1C12	F1C11	F1C10	F1C9	F1C8	xxxx xxxx b
FC1L	Freq. Config. 1 Low Byte	01h	F1C7	F1C6	F1C5	F1C4	F1C3	F1C2	F1C1	F1C0	xxxx xxxx b
FC2H	Freq. Config. 2 High Byte	02h	F2C15	F2C14	F2C13	F2C12	F2C11	F2C10	F2C9	F2C8	xxxx xxxx b
FC2L	Freq. Config. 2 Low Byte	03h	F2C7	F2C6	F2C5	F2C4	F2C3	F2C2	F2C1	F2C0	xxxx xxxx b
FC3H	Freq. Config. 3 High Byte	04h	F3C15	F3C14	F3C13	F3C12	F3C11	F3C10	F3C9	F3C8	xxxx xxxx b
FC3L	Freq. Config. 3 Low Byte	05h	F3C7	F3C6	F3C5	F3C4	F3C3	F3C2	F3C1	F3C0	xxxx xxxx b
FC4H	Freq. Config. 4 High Byte	06h	F4C15	F4C14	F4C13	F4C12	F4C11	F4C10	F4C9	F4C8	xxxx xxxx b
FC4L	Freq. Config. 4 Low Byte	07h	F4C7	F4C6	F4C5	F4C4	F4C3	F4C2	F4C1	F4C0	xxxx xxxx b
FCA	MSB for all Freq. Conf.	08h	F4C17	F4C16	F3C17	F3C16	F2C17	F2C16	F1C17	F1C16	xxxx xxxx b
FCON	FSK modulation control	09h	FSK7	FSK6	FSK5	FSK4	FSK3	FSK2	FSK1	FSK0	xxxx xxxx b
ACON0	ASK modulation control 0	0Ah	ASK0	X	X	X	AMH03	AMH02	AMH01	AMH00	xxxx xxxx b
ACON1	ASK modulation control 1	0Bh	ASK1	X	X	X	AMH13	AMH12	AMH11	AMH10	xxxx xxxx b
ACON2	ASK modulation control 2	0Ch	CASC	ENRAD	ENPF	ENSDO	AML3	AML2	AML1	AML0	x0xx xxxx b
MRCON	Modulation ramp control	0Dh	X	RMP6	RMP5	RMP4	RMP3	RMP2	RMP1	RMP0	xxxx xxxx b
TXCON	Transmitter Control	0Eh	PD	PDCK	XOSL	FBSL	PAM1	PAM0	ENXR	PLLEN	00xx xxx0 b
BDSEL	Baud rate Selection	0Fh	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	xxxx xxxx b
SCSEL	Scaler Selection	10h	CSS2	CSS1	CSS0	PSC2	PSC1	PSC0	ASC1	ASC0	1011 00xx b
ATUNE	Antenna Tuning	11h	ATI2	ATI1	ATI0	ATS4	ATS3	ATS2	ATS1	ATS0	xxxx xxxx b
TEST1	TEST1	12h	X	X	X	X	X	X	X	X	
TEST2	TEST2	13h	X	X	X	X	X	X	X	X	

Note

1. Bits marked ‘X’ are reserved for future use or device test. Any read operation yields an undefined result
2. reset condition after reset command (en set low for at least 2^{16} reference clock cycles). Register SCSEL and bit PDCK of TXCON are reset only if SDIO=0

5.9.2 General SFR access information

If SCK is high at the rising edge of EN, the data is transferred with the rising edge of SCK (like shown in the write and read-access diagrams), if SCK is low at the rising edge of EN, the data is transferred with the falling edge of SCK.

EN must be forced low after the last bit of all transmitted bytes in order to signal end of transmission.

Note: if EN is kept low for 2^{16} clocks the power down state is entered and the crystal oscillator is switched off.

SFR block diagram

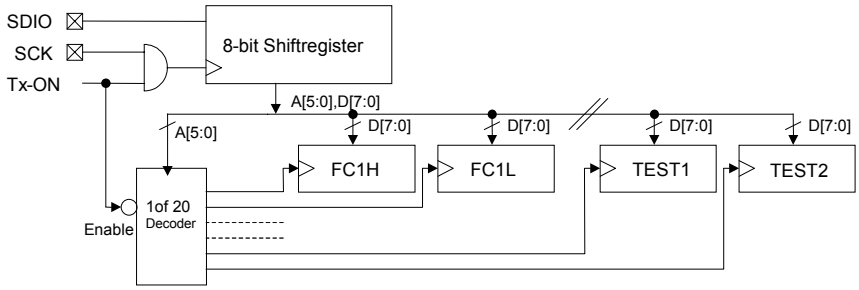


Figure 18. Serial configuration interface block diagram

Write access to SFR

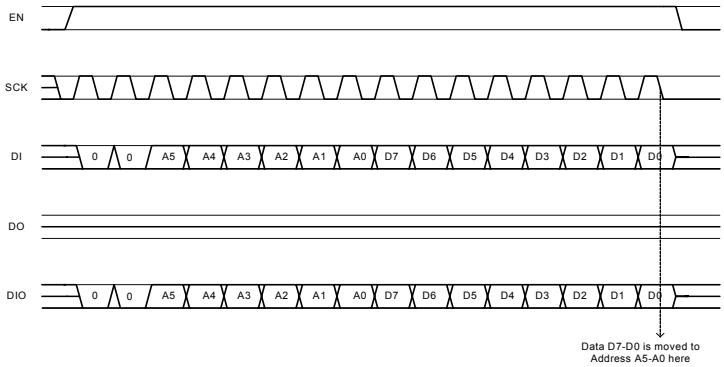


Figure 19. Write Serial Interface Timing diagram

Read access to SFR

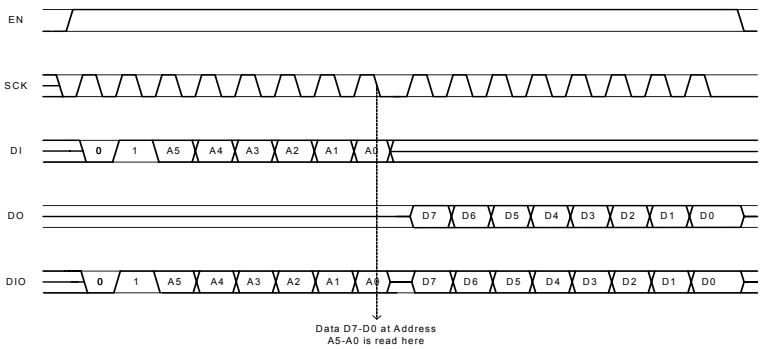


Figure 20. Read Serial Interface Timing diagram

Access to SFR with auto-increment function

If the SPI clock SCK is still applied after the first transferred 8 data bits, the auto-increment function automatically increases the address for the following next 8 data bits by one. This enables writing data to a contiguous range of bytes without having to set the address for every single data-byte. The auto-increment function is terminated with the falling edge of EN.

Write access to SFR with auto-increment function

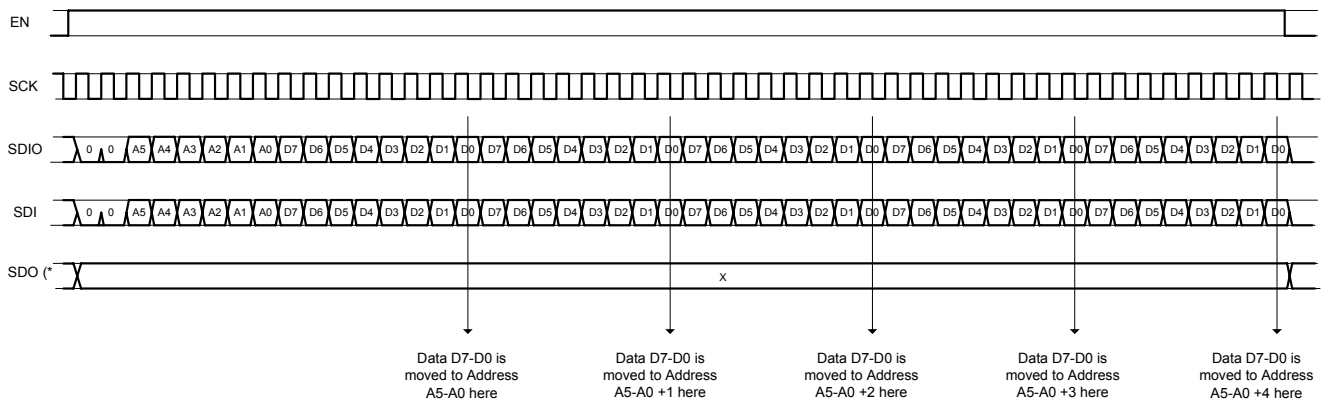


Figure 21. Write Serial Interface auto-increment Timing diagram

EN must be forced low after registers have been written / read in order to signal end of Write / Read. The diagram shows an example, where 5 successive bytes are stored

Read access to SFR with auto-increment function

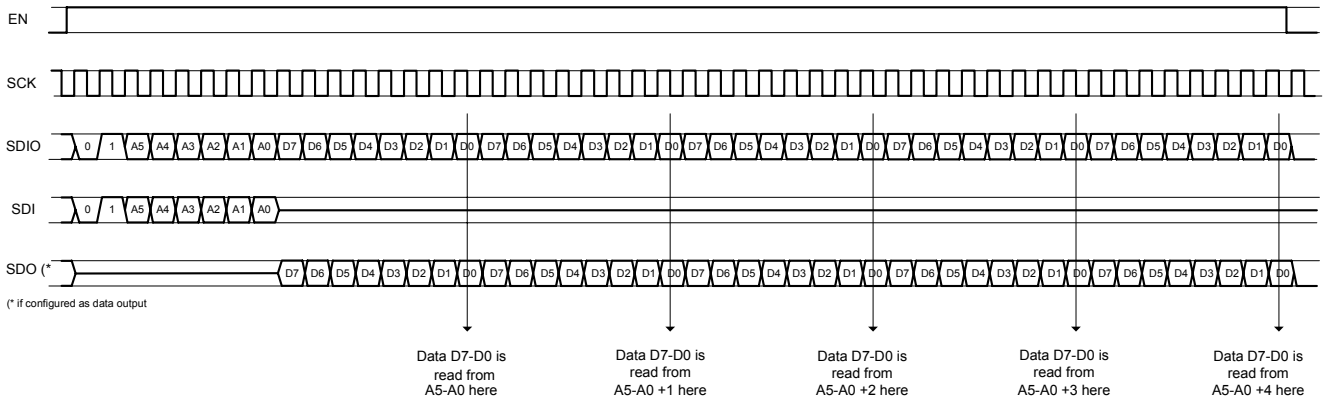


Figure 22. Read Serial Interface auto-increment Timing diagram

EN must be forced low after registers have been written / read in order to signal end of Write / Read. The diagram shows an example, where 5 successive bytes are stored.

5.9.3 Transmit data command

Transmit configuration

Some transmit-configuration bits have to be sent via SPI before every transmit command. (A to F, see transmit data diagram).

Other configuration settings are stored in the registers and the state machine keeps its behaviour until these bits are altered.

5.9.3.1 Description of the configuration bits

Synchronization:

Bit A = 1: Synchronization of the data at the falling or at the rising edge of SCK with the baud rate clock (CLK_{ASC}) (also dependent of register setting)

Bit A = 0: no synchronization of the transmit-data

Power amplifier:

The power amplifier is always turned on with the ninth non-significant edge of SCK. The configuration bit B is used to turn off the power amplifier.

Bit B = 1: The power amplifier is turned off after falling edge of EN (synchronized with baud rate, if enabled). Data is transmitted after the power amplifier is turned on. During transmission EN has to be kept 1 and the data at SDIO is transmitted transparently or synchronized with the baud rate.

Bit B = 0: Data transmission starts after the power amplifier is turned on. With the falling edge of EN the actual data bit at SDIO is latched and a constant carrier will be transmitted either in NRZ mode (bit C=0) or with Manchester coding (bit C=1) until the power amplifier is turned off.

Data Coding:

Bit C = 1: Data is XOR'd (Manchester generation) with baud rate clock. If C=1 the value of "A" will be ignored and the data transmission will be done synchronized to the baud rate clock.

Bit C = 0: NRZ mode selected.

Modulation and Power Settings:

Bit D = 1: Modulation and amplitude/power settings of ACON1 are applied. (according to Figure 12)

Bit D = 0: Modulation and amplitude/power settings of ACON0 are applied. (according to Figure 12)

Frequency Settings

Bits E, F: selection of frequency configuration registers.

Table 31 Frequency Selection (Bit E, Bit F)

Bit E	Bit F	FCON	Note
0	0	FCC1H, FCC1L, F1C16, F1C17	
0	1	FCC2H, FCC2L, F2C16, F2C17	
1	0	FCC3H, FCC3L, F3C16, F3C17	
1	1	FCC4H, FCC4L, F4C16, F4C17	

Transmission command

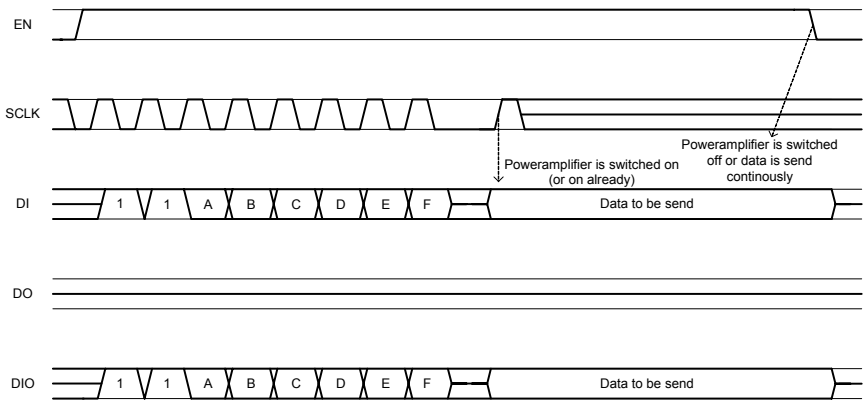


Figure 23. Transmit data timing diagram

A to F contain configuration information for the transmit-operation.

Example of transparent data transmission

Bit A=0: no synchronization of the transmit data

Bit B=1: The power amplifier is turned off after falling edge of EN. Data is transmitted after the power amplifier is turned on. During transmission EN has to be kept 1 and the data at SDIO is transmitted transparently.

Bit C=0: NRZ mode selected.

Bit D=0: Modulation and amplitude/power settings of ACON0 are applied (according to Figure 12) .

Bit E=0, F=0: selection of frequency configuration register FC1.

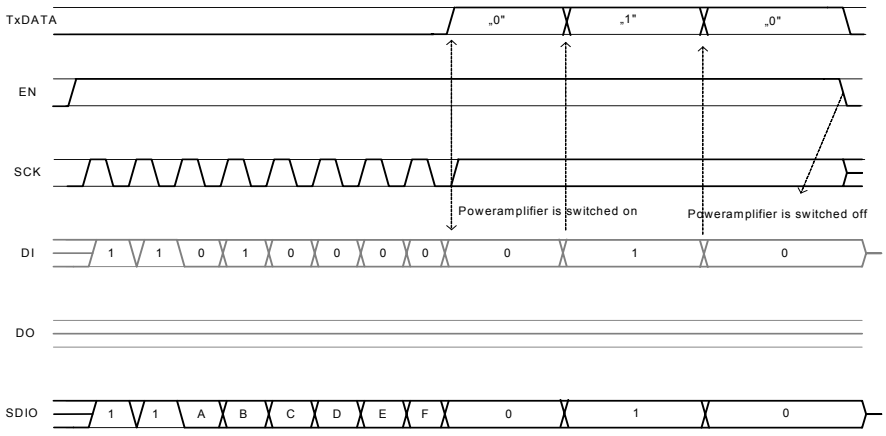


Figure 24. Transmit data Example 1

Example of synchronized data transmission

Phase 1: Data transmission (see Figure 25)

Bit A=1: Synchronization of the data with the baud rate clock CLK_{ASC} (= afterscaler clock output, see Figure 17)

Bit B=0: Data transmission starts after the power amplifier is turned on. With the falling edge of EN the actual data bit at SDIO is latched and a constant carrier will be transmitted with Manchester coding (bit C=1) until the power amplifier is turned off.

Bit C=1: Data is XOR'd (Manchester generation) with baud rate clock. The value of "A" will be ignored and the data transmission will be done synchronized to the baud rate clock.

Bit D=0: Modulation and amplitude/power settings of ACON0 are applied (according to Figure 12).

Bit E=0, F=0: selection of frequency configuration register FC1.

Phase 2: End of data transmission (see Figure 25)

Bit A=1: Synchronization of the data with the baud rate clock CLK_{ASC} (= afterscaler clock output, see Figure 17)

Bit B=1: The power amplifier is turned off after falling edge of EN (synchronized with baud rate).
Data is transmitted after the power amplifier is turned on. During transmission EN has to be kept 1 and the data at SDIO is transmitted synchronized with the baud rate.

Bit C=1: Data is XOR'd (Manchester generation) with baudrate clock. The value of "A" will be ignored and the data transmission will be done synchronized to the baudrate clock.

Bit D=0: Modulation and amplitude/power settings of ACON0 are applied (according to Figure 12).

Bit E=0, F=0: selection of frequency configuration register FC1.

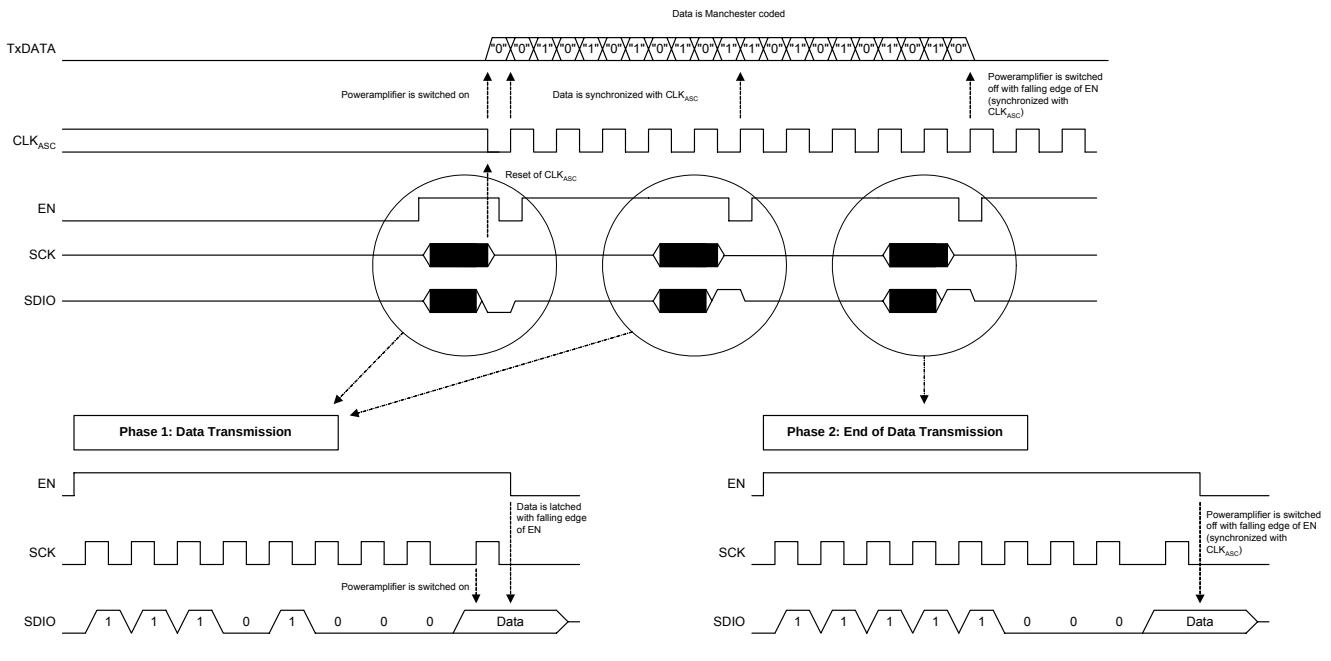


Figure 25. Transmit data Example 2

5.10 Antenna tuning

5.10.1 Antenna tuning configuration

For the PCF7900VHN and PCH7900VTT the output capacitance of the PAOUT pin can be adjusted in 32 binary weighted steps in order to achieve proper output matching and to compensate manufacturing tolerances of passive elements used on the antenna PCB. The full capacitance range will be 5pF for PCF7900VHN and PCH7900VTT. The antenna tuning is supported by a state machine and a measurement unit. The measurement unit is based on a break-before-make sample & hold topology with two sampling paths in parallel where the peak value of the voltage at PAOUT is compared for two consecutive capacitor values.(see figure)

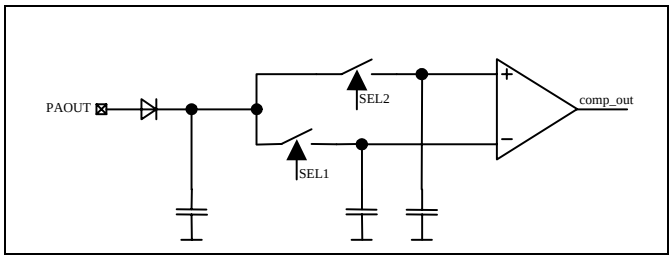


Figure 26. antenna tuning measurement unit

If the output amplitude of the second measurement is higher than the first one, the measurement unit signals a “high” level, if it is lower, the output will be “low”. The best matching is achieved at the maximum amplitude.

Table 32 Antenna Tuning, ATUNE

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	Bit 0
ATI2	ATI1	ATI0	ATS4	ATS3	ATS2	ATS1	ATS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address = 11H

Table 33 Antenna Tune Increment (ATI)

ATI2	ATI1	ATI0	Step width	Note
0	0	0	1	
0	0	1	2	
0	1	0	3	
….	….	….	….	
1	1	1	8	

Some antenna tune-configuration bits have to be set via SPI before the antenna tune command is executed.

The bits ATS[4:0], (see Table 34 Antenna Tune Start), indicate the starting value of the adjustable pin-capacitance, the bits ATI[2:0], see Table 33 Antenna Tune Increment, determines the step-width for the antenna tune command.

Table 34 Antenna Tune Start (ATS)

ATS4	ATS3	ATS2	ATS1	ATS0	VHN: Cp [pF]
0	0	0	0	0	0
0	0	0	0	1	0.16
0	0	0	1	0	0.32
					….
1	1	1	1	1	5

Antenna tuning sequence

The 8-bit antenna-tune command starts a state-machine. At every non-significant edge clock edge (SCK) the output capacitance will be incremented from the selected start-value by the selected step-size e.g. if the ATS[4:0] is set to 0x10h and ATI[2:0] is set to 0x4h then the automatic tuning starts with step 16 and will be incremented by 4 at each non-significant clock edge. If the next step would exceed the maximum step, the auto increment continues counting and the current ATUNE value is set to the current counting value modulo 31.

At the first non-significant edge after the command the RF output is activated and a constant carrier is transmitted with the frequency chosen in the configuration bits “E” and “F”. The selected output power should be as high as possible but one has to take care on clipping of the output voltage depending on the antenna matching circuitry especially at lower supply voltage levels. Bit “D” can be used to select an appropriate power level. The Bits “A” and “C” should be set to 0 where bit “B” can be set or not.

The first edge after the command also sets SDIO or SDO (if the 4-wire interface is used) to output mode and the output state then corresponds to the actual output state of the measurement unit. The output is valid after the capacitor value is selected (at the second non-significant clock edge). At the first edge when the power amplifier is activated both inputs of the measurement unit are on the same voltage level so the output state depends on the internal offset voltages and is invalid until the next non-significant edge.

The internal sample & hold structure is synchronized to the reference clock of the crystal oscillator. Depending on the phase shift between SCK and the reference clock a new capacitor value is activated latest two reference clock cycles after a non-significant edge of SCK.

After selecting the new capacitor value the sampling structure and the comparator need some time to be settled. So the total response time is given by:

$$t_{valid} = 2 \times t_{REF} + t_{resp,comp}$$

It is recommended to evaluate the SDIO/SDO pin short before the next non-significant edge of SCK (e.g. rising edge in fig 25) in order to allow for the longest possible settling time.

The command has to be stopped by disabling EN after the pin SDIO/SDO changes from “High” to “Low” (indicates a decreasing RF level) but before the next non-significant edge of SCK occurs. At this point the actual setting of the tuning capacitance is stored in the ATUNE register. The tuning value for the maximum output voltage is then the actual register content minus one step width – so the last step before the actual step corresponds to the maximum output power.

The actual ATUNE register content can also be read out (by use of a standard read command) e.g. to be stored in a non-volatile memory with other tuning or trimming data. It is also possible to directly write to the ATUNE register.

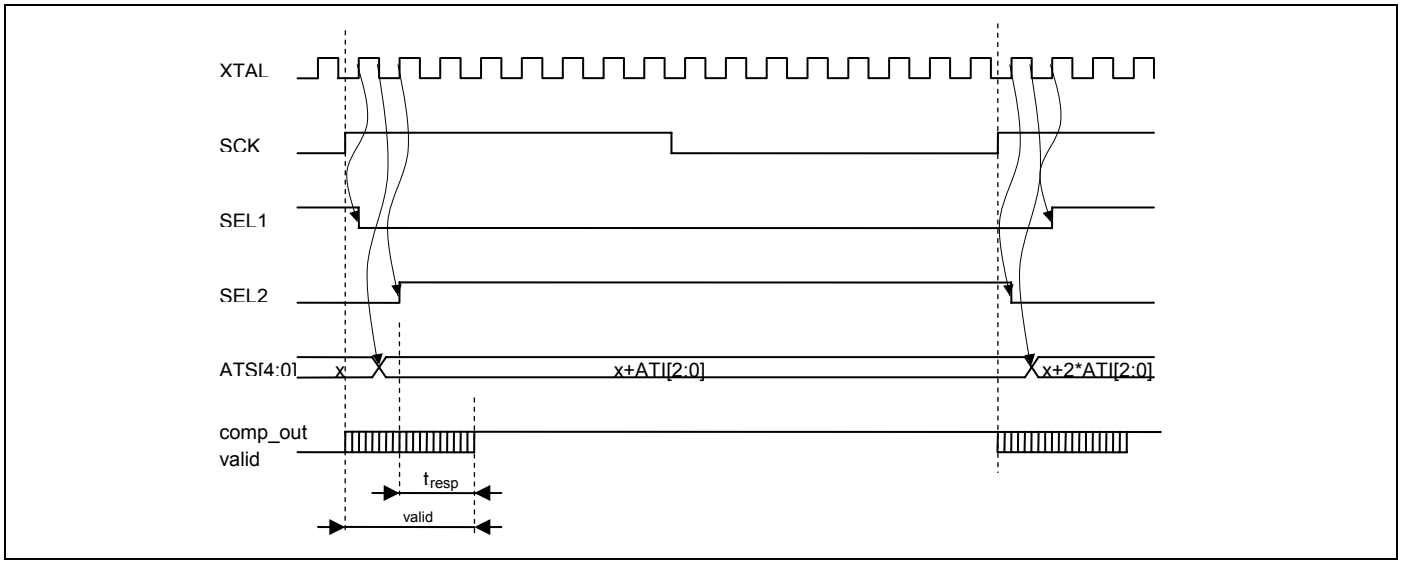


Figure 27. timing of antenna tuning measurement unit

Remark: the maximum usable clock frequency of SCK is dependent on the timing how SDO is evaluated. It is recommended to readout SDO short before the next non-significant edge at SCK would occur (rising edge of SCK in the picture above). In this case a maximum frequency of 1MHz at SCK would be possible.

5.10.2 Antenna Tune command

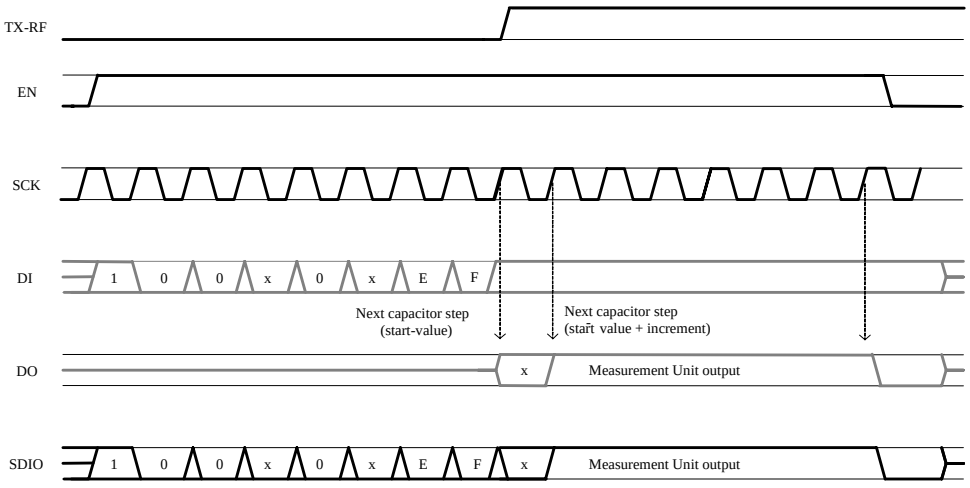


Figure 28. Antenna Tune command overview

Remark: The settings of the configuration bits A to F of the antenna tune command are equal to the corresponding bits of the transmit command (see section 5.9.3.1). If the antenna tune command is send while the device is in transmitter active state and the device should continue transmission after tuning, the setting of the configuration bits of the antenna tune command should be identical to the bit configuration used for the transmit command.

5.11 Test Circuit

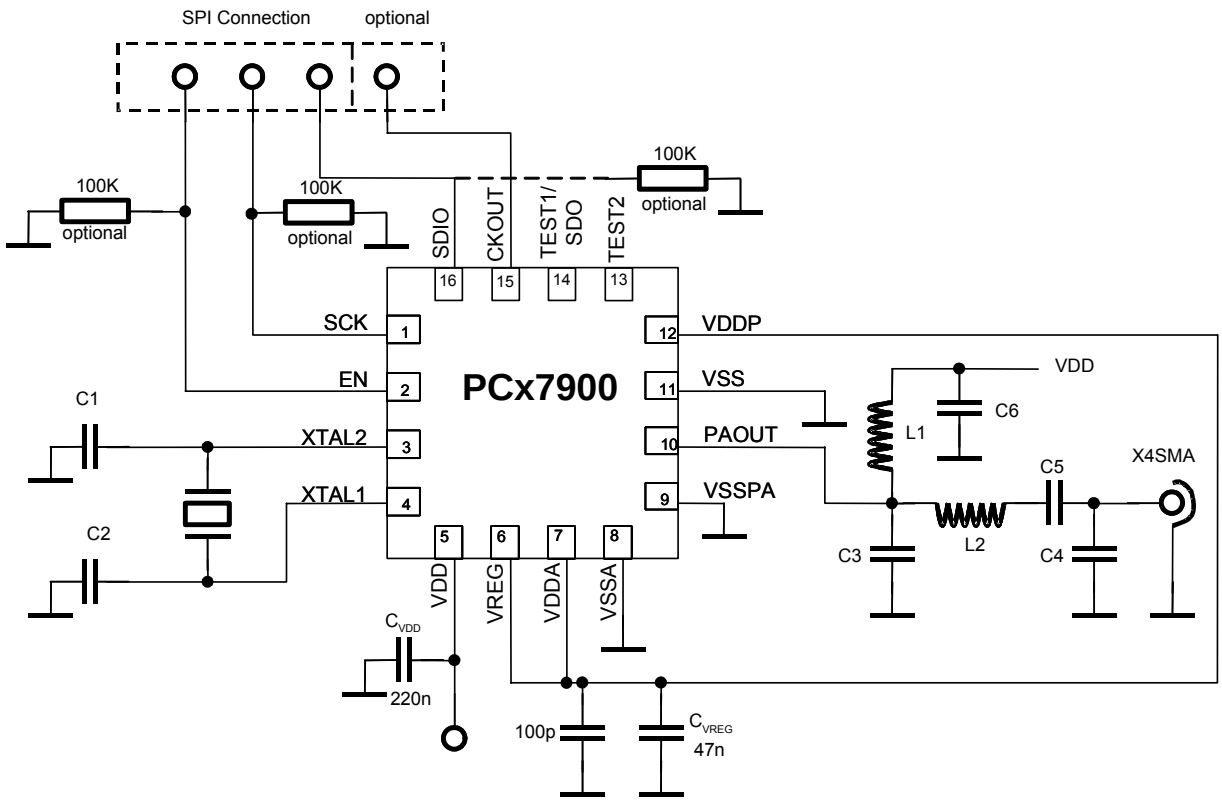


Figure 29 Test circuit

Notes

1. C1 and C2 are used as load capacitances acc. to the crystal specification to operate the crystal oscillator at its nominal frequency.
2. The below listed load tank configurations are used for device characterization and are not optimised for maximum output power !

Load tank circuit configuration for ~200 Ohm:

Table 35 Load tank circuit components

component	315 MHz	434 MHz	868 MHz	Note
L1	82 nH	68 nH	47 nH	
L2	47 nH	27 nH	10 nH	
C3	~ 5.6 pF	~ 4.1 pF	~ 2.2 pF	1
C4	6.8 pF	4.7 pF	5.6 pF	
C5	47 pF	27 pF	15 pF	
C6	100 pF	100 pF	100 pF	

Note

1. Value depending on device internal antenna tuning configuration

6 LIMITING VALUES

All values are in accordance with Absolute Maximum Rating System (IEC 134). Stress above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Operating Conditions and Electrical Characteristics section of this specification is not implied.

PARAMETER	MIN	MAX	UNIT
Operating temperature range (HVQFN16)	-40	+85	°C
Operating temperature range (TSSOP16)	-40	+125	°C
Storage temperature range	-55	+125	°C
Voltage at any I/O and V_{DD}, V_{REG}, V_{DDA}, V_{DDP} pin to V_{SS}, V_{SSA}, V_{SSPA}	-0.5	3.6	V
Voltage at any I/O pin to V_{SS}	-0.5	V_{DD} +0.3	V
Voltage at PAOUT pin to V_{SSPA}	-0.5	7.2	V
Peak output current for I/O pins		15	mA
Latch-up current, Note 1	100		mA
ESD, human body model, Note 2	2		kV
ESD, machine model, Note 3	200		V
Power dissipation		120	mW

Notes

1. According to JEDEC, JESD 17
2. According to JEDEC, JESD 22-A114
3. According to JEDEC, JESD 22-A115

7 ELECTRICAL CHARACTERISTICS

7.1 Operating Conditions

T_{AMB} = -40 to +125°C (TSSOP16) respectively -40 to +85°C (HVQFN16), V_{DD} = 2.7V, V_{SS} = 0V, Capacitor (47 nF) connected between V_{REG} and V_{SS}. (Unless otherwise specified)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage range		1.7		3.6	V
$V_{DD, XO}$	Supply voltage range XTAL Oscillator		1.7		3.6	V
$V_{DD, PLL}$	Supply voltage range PLL Note 1		2.1		3.6	V
f_{TX}	Carrier frequency range	HVQFN16: T_{AMB} = -40 to +85°C TSSOP16: T_{AMB} = -40 to +125°C	300 300		920 460	MHz MHz
f_{VCO}	VCO Frequency		300		920	MHz
f_{XTAL}	XTAL Oscillator Frequency		9		19	MHz
Power Fail Detection						
$V_{PFD,FIX}$	Power Fail Detection Level	T_{AMB} = 25°C, ENRAD = 0	1.85	2.0	2.15	V
$V_{PFD,ADAPT,868}$	Power Fail Detection Level	f_{PLL} = 868 MHz, ENRAD = 1 T_{AMB} = -40°C T_{AMB} = 25°C T_{AMB} = 85°C	 1.7	 2.0 1.95 1.9	 2.25 	 V V V
$V_{PFD,ADAPT,630}$	Power Fail Detection Level	f_{PLL} = 630 MHz, ENRAD = 1 T_{AMB} = -40°C T_{AMB} = 25°C T_{AMB} = 85°C	 1.5	 1.8 1.75 1.7	 2.0 	 V V V
$t_{PFD,LAT}$	Power Fail Detection latency time			0.5	1	us
Voltage Regulator						
$t_{REG,START}$	Regulator startup time			5	20	us
C_{VREG}	External blocking capacitor, Note 1		22	47		nF

Note

1. The available supply voltage range can be extended using the Power Fail Detection circuitry in adaptive mode. If enabled, the minimum PLL supply voltage corresponds with the actual Power Fail Detection Level ($V_{PFD,ADAPT}$), which is a function of the PLL frequency (f_{PLL}).

7.2 AC/DC Characteristics

T_{AMB} = -40 to +125°C (TSSOP16) respectively -40 to +85°C (HVQFN16), V_{DD} = 2.7V, V_{SS} = 0V, Capacitor (47 nF) connected between V_{REG} and V_{SS}. (Unless otherwise specified)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Current Consumption						
$I_{DD,PD}$	Supply current: Power down	HVQFN16: T_{AMB} = -40 to +85°C		50	1000	nA
		TSSOP16: T_{AMB} = -40 to +125°C		50	2000	nA
$I_{DD,XO}$	Supply current - XTAL Active	f_{XTAL} = 9.18 MHz		180	380	µA
	XTAL on, PLL off, PA off	f_{XTAL} = 13.08 MHz		250	450	µA
		f_{XTAL} = 18.37 MHz		270	550	µA
$I_{DD,XOstup}$	Crystal oscillator start-up peak current				6	mA
$\Delta I_{DD,PLL}$	Supply current - PLL Active	ENRAD = 0, Note 3, 4				
	XTAL on, PLL on, PA off	f_{PLL} = 434 MHz		1.3	2.0	mA
		f_{PLL} = 630 MHz		1.9	2.9	mA
		f_{PLL} = 869 MHz		2.7	4.0	mA
$I_{DD,TX\ (PAM2)}$	Supply current – Transmitter Active	PAM = 2, AMH = “1111”, CASC = 1				
	XTAL on, PLL on, PA on	HVQFN16: T_{AMB} = -40 to +85°C				
	Note 1	f_{TX} = 315 MHz, f_{PLL} = 630 MHz	5.5	7.0	8.5	mA
		f_{TX} = 434 MHz, f_{PLL} = 869 MHz	6.8	8.8	10.8	mA
		f_{TX} = 869 MHz	6.5	8.5	10.5	mA
		TSSOP16: T_{AMB} = -40 to +125°C				
		f_{TX} = 315 MHz, f_{PLL} = 630 MHz	4.5	7.0	8.5	mA
		f_{TX} = 434 MHz, f_{PLL} = 869 MHz	6.3	8.8	10.8	mA
$I_{DD,TX\ (PAM3)}$	Supply current – Transmitter Active	PAM = 3, AMH = “1111”, CASC = 0				
	XTAL on, PLL on, PA on	HVQFN16: T_{AMB} = -40 to +85°C				
	Note 1,2	f_{TX} = 315 MHz, f_{PLL} = 630 MHz	7.5	11.5	17.6	mA
		f_{TX} = 434 MHz, f_{PLL} = 869 MHz	8.0	12.0	19.0	mA
		f_{TX} = 868 MHz	10.0	14.5	19.0	mA
		TSSOP16: T_{AMB} = -40 to +125°C				
		f_{TX} = 315 MHz, f_{PLL} = 630 MHz	7.0	11.5	15.5	mA
		f_{TX} = 434 MHz, f_{PLL} = 869 MHz	7.5	12.0	16.0	mA

Notes

1. Load tank circuit according to Figure 29 Test circuit.
2. Maximum power setting
3. Total current consumption when PLL is running: $I_{DD,PLL} = I_{DD,XO} + \Delta I_{DD,PLL}$
4. The PLL supply current may be reduced slightly (single digit percent range) by selecting the adaptive voltage regulator mode (ENRAD = 1)

7.3 Serial Interface Characteristics

7.3.1 AC/DC Characteristics

T_{AMB} = -40 to +125°C (TSSOP16) respectively -40 to +85°C (HVQFN16), V_{DD} = 2.7V, V_{SS} = 0V, Capacitor (47 nF) connected between V_{REG} and V_{SS}. (Unless otherwise specified)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I/O Pins (SCK, EN, SDIO, SDO, CKOUT)						
V_{IL}	Input low voltage		-0.1		0.2 V_{DD}	V
V_{IH}	Input high voltage		0.8 V_{DD}		V_{DD} + 0.1	V
I_{IL}	Input low current	V_{IL} = 0			0.5	µA
I_{IH}	Input high current	V_{IH} = V_{DD}			0.5	µA
V_{OL}	Output low voltage	I_O = 4mA			0.4	V
V_{OH}	Output high voltage	I_O = -4mA	V_{DD} - 0.4			V
C_I	Pin capacitance	V_{IN} = 0.1V_{RMS}, f = 1MHz		1.6	2	pF

7.3.2 Timing Specifications

T_{AMB} = -40 to +125°C (TSSOP16) respectively -40 to +85°C (HVQFN16), V_{SS} = 0V, Capacitor (47 nF) connected between V_{REG} and V_{SS}. (Unless otherwise specified)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
f_{SCK}	Input clock frequency				2	MHz
f_{SCK_ATUNE}	Input clock frequency for antenna tuning		0.2		1	MHz
$t_{PW,SCK}$	Input clock pulse width		200			ns
$t_{RISE,SCK}$	Input clock rise time				50	ns
$t_{FALL,SCK}$	Input clock fall time				50	ns
$t_{PW,EN}$	Enable signal pulse width		500			ns
$t_{RISE,EN}$	Enable signal rise time				50	ns
$t_{FALL,EN}$	Enable signal fall time				50	ns
$t_{SETUP,SDIO}$	Setup time	Note 1			20	ns
$t_{FALL,SDIO}$	Hold time	Note 2			20	ns
$t_{SDO,DLY}$	SDO delay time	Note 3			50	ns

Notes

1. Minimum time SDIO must be settled before clock edge.
2. Minimum time SDIO must be hold after clock edge.
3. Settling time of SDO after clock edge (only for 4 wire interface)

7.4 Transmitter AC/DC Conditions

T_{AMB} = -40 to +125°C (TSSOP16) respectively -40 to +85°C (HVQFN16), V_{DD} = 2.7V, V_{SS} = 0V, Capacitor (47 nF) connected between V_{REG} and V_{SS}. (Unless otherwise specified)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
XTAL Oscillator						
R_{MARGIN}	Oscillator start-up margin	T_{AMB} = 25°C, C_1 = C_2 = 15pF Note 1,2,3 f_{TXAL} = 9.18 MHz f_{TXAL} = 13.08 MHz f_{TXAL} = 18.37 MHz	 2.2 1.4 700	 4.1 2.5 1300		 kΩ kΩ Ω
C_{XTAL1}	Pin capacitance	T_{AMB} = 25°C		3.5	3.9	pF
C_{XTAL2}	Pin capacitance	T_{AMB} = 25°C		2.1	2.9	pF
$t_{XTAL,SET}$	XTAL Oscillator settling time			0.5	1.5	ms

Notes

1. R_{MARGIN} is the maximum resistance that can be put in series to the crystal without causing oscillation dropouts
2. The given R_{MARGIN} (Oscillation margin) is tested and guaranteed only at room temperature (Tamb = 25°C). The minimum value occurs at high temperature and a minimum supply voltage of V_{DD} = 2.1V
3. To guarantee sufficient oscillation start-up margin every reference application board has to be checked individually by the customer.

T_{AMB} = -40 to +125°C (TSSOP16) respectively -40 to +85°C (HVQFN16), V_{DD} = 2.7V, V_{SS} = 0V, Capacitor (47 nF) connected between V_{REG} and V_{SS}. (Unless otherwise specified)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
PLL Synthesizer						
BW_{LOOP}	Loop bandwidth	f_{XTAL} = 9.18 MHz		50		kHz
	Note 1	f_{XTAL} = 13.08 MHz		70		kHz
		f_{XTAL} = 18.37 MHz		100		kHz
PN_{PLL}	Phase Noise	PAM = 3, AMH = ‘1111 ‘,CASC=0				
	f_{TX} = 315MHz and 434 MHz	10 kHz offset		-78	-72	dBc/Hz
	Note 2	100 kHz offset		-76	-70	dBc/Hz
		1 MHz offset		-87	-81	dBc/Hz
		10 MHz offset		-115	-105	dBc/Hz
$PN_{PLL,868}$	Phase Noise	PAM = 3, AMH = ‘1111 ‘,CASC=0				
	f_{TX} = 869 MHz	10 kHz offset		-81	-75	dBc/Hz
	Note 3	100 kHz offset		-79	-73	dBc/Hz
		1 MHz offset		-90	-84	dBc/Hz
		10 MHz offset		-114	-104	dBc/Hz
E_{REF}	Reference spurious emissions	PAM = 2, AMH = ‘1111 ‘,CASC=1				
	$f_{TX} \pm f_{XTAL,}$	f_{TX} = 315 MHz, f_{XTAL} = 18.37 MHz		-42	-32	dBc
		f_{TX} = 434 MHz, f_{XTAL} = 13.08 MHz		-43	-33	dBc
		f_{TX} = 869 MHz, f_{XTAL} = 13.08 MHz, Note 3		-46	-34	dBc
t_{ACQ}	PLL Acquisition time			0.1	0.5	ms

Notes

1. Derived from simulation, not tested.
2. Load tank circuit according to Figure 29 Test circuit.
3. Valid only for HVQFN16 package at 869MHz

T_{AMB} = -40 to +125°C (TSSOP16) respectively -40 to +85°C (HVQFN16), V_{DD} = 2.7V, V_{SS} = 0V, Capacitor (47 nF) connected between V_{REG} and V_{SS}. (Unless otherwise specified)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Power Amplifier, Note 1						
$P_{OUT,MAX}$	Maximum output power	T_{AMB} = 25°C, V_{DD} = 3.6V PAM=3, AMH = "1111", CASC = 0				
		f_{out} = 315 MHz			12	dBm
		f_{out} = 434 MHz			12	dBm
		f_{out} = 869 MHz			12	dBm
$P_{OUT,NOM}$	Nominal output power	T_{AMB} = 25°C PAM=2, AMH = "1111", CASC=1				
		f_{out} = 315 MHz, f_{PLL} = 630 MHz	3.0	4.7	6.4	dBm
		f_{out} = 434 MHz, f_{PLL} = 869 MHz	4.3	6	7.7	dBm
		f_{out} = 869 MHz, f_{PLL} = 869 MHz	1.5	4	6.5	dBm
$dP_{OUT,VDD}$	Supply voltage dependency of P_{OUT}	T_{AMB} = 25°C, V_{DD} = 2.1V to 3.6V PAM=2, AMH ="1111", CASC=1	-1.5		+0.8	dBm
$dP_{OUT,TEMP}$	Temperature dependency of P_{OUT}	PAM=2, AMH = "1111", CASC=1 HVQFN16 and TSSOP16:				
		T_{AMB} = -40 to +85°C	-1.2		+1.2	dBm
		TSSOP16:				
		T_{AMB} = -40 to +125°C,	-2.0		+1.2	dBm

Notes

1. Load tank circuit according to fig. Figure 29 Test circuit

T_{AMB} = -40 to +125°C (TSSOP16) respectively -40 to +85°C (HVQFN16), V_{DD} = 2.7V, V_{SS} = 0V, Capacitor (47 nF) connected between V_{REG} and V_{SS}. (Unless otherwise specified)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Antenna Tuning, PCH7900VTT (TSSOP16)						
$C_{TUNE,MIN}$	Antenna tuning capacitor	T_{AMB} = 25°C, ATS = '00000'	2.7	2.9	3.1	pF
$C_{TUNE,MAX}$	Antenna tuning capacitor	T_{AMB} = 25°C, ATS = '11111'	7.7	7.9	8.1	pF
Q_{TUNE}	Antenna tuning capacitor	T_{AMB} = 25°C, ATS = '01111' f_{out} = 434 MHz		15		
Antenna Tuning, PCF7900VHN (HVQFN16)						
$C_{TUNE,MIN}$	Antenna tuning capacitor	T_{AMB} = 25°C, ATS = '00000'	2.5	2.7	2.9	pF
$C_{TUNE,MAX}$	Antenna tuning capacitor	T_{AMB} = 25°C, ATS = '11111'	7.5	7.7	7.9	pF
Q_{TUNE}	Antenna tuning capacitor	T_{AMB} = 25°C, ATS = '01111' f_{out} = 434 MHz		15		
Modulation						
$f_{MOD,ASK}$	ASK modulation frequency				50	kHz
$f_{MOD,FSK}$	FSK modulation frequency				50	kHz

Notes

1. The general supply block capacitor C_{VDD} should be selected at least 2 times the value of C_{VREG}

8 TEST SETUP

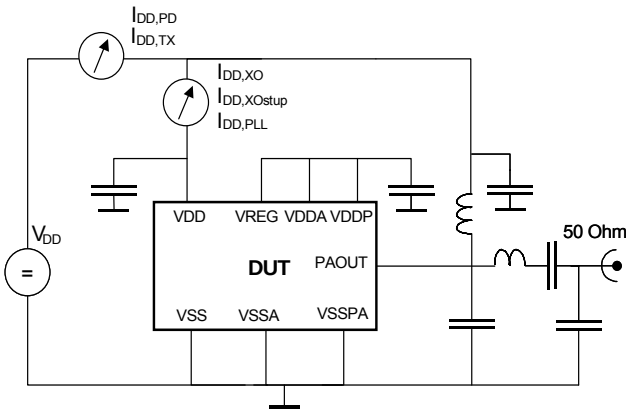


Figure 30. Current and RF measurement set-up

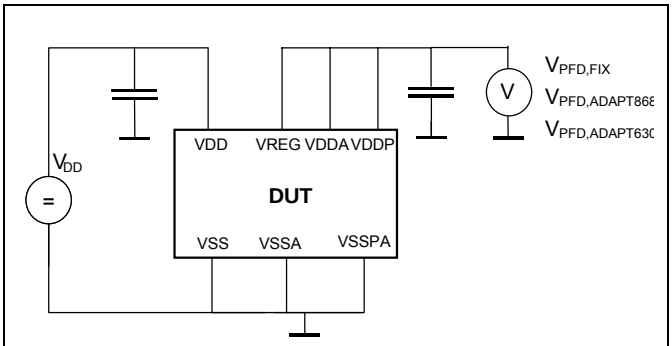


Figure 31. Regulator and PFD measurement set-up

9 APPLICATION NOTES

see AN10506_1 : UHF Transmitter PCx7900 (FranTIC)

10 REVISION HISTORY

Revision	Page	Description
2005 May 02		Draft release Preliminary Specification
2005 May 25		Preliminary Specification
2005 Jul 28		Preliminary Specification update + Reflect changes implemented for V1 + Replace PCJ7900 version by PCH7900 version + Test circuit updated
2005 Aug 03		Preliminary Specification update + Typo corrected, as device version yields V0 rather than V1
2005 Nov 22	 7 4	Preliminary Specification update + Pin Assignment + ORDERING INFORMATION updated and limited to two PA Capacitor options per package

		+ Update of chapter 5.2 Functional Blocks Overview + Update of chapter 5.4 Reference Clock generation + Update of chapter 5.5 Power Amplifier Control and ASK Modulation + corrections/completion of chapter 5.6 Voltage regulation and power fail detection + corrections/completion of chapter 5.7 Frequency Control and FSK Operation + corrections/completion of chapter 5.8 Baudrate Generation + corrections/completion of chapter 5.10 Antenna tuning
2005 Aug 03		Preliminary Specification update + Typo corrected, as device version yields V0 rather than V1
2005 Aug 03		Preliminary Specification update + Typo corrected, as device version yields V0 rather than V1
2006 Feb 07		Preliminary Specification update + Corrections/completion of chapter 5.3 Transmitter operating modes + Corrections/completion of chapter 5.6 Voltage regulation and power fail detection + Corrections/completion of chapter 5.9 General SPI Information + TSSOP16 outlines added + Update chapter 7 ELECTRICAL CHARACTERISTICS
2007 Dec 13		Preliminary Specification update + Editorial correction and updates + Corrections of chapter 5.8 Baudrate Generation
2007 Dec 13		Preliminary Specification update + update functional description chapter 5.1 Figure 4,Figure 5 + update interface configuration chapter 5.2 + correct and update command overview chapter 5.3 + update SASK settings description chapter 5.5 + update SFSK timing description chapter 5.7 + update/correct SFR rest values chapter 5.9 + correct SFR block diagram chapter 5.9 + update 7.4
2006 Dec 10		Product Specification (first release)
2007 Dec 13	7	Pin Description updated. Change to NXP

11 LEGAL INFORMATION

11.1 Data sheet status

Document status	Product status	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification or product development
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification
Product [short] data sheet	Production	This document contains the product specification

11.2 Definitions

Draft

The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet
A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

11.3 Disclaimers

General

Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes
NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use
NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications
Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values
Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale
NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license
Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Please be aware that important notices concerning this document and the product(s) described herein, have been included in the section 'Legal information'.

For more information, please visit: http://www.nxp.com
For sales office addresses, email to: sales.addresses@www.nxp.com