High-Performance, Two-Channel, 24-Bit, 216kHz Sampling Multi-Bit Delta-Sigma Analog-to-Digital Converter

FEATURES

- Supports Linear PCM, 1-Bit Direct Stream Digital (DSD), and Multi-Bit Modulator Output Data
  - Supports PCM Output Sampling Rates from 8kHz to 216kHz
  - Choose from 64x or 128x Oversampled Output Rates for DSD
- Differential Voltage Inputs
- On-Chip Voltage Reference Improves Power Supply Noise Rejection
- Dynamic Performance: Multi-Bit Modulator Output with 6.144MHz Modulator Clock
  - 6-Bit Modulator Data
  - Dynamic Range (–60dB input, A-weighted): 124dB typical
  - Dynamic Range (–60dB input, 20kHz Bandwidth): 122dB typical
  - Total Harmonic Distortion + Noise (–1dB input, 20kHz bandwidth): –108dB typical
- Dynamic Performance: PCM Output with 24-Bit Word Length
  - Dynamic Range (–60dB input, A-weighted): 123dB typical
  - Dynamic Range (–60dB input, 20kHz bandwidth): 121dB typical
  - Total Harmonic Distortion + Noise (–1dB input, 20kHz bandwidth): –108dB typical
- Dynamic Performance: DSD Output with 5.6448MHz bit rate
  - Dynamic Range (–60dB input, 20kHz bandwidth): 121dB typical
  - Total Harmonic Distortion + Noise (–1dB input, 20kHz bandwidth): –108dB typical
- Low Power Dissipation:
  - 305mW typical for 48kHz sampling rate
  - 330mW typical for 96kHz sampling rate
  - 340mW typical for 192kHz sampling rate
- Linear Phase Digital Decimation Filtering
  - Select from Classic or Low Group Delay Filter Responses
- Digital High-Pass Filtering Removes DC Offset
  - Left and Right Channel Filters May Be Disabled Independently
- PCM Audio Serial Port Interface
  - Master or Slave Mode Operation
  - Supports Left-Justified, I^2S™, and TDM Data Formats
- PCM Output Word Length Reduction
- Overflow Indicators for the Left and Right Channels
- Analog Power Supply: +4.0V nominal
- Digital Power Supply: +3.3V nominal
- Power-Down Mode: 4mW typical
- Package: TQFP-48, RoHS compliant

APPLICATIONS

- Digital Audio Recorders and Mixing Desks
- Digital Live Sound Consoles
- Digital Audio Effects Processors
- Surround Sound Encoders
- Broadcast Studio Equipment
- Audio Test and Measurement
- Sonar Systems
- High-Performance Data Acquisition

DESCRIPTION

The PCM4222 is a high-performance, two-channel analog-to-digital (A/D) converter designed for use in professional audio applications. Offering outstanding dynamic performance, the PCM4222 supports 24-bit linear PCM, 1-bit Direct Stream Digital (DSD), and 6-bit modulator data outputs. The supported output formats make the PCM4222 ideal for digital audio recording and processing applications. The multi-bit modulator output adds versatility, allowing customers to design their own digital decimation filter and processing hardware. The on-chip, linear phase decimation filtering engine supports Classic and Low Group Delay filter responses, allowing optimization for either studio or live sound applications.

The PCM4222 includes three PCM sampling modes, supporting output sampling rates from 8kHz to 216kHz. The DSD output supports either 64x or 128x oversampled bit rates. The PCM4222 is configured using dedicated control pins for selection of output modes, PCM audio data formats and word length, decimation filter response, high-pass filter disable, and reset/power-down functions.

While providing uncompromising performance, the PCM4222 addresses power concerns with just over 300mW typical total power dissipation, making the device suitable for multi-channel audio systems. The PCM4222 is typically powered from a +4.0V analog supply and a +3.3V digital supply. The digital I/O is logic-level compatible with common digital signal processors, digital interface transmitters, and programmable logic devices. The PCM4222 is available in a TQFP-48 package, which is RoHS-compliant.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

	VALUE
Power Supplies:	
VCC1, VCC2	–0.3V to +6.0V
VDD	–0.3V to +4.0V
Digital input voltage	
All digital input and I/O pins	–0.3V < (VDD + 0.3V) < +4.0V
Analog input voltage	
VINL+, VINL–, VINR+, VINR–	–0.3V < (VCC + 0.3V) < +6.0V
Input current (all pins except power and ground)	±10mA
Ambient operating temperature	–40°C to +85°C
Storage temperature	–65°C to +150°C

(1) These limits are stress ratings only. Stresses beyond these limits may result in permanent damage. Extended exposure to absolute maximum ratings may degrade device reliability. Normal operation or performance at or beyond these limits is not specified or ensured.

ELECTRICAL CHARACTERISTICS: DIGITAL and DYNAMIC PERFORMANCE

All specifications are at T_A = +25°C, VCC1 = VCC2 = +4.0V and VDD = +3.3V unless otherwise noted.

PARAMETER	CONDITIONS	PCM4222			UNITS
		MIN	TYP	MAX	
DIGITAL I/O CHARACTERISTICS (Applies to all digital I/O pins)					
High-level input voltage, V_{IH}		0.7 × VDD		VDD	V
Low-level input voltage, V_{IL}		0		0.3 × VDD	V
High-level input current, I_{IH}			1	10	µA
Low-level input current, I_{IL}			1	10	µA
High-level output voltage, V_{OH}	I_O = –2mA	0.8 × VDD		VDD	V
Low-level output voltage, V_{OL}	I_O = +2mA	0		0.2 × VDD	V
Input capacitance, C_{IN}			3		pF
PCM OUTPUT SAMPLING RATE, f_S					
	Normal mode	8		54	kHz
	Double Speed mode	54		108	kHz
	Quad Speed mode	108		216	kHz
DSD OUTPUT RATE, f_{DSD}					
	64x output mode	0.512		3.456	MHz
	128x output mode	1.024		6.912	MHz
MULTI-BIT MODULATOR OUTPUT RATE, f_{MOD}					
		1.024		6.912	MHz
MASTER CLOCK INPUT					
Normal mode, MCKI = 256f_S		2.048		13.824	MHz
Double Speed mode, MCKI = 128f_S		6.912		13.824	MHz
Quad Speed mode, MCKI = 64f_S		6.912		13.824	MHz
DSD 64x output mode, MCKI = 4 × f_{DSD}		2.048		13.824	MHz
DSD 128x output mode, MCKI = 2 × f_{DSD}		2.048		13.824	MHz
Multi-bit modulator output, MCKI = 2 × f_{MOD}		2.048		13.824	MHz
DYNAMIC PERFORMANCE(1)					
PCM output, Normal mode, f_S = 48kHz	**BW = 22Hz to 20kHz**				
Total harmonic distortion + noise (THD+N)	f = 997Hz, –1dB input		–108	–101	dB
	f = 997Hz, –20dB input		–100		dB
	f = 997Hz, –60dB input		–61		dB
Dynamic range, no weighting	f = 997Hz, –60dB input		121		dB
Dynamic range, A-weighted	f = 997Hz, –60dB input	118	123		dB
Channel separation/interchannel isolation	f = 10kHz, –1dB input	115	135		dB
PCM output, Double Speed mode, f_S = 96kHz	**BW = 22Hz to 40kHz**				
Total harmonic distortion + noise (THD+N)	f = 997Hz, –1dB input		–108		dB
	f = 997Hz, –20dB input		–98		dB
	f = 997Hz, –60dB input		–58		dB
Dynamic range, no weighting	f = 997Hz, –60dB input		118		dB
Dynamic range, A-weighted	f = 997Hz, –60dB input		123		dB
Channel separation/interchannel isolation	f = 10kHz, –1dB input		135		dB

(1) Typical PCM output performance is measured and characterized with an Audio Precision SYS-2722 192kHz test system and a PCM4222EVM evaluation module using the bandwidth and weighting settings as noted in the *Conditions* column. Typical DSD and Multi-Bit output performance is characterized using an Audio Precision SYS-2722 analog generator, a PCM4222EVM evaluation module, and a separate data acquisition system for collection and signal processing. The bandwidth and input settings used for these measurements are noted in the *Conditions* column. Master mode operation is utilized for all modes, with the master clock input frequency (MCKI) set to 12.288MHz for PCM and MBM output modes, and 11.2896MHz for DSD output mode.

ELECTRICAL CHARACTERISTICS: DIGITAL and DYNAMIC PERFORMANCE (continued)

All specifications are at T_A = +25°C, VCC1 = VCC2 = +4.0V and VDD = +3.3V unless otherwise noted.

PARAMETER	CONDITIONS	PCM4222			UNITS
		MIN	TYP	MAX	
PCM output, Quad Speed mode, f_S = 192kHz	**BW = 22Hz to 80kHz**				
Total harmonic distortion + noise (THD+N)	f = 997Hz, –1dB input		–106		dB
	f = 997Hz, –20dB input		–91		dB
	f = 997Hz, –60dB input		–52		dB
Dynamic range, no weighting	f = 997Hz, –60dB input		112		dB
Dynamic range, A-weighted	f = 997Hz, –60dB input		123		dB
Channel separation/interchannel isolation	f = 10kHz, –1dB input		135		dB
PCM output, Quad Speed mode, f_S = 192kHz	**BW = 22Hz to 40kHz**				
Total harmonic distortion + noise (THD+N)	f = 997Hz, –1dB input		–107		dB
	f = 997Hz, –20dB input		–98		dB
	f = 997Hz, –60dB input		–58		dB
Dynamic range, no weighting	f = 997Hz, –60dB input		118		dB
Dynamic range, A-weighted	f = 997Hz, –60dB input		123		dB
Channel separation/interchannel isolation	f = 10kHz, –1dB input		135		dB
DSD output: 64x mode, 2.8224MHz output rate	**BW = 20Hz to 20kHz**				
Total harmonic distortion + noise (THD+N)	f = 997Hz, –1dB input		–108		dB
Dynamic range, no weighting	f = 997Hz, –60dB input		118		dB
Channel separation/interchannel isolation	f = 10kHz, –1dB input		135		dB
DSD output: 128x mode, 5.6448MHz output rate	**BW = 20Hz to 20kHz**				
Total harmonic distortion + noise (THD+N)	f = 997Hz, –1dB input		–108		dB
Dynamic range, no weighting	f = 997Hz, –60dB input		121		dB
Channel separation/interchannel isolation	f = 10kHz, –1dB input		135		dB
Multi-bit modulator (MBM) output, 6.144MHz output rate	**BW = 20Hz to 20kHz**				
Total harmonic distortion + noise (THD+N)	f = 997Hz, –1dB input		–108		dB
Dynamic range, no weighting	f = 997Hz, –60dB input		122		dB
Dynamic range, A-weighted	f = 997Hz, –60dB input		124		dB
Channel separation/interchannel isolation	f = 10kHz, –1dB input		135		dB
Digital decimation filter characteristics: Classic response					
Passband				$0.4535 \times f_S$	Hz
Passband ripple				±0.00015	dB
Stop band		$0.5465 \times f_S$			Hz
Stop band attenuation		–100			dB
Group delay				$39/f_S$	Seconds
Digital decimation filter characteristics: Low Group Delay response					
Passband				$0.4167 \times f_S$	Hz
Passband ripple				±0.001	dB
Stop band		$0.5833 \times f_S$			Hz
Stop band attenuation		–90			dB
Group delay				$21/f_S$	Seconds
Digital high-pass filter characteristics					
–3dB corner frequency	High-pass filter enabled			$f_S/48000$	Hz

ELECTRICAL CHARACTERISTICS: ANALOG INPUTS, OUTPUTS, AND DC ERROR

All specifications are at T_A = +25°C, VCC1 = VCC2 = +4.0V, and VDD = +3.3V, unless otherwise noted.

PARAMETER	CONDITIONS	PCM4222			UNITS
		MIN	TYP	MAX	
ANALOG INPUTS	**Applies to VINL+, VINL–, VINR+, and VINR–**				
Full-scale input range	Differential input		5.6		V_{PP}
	Per input pin		2.8		V_{PP}
Input impedance	Per input pin		2.8		kΩ
Common-mode rejection			100		dB
ANALOG OUTPUTS					
Common-mode output, left channel	Measured from VCOML (pin 13) to AGND		0.4875 × VCC2		V
Common-mode output, right channel	Measured from VCOMR (pin 48) to AGND		0.4875 × VCC1		V
Common-mode output current	Applies to VCOML or VCOMR			200	µA
DC ERROR					
Output offset error	Digital high-pass filter disabled		3		mV
Offset drift	Digital high-pass filter disabled		3.5		µV/°C

ELECTRICAL CHARACTERISTICS: POWER SUPPLIES

All specifications are at T_A = +25°C, VCC1 = VCC2 = +4.0V, VDD = +3.3V, and MCKI = 12.288MHz, unless otherwise noted.

PARAMETER	CONDITIONS	PCM4222			UNITS
		MIN	TYP	MAX	
POWER SUPPLIES					
Recommended supply voltage range					
VCC1, VCC2	0°C < T_A ≤ +85°C	+3.8	+4.0	+4.2	V
VCC1, VCC2	–40°C ≤ T_A ≤ 0°C	+3.9	+4.0	+4.2	V
VDD	–40°C ≤ T_A ≤ +85°C	+2.4	+3.3	+3.6	V
Supply current: power-down	$\overline{RST}$ (pin 36) held low with no clocks applied				
ICC1 + ICC2	VCC1 = VCC2 = +4.0V		600		µA
IDD	VDD = +3.3V		325		µA
Supply current: f_S = 48kHz					
ICC1 + ICC2	VCC1 = VCC2 = +4.0V		65	75	mA
IDD	VDD = +3.3V		14	18	mA
Supply current: f_S = 96kHz					
ICC1 + ICC2	VCC1 = VCC2 = +4.0V		65		mA
IDD	VDD = +3.3V		21		mA
Supply current: f_S = 192kHz					
ICC1 + ICC2	VCC1 = VCC2 = +4.0V		65		mA
IDD	VDD = +3.3V		24		mA
Total power dissipation: power-down			3.5		mW
Total power dissipation: f_S = 48kHz			305	360	mW
Total power dissipation: f_S = 96kHz			330		mW
Total power dissipation: f_S = 192kHz			340		mW

ELECTRICAL CHARACTERISTICS: AUDIO INTERFACE TIMING

All specifications are at T_A = +25°C, VCC1 = VCC2 = +4.0V, and VDD = +3.3V, unless otherwise noted.

PARAMETER	CONDITIONS	PCM4222			UNITS
		MIN	TYP	MAX	
AUDIO SERIAL PORT (PCM OUTPUT)					
LRCK period, t_{LRCKP}	All data formats	4.62		125	µs
LRCK high/low time, t_{LRCKHL}	**Left-Justified and I²S data formats**	0.45 × t_{LRCKP}		0.55 × t_{LRCKP}	µs
LRCK high/low time, t_{LRCKHL}	**TDM data formats**	0.45 × t_{LRCKP}		0.55 × t_{LRCKP}	µs
BCK period, t_{BCKP}	**Left-Justified and I²S data formats**				
	Normal sampling	t_{LRCKP}/128			ns
	Double Speed sampling	t_{LRCKP}/64			ns
	Quad Speed sampling	t_{LRCKP}/64			ns
BCK period, t_{BCKP}	**TDM data formats**				
	Normal sampling	t_{LRCKP}/256			ns
	Double Speed sampling	t_{LRCKP}/128			ns
	Quad Speed sampling	t_{LRCKP}/64			ns
BCK high/low time, t_{BCKHL}	All data formats	0.45 × t_{BCKP}		0.55 × t_{BCKP}	ns
Data output delay, t_{DO}	All data formats			10	ns
DSD OUTPUT					
DSDCLK period, $t_{DSDCLKP}$	64x output rate	289		1954	ns
	128x output rate	144.5		977	ns
DSDCLK high/low time, $t_{DSDCLKHL}$		0.45 × $t_{DSDCLKP}$		0.55 × $t_{DSDCLKP}$	ns
Data output delay, t_{DSDO}				10	ns
MULTI-BIT MODULATOR OUTPUT					
MCKI period, t_{MCKIP}		72.3		488.3	ns
MCKI high/low time, t_{MCKIHL}		0.45 × t_{MCKIP}		0.55 × t_{MCKIP}	ns
WCKO period, t_{WCKOP}		144.5		977	ns
WCKO high/low time, t_{WCKOHL}		0.45 × t_{WCKOP}		0.55 × t_{WCKOP}	ns
Data output delay, t_{MODO}				15	ns

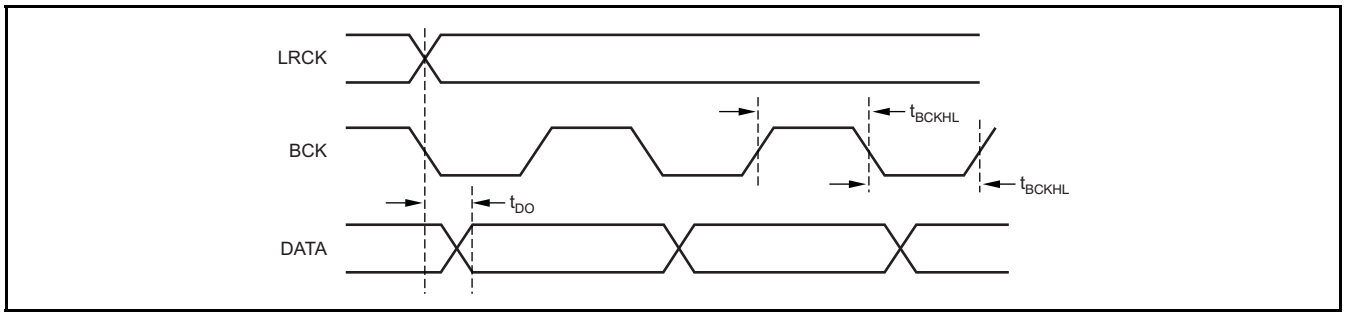


Figure 1. Audio Serial Port Timing: Left-Justified and I²S Data Formats

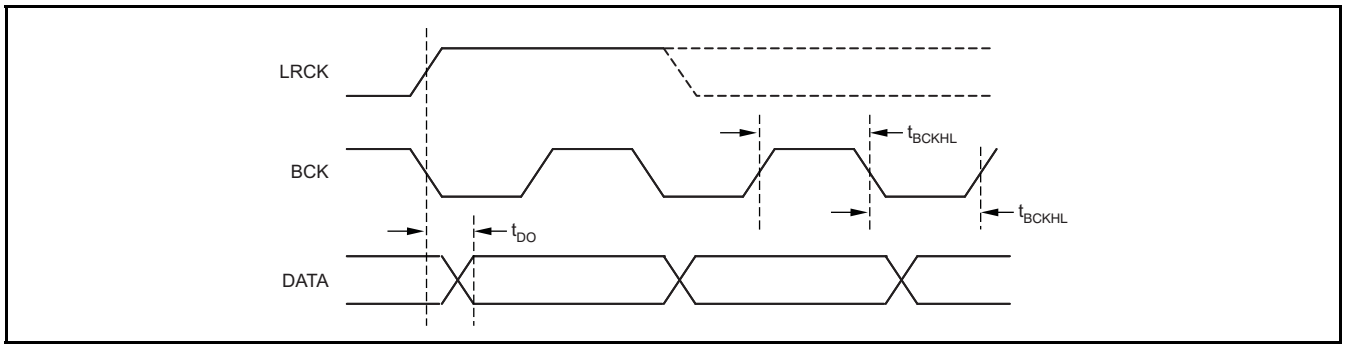


Figure 2. Audio Serial Port Timing: TDM Data Formats

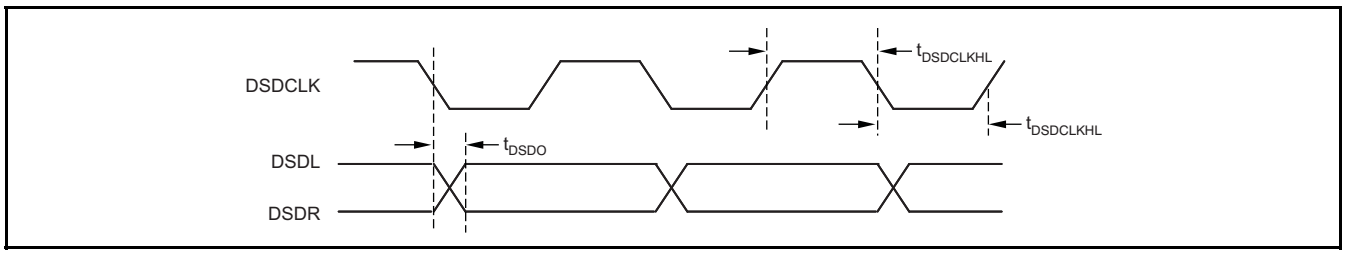


Figure 3. Direct Stream Digital (DSD) Output Timing

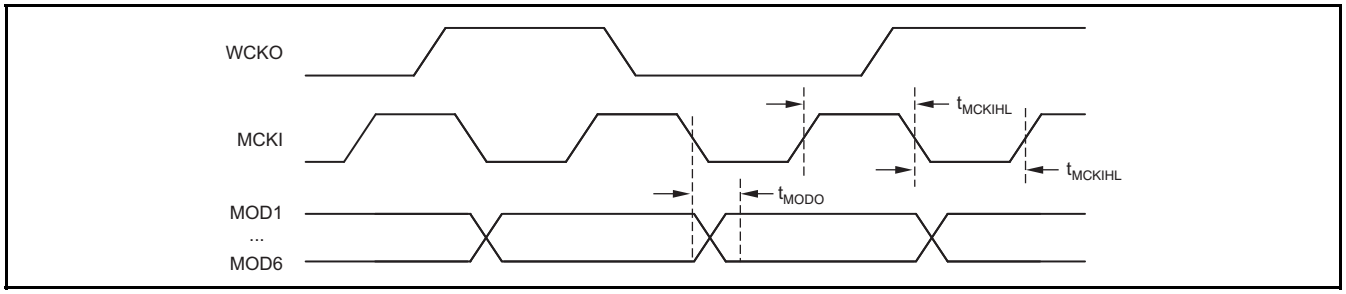
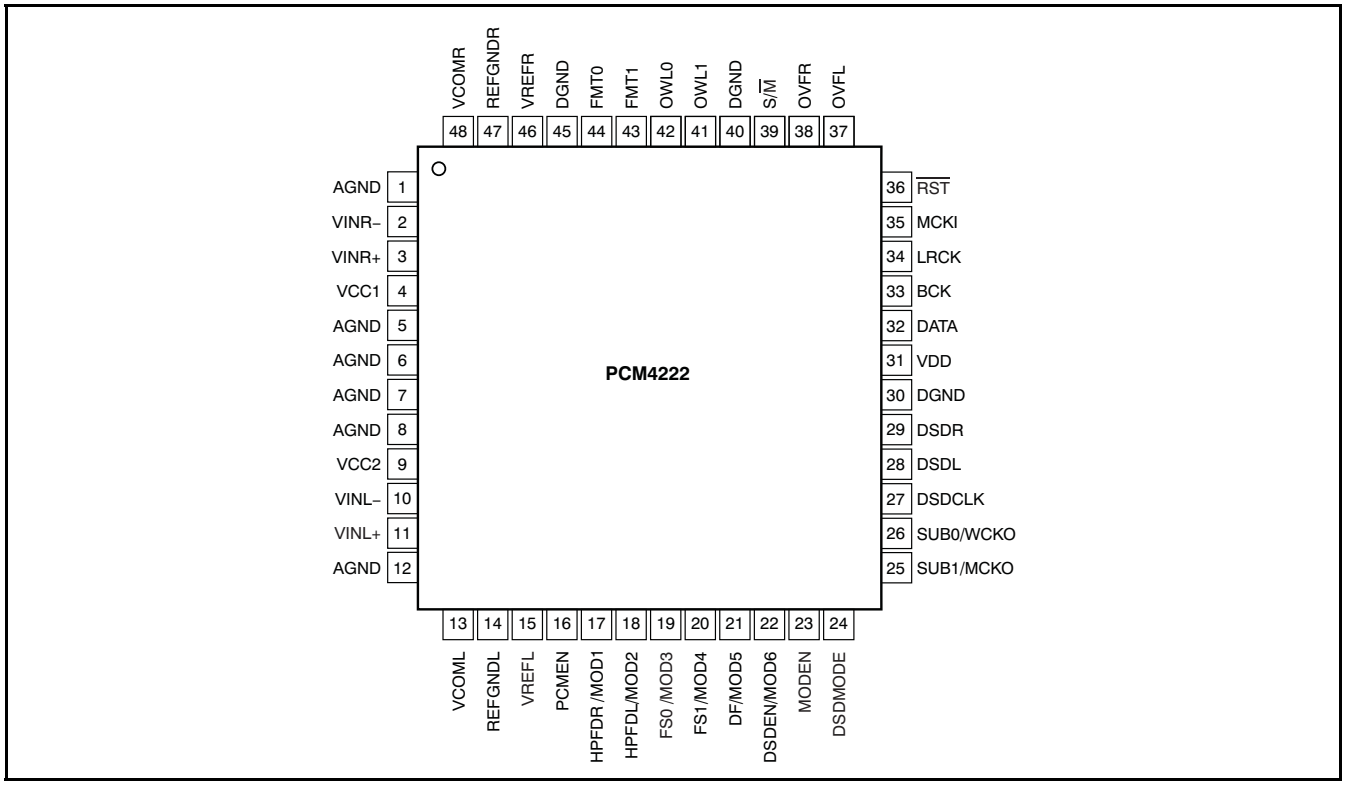


Figure 4. Multi-Bit Modulator (MBM) Output Timing

PIN CONFIGURATION

TQFP-64
Top View



PIN DESCRIPTIONS

NAME	PIN NUMBER	I/O	DESCRIPTION
AGND	1	Ground	Analog ground
VINR–	2	Input	Right channel inverting, 2.8V_{PP} nominal full-scale
VINR+	3	Input	Right channel noninverting, 2.8V_{PP} nominal full-scale
VCC1	4	Power	Analog supply, +4.0V nominal
AGND	5	Ground	Analog ground
AGND	6	Ground	Analog ground
AGND	7	Ground	Analog ground
AGND	8	Ground	Analog ground
VCC2	9	Power	Analog supply, +4.0V nominal
VINL–	10	Input	Left channel inverting, 2.8V_{PP} nominal full-scale
VINL+	11	Input	Left channel noninverting, 2.8V_{PP} nominal full-scale
AGND	12	Ground	Analog ground
VCOML	13	Output	Left channel common-mode voltage, (0.4875 × VCC2) nominal
REFGNDL	14	Ground	Left channel reference ground. Connect to analog ground.
VREFL	15	Output	Left channel reference output for decoupling purposes only.
PCMEN	16	Input	PCM output enable (active high)
HPFDR or MOD1	17	I/O	Right channel high-pass filter disable input (active high), or modulator Data output 1 (LSB) when MODEN = high.
HPFDL or MOD2	18	I/O	Left channel high-pass filter disable input (active high), or modulator data output 2 when MODEN = high.
FS0 or MOD3	19	I/O	PCM sampling mode selection input, or modulator data output 3 when MODEN = high.
FS1 or MOD4	20	I/O	PCM sampling mode selection input, or modulator data output 4 when MODEN = high.
DF or MOD5	21	I/O	Digital decimation filter response selection Input, or modulator data output 5 when MODEN = high.

PIN DESCRIPTIONS (continued)

NAME	PIN NUMBER	I/O	DESCRIPTION
DSDEN or MOD6	22	I/O	DSD output enable input (active high), or modulator data output 6 (MSB) when MODEN = high.
MODEN	23	Input	Multi-bit modulator output enable (Active High)
DSDMODE	24	Input	DSD output mode/rate
SUB1 or MCKO	25	I/O	TDM active sub-frame selection input, or master clock output when MODEN = high.
SUB0 or WCKO	26	I/O	TDM active sub-frame selection input, or modulator left/right word clock output when MODEN = high.
DSDCLK	27	Output	DSD data clock
DSDL	28	Output	Left channel DSD data
DSDR	29	Output	Right channel DSD data
DGND	30	Ground	Digital ground
VDD	31	Power	Digital supply, +3.3V nominal
DATA	32	Output	PCM output data
BCK	33	I/O	PCM bit or data clock
LRCK	34	I/O	PCM left/right Word clock
MCKI	35	Input	Master clock
$\overline{\text{RST}}$	36	Input	Reset and power-down
OVFL	37	Output	Left channel overflow flag (Active high)
OVFR	38	Output	Right channel overflow flag (Active high)
S/$\overline{\text{M}}$	39	Input	PCM output slave/master mode
DGND	40	Output	Digital ground
OWL1	41	Input	PCM output word length
OWL0	42	Input	PCM output word length
FMT1	43	Input	PCM output data format
FMT0	44	Input	PCM output data format
DGND	45	Ground	Digital ground
VREFR	46	Output	Right channel reference output for decoupling purposes only.
REFGNDR	47	Ground	Right channel reference ground. Connect to analog ground.
VCOMR	48	Output	Right channel common-mode voltage (0.4875 x VCC1 nominal)

TYPICAL CHARACTERISTICS

At T_A = +25°C, VCC1 = VCC2 = +4.0V, and VDD = +3.3V, unless otherwise noted.

FFT PLOT

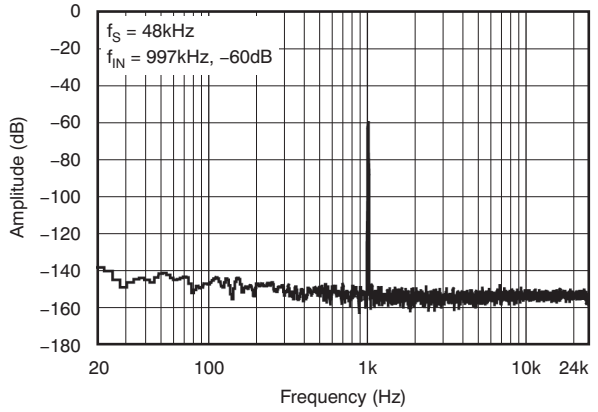


Figure 5.

FFT PLOT

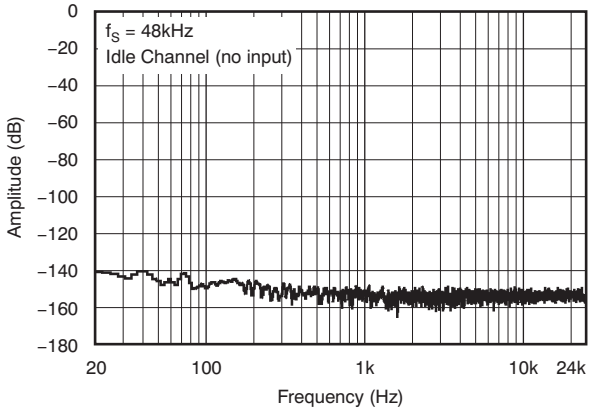


Figure 6.

THD+N vs INPUT FREQUENCY

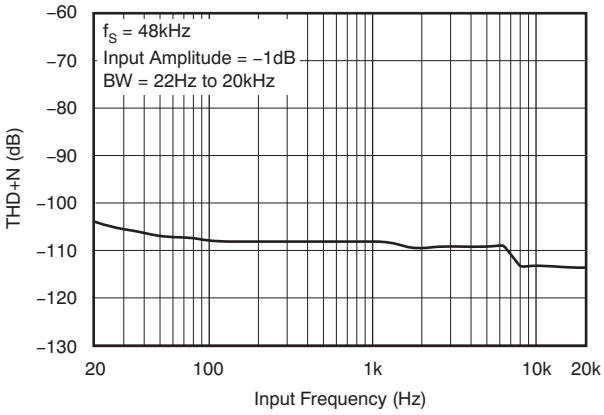


Figure 7.

THD+N vs INPUT AMPLITUDE

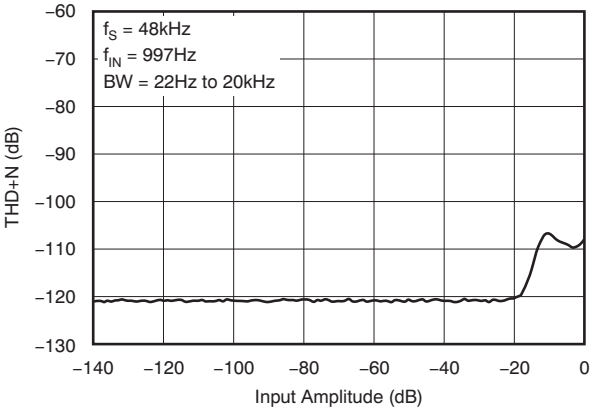


Figure 8.

CHANNEL SEPARATION vs INPUT FREQUENCY

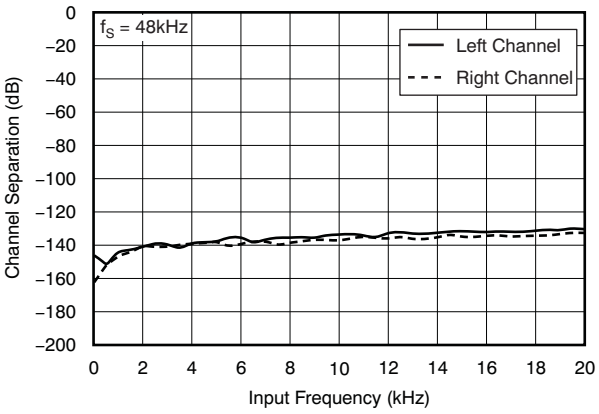


Figure 9.

LINEARITY

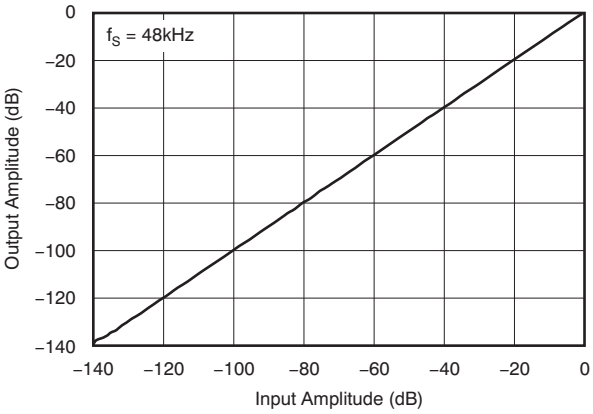


Figure 10.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, VCC1 = VCC2 = +4.0V, and VDD = +3.3V, unless otherwise noted.

FFT PLOT

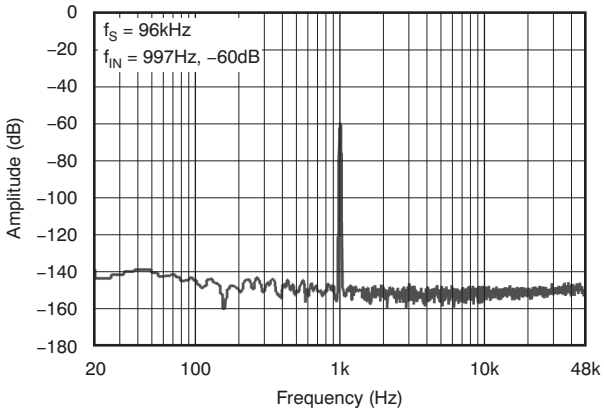


Figure 11.

FFT PLOT

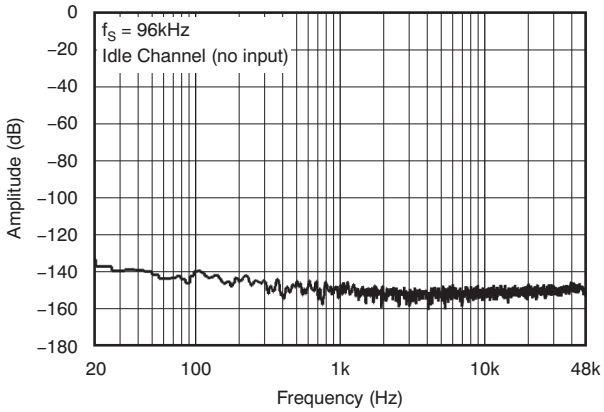


Figure 12.

THD+N vs INPUT FREQUENCY

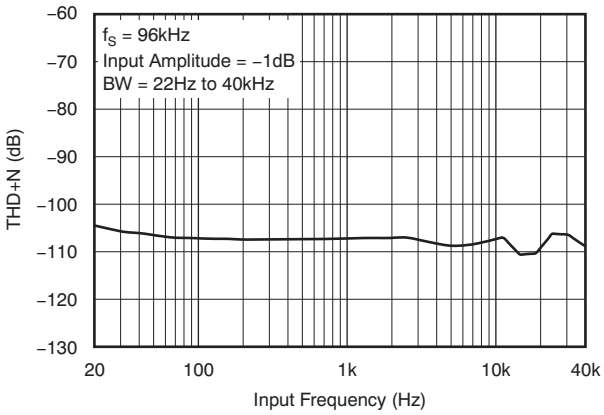


Figure 13.

THD+N vs INPUT AMPLITUDE

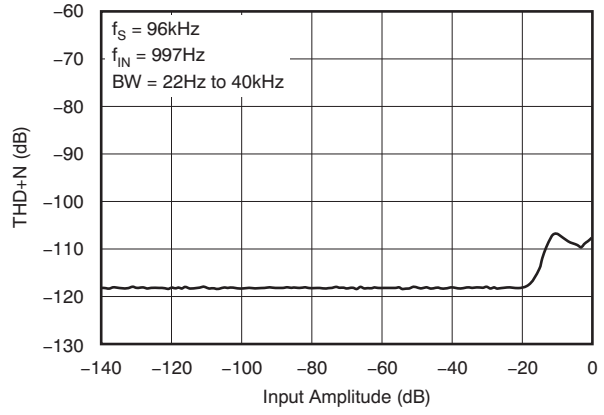


Figure 14.

CHANNEL SEPARATION vs INPUT FREQUENCY

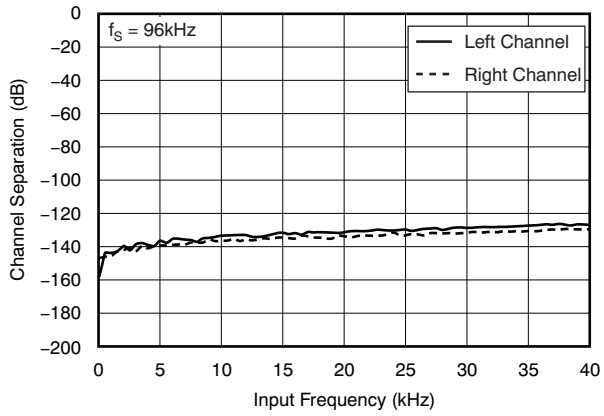


Figure 15.

LINEARITY

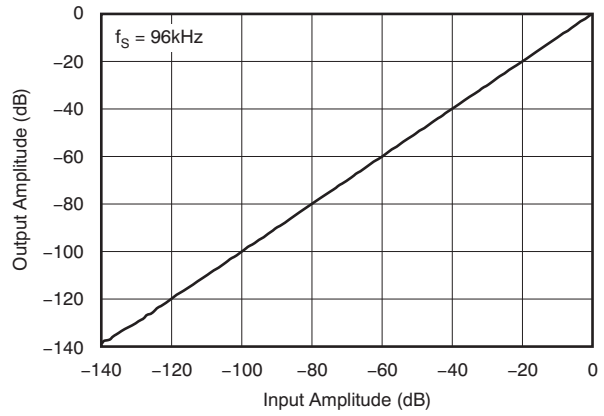


Figure 16.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, VCC1 = VCC2 = +4.0V, and VDD = +3.3V, unless otherwise noted.

FFT PLOT

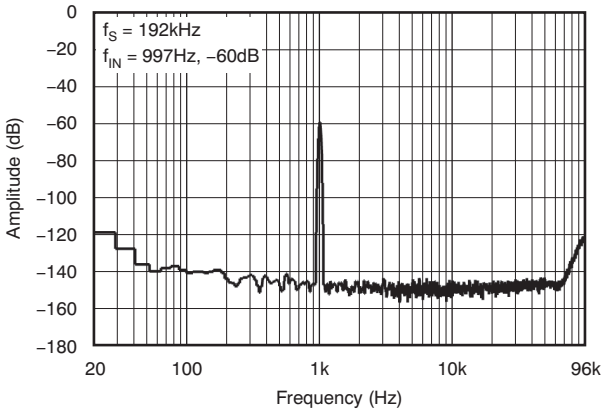


Figure 17.

FFT PLOT

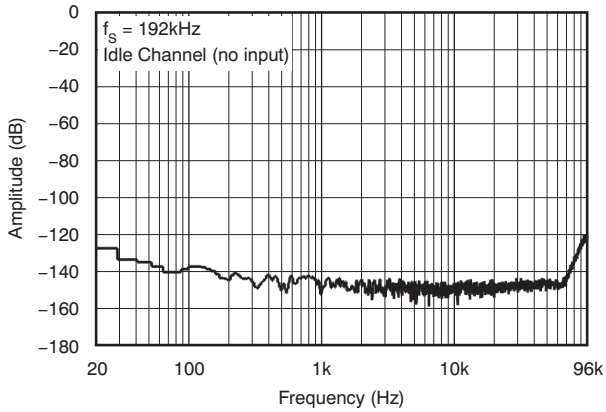


Figure 18.

THD+N vs INPUT FREQUENCY

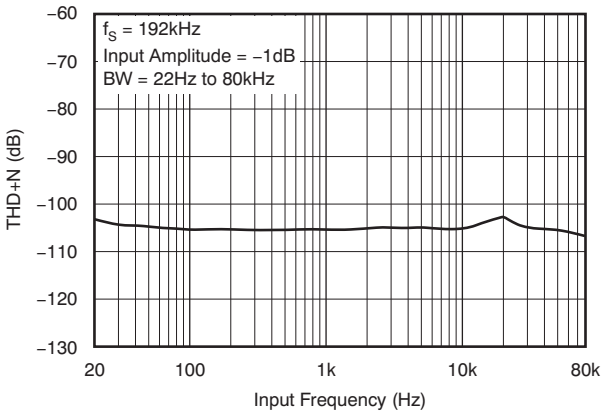


Figure 19.

THD+N vs INPUT AMPLITUDE

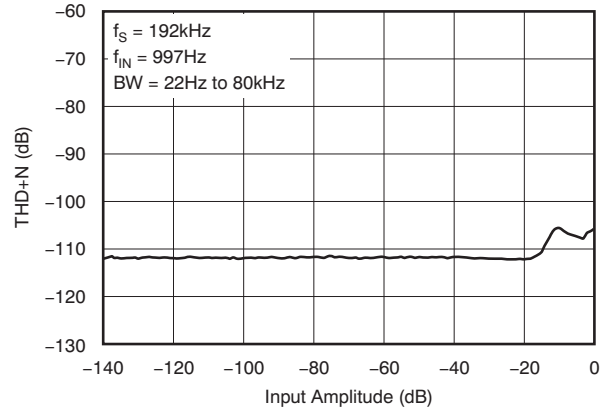


Figure 20.

CHANNEL SEPARATION vs INPUT FREQUENCY

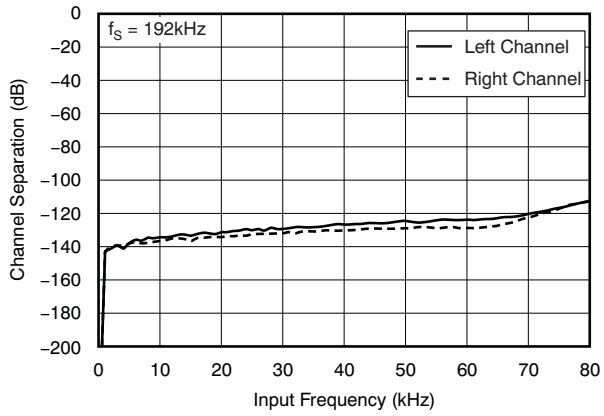


Figure 21.

LINEARITY

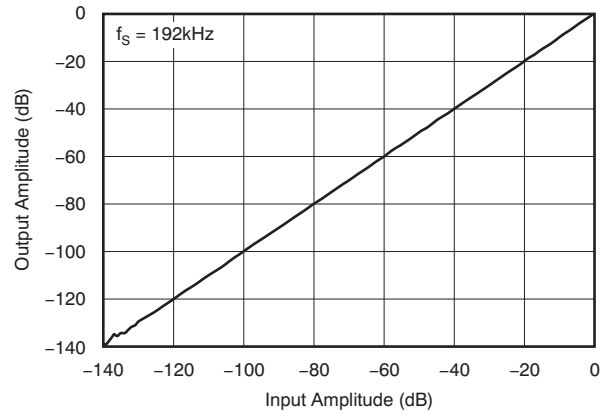


Figure 22.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, VCC1 = VCC2 = +4.0V, and VDD = +3.3V, unless otherwise noted.

FREQUENCY RESPONSE (up to 20kHz)

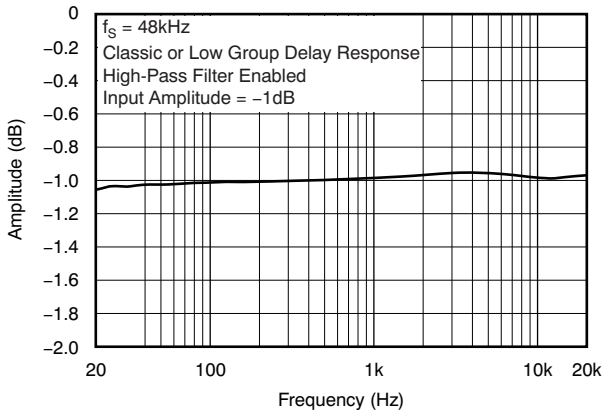


Figure 23.

FREQUENCY RESPONSE (up to 40kHz)

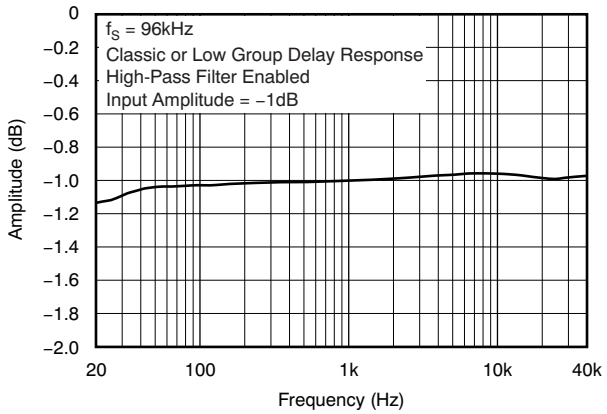


Figure 24.

FREQUENCY RESPONSE (up to 80kHz)

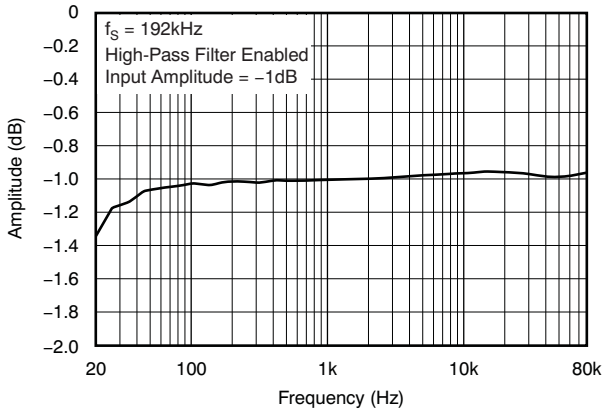


Figure 25.

DIGITAL DECIMATION FILTER, CLASSIC RESPONSE Overall Frequency Response

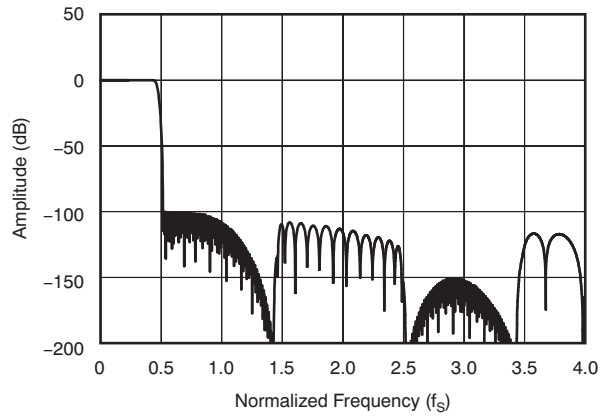


Figure 26.

DIGITAL DECIMATION FILTER, CLASSIC RESPONSE Stop Band Detail

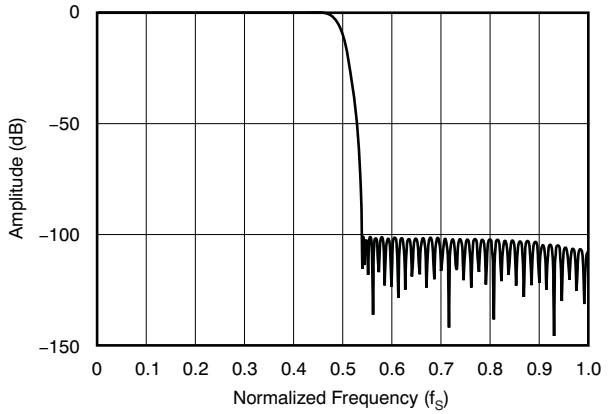


Figure 27.

DIGITAL DECIMATION FILTER, CLASSIC RESPONSE Passband Ripple Detail

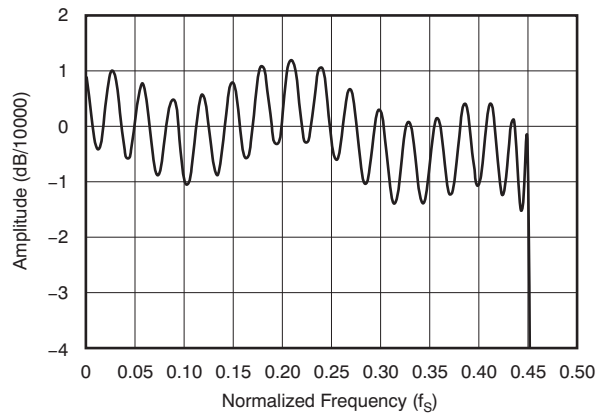


Figure 28.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, VCC1 = VCC2 = +4.0V, and VDD = +3.3V, unless otherwise noted.

DIGITAL DECIMATION FILTER, CLASSIC RESPONSE
Transition Band Detail

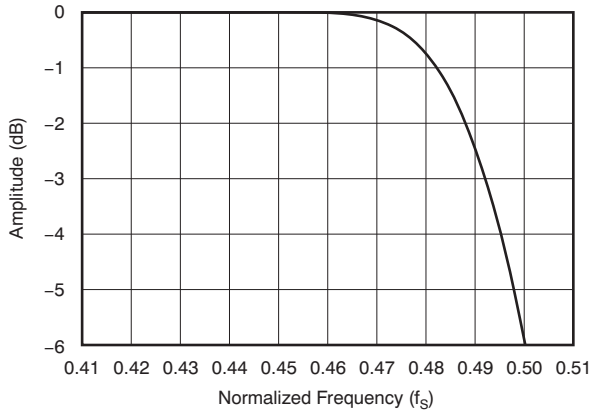


Figure 29.

DIGITAL DECIMATION FILTER, LOW GROUP DELAY RESPONSE
Overall Frequency Response

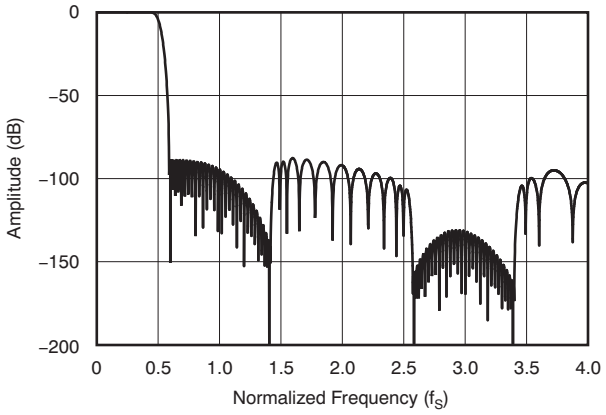


Figure 30.

DIGITAL DECIMATION FILTER, LOW GROUP DELAY RESPONSE
Stop Band Detail

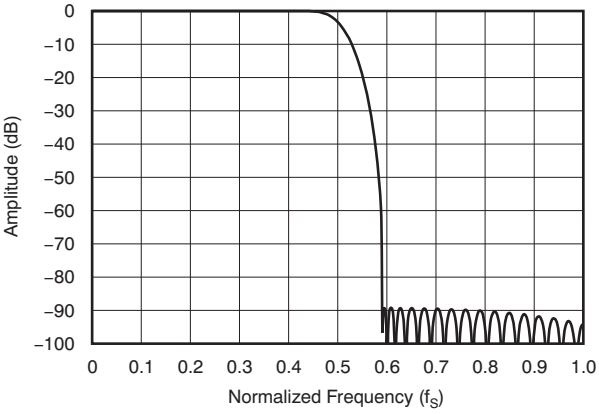


Figure 31.

DIGITAL DECIMATION FILTER, LOW GROUP DELAY RESPONSE
Passband Ripple Detail

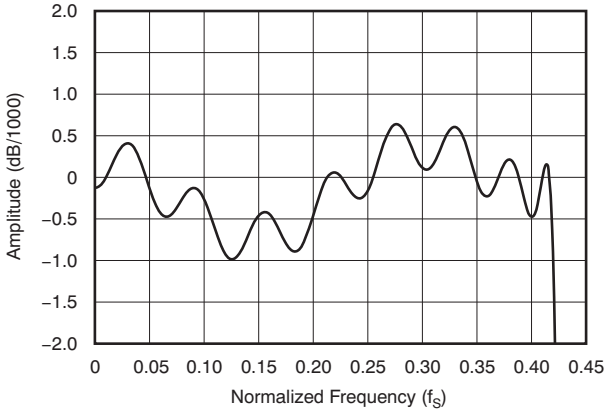


Figure 32.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, VCC1 = VCC2 = +4.0V, and VDD = +3.3V, unless otherwise noted.

DIGITAL DECIMATION FILTER, LOW GROUP DELAY RESPONSE
Transition Band Detail

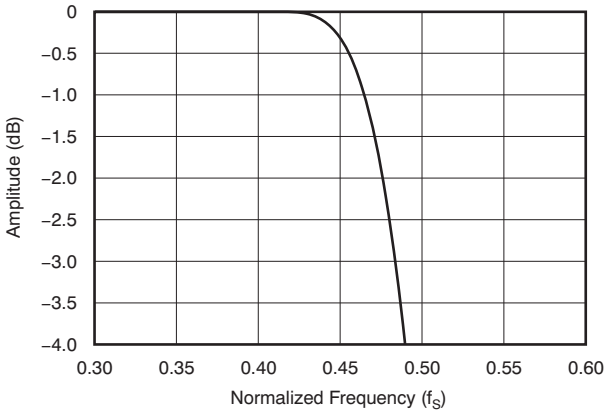


Figure 33.

DIGITAL HIGH-PASS FILTER
Passband Response

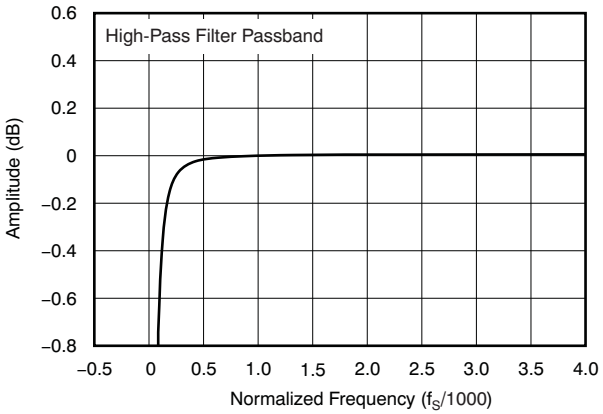


Figure 34.

DIGITAL HIGH-PASS FILTER
Stop Band Response

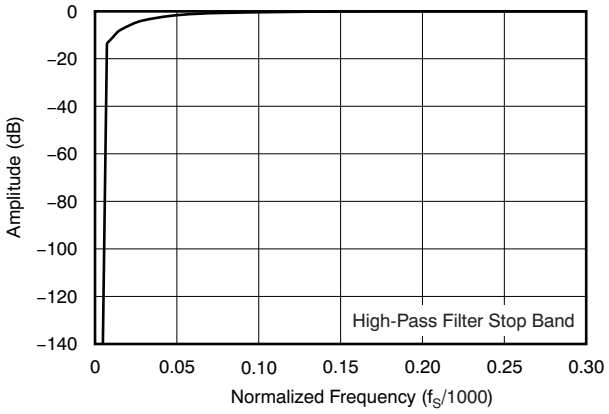


Figure 35.

PRODUCT INFORMATION

The PCM4222 is a two-channel, multi-bit delta-sigma (ΔΣ) analog-to-digital (A/D) converter. The 6-bit outputs from the delta-sigma modulators are routed to the digital decimation filter, where the output of the filter provides linear PCM data. The linear PCM data are output at the audio serial port interface for connection to external processing and logic circuitry. The multi-bit modulator outputs are also routed to a direct stream digital (DSD) engine, which converts the multi-bit data to one-bit DSD data. The DSD data are output at a separate serial interface, allowing both PCM and DSD data to be output simultaneously from the PCM4222. The multi-bit modulator data may also be output directly, for use by external digital filtering and processing hardware. When the modulator output mode is enabled, the PCM and DSD outputs are not available.

Figure 36 shows a simplified functional block diagram for the PCM4222, highlighting the interconnection between the various functional blocks. The pin names noted in parentheses on the block diagram reflect the pin configuration for the Multi-Bit Modulator (MBM) output mode.

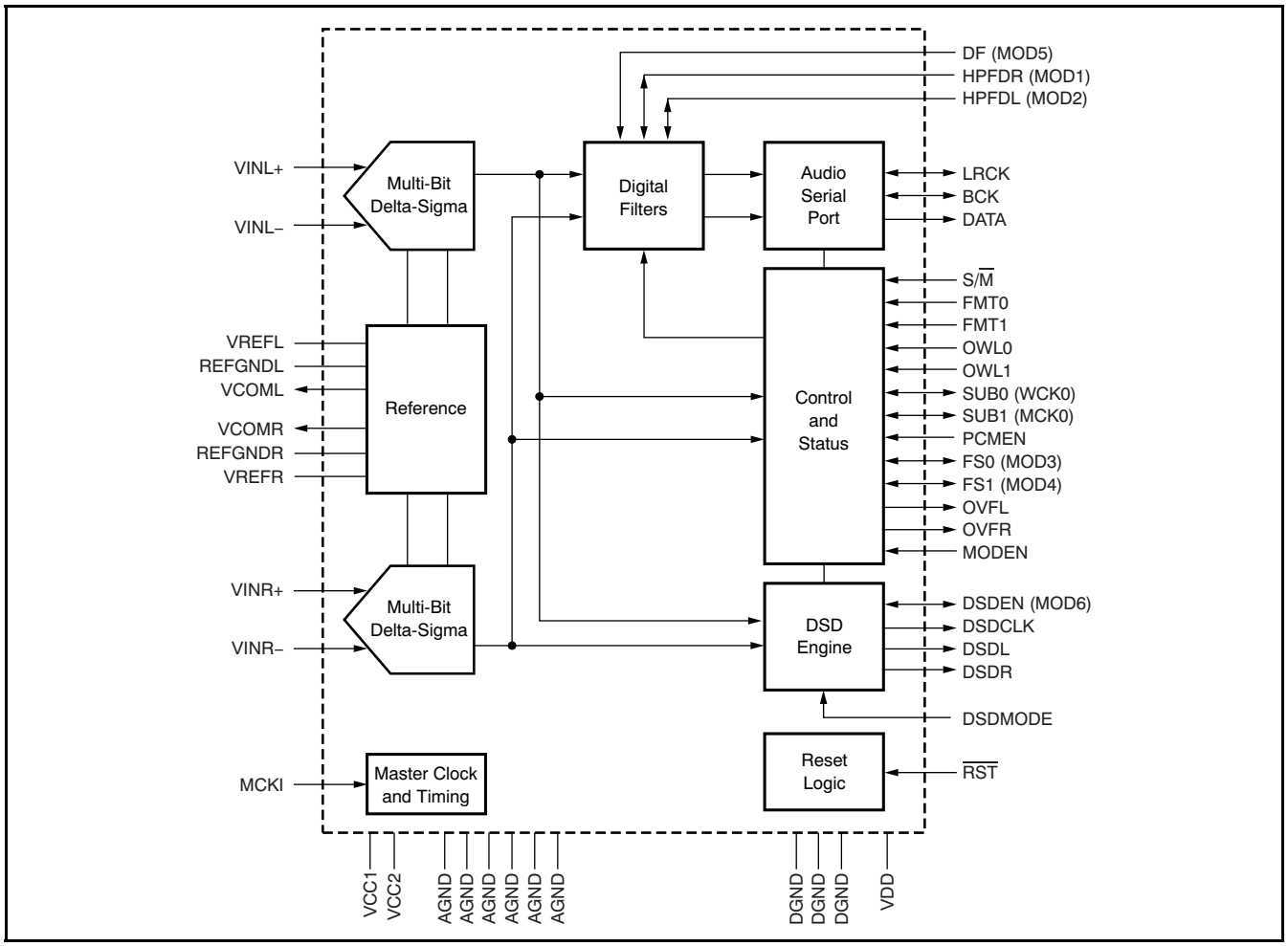


Figure 36. Functional Block Diagram

PRODUCT INFORMATION (continued)

ANALOG INPUTS

The PCM4222 includes two analog inputs, referred to as the *left* and *right* channels. Each channel includes a pair of differential voltage input pins. The left channel inputs are named VINL– (pin 10) and VINL+ (pin 11), respectively. The right channel inputs are named VINR– (pin 2) and VINR+ (pin 3), respectively. Each pin of an input pair has a nominal full scale input of $2.8V_{PP}$. The full-scale input for a given pair is specified as $5.6V_{PP}$ differential in the Electrical Characteristics table. Figure 37 shows the full-scale input range of the PCM4222, with the input signals centered on the nominal common-mode voltage of +1.95V.

In a typical application, the front end is driven by a buffer amplifier or microphone/line level preamplifier. Examples are given in the Input Buffer Circuits section of this datasheet. The analog inputs of the PCM4222 may be driven up to the absolute maximum input rating without instability. If the analog input voltage is expected to exceed the absolute maximum input ratings in a given application, it is recommended that input clamping or limiting be added to the analog input circuitry prior to the PCM4222 in order to provide protection against damaging the device. Specifications for the analog inputs are given in the Electrical Characteristics and Absolute Maximum Ratings tables of this datasheet.

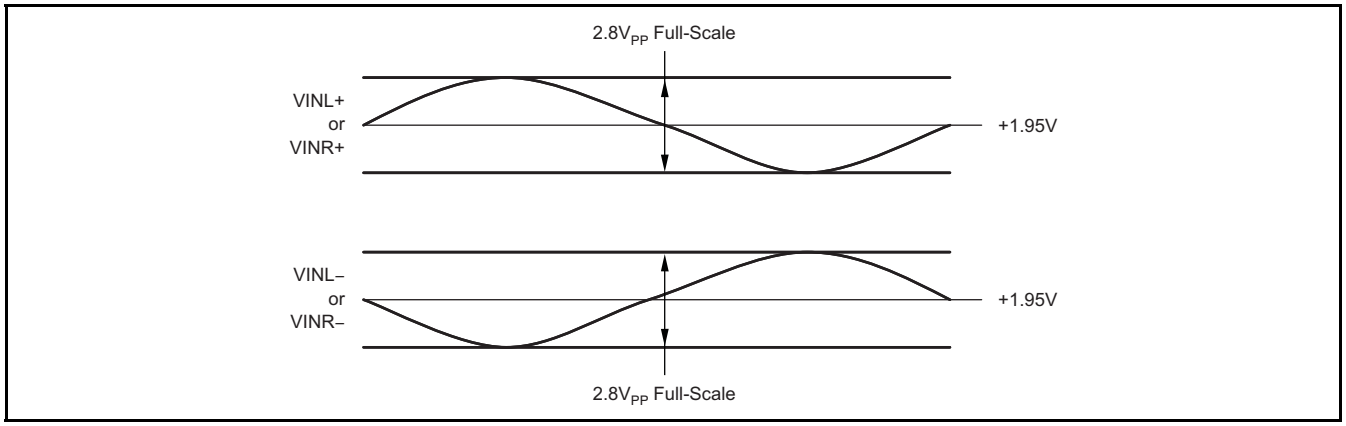


Figure 37. Full-Scale Analog Input Range

VOLTAGE REFERENCE

The PCM4222 includes an on-chip, band-gap voltage reference. The band-gap output voltage is buffered and then routed to the two delta-sigma modulators. The inclusion of an on-chip reference circuit enhances the power-supply noise rejection of the PCM4222. The buffered reference voltage for each channel is filtered using external capacitors. The capacitors are connected between VREFL (pin 15) and REFGNDL (pin 14) for the left channel, and VREFR (pin 46) and REFGNDR (pin 47) for the right channel. Figure 38 illustrates the recommend reference decoupling capacitor values and connection scheme.

The 10nF to 100nF capacitors in Figure 38 may be metal film or X7R/C0G ceramic chip capacitors. The 100µF capacitors may be polymer tantalum chip (Kemet T520 series or equivalent) or aluminum electrolytic.

The VREFL and VREFR pins are not designed for biasing external input circuitry. Two common-mode voltage outputs are provided for this purpose, and are discussed in the following section.

PRODUCT INFORMATION (continued)

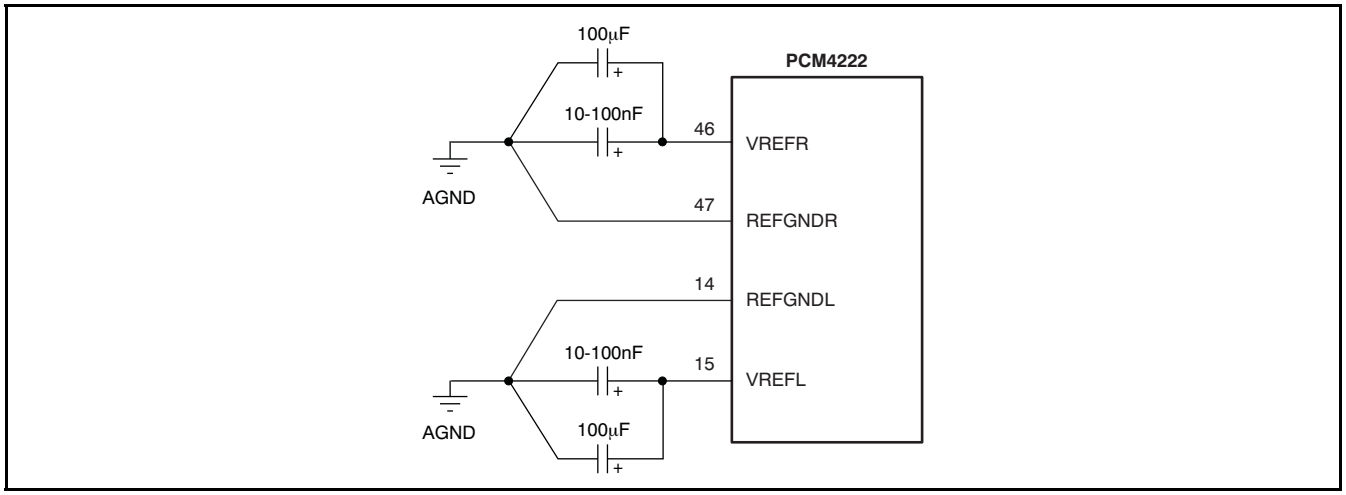


Figure 38. Recommended Reference Capacitor Connections and Values

COMMON-MODE VOLTAGE OUTPUTS

The PCM4222 includes two dc common-mode voltage outputs, VCOML (pin 13) and VCOMR (pin 48), which correspond to the left and right input channels, respectively. The common-mode voltage is utilized to bias internal op amps within the modulator section of the PCM4222, and may be used to bias external input circuitry when proper design guidelines are followed. The common-mode voltages are derived from the VCC1 and VCC2 analog power supplies using internal voltage dividers. The voltage divider outputs are buffered and then routed to internal circuitry and the VCOML and VCOMR outputs.

The common-mode output voltage is nominally equal to (0.4875 × VCC1) for VCOMR and (0.4875 × VCC2) for VCOML. Given an analog supply voltage of +4.0V connected to both VCC1 and VCC2, the resulting common-mode voltages are +1.95V.

The common-mode voltage outputs have limited drive capability. If multiple bias points are to be driven, or the external bias nodes are not sufficiently high impedance, an external output buffer is recommended. Figure 39 shows a typical buffer configuration using the OPA227. The op amp utilized in the buffer circuit should exhibit low dc offset and drift characteristics, as well as low output noise.

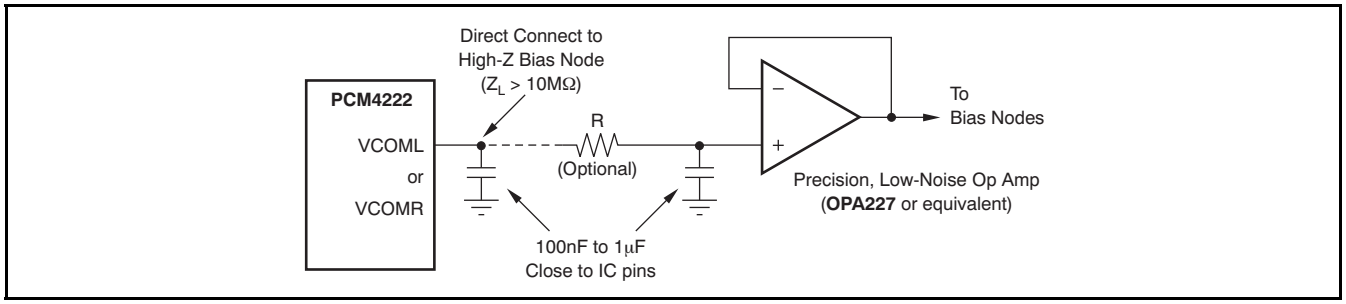


Figure 39. Common-Mode Output Connections

PRODUCT INFORMATION (continued)

MASTER CLOCK INPUT

The PCM4222 requires a master clock for operating the internal logic and modulator circuitry. The master clock is supplied from an external source, connected at the MCKI input (pin 35). Table 1 summarizes the requirements for various operating modes of the PCM4222. Referring to Table 1, the term f_S refers to the PCM4222 PCM output sampling rate (that is, 48kHz, 96kHz, 192kHz, etc.). Refer to the Electrical Characteristics table for timing specifications related to the master clock input, as well as the output sampling and data rates for the PCM, DSD, and multi-bit output modes.

For best performance, the master clock jitter should be maintained below 40ps peak amplitude.

Table 1. Master Clock Requirements

OPERATING MODE	REQUIRED MASTER CLOCK (MCKI) RATE
PCM Normal	$256f_S$
PCM Double Speed	$128f_S$
PCM Quad Speed	$64f_S$
DSD with 64x output rate	4x the desired DSD output rate
DSD with 128x output rate	2x the desired DSD output rate
Multi-bit modulator (MBM)	2x the desired modulator output rate

RESET AND POWER-DOWN OPERATION

The PCM4222 includes an external reset input, $\overline{RST}$ (pin 36), which may be utilized to force an internal reset initialization or power down sequence. The reset input is active low. Figure 40 shows the required timing for an external forced reset.

A power-down state for the PCM422 may be initiated by forcing and holding the reset input low for the duration of the desired power-down condition. Minimum power is consumed during this state when all clock inputs for the PCM4222 are forced low. Before releasing the reset input by forcing a high state, the master clock should be enabled so that the PCM4222 can execute a reset initialization sequence.

While the $\overline{RST}$ pin is forced low, or during reset initialization, the audio data and clock outputs are driven to fixed states. The following is a summary of the PCM, DSD, and Multi-Bit Modulator audio interfaces. The conditions noted assume that the given interface has been enabled (that is, PCMEN, DSDEN, or MODEN forced high).

- For PCM mode, the audio serial port LRCK, BCK and DATA are driven low if the port is configured for Master mode operation. For Slave mode, the DATA pin is forced low.
- For DSD mode, the DSDL, DSDR, and DSDCLK outputs are driven low.
- For the Multi-Bit Modulator (or MBM) mode, the WCKO, MCKO, and MOD1–MOD6 outputs are all driven low.

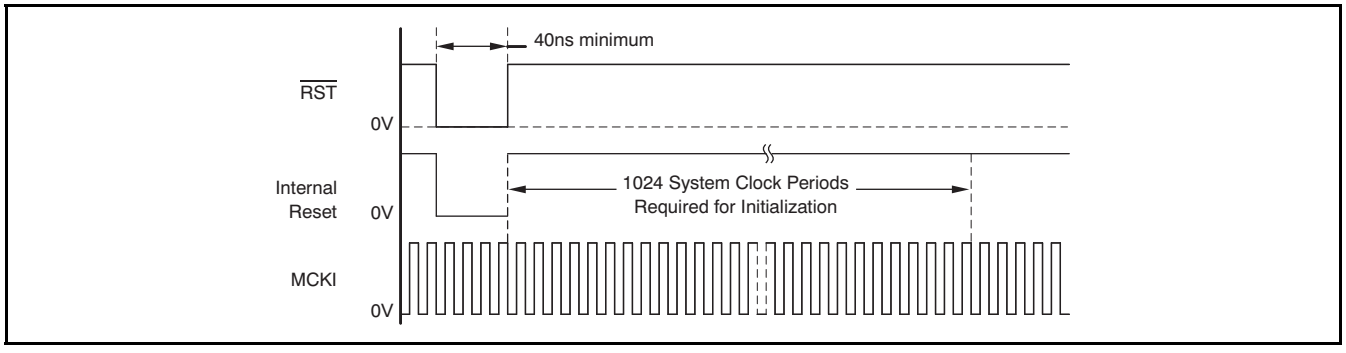


Figure 40. External Reset Sequence

DISABLED STATES FOR THE PCM4222 AUDIO INTERFACES

When a particular mode is disabled, the output data and clocks associated with that mode are driven low. The exception is when MODEN is driven low, disabling the multi-bit modulator output. For this case, the data and clock outputs associated with the modulator output are re-mapped to functions utilized for either PCM or DSD mode operation.

PCM OUTPUT AND SAMPLING MODES

The PCM4222 supports 24-bit linear PCM output data when the PCMEN input (pin 16) is forced high. The PCM output is disabled when PCMEN is forced low. The 24-bit output data may be dithered to 20-, 18-, or 16-bits using internal word length reduction circuitry. Refer to the Output Word Length Reduction section of this data sheet for additional information.

The PCM4222 supports three PCM sampling modes, referred to as Normal, Double Speed, and Quad Speed. The sampling mode is determined by the state of the FS0 and FS1 inputs (pins 19 and 20, respectively). Table 2 summarizes the sampling modes available for the PCM4222.

Normal sampling mode supports output sampling rates from 8kHz to 54kHz. The ΔΣ modulator operates with 128x oversampling in this mode. Both the Classic and Low Group Delay decimation filter responses are available in Normal mode. The master clock (MCKI) rate must be 256x the desired output sampling rate for Normal operation.

The Double Speed sampling mode supports output sampling rates from 54kHz to 108kHz. The delta-sigma modulator operates with 64x oversampling in this mode. Both the Classic and Low Group Delay decimation filter responses are available in Double Speed mode. The master clock (MCKI) rate must be 128x the desired output sampling rate for Double Speed operation.

Quad Speed sampling mode supports output sampling rates from 108kHz to 216kHz. The delta-sigma modulator operates with 32x oversampling in this mode. Only the Low Group Delay decimation filter response is available in Quad Speed mode. The master clock (MCKI) rate must be 64x the desired output sampling rate for Quad Speed operation.

Table 2. PCM Sampling Mode Configuration

FS1 (pin 20)	FS0 (pin 19)	SAMPLING MODE
LO	LO	Normal, 8kHz ≤ f_S ≤ 54kHz
LO	HI	Double Speed, 54kHz < f_S ≤ 108kHz
HI	LO	Quad Speed, 108kHz < f_S≤ 216kHz
HI	HI	Reserved

AUDIO SERIAL PORT INTERFACE

The PCM output mode supports a three-wire synchronous serial interface. This interface includes a serial data output (DATA, pin 32), a serial bit or data clock (BCK, pin 33), and a left/right word clock (LRCK, pin 34). The BCK and LRCK clock pins may be inputs or outputs, dependent upon the Slave or Master mode configuration. Figure 41 illustrates Slave and Master mode serial port connections to an external audio signal processor or host device.

The audio serial port supports four data formats that are illustrated in Figure 42, Figure 44, and Figure 45. The I^2S and Left-Justified formats support two channels of audio output data. The TDM data formats can support up to eight channels of audio output data on a single data line. The audio data format is selected using the FMT0 and FMT1 inputs (pins 44 and 43, respectively). Table 3 summarizes the audio data format options. For all formats, audio data are represented as two's complement binary data, with the MSB transmitted first. Regardless of the format selection, audio data are always clocked out of the port on the falling edge of the BCK clock.

Table 3. PCM Audio Data Format Selection

FMT1 (pin 43)	FMT0 (pin 44)	AUDIO DATA FORMAT
LO	LO	Left-Justified
LO	HI	I^2S
HI	LO	TDM
HI	HI	TDM with data delayed one BCK cycle from LRCK rising edge

The LRCK clock rate should always be operated at the desired output sampling rate, or f_S. In Slave mode, the LRCK clock is an input, with the rate set by an external audio bus master (that is, a clock generator, digital signal processor, etc.). In Master mode, the LRCK clock is an output, derived from the master clock input using on-chip clock dividers (as is the BCK clock). The clock divider is configured using the FS0 and FS1 pins, which are discussed in the PCM Output and Sampling Modes section of this datasheet.

For the I^2S and Left-Justified data formats, the BCK clock output rate is fixed in Master mode, with the Normal mode being $128f_S$ and the Double and Quad Speed modes being $64f_S$. In Slave Mode, a BCK clock input rate of $64f_S$ or $128f_S$ is recommended for Normal mode, while $64f_S$ is recommended for Double and Quad Rate modes.

For the TDM data formats, the BCK rate depends upon the sampling mode for either Slave or Master operation. For Normal sampling, the BCK must be $256f_S$. Double Speed mode requires $128f_S$, while Quad Speed mode requires $64f_S$. This requirement limits the maximum number of channels carried by the TDM formats to eight for Normal mode, four for Double Rate mode, and two for Quad Rate mode.

When using the TDM formats, the sub-frame assignment for the device must be selected using the SUB0 and SUB1 inputs (pins 26 and 25, respectively). Table 4 summarizes the sub-frame selection options. A sub-frame contains two 32-bit time slots, with each time slot carrying 24-bits of audio data corresponding to either the left or right channel of the PCM4222. Refer to Figure 43 through Figure 45 for TDM interfacing connections and sub-frame formatting details. For the TDM format with one BCK delay, the serial data output is delayed by one BCK period after the rising edge of the LRCK clock.

Table 4. TDM Sub-frame Assignment

SUB1 (pin 25)	SUB0 (pin 26)	SUB-FRAME ASSIGNMENT
LO	LO	Sub-frame 0
LO	HI	Sub-frame 1
HI	LO	Sub-frame 2
HI	HI	Sub-frame 3

When using TDM formats with Double Speed sampling, it is recommended that the SUB1 pin be forced low. When using TDM formats with Quad Speed sampling, it is recommended that both the SUB0 and SUB1 pins be forced low.

For all serial port modes and data formats, when driving capacitive loads greater than 30pF with the data and clock outputs, it is recommended that external buffers be utilized to ensure data and clock integrity at the receiving device(s).

For specifications regarding audio serial port operation, the reader is referred to the Electrical Characteristics: Audio Interface Timing table, as well as Figure 1 and Figure 2 in this datasheet.

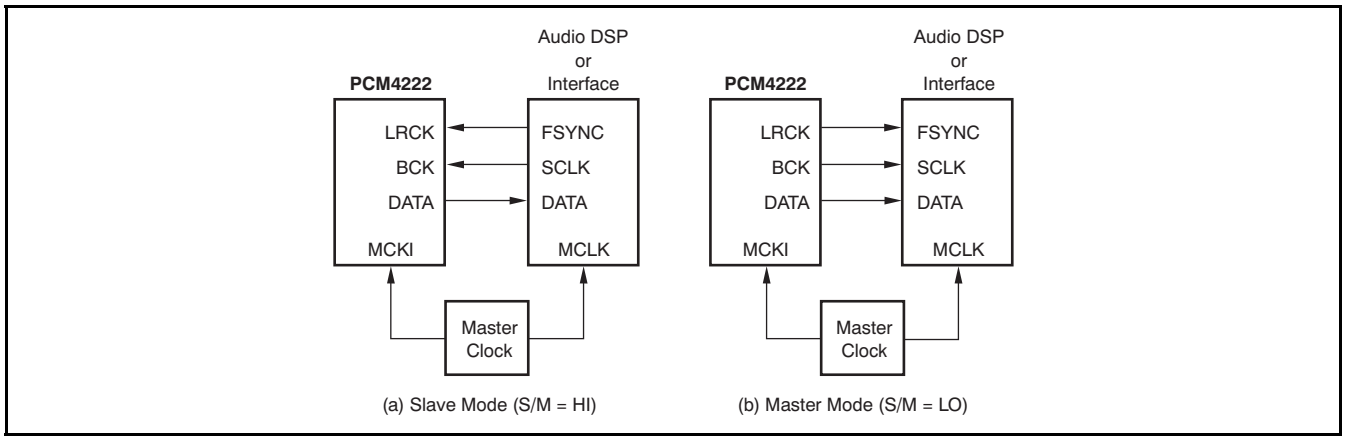


Figure 41. Slave and Master Mode Operation

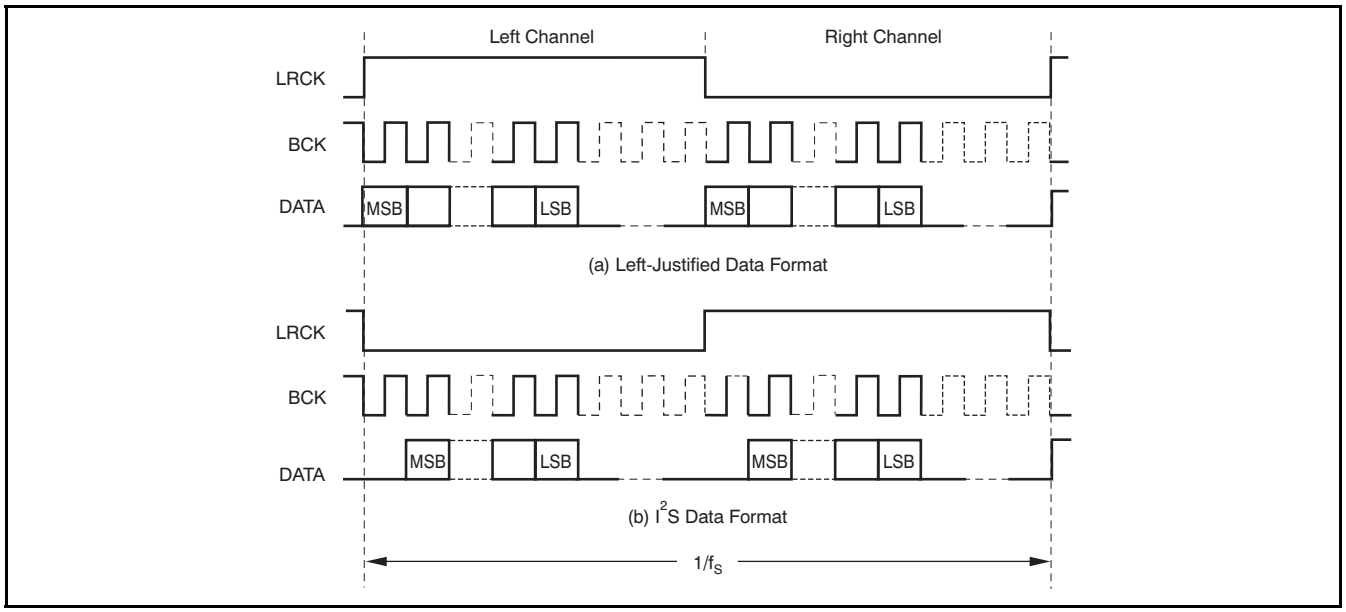


Figure 42. Left-Justified and I^2S Data Formats

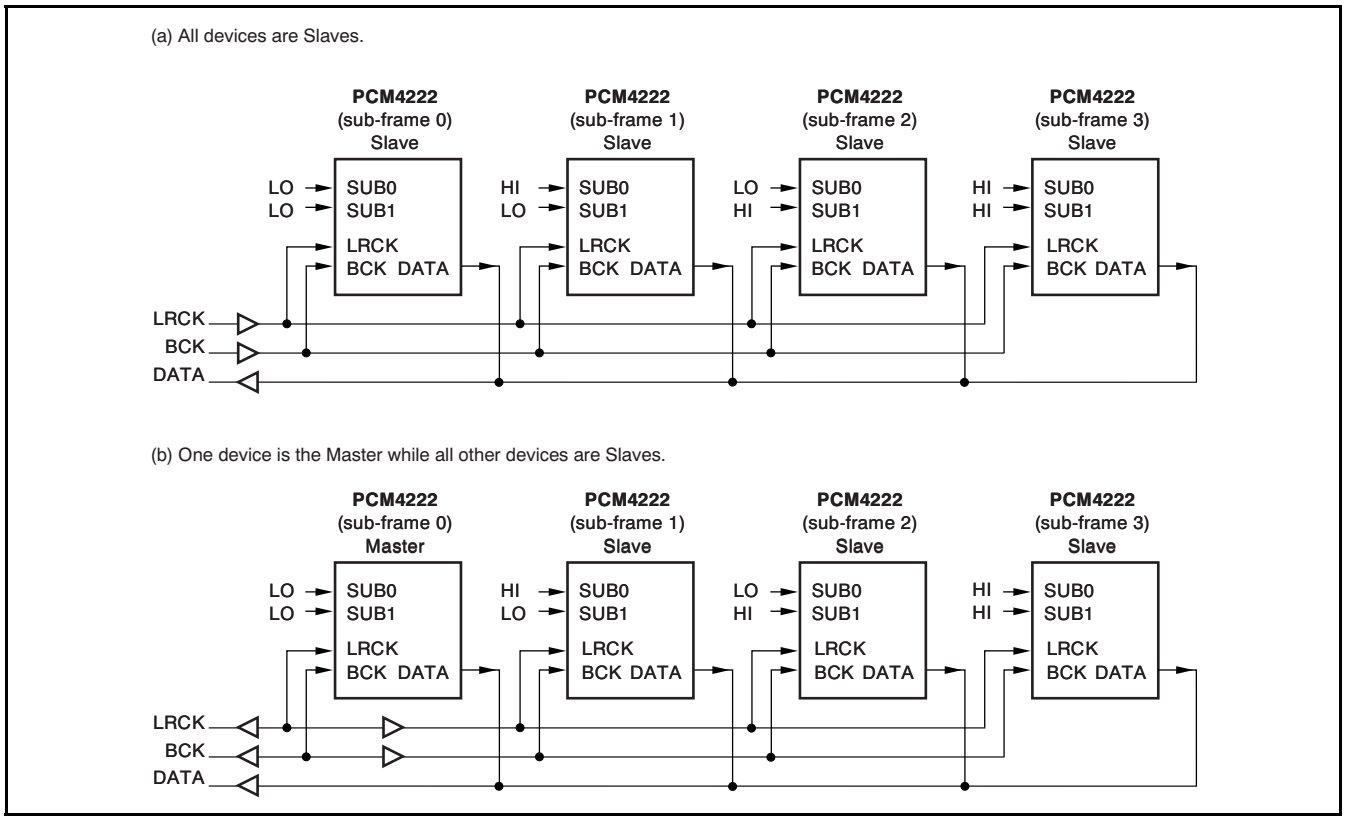
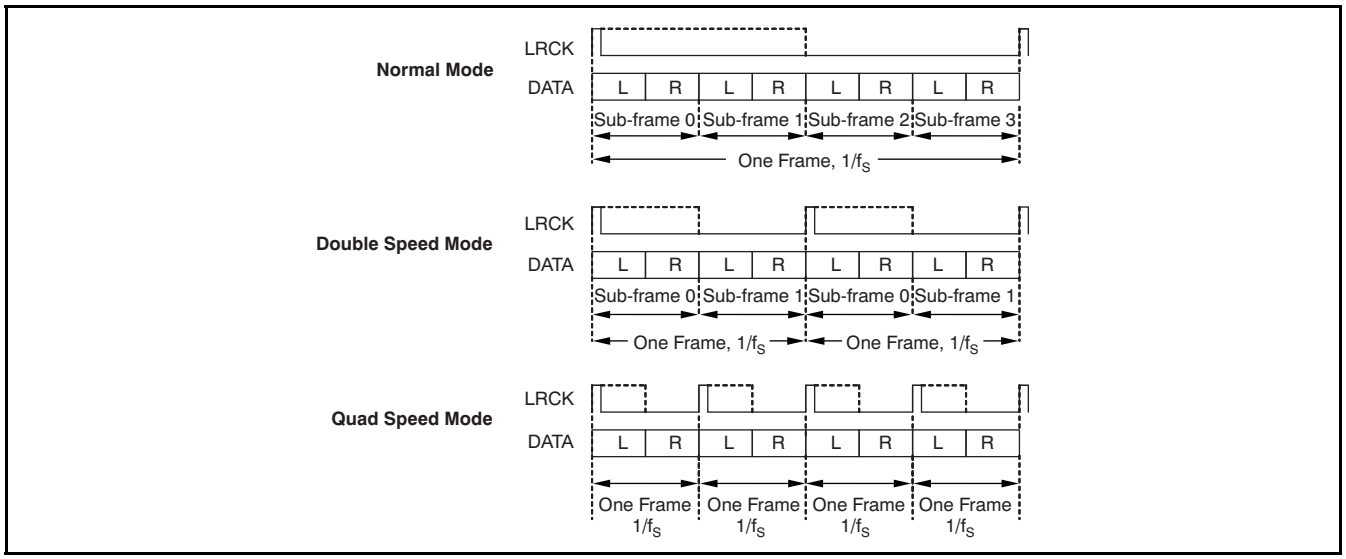
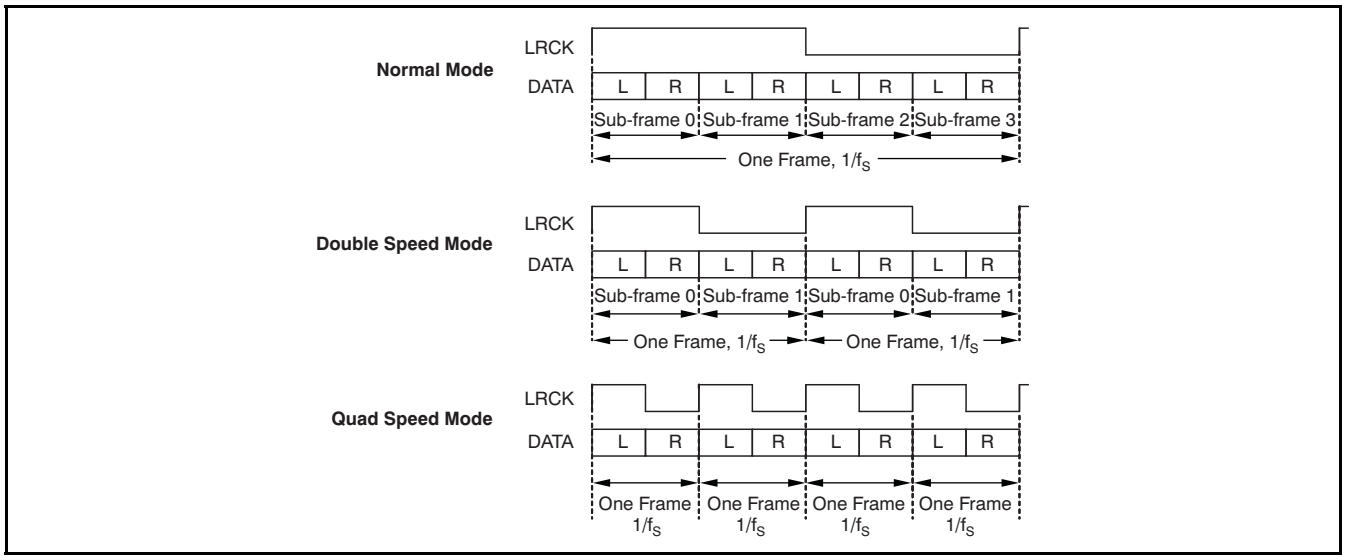


Figure 43. TDM Mode Interface Connections (PCM Normal Mode Shown)



Each L or R channel time slot is 32-bits long, with 24-bit data Left-Justified in the time slot. Audio data is MSB first. Sub-frame assignments for each PCM4222 device are selected by the corresponding SUB0 and SUB1 pin settings.

Figure 44. TDM Data Formats: Slave Mode



Each L or R channel time slot is 32-bits long, with 24-bit data Left-Justified in the time slot. Audio data is MSB first. Sub-frame assignments for each PCM4222 device are selected by the corresponding SUB0 and SUB1 pin settings.

Figure 45. TDM Data Formats: Master Mode

DIGITAL DECIMATION FILTER

The PCM4222 digital decimation filter is a linear phase, multistage finite impulse response (FIR) design with two user-selectable filter responses. The decimation filter provides the digital downsampling and low-pass anti-alias filter functions for the PCM4222.

The Classic filter response is typical of traditional audio data converters, with Figure 26 through Figure 29 detailing the frequency response, and the related specifications given in the Electrical Characteristics table. The group delay for the Classic filter is $39/f_S$, or 812.5µs for f_S = 48kHz and 406.25µs for f_S = 96kHz. The Classic filter response is not available for the Quad Speed sampling mode.

The Low Group Delay response provides a lower latency option for the decimation filter, and is detailed in Figure 30 through Figure 33, with the relevant specifications given in the Electrical Characteristics table. The Low Group Delay filter response is available for all sampling modes. The group delay for this filter is $21/f_S$, or 437.5µs for f_S = 48kHz, 218.75µs for f_S = 96kHz, and 109.375µs for f_S = 192kHz.

The decimation filter response is selected using the DF input (pin 21), with the settings summarized in Table 5. For Quad Speed sampling mode operation, the Low Group Delay filter is always selected, regardless of the DF pin setting.

Table 5. Decimation Filter Response Selection

DF (pin 21)	DECIMATION FILTER RESPONSE
LO	Classic response, with group delay = $39/f_S$
HI	Low Group Delay response, with group delay = $21/f_S$

DIGITAL HIGH-PASS FILTER

The PCM4222 incorporates digital high-pass filters for both the left and right audio channels, with the purpose of removing the ΔΣ modulator dc offset from the audio output data. Figure 34 and Figure 35 detail the frequency response for the digital high-pass filter. The f_{-3dB} frequency is approximately $f_S/48000$, where f_S is the PCM output sampling rate.

Two inputs, HPFDR (pin 17) and HPFDL (pin 18), allow the digital high-pass filter to be enabled or disabled individually for the right and left channels, respectively. Table 6 summarizes the operation of the high-pass filter disable pins.

Table 6. Digital High-Pass Filter Configuration

HPFDR (pin 17) or HPFDL (pin 18)	HIGH-PASS FILTER STATE
LO	Enabled for the corresponding channel
HI	Disabled for the corresponding channel

PCM OUTPUT WORD LENGTH REDUCTION

The PCM4222 is typically configured to output 24-bit linear PCM audio data. However, internal word length reduction circuitry may be utilized to reduce the 24-bit data to 20-, 18-, or 16-bit data. This reduction is accomplished by using a Triangular PDF dithering function. The OWL0 (pin 42) and OWL1 (pin 41) inputs are utilized to select the output data word length. Table 7 summarizes the output word length configuration options.

Table 7. PCM Audio Data Word Length Selection

OWL1 (pin 41)	OWL0 (pin 42)	OUTPUT WORD LENGTH
LO	LO	24 bits
LO	HI	18 bits
HI	LO	20 bits
HI	HI	16 bits

OVERFLOW INDICATORS

The PCM4222 includes two active-high digital overflow outputs, OVFL (pin 37) and OVFR (pin 38), corresponding to the left and right channels, respectively. These outputs are functional when the PCM output mode is enabled, as the overflow detection circuitry is incorporated into the digital filter engine. The overflow indicators are forced high whenever a digital overflow is detected for a given channel. The overflow indicators may be utilized as clipping flags, and monitored using a host processor or light-emitting diode (LED) indicators. When driving a LED, the overflow output may be buffered to ensure adequate drive for the LED. A recommended buffer is Texas Instruments' SN74LVC1G125. Equivalent buffers may be substituted

DIRECT STREAM DIGITAL (DSD) OUTPUT OPERATION

The PCM4222 supports 1-bit, direct stream digital (DSD) output data. The DSD data stream is utilized as the format for super audio CD (SACD) data. An on-chip DSD engine converts the multi-bit delta-sigma modulator output data to 1-bit DSD output data. Figure 46 shows a simplified functional block diagram for this process. The PCM4222 allows for the simultaneous output of both PCM and DSD output data, enabling both data types to be captured for recording and editing purposes.

The DSD engine operates in a Master mode configuration, with one data clock output and two data outputs, corresponding to the left and right channels, respectively. The DSDCLK output (pin 27) functions as the DSD data or bit clock and operates at the output data rate, which is typically set to either 64x or 128x the base rate of 44.1kHz. This configuration results in an output data rate of either 2.8224MHz or 5.6448MHz. The 2.8224MHz is the standard playback rate for SACD, while the 128x rate may be desirable for recording or processing purposes. The DSDL (pin 28) and DSDR (pin 29) outputs are utilized for the left and right channel data, respectively.

The DSD output mode is enabled using the DSDEN input (pin 22). Table 8 summarizes the function of this pin. The DSD output rate is selected using the DSDMODE input (pin 24). Table 9 summarizes the operation of this pin.

Table 8. DSD Output Configuration

DSDEN (pin 22)	DSD OUTPUT MODE
LO	DSD Output Mode is disabled with clock and data outputs forced low
HI	DSD Output Mode is enabled

Table 9. DSD Output Rate Selection

DSDMODE (pin 24)	DSD OUTPUT RATE
LO	64x Oversampled Data
HI	128x Oversampled Data

When driving capacitive loads greater than 30pF with the DSD data and clock outputs, it is recommended that external buffers be utilized to ensure data and clock integrity at the receiving device(s).

Details regarding dynamic performance for the DSD output are shown in the Electrical Characteristics table of this datasheet. Figure 3 and the Electrical Characteristics: Audio Interface Timing table detail the timing parameters for the DSD output.

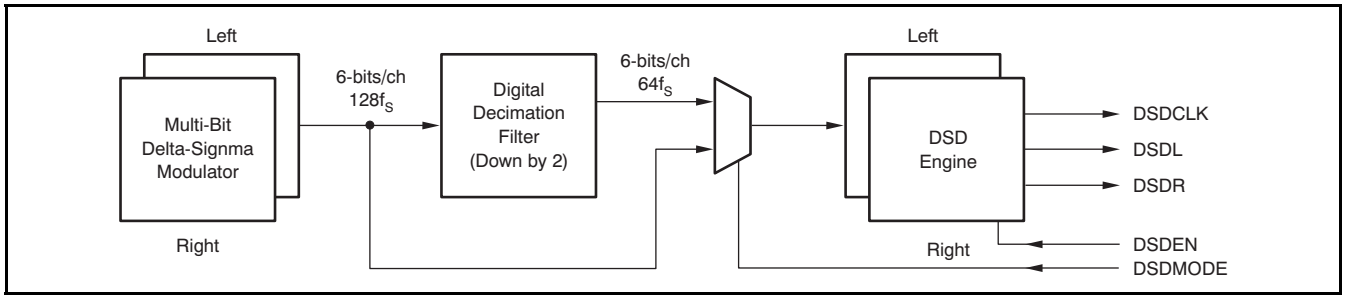


Figure 46. Simplified Block Diagram for DSD Mode Operation

MULTI-BIT MODULATOR (MBM) OUTPUT OPERATION

The PCM4222 supports direct data output from the multi-bit delta sigma modulators. This mode allows the use of external, user-defined digital filtering and/or processing. Figure 47 illustrates the functional concept for the multi-bit modulator (or MBM) output mode, as well as the output data format.

The MBM output mode is enabled or disabled using the MODEN input (pin 23). Table 10 summarizes the operation of the MODEN pin. When MBM mode is enabled, both the PCM and DSD output modes are disabled, and multiple pins are re-mapped. Table 11 summarizes the pin mapping for MBM mode, compared to the PCM and DSD output modes. The PCMEN input (pin 16) must be forced high when the multi-bit output is enabled; forcing this input high enables both the left and right channel multi-bit output data.

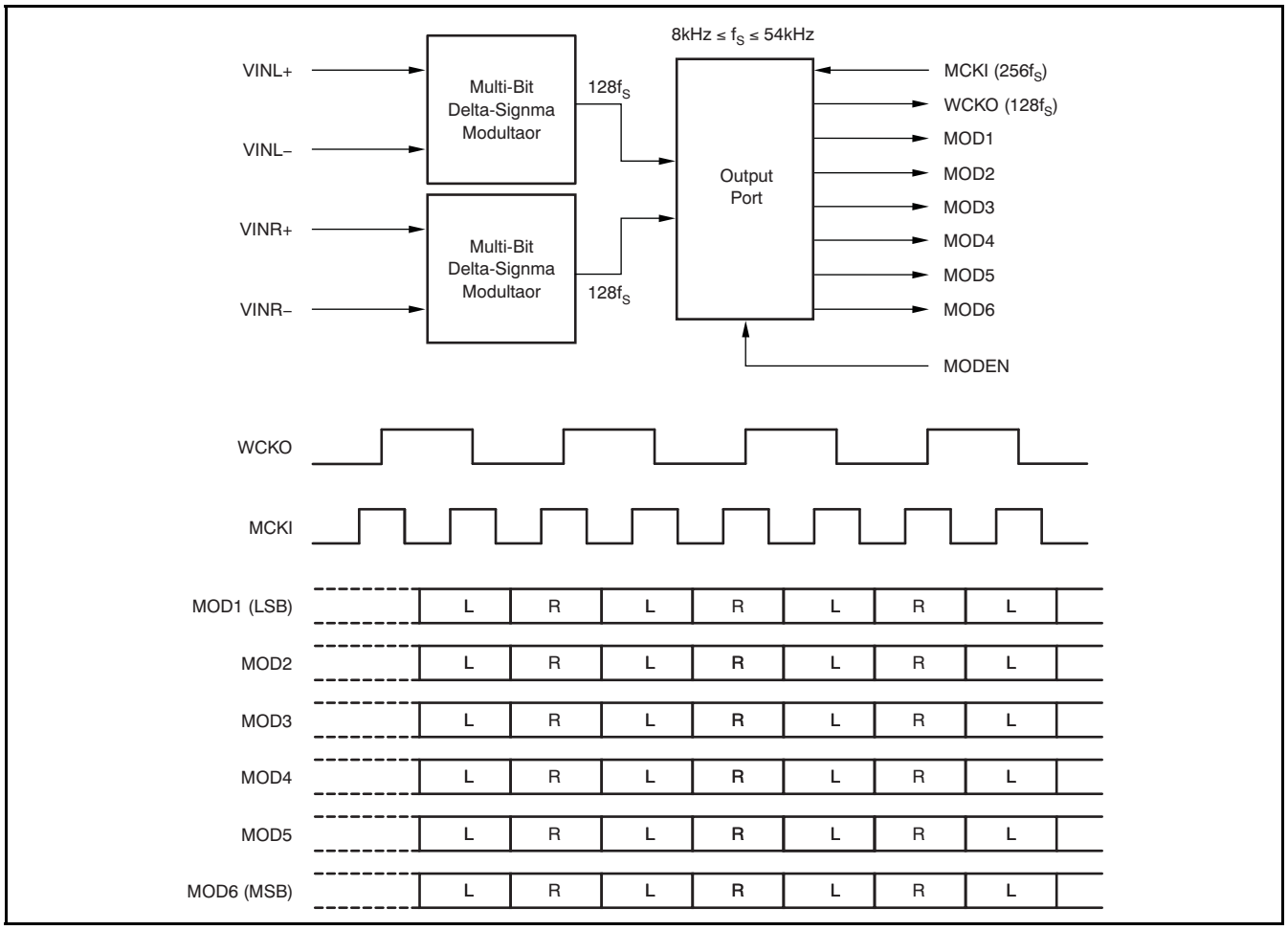


Figure 47. Multi-Bit Modulator (MBM) Output Function and Interface Format

Table 10. Multi-bit Modulator (MBM) Mode Configuration

MODEN (pin 23)	MULTI-BIT MODULATOR OUTPUT
LO	MBM Mode Disabled. Pins 17–22, 25, and 26 are mapped for PCM and DSD mode operation
HI	MBM Mode Enabled. Pins 17–22, 25, and 26 are mapped for MBM operation. PCM and DSD modes are disabled.

When driving capacitive loads greater than 30pF with the MBM data and clock outputs, it is recommended that external buffers be utilized to ensure data and clock integrity at the receiving device(s).

Refer to the Electrical Characteristics: Audio Interface Timing table and Figure 4 for parameters and timing information related to MBM operation.

Table 11. MBM Mode Pin Mapping vs PCM and DSD Modes

PIN NUMBER	MBM MODE FUNCTION	PCM AND DSD MODE FUNCTION
17	MOD1 data output (LSB)	HPFDR
18	MOD2 data output	HPFDL
19	MOD3 data output	FS0
20	MOD4 data output	FS1
21	MOD5 data output	DF
22	MOD6 data output	DSDEN
25	MCKO master clock output ($f_{MCKO} = f_{MCKI}$)	SUB1
26	WCKO word clock output ($f_{WCKO} = f_{MCKO} \div 2$)	SUB0

TYPICAL CONNECTIONS

Figure 48 and Figure 49 provide typical connection diagrams for the PCM4222. Figure 48 illustrates an application where both PCM and DSD outputs are available. Figure 49 illustrates connections for a typical application using the Multi-Bit Modulator output mode. Both figures show recommended power-supply bypass and reference filter capacitors. These components should be located as close to the corresponding PCM4222 package pins as physically possible. Larger power-supply bypass capacitors may be placed on the bottom side of the printed circuit board (PCB). However, reference decoupling capacitors should be located on the top side of the PCB to avoid issues with added via inductance.

As Figure 48 illustrates, the audio host device may be a digital signal processor (DSP), digital audio interface transmitter (DIT), or a programmable logic device. DSD data capture may be accomplished using a programmable logic device or an audio host capable of capturing/processing the 1-bit data.

In Figure 49, the modulator output may be connected to a programmable logic device that is configured to perform digital decimation filtering and post-processing tasks.

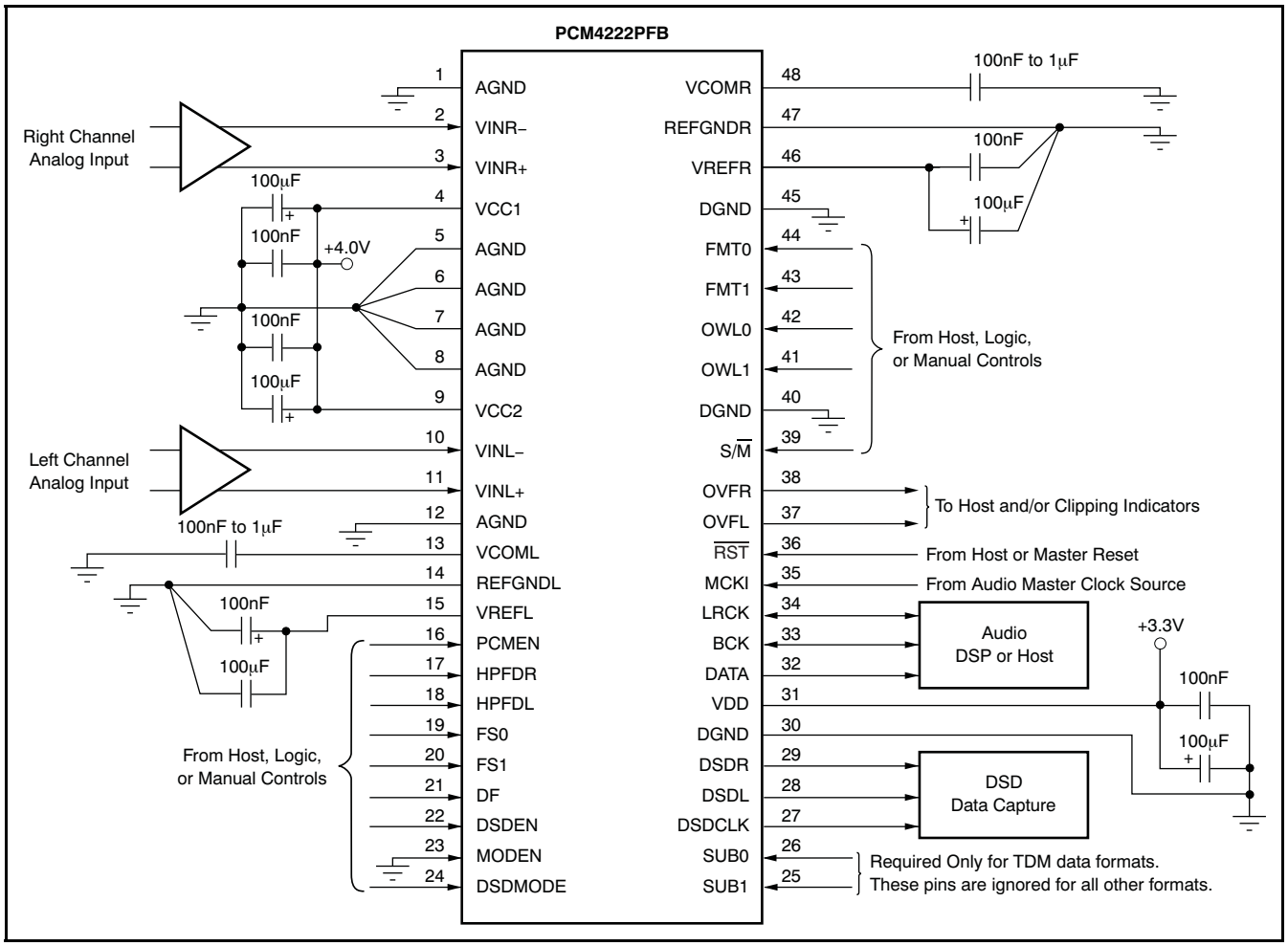


Figure 48. Typical Connections for PCM and DSD Output Modes

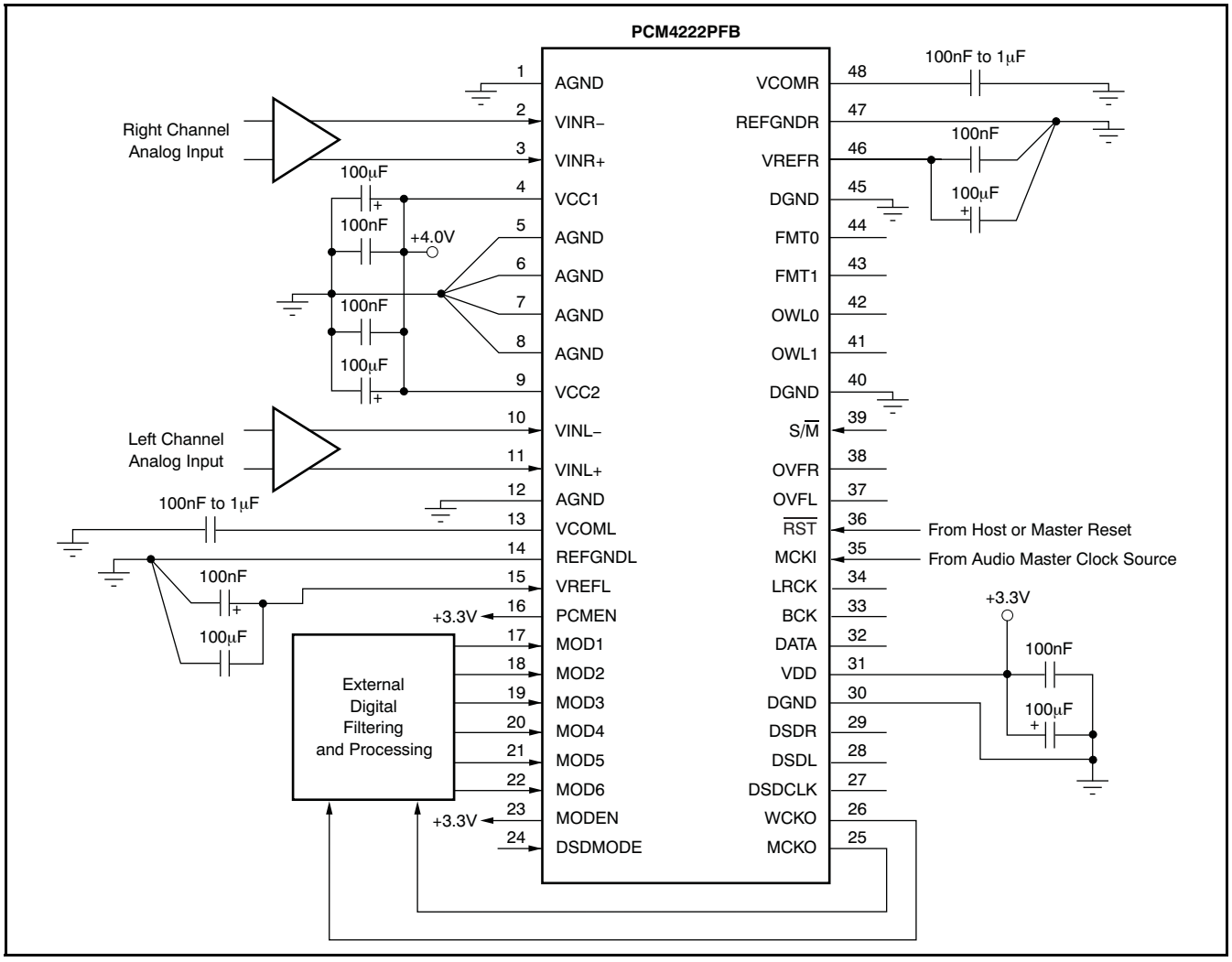


Figure 49. Typical Connections for MBM Output Mode

INPUT BUFFER CIRCUITS

The PCM4222 is typically preceded in an application by an input buffer or preamplifier circuit. The input circuit is required to perform anti-aliasing filtering, in addition to application-specific analog gain scaling, limiting, or processing that may be needed. At a minimum, first-order, low-pass anti-aliasing filtering is necessary. The input buffer must be able to perform the input filtering requirement, in addition to driving the switched-capacitor inputs of the PCM4222 device. The buffer must have adequate bandwidth, slew rate, settling time, and output drive capability to perform these tasks.

Figure 50 illustrates the input buffer/filter circuit utilized on the PCM4222EVM evaluation module. This circuit has been optimized for measurement purposes, so that it does not degrade the dynamic characteristics of the PCM4222. The resistors are primarily 0.1% metal film. The 40.2Ω resistor is 1% tolerance thick film. The 1nF and 2.7nF capacitors may be either PPS film or C0G ceramic capacitors; both types perform with equivalent results in this application. Surface-mount devices are utilized throughout because they provide superior performance when combined with a wideband amplifier such as the OPA1632. The DGN package version of the OPA1632 is utilized; this package includes a thermal pad on the bottom side. The thermal pad must be soldered to the PCB ground plane for heat sink and mechanical support purposes.

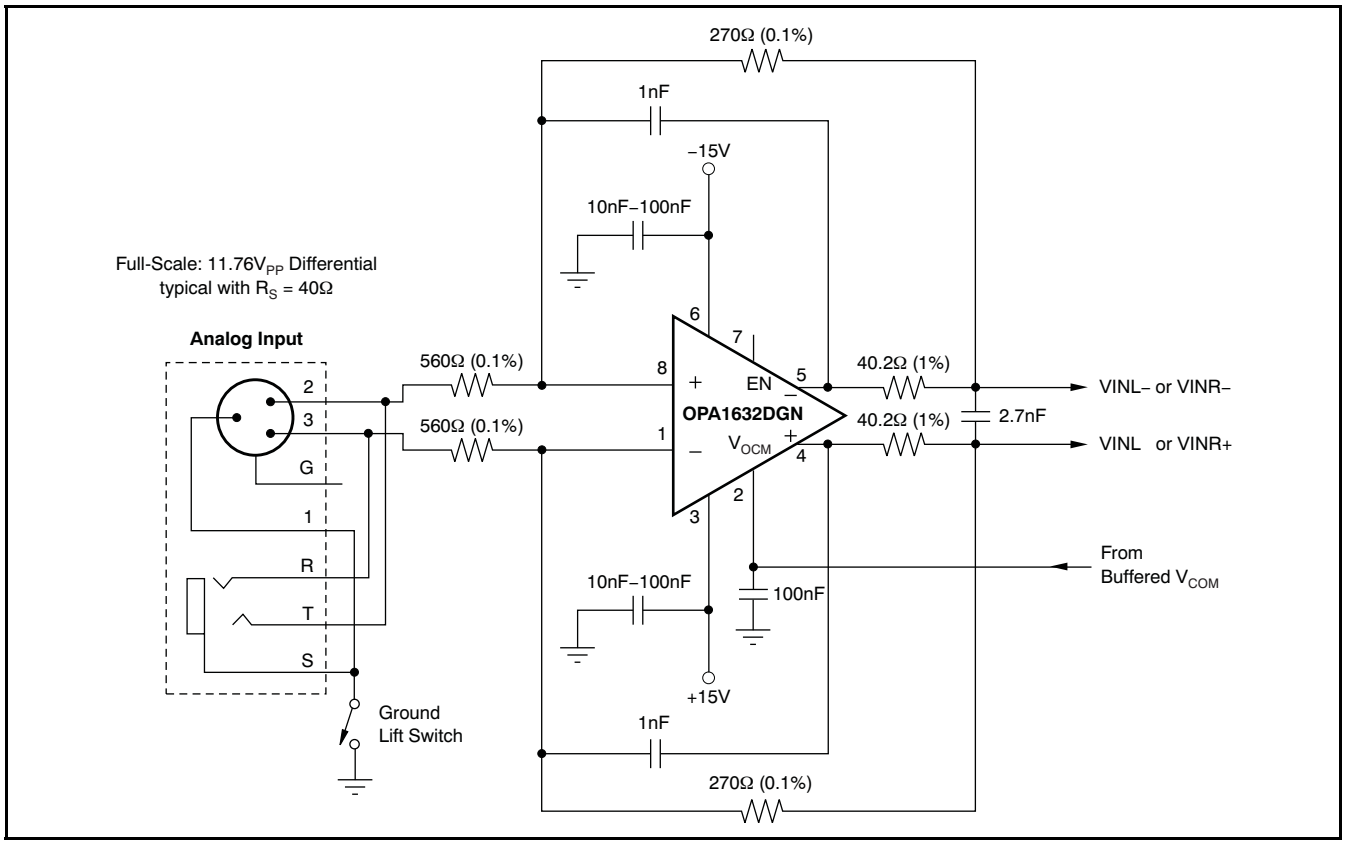
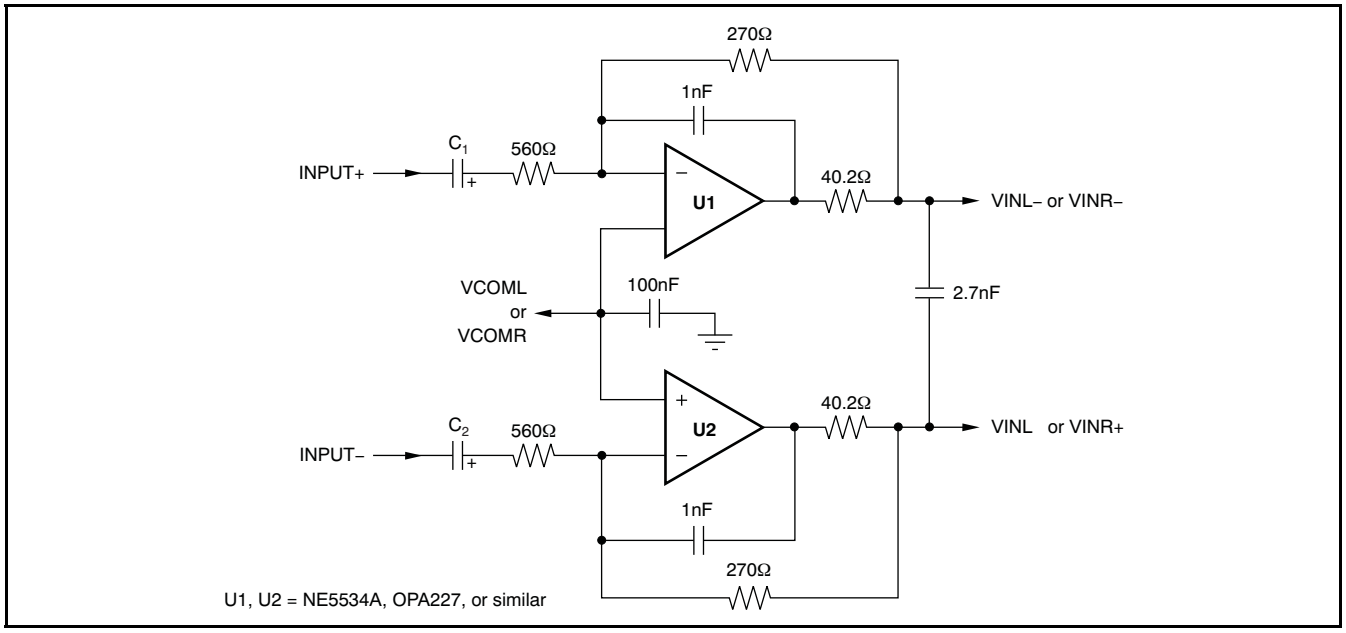


Figure 50. Differential Input Buffer Circuit Utilizing the OPA1632

Figure 51 demonstrates the same circuit topology of Figure 50, while using standard single or dual op amps. The noise level of this circuit is adequate for obtaining the typical A-weighted dynamic range performance for the PCM4222. However, unweighted performance may suffer, depending upon the op amp noise specifications. Near-typical THD+N can be achieved with this configuration, although this performance also depends on the op amps used for the application. The NE5534A and OPA227 (the lower cost 'A' version) are good candidates from a noise and distortion perspective, and are reasonably priced. More expensive lower-noise models, such as the OPA211, should also work well for this configuration. Feedback and input resistor values may be changed to alter circuit gain. However, it is recommmended that all circuit changes be simulated and then tested on the bench using a working prototype to verify performance.

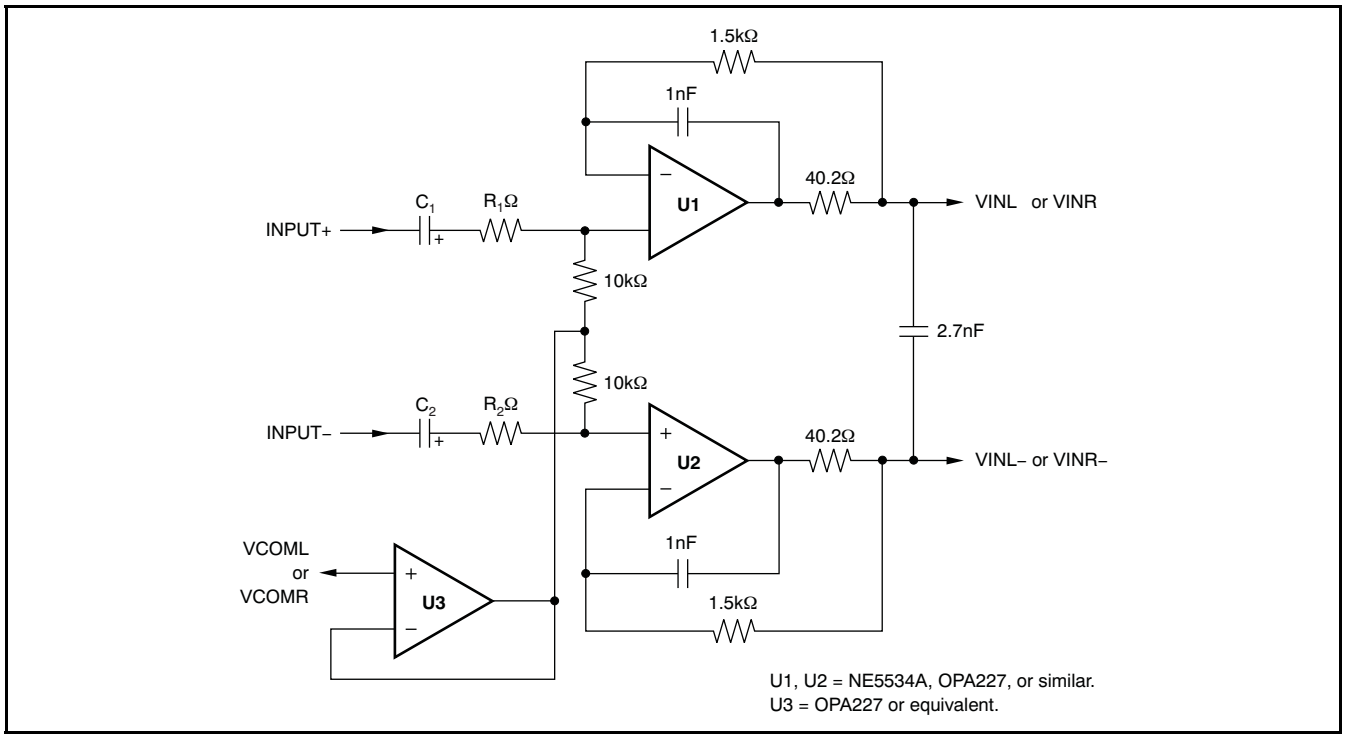
Figure 52 illustrates a differential input circuit that employs a noninverting architecture. The total noise and distortion is expected to be higher than that measured for Figure 50 and Figure 51. As with Figure 51, the NE5534A and OPA227 are good candidates for this circuit, although similar op amps should yield equivalent results.

A useful tool for simulating the circuits shown here is TINA-TI, a free schematic capture and SPICE-based simulator program available from the Texas Instruments web site. This tool includes macro models for many TI and Burr-Brown branded amplifiers and analog integrated circuits. TINA-TI runs on personal computers using Microsoft Windows® operating systems.



C_1 and C_2 provide ac coupling. They may be removed if the dc offset from the preceeding circuit is negligible.

Figure 51. Alternative Buffer Circuit Using Standard Op Amps



R_1 and R_2 are optional. When used, values may be selected for the desired attenuation.

C_1 and C_2 provide ac coupling. They may be removed if the dc offset from the preceeding circuit is negligible.

Figure 52. Noninverting Differential Input Buffer Utilizing Standard Op Amps

IINTERFACING TO DIGITAL AUDIO TRANSMITTERS (AES3, IEC60958-3, and S/PDIF)

The serial output of audio analog-to-digital converters are often times interfaced to transmitter devices that encode the serial output data to either the AES3 or IEC60958-3 (or S/PDIF) interface formats. Texas Instruments manufactures several devices that perform this encoding, including the DIT4192, DIX4192, SRC4382, and SRC4392. This section describes and illustrates the audio serial port interface connections required for communications between the PCM4222 and these devices. Register programming details for the DIX4192 and SRC4382/4392 are also provided.

Figure 53 shows the interface between a PCM4222 and a DIT4192 transmitter. This configuration supports sampling frequencies and encoded frame rates from 8kHz to 216kHz. For this example, the audio data format must be either Left-Justified or I^2S; TDM formats are not supported by the DIT4192. In addition, the PCM4222 VDD supply and DIT4192 VIO supply must be the same voltage, to ensure logic level compatibility.

Figure 54 illustrates the audio serial port interface between the PCM4222 and either a DIX4192 transceiver or SRC4382/SRC4392 combo sample rate converter/transceiver device. Port A of the DIX4192 or SRC4382/SRC4392 is utilized for this example. Data acquired by Port A are sent on to the DIT function block within the interface device for AES3 encoding and transmission.

The DIX4192 and SRC4382/SRC4392 are software-configurable, with control register and data buffer settings that determine the operation of internal function blocks. Table 12 and Table 13 summarize the control register settings for the Port A and the DIT function blocks for both A/D Converter Master and Slave modes, respectively. Input sampling and encoded frame rates from 8kHz to 216kHz are supported with the appropriate register settings.

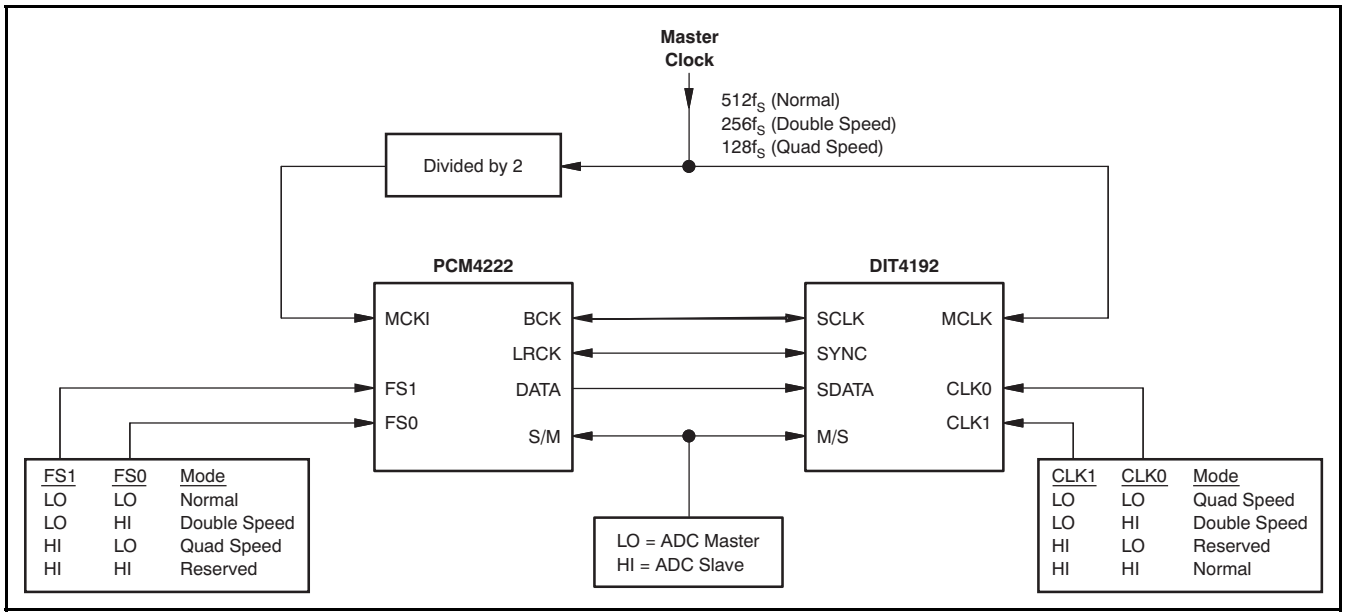
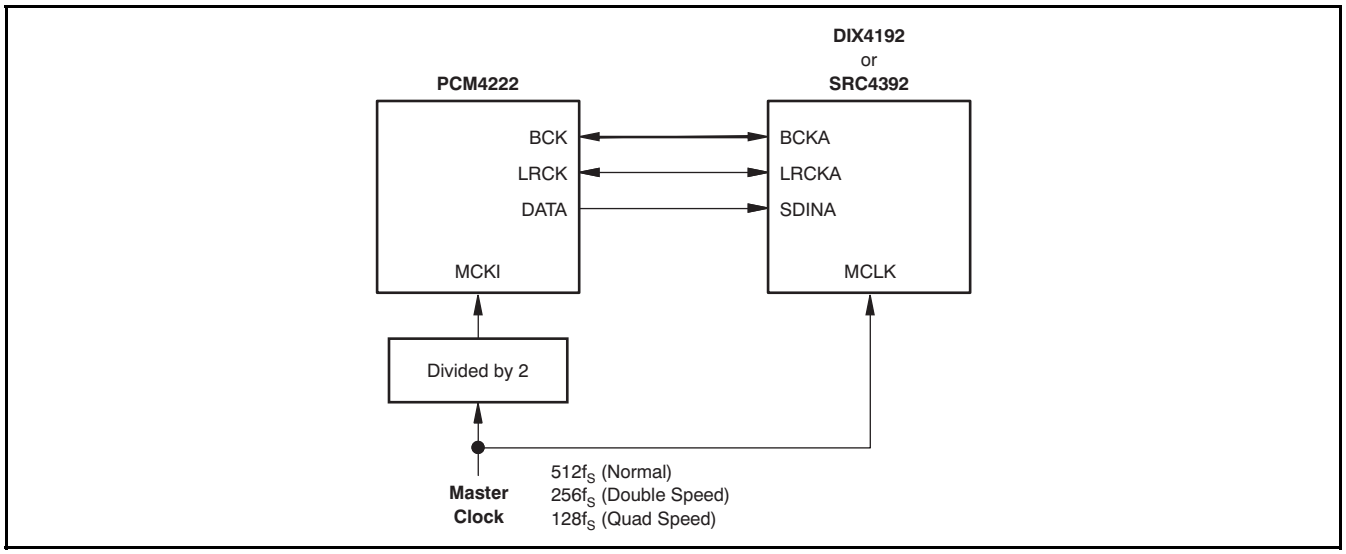


Figure 53. Interfacing the PCM4222 to a DIT4192



VDDPCM4222 = VIODIX4192 or SRC4392.

Audio data format if I^2S or Left Justified.

Interface supports ADC Slave or Master configurations, depending on DIX4192, SRC4382, or SRC4392 register setup.

Figure 54. Interfacing the PCM4222 to a DIT4192, SRC4382, or SRC4392

Table 12. Register Configuration Sequence for an ADC Master Mode Interface

REGISTER ADDRESS (hex)	REGISTER DATA (hex)	COMMENTS
7F	00	Select Register Page 0
03	00 01	Port A is Slave mode with Left-Justified audio data format, or Port A is Slave mode with I^2S Data format
04	00	Default for Port A Slave mode operation
07	64 24 04	Divide MCLK by 512 for Normal sampling,or Divide MCLK by 256 for Double Speed Sampling, or Divide MCLK by 128 for Quad Speed sampling
08	00	Line Driver and AESOUT buffer enabled
09	01	Data buffers on Register Page 2 are the source for the DIT channel status (C) and user (U) data
01	34	Power up Port A and the DIT

Table 13. Register Configuration Sequence for an ADC Slave Mode Interface

REGISTER ADDRESS (hex)	REGISTER DATA (hex)	COMMENTS
7F	00	Select Register Page 0
03	08 09	Port A is Master mode with Left-Justified audio data format, or Port A is Master mode with I^2S Data format
04	03 01 00	Divide MCLK by 512 for Normal sampling, or Divide MCLK by 256 for Double Speed sampling, or Divide MCLK by 128 for Quad Speed sampling
07	64 24 04	Divide MCLK by 512 for Normal sampling,or Divide MCLK by 256 for Double Speed Sampling, or Divide MCLK by 128 for Quad Speed sampling
08	00	Line Driver and AESOUT buffer enabled
09	01	Data buffers on Register Page 2 are the source for the DIT channel status (C) and user (U) data
01	34	Power up Port A and the DIT

The DIT channel status (C) and user (U) data bits in register page 2 may be programmed after the DIT block has powered up. To program these bits, disable buffer transfers by setting the BTD bit in control register 0x08 to '1'. Then, select register page 2 using register address 0x7F. You can now load the necessary C and U data registers for the intended application by writing the corresponding data buffer addresses. When you have finished writing the C and U data, select register page 0 using register address 0x7F. Re-enable buffer transfers by setting the BTD bit in control register 0x08 to '0'.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
PCM4222PFB	PREVIEW	TQFP	PFB	48	250	TBD	Call TI	Call TI
PCM4222PFBR	PREVIEW	TQFP	PFB	48	1000	TBD	Call TI	Call TI

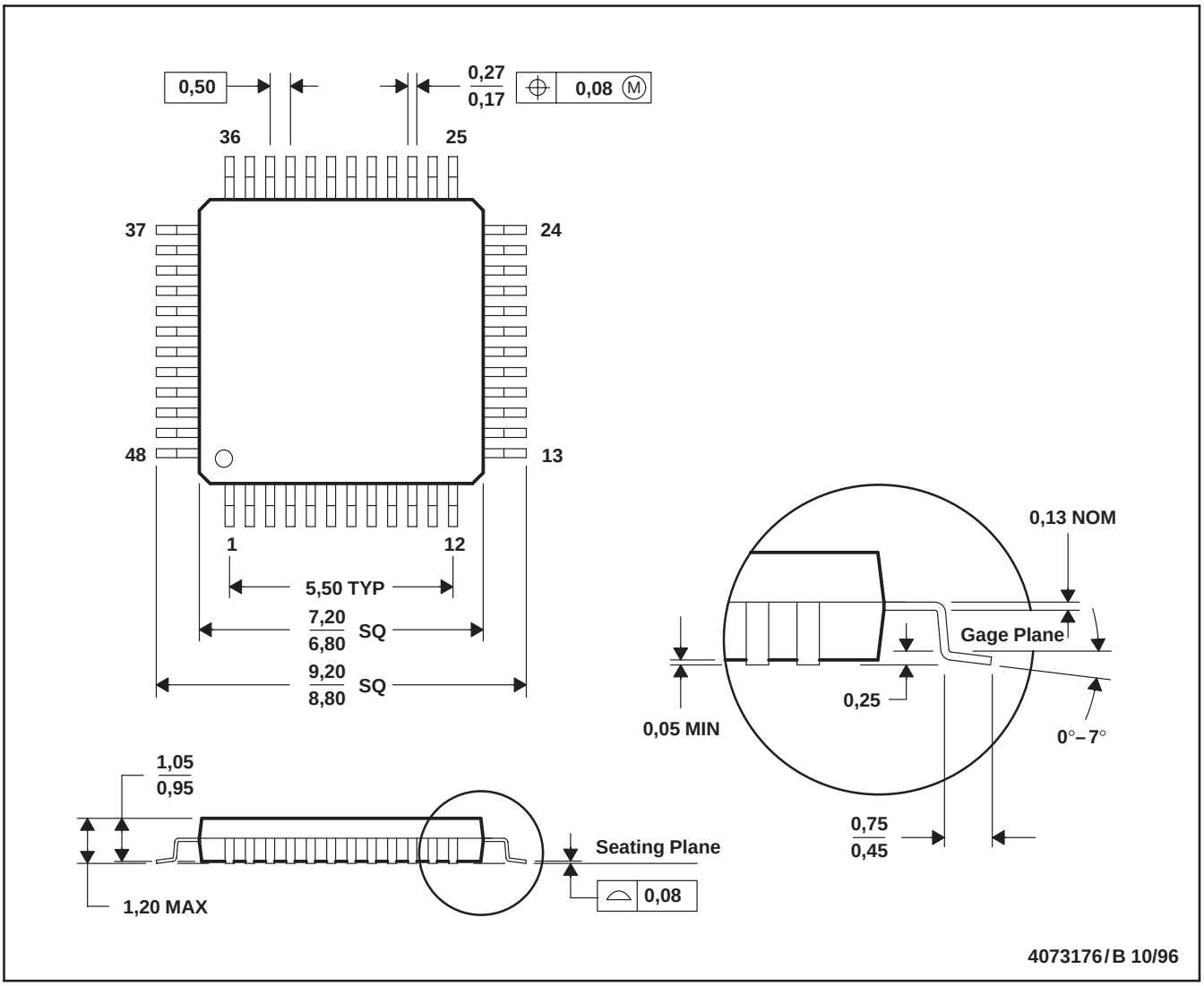
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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