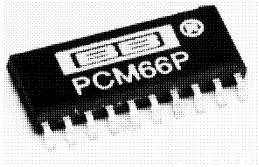
BURR - BROWN®

PCM66P



16-Bit CMOS Monolithic Audio DIGITAL-TO-ANALOG CONVERTER

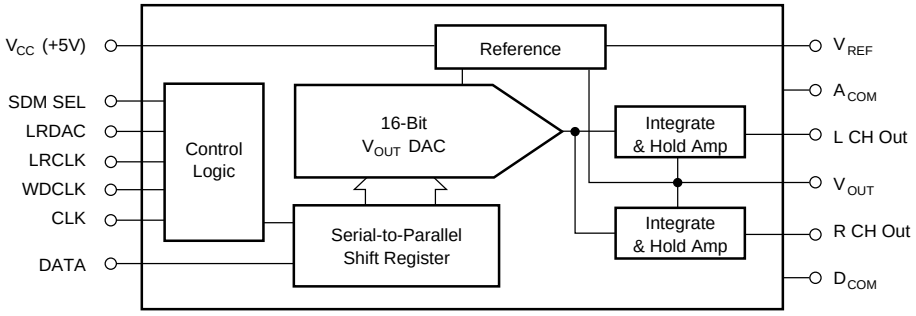
FEATURES

- LOW COST 16-BIT 2-CHANNEL CMOS MONOLITHIC D/A CONVERTER
- SINGLE SUPPLY +5V OPERATION
- 50mW POWER DISSIPATION
- GLITCH-FREE VOLTAGE OUTPUTS
- LOW DISTORTION: –86dB max THD + N
- COMPLETE WITH REFERENCE
- SERIAL INPUT FORMAT
- SINGLE OR DUAL DAC MODE OPERATION
- PLASTIC 20-PIN SOIC PACKAGE

DESCRIPTION

The PCM66P is a low cost, dual output 16-bit CMOS digital-to-analog converter. The PCM66P features true glitch-free voltage outputs, internal reference and requires only a single +5V supply. Total power dissipation is less than 50mW max. Low maximum Total Harmonic Distortion + Noise (–86dB max; PCM66P-J) is 100% tested. Either one or two channel output modes are fully user selectable.

The PCM66P comes in a space-saving 20-pin plastic SOIC package. PCM66P accepts a serial data input format and is compatible with other Burr-Brown PCM products such as the industry standard PCM56P.



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SPECIFICATIONS

ELECTRICAL

All specifications at 25°C, and $+V_{CC}$ = +5V unless otherwise noted.

PARAMETER	CONDITIONS	PCM66P AND PCM66P, J MIN	TYP	MAX	UNITS
RESOLUTION				16	Bits
DYNAMIC RANGE			96		dB
DIGITAL INPUT			TTL Compatible CMOS		
Logic Family					
Logic Level: V_{IH}	I_{IH} = +40µA max	+2.4		+5.25	V
V_{IL}	I_{IL} = –40µA max	0		0.8	V
Data Format			Serial BTC[1]		
Input Clock Frequency		8.5			MHz
DYNAMIC CHARACTERISTICS					
TOTAL HARMONIC DISTORTION + N[2]					
PCM60P/66P: f = 991Hz (0dB)[3]	f_S = 176.4kHz[4]		–88	–82	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–68		dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–28		dB
PCM60P-J/66P-J: f = 991Hz (0dB)	f_S = 176.4kHz		–92	–86	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–68		dB
f = 99lHz (–60db)	f_S = 176.4kHz		–28		dB
CHANNEL SEPARATION		+80	+85		dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error	V_{OUT} = 2.6		±2	±10	%
Gain Mismatch	Channel to Channel		±1		%
Bipolar Zero Error[5]			±30		mV
Gain Drift	0°C to 70°C		100		ppm/°C
Warm-up Time		1			minute
IDLE CHANNEL SNR[6]	20-20kHz with A-weighted filter		±90		dB
ANALOG OUTPUT					
Output Range			2.6		Vp-p
Output Impedance			2		Ω
Short Circuit Duration	To Be Determined				
Settling Time	Suffieicnt to Meet 176.4kHz THD + N Specs				
Glitch Energy	Meets All THD + N Specs Without External Output Deglitching				
POWER SUPPLY REQUIREMENTS					
$+V_{CC}$ Supply Voltage		+4.75	+5	+5.25	V
Supply Current			+9.5		mA
Power Dissipation	V_{CC} = +5V			50	mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–30		+70	°C
Storage		–60		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$) / $Signal_{RMS}$. (3) D/A converter output frequency/signal level (on both left and right channels). (4) D/A converter sample frequency (4 x 44.1kHz; 4 times oversampling per channel). (5) Offset error at bipolar zero. (6) Ratio of output at BPZ (Bipolar Zero) to the full scale range using 20kHz low pass filter in addition to an A-weighted filter.

PCM66P PIN ASSIGNMENTS

PIN	DESCRIPTION	MNEMONIC
1	Left/Right Clock	LRCLK
2	Word Clock	WDCLK
3	Clock Input	CLK
4	Data Input	DATA
5	No Connection	NC
6	Digital Common	D_{COM}
7	Analog Common	A_{COM}
8	Left Channel V_{OUT}	L CH Out
9	Output Common	V_{COM}
10	Right Channel V_{OUT}	R CH Out
11	Analog Supply	$+V_{CC}$
12	Analog Supply	$+V_{CC}$
13	Reference Decouple	C_{REF}
14	Reference Sense	V_{REF} SENSE
15	Reference Output	V_{REF}
16	Analog Supply	$+V_{CC}$
17	Analog Supply	$+V_{CC}$
18	Digital Supply	$+V_{CC}$
19	Single DAC Mode	SDM SEL
20	Left/Right DAC Select	LRDAC

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PCM66P	20-Pin SOIC	248
PCM66P, J	20-Pin SOIC	248

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

PCM66P -X

Basic Model Number
P: Plastic
Performance Grade Code

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	±10V
Input Voltage Range	–3V to +5.25V
Power Dissipation	50mW
Operating Temperature	–30°C to +70°C
Storage Temperature	–60°C to +100°C
Lead Temperature (soldering, 10s)	+300°C

THEORY OF OPERATION

The PCM66P is a dual output, 16-bit CMOS digital-to-analog audio converter. The PCM66P, complete with internal reference, has two glitch-free voltage outputs and requires only a single +5V power supply. Output modes using either one or two channels per DAC are user selectable. The PCM66P accepts a serial data input format that is compatible with other Burr-Brown PCM products such as the industry standard PCM56P.

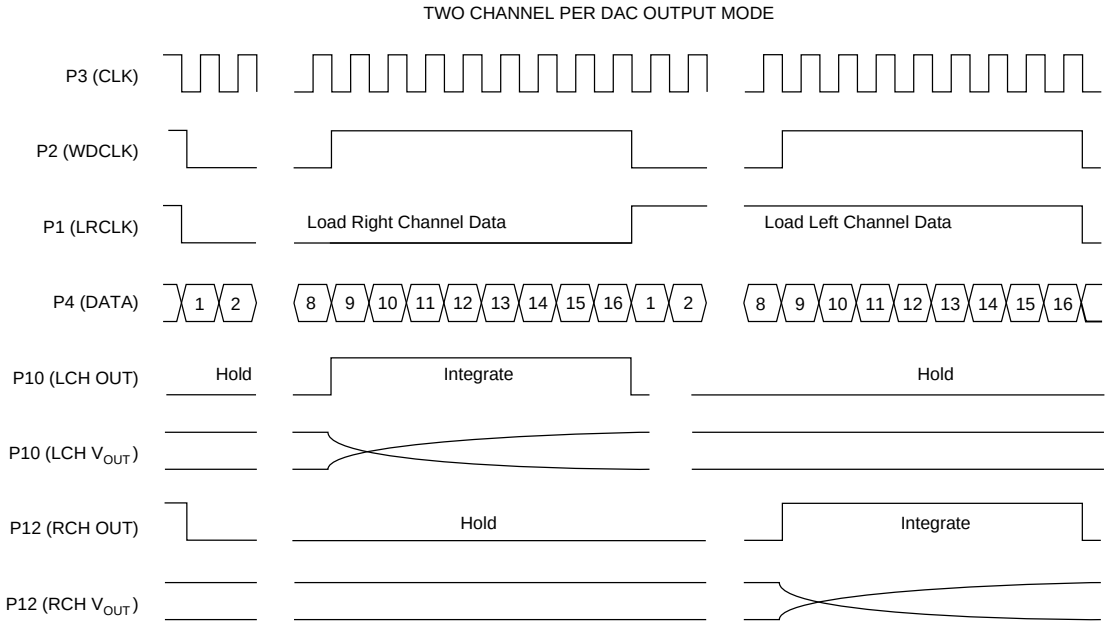
ONE DAC TWO-CHANNEL OPERATION

Normally, the PCM66P is operated with a continuous clock input in a two-channel output mode. This mode is selected when SDM SEL is held low (single DAC mode select). Refer to the truth table shown by Table I for exact control logic relationships. Data for left and right channel output is loaded alternately into the PCM66P while the control logic switches the left and right output amplifiers between the appropriate integrate and hold modes. Data word latching is controlled by WDCLK (word clock) and channel selection is made by LRCLK (left/right clock). Figure 1 shows the timing for the single DAC two-channel mode of operation. The block diagram in Figure 2 shows how a single DAC output provides switched output to both integrate and hold amplifiers. Output between left and right channels in this mode is not in phase. See Figure 3 for proper connection of the PCM66P in the two-channel DAC mode.

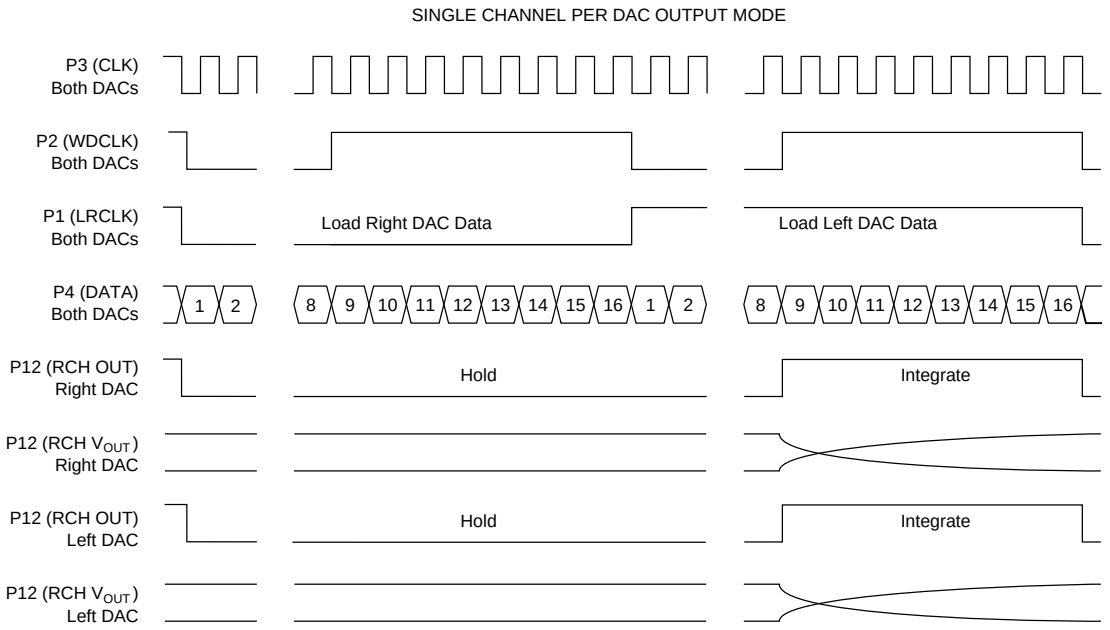
PIN FUNCTIONS				SERIAL DATA WORD INPUT	LEFT CHANNEL OUTPUT	RIGHT CHANNEL OUTPUT
SDM SEL	LRDAC	LRCLCK	WDCLK			
0	X	0	0	Right	Hold	Hold
0	X	0	1	Right	Integrate	Hold
0	X	1	0	Left	Hold	Hold
0	X	1	1	Left	Hold	Integrate
1	0	0	0	Inhibited	V_{COM}	Hold
1	0	0	1	Inhibited	V_{COM}	Hold
1	0	1	0	Left	V_{COM}	Integrate
1	0	1	1	Left	V_{COM}	Integrate
1	1	0	0	Right	V_{COM}	Hold
1	1	0	1	Right	V_{COM}	Hold
1	1	1	0	Inhibited	V_{COM}	Integrate
1	1	1	1	Inhibited	V_{COM}	Integrate

NOTE: Positive edge of CLK (P3) latches LRCLK (P1), WDCLK (P2), and DATA (P4).

TABLE I. PCM66P Logic Truth Table.



NOTES: Single DAC Mode Select = 0; L/R DAC Select = X; WDCLK = 50% duty cycle; Serial Data is read in MSB first with BTC coding (MSB = Bit 1).



NOTES: Single DAC Mode Select = 1; L/R DAC Select = 0 (Left DAC) or 1 (Right DAC).

FIGURE 1. PCM66P Timing Diagram.

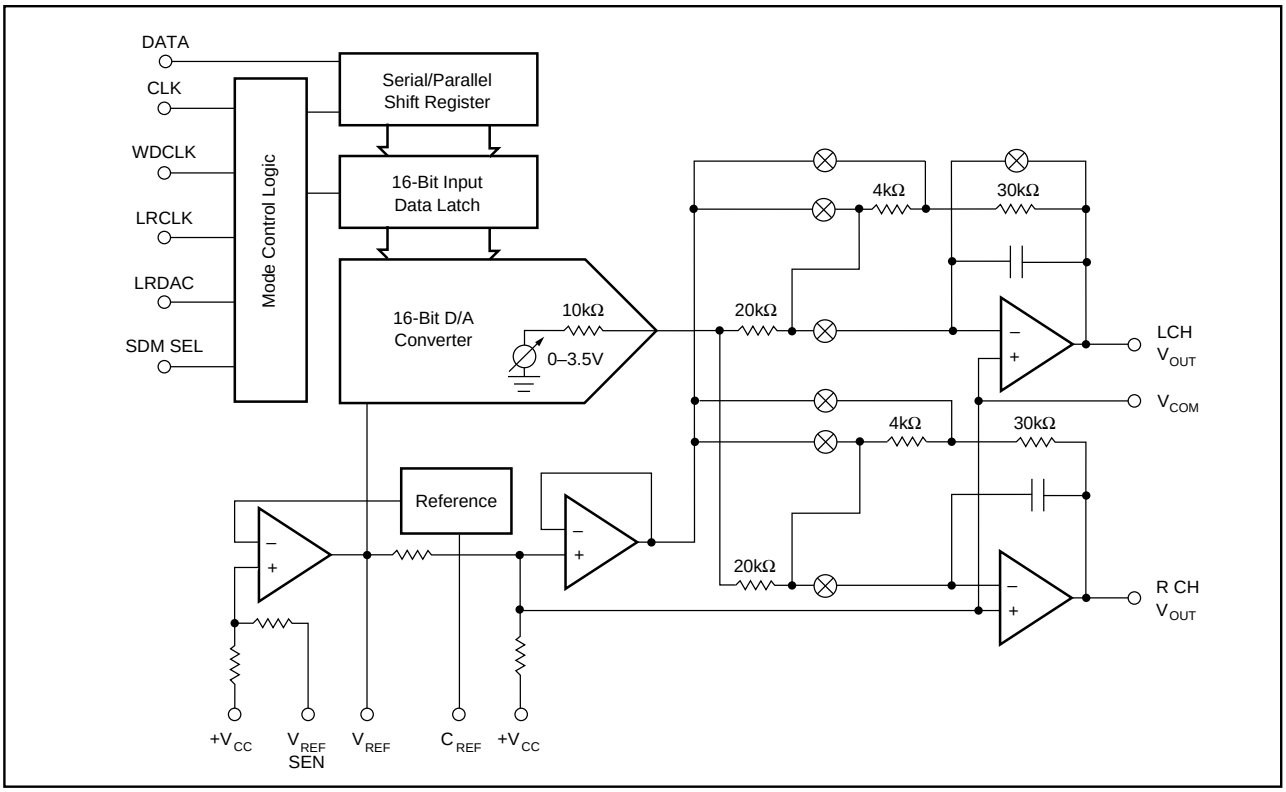


FIGURE 2. PCM66P Block Diagram.

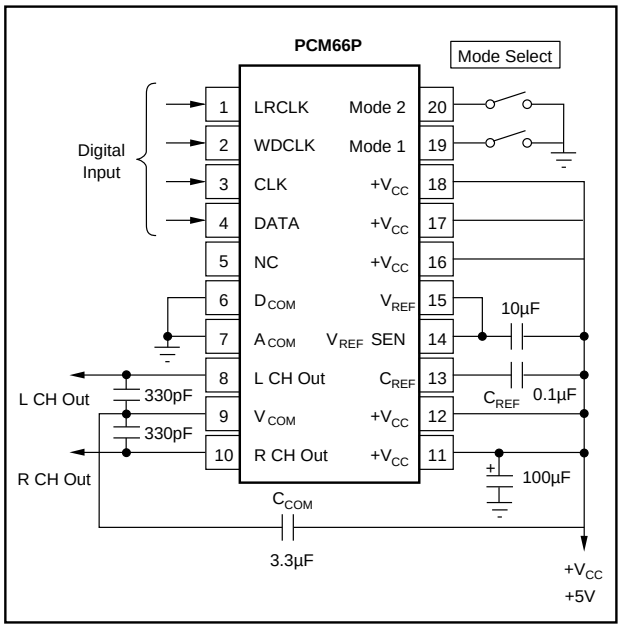


FIGURE 3. PCM66P Connection Diagram.

TWO DAC TWO-CHANNEL OPERATION

In phase, two-channel output can be obtained by using two PCM66Ps and choosing the single DAC mode (setting SDM SEL high). With the use of a high or low input level on LRDAC (P left/right DAC select), each DAC can have its right channel output dedicated to either left or right data input with no additional input signals being required to latch the appropriate data from an alternating L/R data word input stream. In the single DAC mode, the PCM66P's left channel output is disabled and held at $+V_{COM}$. In this mode both DACs share common inputs for DATA, CLK, WDCLK, and LRCLK. Otherwise circuit connection is the same as the two-channel DAC mode, with the exception of LRDAC whose level selects whether the single DAC will output dedicated left or right channel data.

INTEGRATE AND HOLD OUTPUT AMPLIFIERS

The PCM66P incorporates integrate and hold amplifiers on each output channel. This allows a single, very fast DAC to feed both amplifiers and reduce circuit complexity. It also serves to block the output glitch from the DAC to the individual channel outputs and effectively makes the PCM66P outputs "glitch-free." The PCM66P is a single +5V supply device with a voltage output swing of 2.8Vp-p. The outputs swing asymmetrically around V_{COM} ($+V_{CC}$ – 2.33V). See Table II for exact input/output relationships. Since true CMOS amplifiers are used on the PCM66P, the load resistance on the outputs should not be less than 100kΩ and the capacitive loads should not exceed 100pF. For maximum low-distortion performance, output buffer amplifiers should be considered.

DIGITAL INPUT	ANALOG OUTPUT	
Binary Two's Complement (Hex)	DAC Output (V)	Voltage (V) V_{OUT} Mode
7FFF	+FS	+3.5629443
0000	BPZ	+2.1629871
8000	–FS	+0.7630299
2E5B	V_{COM}	+2.6700000

TABLE II. PCM66P Input/Output Relationships.

DISCUSSION OF SPECIFICATIONS

TOTAL HARMONIC DISTORTION + NOISE

The key specification for the PCM66P is total harmonic distortion plus noise. Digital data words are read into the PCM66P at four times the standard audio sampling frequency of 44.1kHz or 176.4kHz for each channel, such that a sine wave output of 991Hz is realized. For production testing, the output of the DAC goes to a programmable gain amplifier to provide gain at lower signal output test levels and then through a 20kHz low pass filter before being fed into an analog type distortion analyzer. Figure 4 shows a block diagram of the production THD + N test setup.

In terms of signal measurement, THD + N is the ratio of $Distortion_{RMS} + Noise_{RMS}/Signal_{RMS}$ expressed in dB. For the PCM66P, THD + N is 100% tested at three different output levels using the test setup shown in Figure 4. It is significant to note that this circuit does not include any output deglitching circuitry. This means the PCM66P meets even its –60dB THD + N specification without use of external deglitchers.

ABSOLUTE LINEARITY

Even though absolute integral and differential linearity specs are not given for the PCM66P, the extremely low THD + N performance is typically indicative of 14-bit to 15-bit integral linearity in the DAC depending on the grade specified. The relationship between THD + N and linearity, however, is not such that an absolute linearity specification for every individual output code can be guaranteed.

IDLE CHANNEL SNR

Another appropriate spec for a digital audio converter is idle channel signal-to-noise ratio (idle channel SNR). This is the ratio of the noise on either DAC output at bipolar zero in relation to the full scale range of the DAC. The output of the DAC is band limited from 20Hz to 20kHz and an A-weighted filter is applied to make this measurement.

OFFSET, GAIN, AND TEMPERATURE DRIFT

The PCM66P is specified for other important parameters such as channel separation and gain mismatch between output channels. And although the PCM66P is primarily meant for use in dynamic applications, typical specs are also given for more traditional DC parameters such as gain error, bipolar zero offset error, and temperature gain drift.

TIMING CONSIDERATIONS

The data format of the PCM66P is binary two's complement (BTC) with the most significant bit (MSB) being first in the serial input bit stream. Table II describes the exact input data to voltage output coding relationship. Any number of bits can precede the 16 bits to be loaded, as only the last 16 will be transferred to the parallel DAC register on the first positive edge of CLK (clock input) after WDCLK (word clock) has gone low. All inputs to the PCM66P are TTL level compatible.

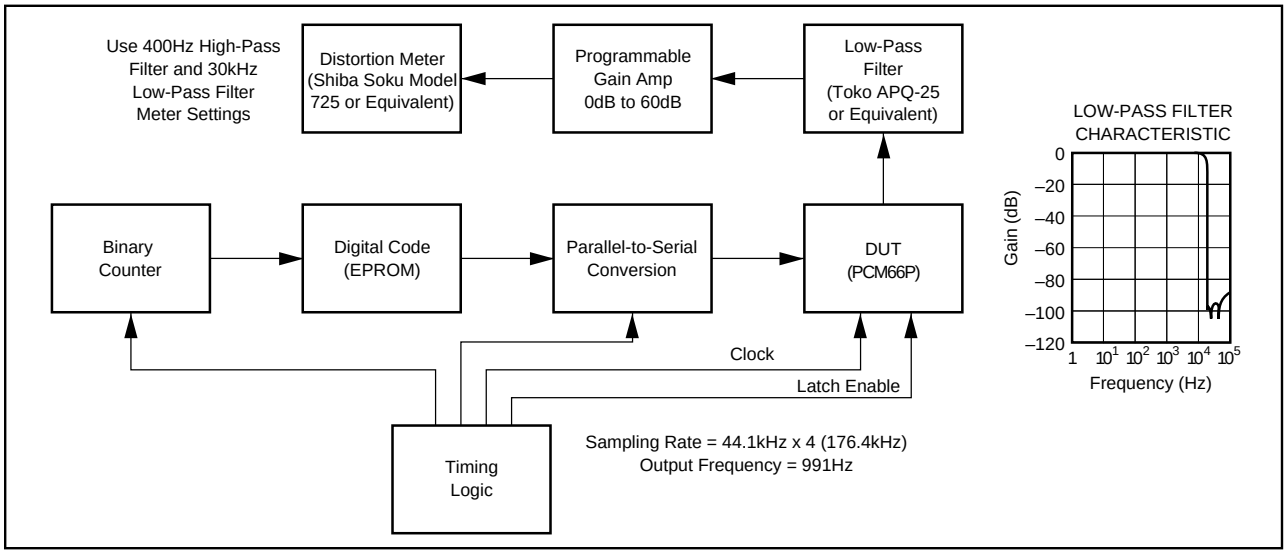


FIGURE 4. THD + N Test Setup Diagram.

WDCLK DUTY CYCLE

WDCLK is the input signal that controls when data is loaded and how long each output is in the integrate mode. It is therefore recommended that a 50% (high) duty cycle be maintained on WDCLK. This will ensure that each output will have enough time to reach its final output value, and that the output level of each channel will be within the gain mismatch specification. Refer to Figure 1 for exact timing relationships of WDCLK to CLK and LRCLK and the outputs of the PCM66P. The WDCLK can be high longer than 50%, as long as setup and hold times shown in Figure 5 are observed and the time high is roughly equivalent for both left and right channels.

SETUP AND HOLD TIME

The individual serial data bit shifts, the serial to parallel data transfer, and left/right control are triggered on positive CLK edges. The setup time required for DATA, WDCLK, and LRCLK to be latched by the next positive going CLK is 15ns minimum. A minimum hold time of 15ns is also required after the positive going CLK edge for each data bit to be shifted into the serial input register. Refer to Figure 5 for the timing relationship of these signals.

MAXIMUM CLOCK RATE

The 100% tested maximum clock rate of 8.47MHz for the PCM66P is derived by multiplying the standard audio sample rate of 44.1kHz times eight (4X oversampling times two channels) times the standard audio word bit length of 24 (44.1kHz x 4 x 2 x 24 = 8.47MHz). Note that this clock rate accommodates a 24-bit word length, even though only 16 bits are actually being used.

"STOPPED-CLOCK" OPERATION

The PCM66P is normally operated with a continuous clock input signal. If the clock is to be stopped between input data words, the last 16 bits shifted in are not actually shifted from the serial register to the latched parallel DAC register until the first clock after the one used to input bit 16 (LSB). This means the data is not shifted into the DHC latch until the start of the next 16-bit data word input, unless at least one additional clock accompanies the 16 used to serially shift in data in the first place. In either case, the setup and hold times for DATA, WDCLK, and LRCLK must still be observed.

INSTALLATION

The PCM66P only requires a single +5V supply. The +5V supply, however, is used in deriving the internal reference. It is therefore very important that this supply be as "clean" as possible to reduce coupling of supply noise to the outputs. If a good analog supply is available at greater than +5V, a zener diode can be used to obtain a stable +5V supply. A 100µF decoupling capacitor as shown in Figure 3 should be used regardless of how good the +5V supply is to maximize power supply rejection. All grounds should be connected to the analog ground plane as close to the PCM66P as possible.

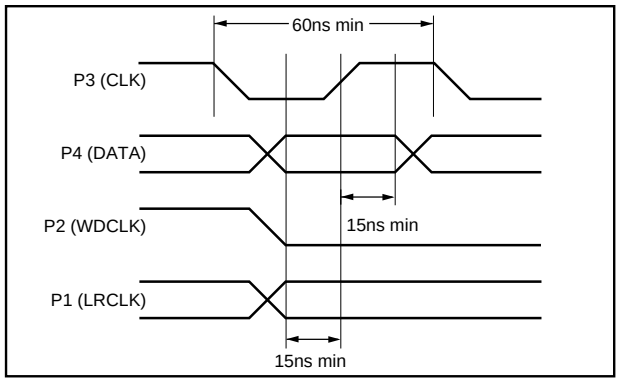


FIGURE 5. PCM66P Setup and Hold Timing Diagram.

FILTER CAPACITOR REQUIREMENTS

As shown in Figure 3, C_{REF} and V_{REF} SENSE should have decoupling capacitors of 0.1µF (C_4) and 10µF (C_5) to $+V_{CC}$ respectively with no special tolerance being required. To maximize channel separation between left and right channels, 5% 300pF capacitors (C_2 and C_3) between V_{COM} and left and right channel outputs are required in addition to a 5% 3µF capacitor (C_1) between V_{COM} and +5V. The ratio of 10k to 1 is the important factor here for proper circuit operation. Placement of all capacitors should be as close to the appropriate pins of the PCM66P as possible to reduce noise pickup from surrounding circuitry.

APPLICATIONS

Probably the most popular use of the PCM66P is in applications requiring single power supply operation. For example, the PCM66P is ideal for automotive compact disk (CD) and digital audio tape (DAT) playback units. To use a more complex bipolar DAC requiring ±5V supplies in the +12V application, for example, would require driving a stable "floating" ground and regulating the +12V to +10V. The single supply CMOS PCM66P would only require a +5V zener diode to regulate its 50mW max supply. The outputs could be AC coupled to the rest of the circuit for perfectly acceptable high dynamic performance. The PCM66P is ideal in any application requiring a minimum of additional circuitry as well as ultra-low-power CMOS performance.

Of course, the PCM66P is the D/A converter of choice in any application requiring very low power dissipation. Portable battery powered test and measurement equipment requiring very low distortion digital to analog converters would be an ideal application for the CMOS PCM66P with its 50mW max power dissipation.