PCS1P2192A

VDP Multiple Pixel Clock Generator

Features

- Generates multiple clock outputs from 20MHz external reference clock
- Input frequency: 20MHz
- Output frequencies:
  - Selectable CLKOUT: 108MHz, 27MHz, 33.2MHz, 85MHz, 65MHz, 25MHz, 45MHz, and 40MHz
  - REFOUT: 20MHz
- Operating Supply Voltage: 3.3V ± 0.3V
- Zero ppm frequency synthesis error on all clock outputs
- 8-pin SOIC package

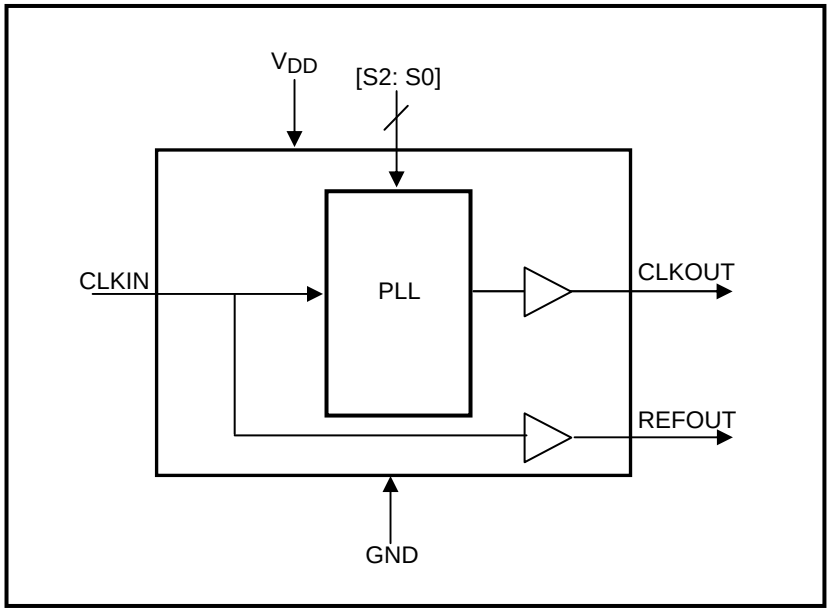
Product Description

The PCS1P2192A is a clock generator that generates multiple selectable pixel clock outputs for Video Display Panel applications from an external 20MHz reference clock. The PLL based clock generator is specifically designed to provide zero ppm frequency synthesis error on all clock outputs. Various pixel clock rates are selectable through frequency selection pins S[2:0] *(*Refer to *Frequency Selection Table)* The device provides a reference clock output additionally. Operating Supply Voltage for this device is 3.3V ± 0.3V. The device is available in an 8-pin SOIC package.

Application

PCS1P2192A is targeted towards Video Display Panel (VDP) applications like VGA, SVGA, XGA, WXGA, UXGA.

Block Diagram



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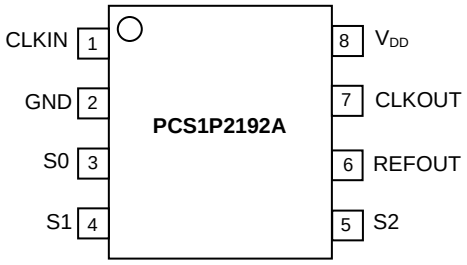
Pin Configuration



Pin Description

Pin#	Pin Name	Type	Description
1	CLKIN	I	20MHz external reference clock input.
2	GND	P	Ground Connection.
3	S0	I	Frequency select. Digital logic input used to select output frequency. Has an internal pull up resistor. (Refer to *Frequency Selection Table*.)
4	S1	I	Frequency select. Digital logic input used to select output frequency. Has an internal pull up resistor. (Refer to *Frequency Selection Table*.)
5	S2	I	Frequency select. Digital logic input used to select output frequency. Has an internal pull up resistor. (Refer to *Frequency Selection Table*.)
6	REFOUT	O	Reference clock output.
7	CLKOUT	O	Clock output.
8	V_{DD}	P	Device Power Supply .

Frequency Selection Table

S2	S1	S0	CLKOUT (MHz)
0	0	0	108
0	0	1	27
0	1	0	33.2
0	1	1	85
1	0	0	65
1	0	1	25
1	1	0	45
1	1	1	40

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any input pin with respect to Ground	-0.5 to +4.6	V
T_{STG}	Storage temperature	-65 to +125	℃
T_s	Max. Soldering Temperature (10 sec)	260	℃
T_J	Junction Temperature	150	℃
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	Operating Voltage	3.0	3.3	3.6	V
T_A	Operating Temperature	0		+85	℃
C_L	Load Capacitance			15	pF
C_{IN}	Input Capacitance			7	pF

DC Electrical Characteristics

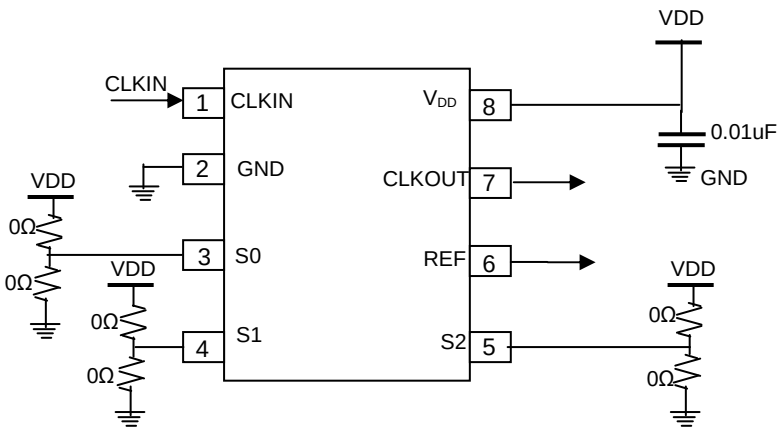
Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage (For CLKIN)	GND-0.3		0.8	V
V_{IH}	Input high voltage (For CLKIN)	2.0		VDD+0.3	V
I_{IL}	Input low current			50	µA
I_{IH}	Input high current			-50	µA
V_{OL}	Output low voltage (VDD = 3.3V, I_{OL} = 8mA)			0.4	V
V_{OH}	Output high voltage (VDD = 3.3V, I_{OH} = -8mA)	2.4			V
I_{DD}	Static supply current[1]			5	mA
I_{CC}	Dynamic supply current (3.3V and no load)		9		mA
V_{DD}	Operating Voltage	3.0	3.3	3.6	V
t_{ON}	Power-up time (first locked cycle after power-up)		1		mS
Z_{OUT}	Output impedance		40		Ω

Note: 1. CLKIN pulled low.

AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input frequency		20		MHz
f_{OUT}	Output frequency		108, 27, 33.2, 85, 65, 25, 45, 40		MHz
t_{LH}[1]	Output rise time (Measured from 20% to 80%)	1.2		2.5	nS
t_{HL}[1]	Output fall time (Measured from 80% to 20%)	0.8		1.6	nS
t_{JC}	Period Jitter		±150		pS
	Frequency Synthesis Error (All Outputs)		0		ppm
t_D	Output duty cycle	40	50	60	%
Note: 1. Measured with a capacitive load of 15pF.					

Typical Application Schematic



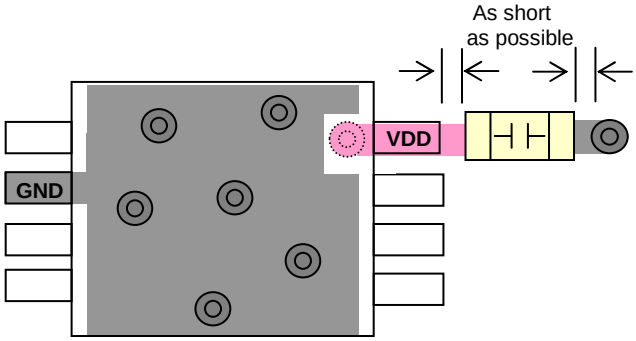
Use either pull-up or pull-down
0Ω Resistor with [S2:S0] for selection of
CLKOUT frequencies.

PCB Layout Recommendation

For optimum device performance, following guidelines are recommended.

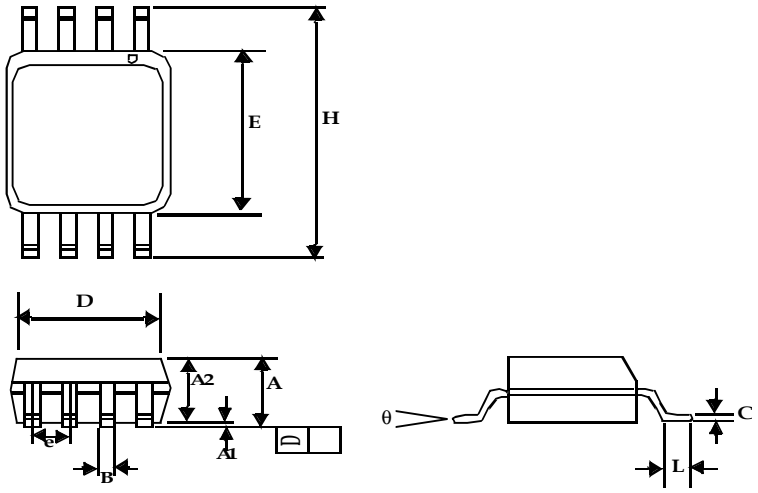
- Dedicated VDD and GND planes.
- The device must be isolated from system power supply noise. A 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin and the ground via should be kept as short as possible. All the VDD pins should have decoupling capacitors.
- In an optimum layout all components are on the same side of the board, minimizing vias through other signal layers.

A typical layout is shown in the figure below.



Package Information

8-Pin SOIC Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°

Ordering Code

Part Number	Marking	Package Type	Temperature
PCS1P2192AG-08SR	ACZ	8-Pin SOIC, TAPE & REEL, Green	0℃ to +85℃

A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-free.

Licensed under U.S Patent #5,488,627 and #5,631,921

Note: This product utilizes US Patent #6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003.

PUBLICATION ORDERING INFORMATION

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