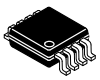
PCS3P2005A

Product Preview

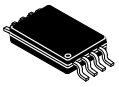
General Purpose Peak EMI Reduction IC

ON Semiconductor®

http://onsemi.com

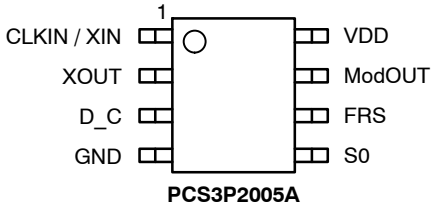


SOIC−8
S SUFFIX
CASE 751BD



TSSOP−8
T SUFFIX
CASE 948AL

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

Description

PCS3P2005A is a versatile, 3.3 V/5 V, 1x spread spectrum frequency modulator designed to reduce electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The device allows significant system cost savings by reducing the number of circuit board layers ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.

PCS3P2005A modulates the output of a PLL in order to "spread" the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is called 'spread spectrum clock generation.'

PCS3P2005A accepts an input from an external reference clock and locks to a 1x modulated clock output. Two logic pins S0 and D_C enable selecting one of the 4 different frequency deviations. Refer to the *Deviation Selection Table* for more details. Frequency Range Selection pin enables operation in one of the two frequency ranges. PCS3P2005A operates over a supply voltage range of 5 V / 3.3 V. PCS3P2005A is available in 8 Pin TSSOP and SOIC Packages, over Commercial and Industrial temperature range.

Applications

PCS3P2005A is targeted for use in a broad range of notebook and desktop PCs and consumer electronic applications.

Features

- 1x, LVCMOS Peak EMI Reduction
- Input Frequency:
  - 10 MHz – 30 MHz @ 3.3 V
  - 30 MHz – 100 MHz @ 5 V
- Output Frequency:
  - 10 MHz – 30 MHz @ 3.3 V
  - 30 MHz – 100 MHz @ 5 V
- Four Different Frequency Deviation Selection
- Selectable Spread Options: Down Spread and Center Spread
- Frequency Range Selection
- Supply Voltage:
  - 5 V ± 0.5 V
  - 3.3 V ± 0.3 V
- 8 Pin TSSOP, SOIC Package
- Commercial and Industrial Temperature Range
- These are Pb−Free Devices

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

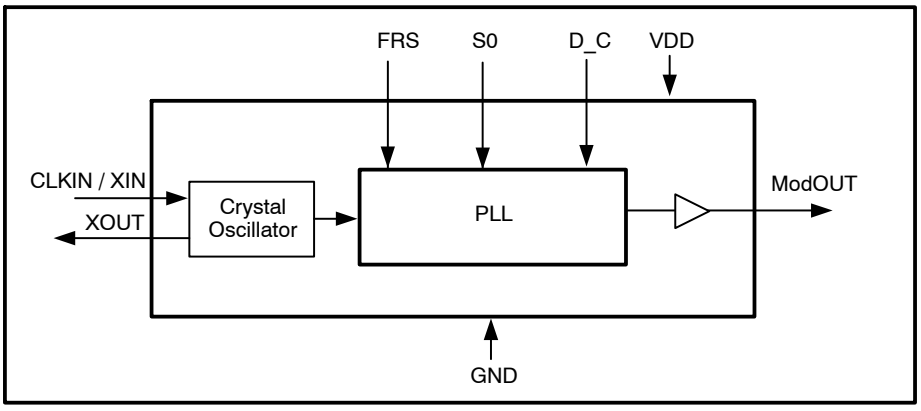


Figure 1. Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VDD, V_{IN}	Voltage on any input pin with respect to Ground	−0.5 to +7.0	V
T_{STG}	Storage temperature	−65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22− A114−B)	2	KV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 2. PIN DESCRIPTION

Pin#	Pin Name	Type	Description
1	CLKIN / XIN	I	External reference Clock input or Crystal connection.
2	XOUT	O	Crystal connection. If using an external reference, this pin must be left unconnected.
3	D_C	I	Deviation Selection. Has an internal pull−up resistor. Refer to *Deviation* Selection *Table*.
4	GND	P	Ground connection.
5	S0	I	Deviation Selection. Has an internal pull−up resistor. Refer to *Deviation Selection Table.*
6	FRS	I	Frequency Range Selection. Has an internal pull−up resistor.
7	ModOUT	O	Buffered Modulated Clock Output.
8	VDD	P	Power supply for the entire chip (3.3 V/5 V).

Table 3. FREQUENCY RANGE SELECTION TABLE

FRS	Frequency (MHz)
0	10 – 30
1	30 – 100

Table 4. DEVIATION SELECTION TABLE

Deviation (%)							
		FS = 0			FS = 1		
D_C	S0	10 MHz	20 MHz	30 MHz	30 MHz	80 MHz	100 MHz
0	0	−4.5	−3.6	−1.7	−4.8	−3.6	−2.6
0	1	−2.6	−2	−1	−2.7	−2	−1.5
1	0	±2.6	±2	±1	±2.75	±2	±1.5
1	1	±1.7	±1.25	±0.7	±1.8	±1.25	±1

Table 5. OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
$VDD_{(5V)}$	Supply Voltage		4.5	5.5	V
$VDD_{(3.3V)}$	Supply Voltage		3	3.6	V
T_A	Operating Temperature	Commercial	0	+70	°C
		Industrial	−40	+85	
C_L	Load Capacitance			15	pF
C_{IN}	Input Capacitance			7	pF

Table 6. DC ELECTRICAL CHARACTERISTICS FOR VDD = 5 V ± 0.5 V

Symbol	Parameter		Min	Typ	Max	Unit
VDD	Operating voltage		4.5	5.0	5.5	V
V_{IL}	Input low voltage		GND − 0.3		0.8	V
V_{IH}	Input high voltage		2.0		VDD + 0.3	V
I_{IL}	Input low current				100	μA
I_{IH}	Input high current				100	μA
V_{OL}	Output low voltage (I_{OL} = 12 mA)				0.4	V
V_{OH}	Output high voltage (I_{OH} = −12 mA)		2.5			V
I_{CC}	Static supply current (CLKIN / XIN pulled to GND)				12	mA
I_{DD}	Dynamic supply current (Unloaded Output)	FS = 0 (@ 30 MHz)			34	mA
		FS = 1 (@ 100 MHz)			40	
Z_{OUT}	Output impedance			30		Ω

Table 7. AC ELECTRICAL CHARACTERISTICS FOR VDD = 5 V ± 0.5 V

Symbol	Parameter		Min	Typ	Max	Unit
CLKIN / XIN	Input Clock Frequency	FRS = 0	10		30	MHz
		FRS = 1	30		100	
MODOUT	Output Clock Frequency	FRS = 0	10		30	MHz
		FRS = 1	30		100	
t_{LH} (Notes 1, 2)	Output Rise time (measured between 20% to 80%)			1.6	2	nS
t_{HL} (Notes 1, 2)	Output Fall time (measured between 80% to 20%)			1.2	1.6	nS
t_D (Notes 1, 2)	Output duty cycle		45	50	55	%
t_{JC} (Note 2)	Jitter (cycle−to−cycle) @ FS = 0, 24 MHz & FS = 1, 80 MHz			±250	±350	pS
t_{ON} (Notes 1, 2)	PLL lock time (Stable VDD, valid Clock presented on CLKIN / XIN)				3	mS

1. All parameters are specified with 15 pF loaded output.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Table 8. DC ELECTRICAL CHARACTERISTICS FOR VDD = 3.3 V ± 0.3 V

Symbol	Parameter		Min	Typ	Max	Unit
VDD	Operating voltage		3	3.3	3.6	V
V_{IL}	Input low voltage		GND − 0.3		0.8	V
V_{IH}	Input high voltage		2.0		VDD + 0.3	V
I_{IL}	Input low current				100	μA
I_{IH}	Input high current				100	μA
V_{OL}	Output low voltage (I_{OL} = 12 mA)				0.4	V
V_{OH}	Output high voltage (I_{OH} = −12 mA)		2.5			V
I_{CC}	Static supply current (CLKIN / XIN pulled to GND)				11	mA
I_{DD}	Dynamic supply current (Unloaded Output)	FS = 0 (@ 30 MHz)			26	mA
		FS = 1 (@ 100 MHz)			32	
Z_{OUT}	Output impedance			40		Ω

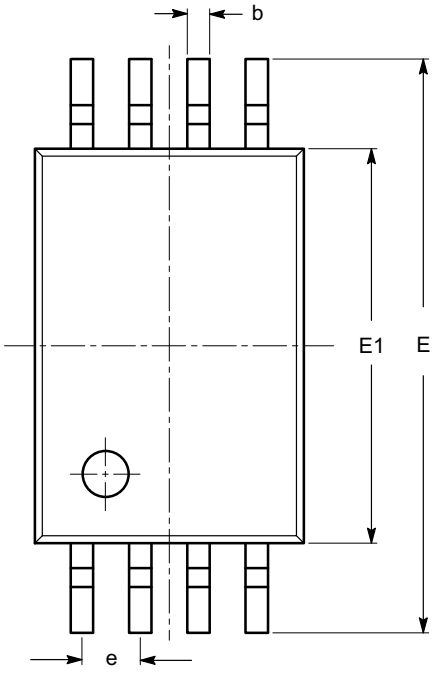
Table 9. AC ELECTRICAL CHARACTERISTICS FOR VDD = 3.3 V ± 0.3 V

Symbol	Parameter		Min	Typ	Max	Unit
CLKIN / XIN	Input Clock Frequency	FRS = 0	10		30	MHz
		FRS = 1	30		100	
MODOUT	Output Clock Frequency	FRS = 0	10		30	MHz
		FRS = 1	30		100	
t_{LH} (Notes 3, 4)	Output Rise time (measured between 20% to 80%)			1.9	2.5	nS
t_{HL} (Notes 3, 4)	Output Fall time (measured between 80% to 20%)			1.5	2	nS
t_D (Notes 3, 4)	Output duty cycle		45	50	55	%
t_{JC} (Note 3)	Jitter (cycle−to−cycle) @ FS = 0, 24 MHz & FS = 1, 80 MHz			±250	±350	pS
t_{ON} (Notes 3, 4)	PLL lock time (Stable VDD, valid Clock presented on CLKIN / XIN)				3	mS

3. All parameters are specified with 15 pF loaded output.
4. Parameter is guaranteed by design and characterization. Not 100% tested in production.

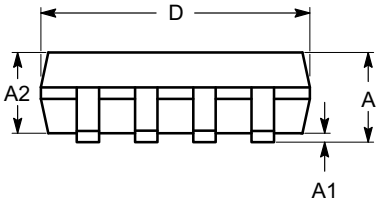
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

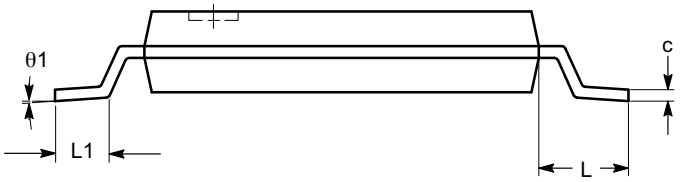


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0º		8º



SIDE VIEW



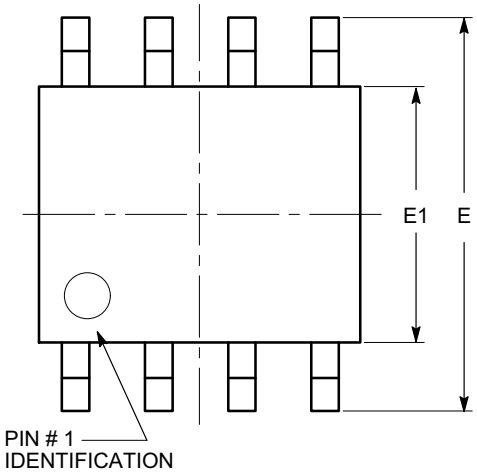
END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

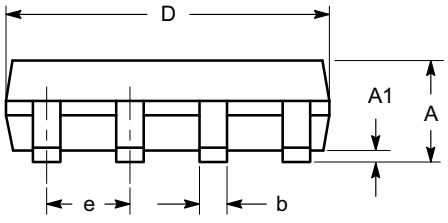
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

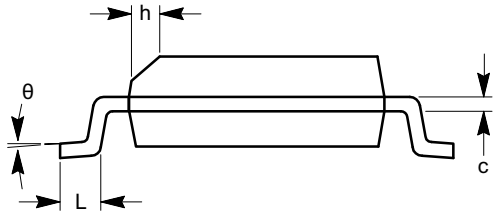


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

Table 10. ORDERING INFORMATION

Part Number	Marking	Package Type	Temperature
PCS3P2005AG−08SR	3P2005AG	8−PIN SOIC, TAPE AND REEL, Green	Commercial
PCS3P2005AG−08ST	3P2005AG	8−PIN SOIC, TUBE, Green	Commercial
PCS3P2005AG−08TR	3P2005AG	8−PIN TSSOP, TAPE AND REEL, Green	Commercial
PCS3P2005AG−08TT	3P2005AG	8−PIN TSSOP, TUBE, Green	Commercial
PCS3I2005AG−08SR	3I2005AG	8−PIN SOIC, TAPE AND REEL, Green	Industrial
PCS3I2005AG−08ST	3I2005AG	8−PIN SOIC, TUBE, Green	Industrial
PCS3I2005AG−08TR	3I2005AG	8−PIN TSSOP, TAPE AND REEL, Green	Industrial
PCS3I2005AG−08TT	3I2005AG	8−PIN TSSOP, TUBE, Green	Industrial

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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