Low Power Peak EMI Reduction IC

Features

- 1x Peak EMI Reduction IC
- Input Frequency: 18MHz-36MHz
- Output Frequency: 18MHz-36MHz
- Frequency Deviation @ 27MHz : -0.25%
- Modulation Rate @ 27MHz : 30.1KHz
- Supply Voltage: 3.3V±0.3V
- Operating current less than 8mA @ 27MHz.
- Spread Spectrum Enable Control.
- Low power CMOS design.
- 8 pin TDFN (2X2) COL package.
- Commercial temperature

Product Description

PCS3P2537A is a versatile Low Power, 1x spread spectrum frequency modulator designed to reduce electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The device allows significant system cost savings by reducing the number of circuit board layers ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.

PCS3P2537A modulates the output of a single PLL in order to "spread" the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is called 'spread spectrum clock generation'.

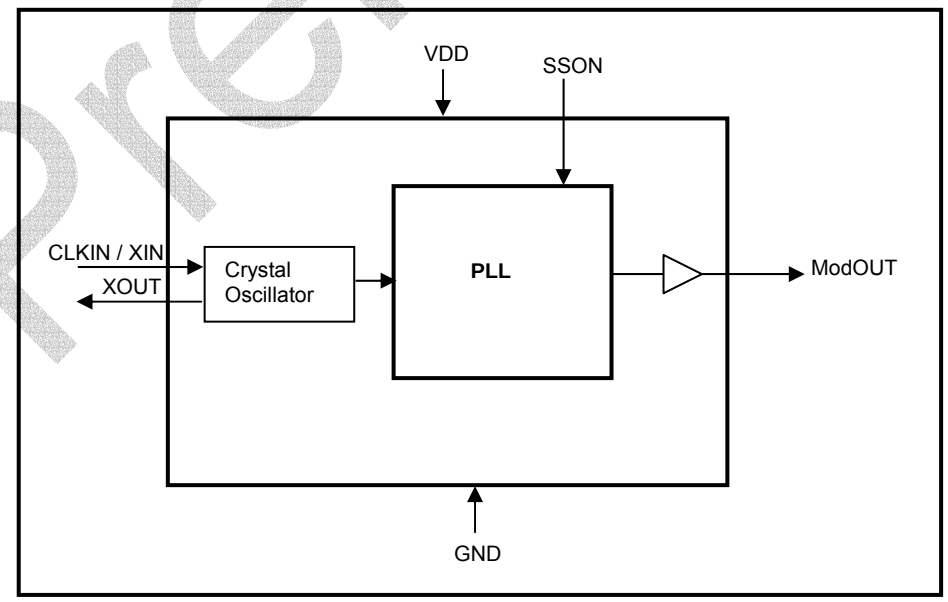
PCS3P2537A has a frequency range of 18MHz-36MHz, and accepts input clock either from a Crystal or from an external reference and locks on to it delivering a 1x spread spectrum clock output. It has an SSON control for enabling and disabling Spread Spectrum function.

PCS3P2537A operates with a supply voltage of 3.3V, and is available in 8L TDFN(2X2) COL package over commercial temperature.

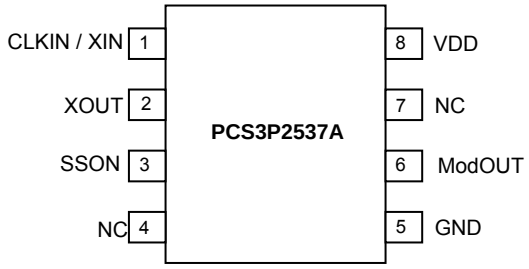
Application

PCS3P2537A is targeted towards PC peripheral devices and embedded systems.

Block Diagram



Pin Configuration (8-pin TDFN Package)



Pin Description

Pin#	Pin Name	Type	Description
1	CLKIN / XIN	I	External reference Clock input or Crystal connection. This pin has dual functions. It can be connected either to an external crystal or an external reference clock.
2	XOUT	O	Crystal connection. If using an external reference, this pin must be left unconnected.
3	SSON	I	When SSON is HIGH, the spread spectrum is enabled and when LOW, it turns off the spread spectrum.
4	NC		No Connect
5	GND	P	Ground connection.
6	ModOUT	O	Spread Spectrum Clock Output.
7	NC		No Connect
8	VDD	P	Power supply for the entire chip

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD, V_{IN}	Voltage on any pin with respect to Ground	-0.5 to +4.6	V
T_{STG}	Storage temperature	-65 to +125	°C
T_A	Operating temperature	-40 to +85	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

DC Electrical Characteristics for 3.3V Supply

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	VSS - 0.3		0.8	V
V_{IH}	Input high voltage	2.0		VDD + 0.3	V
I_{IL}	Input low current			-35	µA
I_{IH}	Input high current			35	µA
V_{OL}	Output low voltage (VDD = 3.3V, I_{OL} = 8mA)			0.4	V
V_{OH}	Output high voltage (VDD = 3.3V, I_{OH} = 8mA)	2.5			V
I_{DD}	Static supply current*			2.5	mA
I_{CC}	Dynamic supply current (3.3V, 27MHz and no load)		7		mA
VDD	Operating Voltage	3	3.3	3.6	V
t_{ON}	Power-up time (first locked cycle after power-up)			5	mS
Z_{OUT}	Output impedance		36		Ω

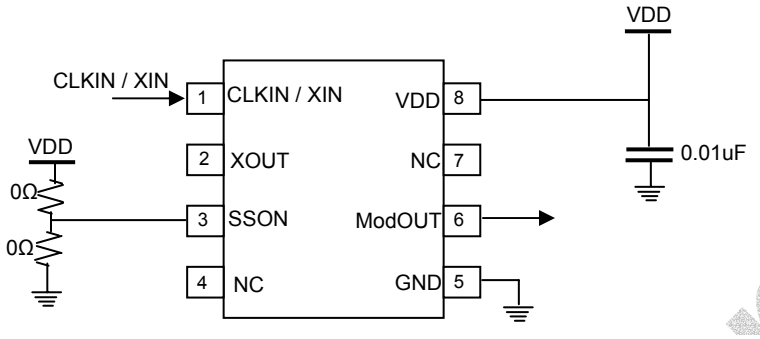
* CLKIN is pulled to GND

AC Electrical Characteristics for 3.3V Supply

Symbol	Parameter	Min	Typ	Max	Unit
CLKIN	Input frequency	18	27	36	MHz
ModOUT	Output frequency	18	27	36	MHz
f_d	Frequency Deviation @ 27MHz	-0.2	-0.25	-0.3	%
MR	Modulation Rate @ 27MHz	30		33	KHz
t_{LH}*	Output rise time (measured from 20% to 80%)			2	nS
t_{HL}*	Output fall time (measured at 80% to 20%)			1.5	nS
t_{JC}	Jitter (cycle to cycle)			200	pS
t_D	Output duty cycle	45	50	55	%

*t_{LH} and t_{HL} are measured into a capacitive load of 15pF

Typical Application Schematic



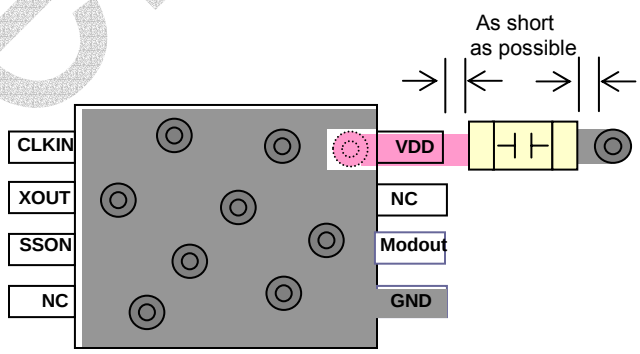
Note: Refer to Pin Description table for Functionality Details

PCB Layout Recommendation

For optimum device performance, following guidelines are recommended.

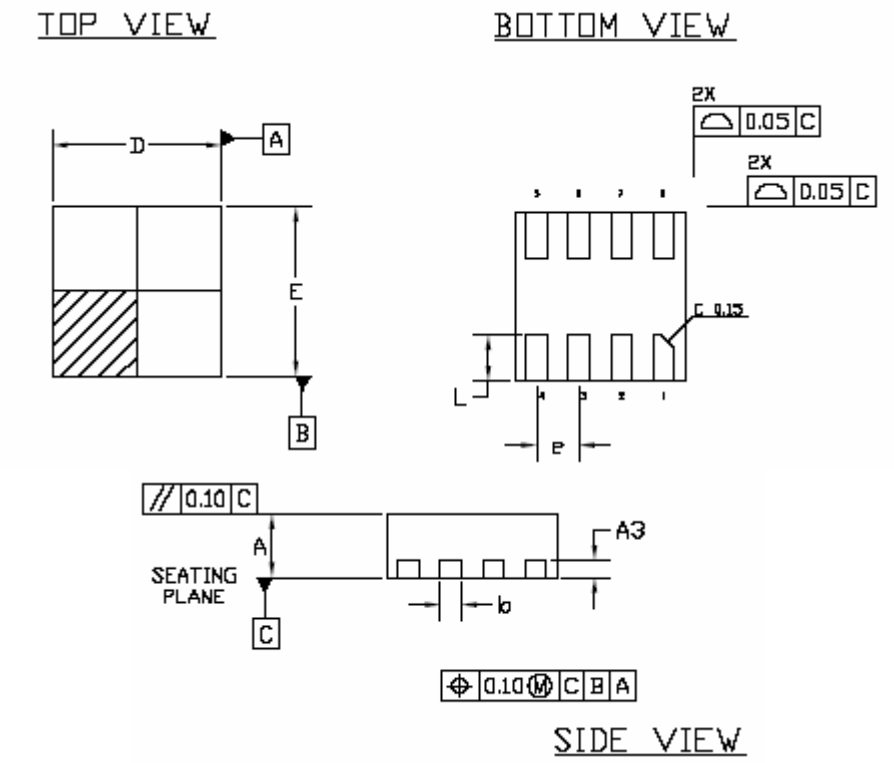
- Dedicated VDD and GND planes.
- The device must be isolated from system power supply noise. A 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin and the ground via should be kept as short as possible. All the VDD pins should have decoupling capacitors.
- In an optimum layout all components are on the same side of the board, minimizing vias through other signal layers.

A typical layout is shown in the figure



Package Information

TDFN COL 2x2 8L package



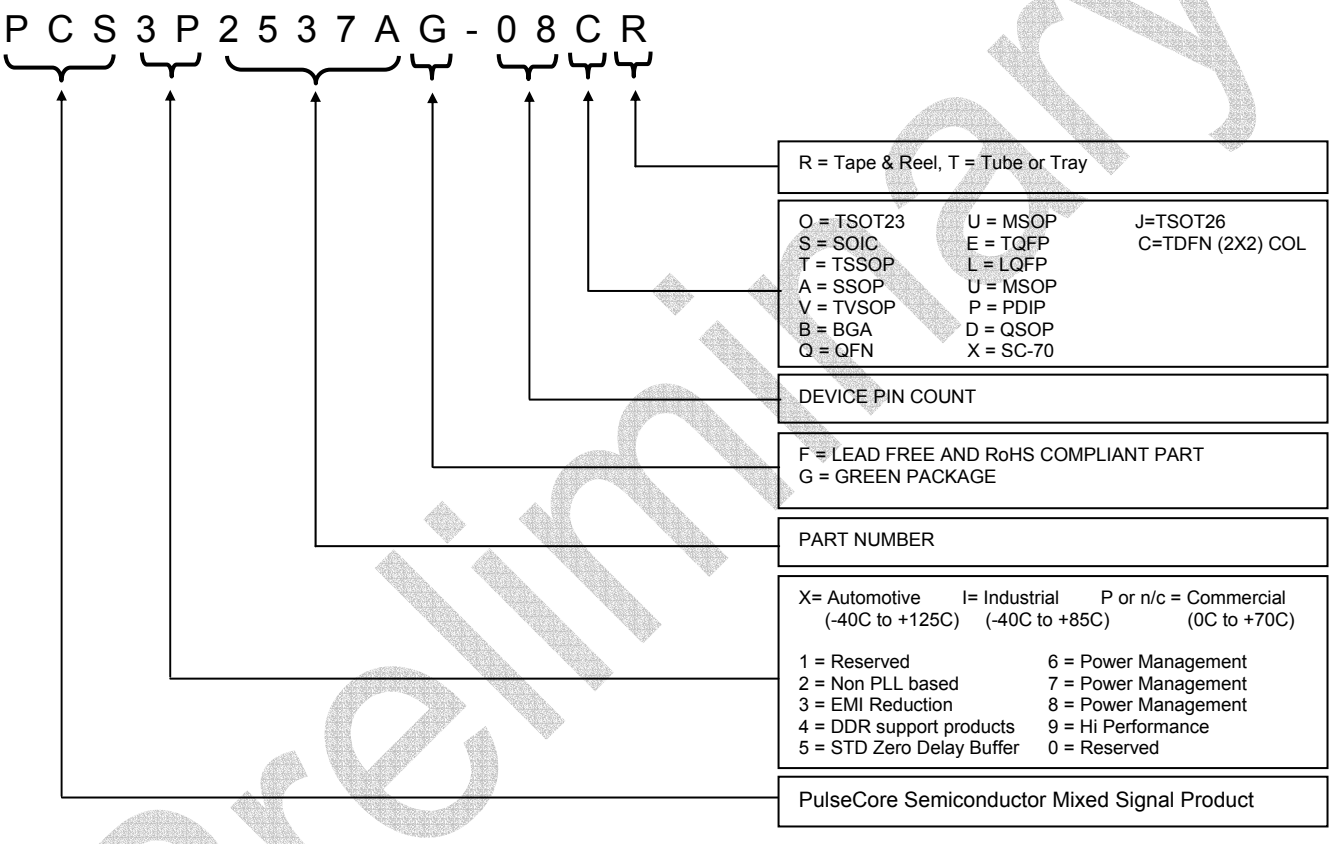
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.027	0.0315	0.70	0.80
A3	0.008 BSC		0.203 BSC	
b	0.008	0.012	0.20	0.30
D	0.077	0.080	1.95	2.05
E	0.077	0.080	1.95	2.05
e	0.020 BSC		0.50 BSC	
L	0.020	0.024	0.50	0.60

Ordering Codes

Part Number	Marking	Package	Temperature
PCS3P2537AG -08-CR	AM1LL	8- pin 2-mm TDFN COL - TAPE & REEL, Green	Commercial

LL = 2 Character LOT #

Device Ordering Information



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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003
Many PulseCore Semiconductor products are protected by issued patents or by applications for patent