ON Semiconductor®

PCS3P8103A

General Purpose Peak EMI Reduction IC

Features

- Generates a 4x low EMI spread spectrum clock
- Input Frequency: 16.667MHz
- Output Frequency: 66.66MHz
- Tri-level frequency Deviation Selection:
- Down Spread, Center Spread and No Spread
- Low inherent Cycle-to-Cycle Jitter
- Supply Voltage: 3.3V±0.3V
- LVCMOS Input and output
- 6L-TSOT-23 (6L-TSOT-26) Package

Product Description

The PCS3P8103A is a versatile spread spectrum frequency modulator designed specifically to provide a 4x output of 66.66MHz from an input clock of 16.667MHz.

The PCS3P8103A reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. It allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, shielding, and other passive components that are traditionally required to pass EMI regulations.

The custom device can generate an EMI reduced clock from crystal, or system clock.

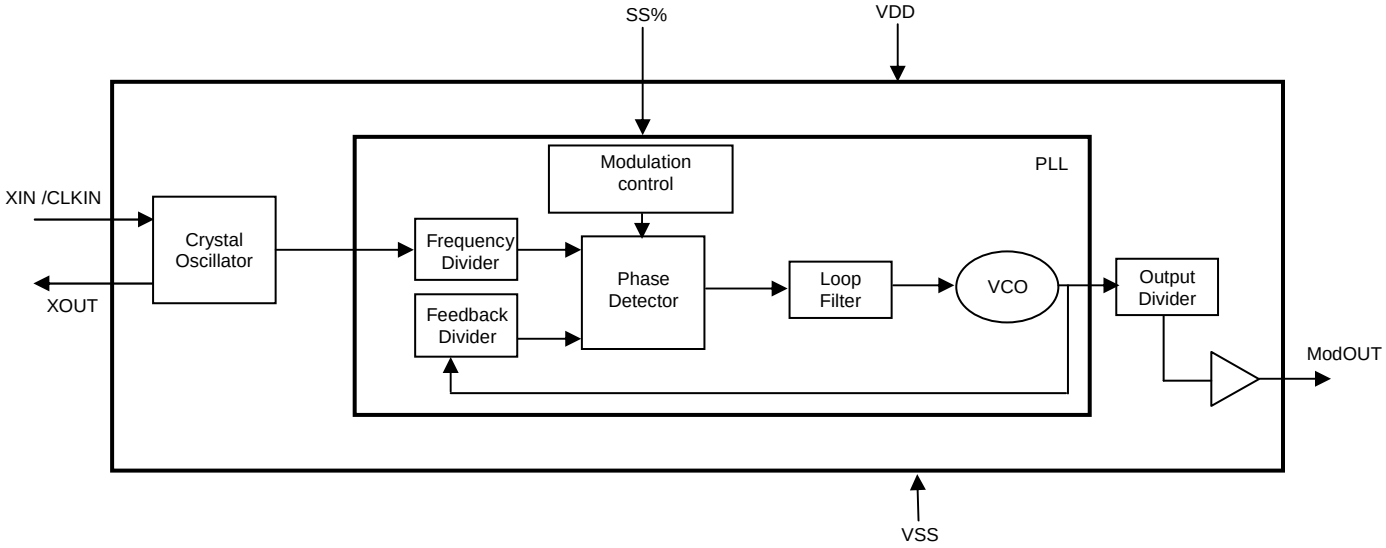
The PCS3P8103A has a 3 level logic control SS% for selecting Center Spread, Down Spread and No-Spread options. Refer to *Output Frequency Deviation table*.

The PCS3P8103A operates from a 3.3V±0.3V supply Voltage and is available in a 6L-TSOT-23 package.

Application

The PCS3P8103A is targeted towards EMI management in applications such as LCD Panels, MFPs, Digital copiers, Networking, PC peripheral devices, consumer electronics, and embedded controller systems.

Block Diagram



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Publication Order Number:
PCS3P8103A/D

Pin Configuration

Pin Description

Pin#	Pin Name	Type	Description
1	SS%	I	Tri-level logic input (1-M-0) used to select Down spread, No spread, and Center spread options. (Refer to *Output Frequency Deviation Selection Table).* Default=M.
2	VSS	P	Ground to entire chip.
3	XIN / CLKIN	I	Crystal connection or External Clock input.
4	XOUT	O	Crystal connection. If using an external reference, this pin must be left unconnected.
5	VDD	P	Power supply for the entire chip.
6	ModOUT	O	Spread Spectrum Clock Output.

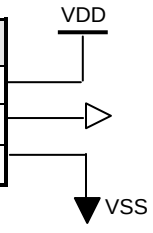
Output Frequency Deviation Selection Table

CLKIN (MHz)	SS%=0	SS%=1	SS%=M
	Center	Down	No Spread
16.667	±1.2%	-0.7%	0

Tri-Level Logic

SS% digital input is designed to sense 3 different logic levels designated as High “1”, Low “0” and Middle “M”. No external application resistors are needed to implement the 3-Level logic control as shown:

Logic	SS%
1	VDD
M	UNCONNECTED
0	VSS



Operating Conditions

Symbol	Parameter	Min	Max	Unit
VDD	Voltage on any input pin with respect to VSS	3.0	3.6	V
T_A	Operating temperature	0	+70	℃
C_L	Load Capacitance		15	pF
C_{IN}	Input Capacitance		7	pF

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD, V_{IN}	Voltage on any pin with respect to Ground	-0.5 to +4.6	V
T_{STG}	Storage temperature	-65 to +125	℃
T_s	Max. Soldering Temperature (10 sec)	260	℃
T_J	Junction Temperature	150	℃
T_{DV}	Static Discharge Voltage (As per JEDEC STD 22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

DC Electrical Characteristics

Symbol	Parameter			Min	Typ	Max	Unit
VDD	Supply Voltage			3	3.3	3.6	
V_{IL}	Input low voltage	Commercial temperature		0		0.15VDD	V
		Industrial temperature		0		0.13 VDD	
V_{IM}	Input Middle Voltage			0.4VDD		0.60VDD	
V_{IH}	Input high voltage			0.85VDD		VDD	V
V_{OL}	Output low voltage (ModOUT Output)		I_{OL}=4mA			0.4	V
V_{OH}	Output high voltage (ModOUT Output)		I_{OH}= -4mA	2.4			V
C_{IN}	Input Capacitance (XIN And XOUT)			6		9	pF
I_{DD}	Dynamic supply current (Unloaded Output)	Commercial temperature				10	mA
		Industrial temperature				12	mA
I_{CC}	Static supply current (XIN / CLKIN pulled to VSS)					0.5	mA

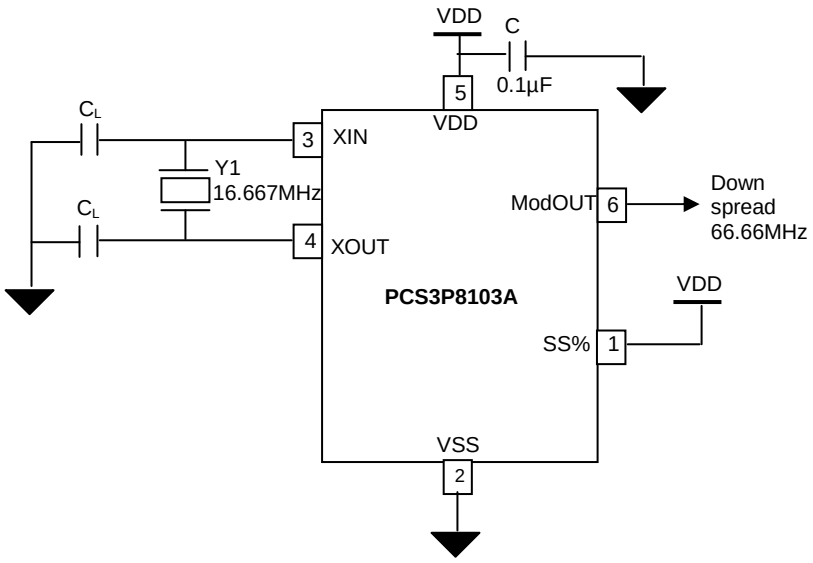
Note. The voltage on any input or I/O pin cannot exceed the power pin during power up.

AC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Unit
f_{IN}	Input Clock frequency			16.667		MHz
f_{OUT}	ModOUT Clock			66.66		MHz
t_{LH}[1, 2]	ModOUT Rise time (Measured from 20% to 80%)				3	nS
t_{HL}[1, 2]	ModOUT Fall time (Measured from 80% to 20%)				2.5	nS
T_{DCIN}	Input Clock Duty Cycle(XIN/CLKIN)		40		60	%
T_{DCOUT}[1, 2]	Output Clock Duty Cycle (ModOUT)		40		60	%
T_{JC}[2]	Cy - Cy Jitter, For ModOUT with Spread ON			±200	±350	pS
T_{JP}[2]	Period Jitter, For ModOUT with Spread OFF			±150		
t_{ON}[2]	PLL Lock Time (Stable power supply, valid input clock to valid Clock on ModOUT)	Commercial temp.			2	mS
		Industrial temp.			3	

Note: 1. Parameters are specified with 15pF loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Application Schematic

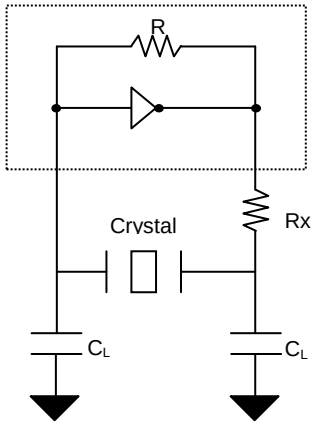


Typical Crystal Specifications

Fundamental AT cut parallel resonant crystal	
Nominal frequency	16.667MHz
Frequency tolerance	± 50ppm or better at 25℃
Operating temperature range	-25℃ to +85℃
Storage temperature	-40℃ to +85℃
Load capacitance	18pF
Shunt capacitance	7pF maximum
ESR	25Ω

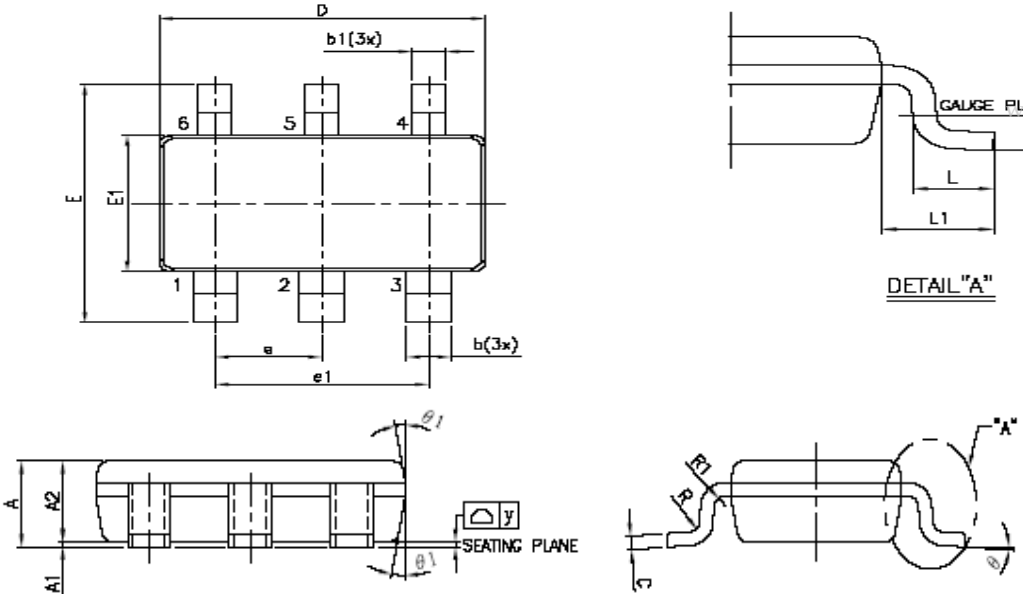
Note: C_L is Load Capacitance and Rx is used to prevent oscillations at overtone frequency of the Fundamental frequency.

Typical Crystal Interface Circuit



$C_L = 2*(C_P – C_S)$,
Where C_P = Load capacitance of crystal.
C_S = Stray capacitance due to $C_{IN,}$ PCB, Trace, etc.

6L-TSOT-23 Package Information



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.0295	0.035	0.75	0.90
A1	0.00	0.0039	0.00	0.10
A2	0.0275	0.0314	0.70	0.80
b	0.0157	0.0197	0.40	0.50
b1	0.0118	0.0157	0.30	0.40
c	0.0031	0.0078	0.08	0.20
D	0.1141		2.90 REF	
E	0.1023	0.1181	2.60	3.00
E1	0.0590	0.0069	1.50	1.70
e	0.0374		0.95 BSC	
e1	0.0748		1.90 BSC	
L	0.0118	0.0236	0.30	0.60
L1	0.0236 REF		0.60 REF	
L2	0.0098 BSC		0.25 BSC	
R	0.0039	…..	0.10	…..
R1	0.0039	0.0098	0.10	0.25
θ	0°	8°	0°	8°
y	….	0.0039	….	0.10

Ordering Code

Part Number	Marking	Package Type	Temperature
PCS3P8103AG-06JR	AZ1	6L-TSOT-23 (6L-TSOT-26), TAPE & REEL, Green	0℃ to +70℃

A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-free.

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003.

PUBLICATION ORDERING INFORMATION

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