PClamp0511ZV

PClamp®

1-Line ESD & Surge Protection

PROTECTION PRODUCTS

Description

PClamp TVS diodes are designed for use in harsh transient environments to protect sensitive electronics from damage or latch-up due to EOS, lightning, CDE, and ESD. They feature large cross-sectional area junctions for conducting high transient currents. These devices offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

The PClamp0511ZV features excellent protection characteristics highlighted by high surge current capability (115A, tp = 8/20µs), low peak ESD clamping voltage, and high ESD withstand voltage (±30kV per IEC 61000-4-2). Each device will protect one power line operating at 5V.

PClamp0511ZV is in a 2-pin DFN package, measuring1.0 x 0.6 x 0.25mm. Leads are spaced at a pitch of 0.65mm and are finished with lead-free NiAu. Each device can protect one bi-directional line operating at ±5 volts. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±30kV air, ±30kV contact discharge). The combination of small size and high ESD and surge capability makes them ideal for use in applications such as cellular phones, battery protection, and VBUS protection.

Features

- High ESD withstand Voltage: ±30kV (Contact) and ±30kV (Air) per IEC 61000-4-2
- High peak pulse current capability: 115A (tp = 8/20µs)
- Small package size (1.0 x 0.6 x 0.25mm)
- Protects one power line
- Low ESD clamping voltage
- Working voltage: ±5.0V
- Solid-state silicon-avalanche technology

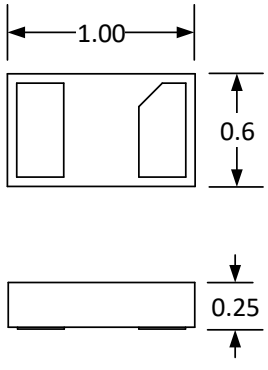
Mechanical Characteristics

- DFN 1.0 x 0.6 x 0.25mm package
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Molding compound flammability rating: UL 94V-0
- Lead Finish: NiAu
- Marking: Marking code
- Packaging: Tape and Reel

Applications

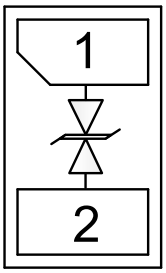
- Cellular Handsets & Accessories
- Industrial Equipment
- Voltage Supply Lines
- Battery protection
- USB VBus

Package Dimension



Nominal Dimensions (mm)

Schematic & Pin Configuration



DFN 1.0 x 0.6 x 0.25 (Bottom View)

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (t_p = 8/20µs)	P_{PK}	1200	W
Peak Pulse Current (t_p = 8/20µs)	I_{PP}	115	A
ESD per IEC 61000-4-2 (Air)(1) ESD per IEC 61000-4-2 (Contact)(1)	V_{ESD}	±30 ±30	kV
Operating Temperature	T_{OP}	-55 to +125	^{O}C
Junction Temperature & Storage Temperature	T_J & T_{STG}	-55 to +150	^{O}C

Electrical Characteristics (T=25^{O}C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}	Pin 1 to 2 or Pin 2 to 1				5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA, Pin 1 to 2 or Pin 2 to 1		6	7	8	V
Reverse Leakage Current	I_R	V_{RWM} = 5V, Pin 1 to 2 or Pin 2 to 1			0.004	0.1	µA
Clamping Voltage	V_C	t_p = 8/20µs	I_{PP}=40A		7.3	8.5	V
			I_{PP}=80A		8.1	9.5	
			I_{PP}=115A		9	10.5	
ESD Clamping Voltage[2]	V_C	tp=0.2/100ns	I_{TLP} = 4A		7		V
			I_{TLP} = 16A		6.9		
Dynamic Resistance[2,3]	R_{DYN}	tp = 0.2/100ns			0.02		Ω
Junction Capacitance	C_J	V_R = 0V, f = 1MHz			200	275	pF

Notes:

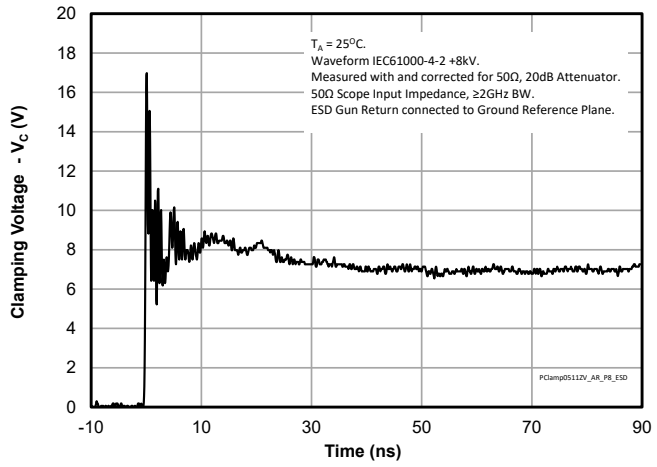
1) ESD gun return path connected to ESD ground plane.

2) Transmission Line Pulse Test (TLP) Settings: t_p = 100ns, t_r = 0.2ns, I_{TLP} and V_{TLP} averaging window: t_1 = 70ns to t_2 = 90ns.

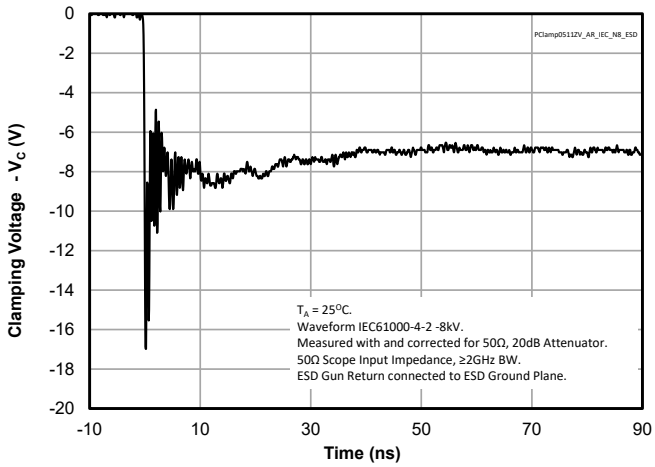
3) Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

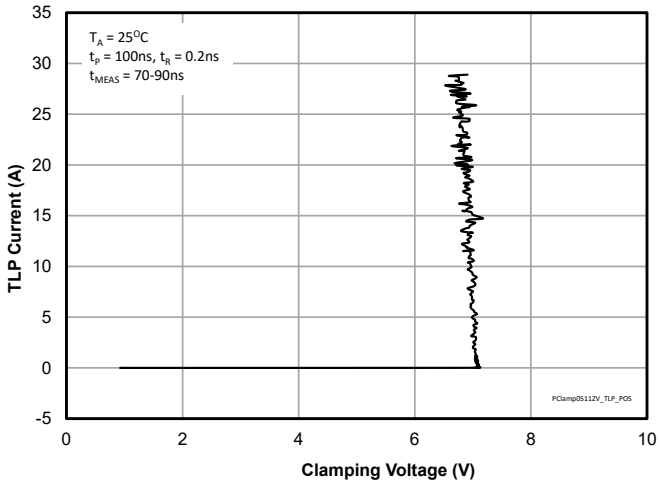
ESD Clamping (+8kV Contact per IEC 61000-4-2)



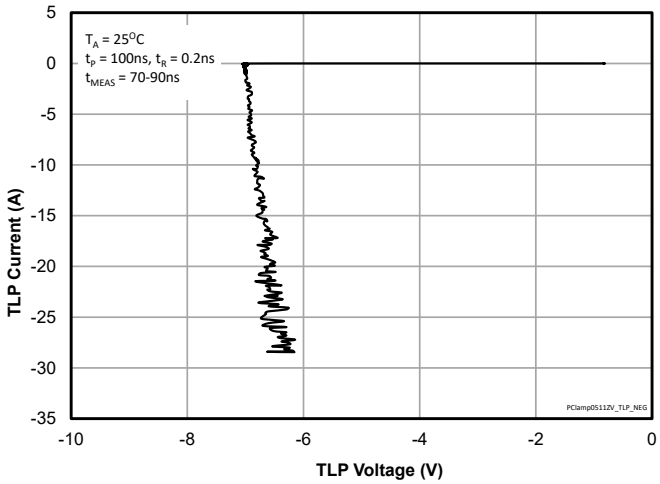
ESD Clamping (-8kV Contact per IEC 61000-4-2)



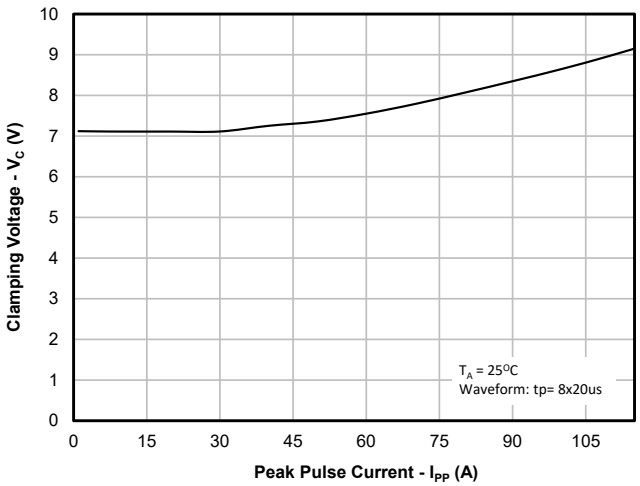
TLP Characteristic (Positive Pulse)



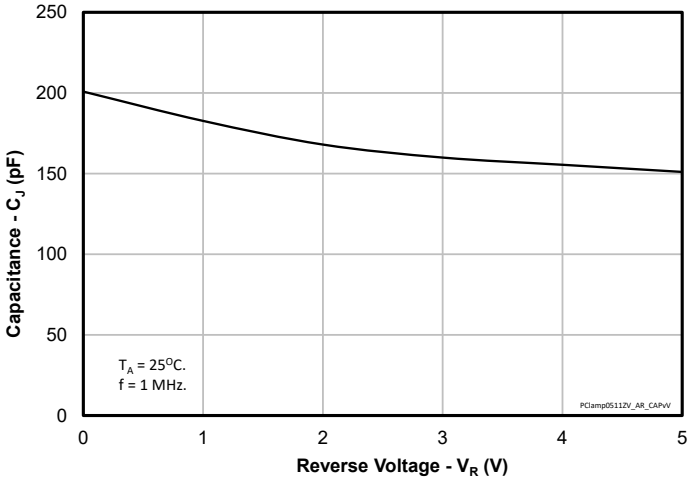
TLP Characteristic (Negative Pulse)



Clamping Voltage vs. Peak Pulse Current (t_p=8/20µs)



Capacitance vs. Reverse Voltage



Application Information

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joints. The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. A minimum area ratio of 0.66 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

Area Ratio = (L * W)/ (2 * (L + W) * T)

Where:
L = Aperture Length
W = Aperture Width
T = Stencil Thickness

Semtech recommends a stencil with square aperture and rounded corners for consistent solder release. The stencil should be laser cut with electro-polished finish. A stencil thickness of 0.100mm (0.004") or 0.125mm (0.005") stencil may be used, however the stencil opening may need to be increased slightly to achieve the desired area ratio to ensure proper solder coverage on the pad.

Recommended Mounting Pattern

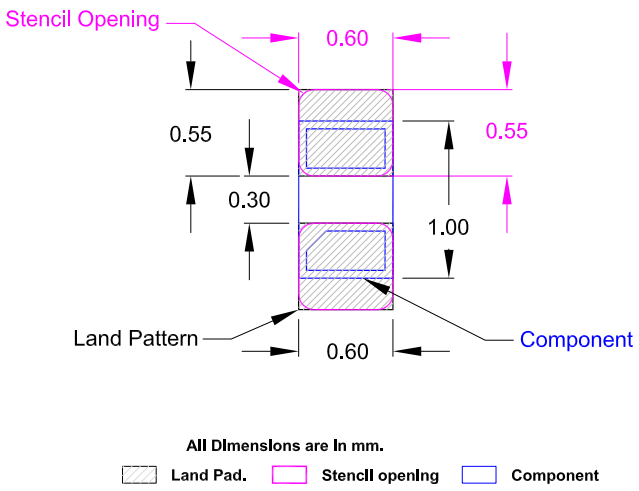
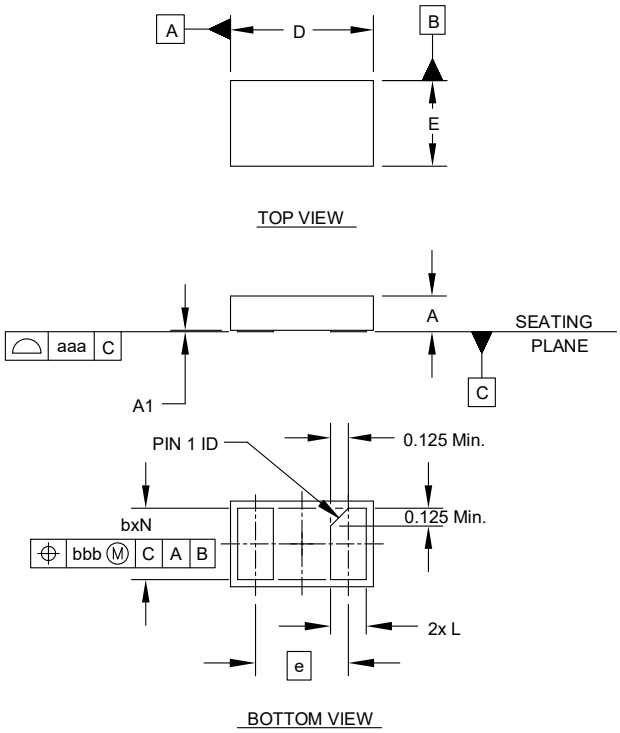


Table 1 - Assembly Guidelines

Assembly Parameter	Recommendation
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular with Rounded Corners
Solder Stencil Thickness	0.100mm (0.004") or 0.125mm (0.005")
Solder Paste Type	Type 4 or Type 5
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Design	SMD or NSMD
PCB Pad Finish	OSP or NiAu

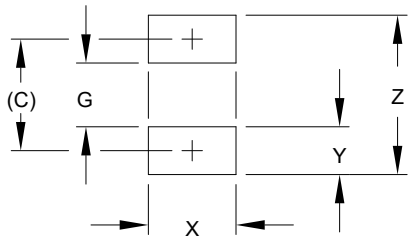
Outline Drawing - DFN 1.0 x 0.6 x 0.25mm 2 Lead



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.235	0.250	0.265
A1	0.00	0.010	0.050
b	0.45	0.50	0.55
D	0.95	1.00	1.05
E	0.55	0.60	0.65
e	0.65 BSC		
L	0.20	0.25	0.30
N	2		
aaa	0.08		
bbb	0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

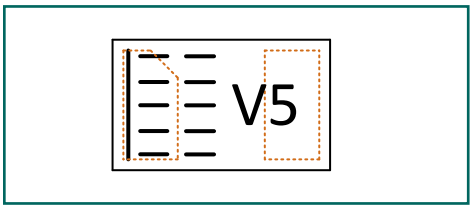
Land Pattern - DFN 1.0 x 0.6 x 0.25mm 2 Lead



DIMENSIONS	
DIM	MILLIMETERS
C	(0.85)
G	0.30
X	0.60
Y	0.55
Z	1.40

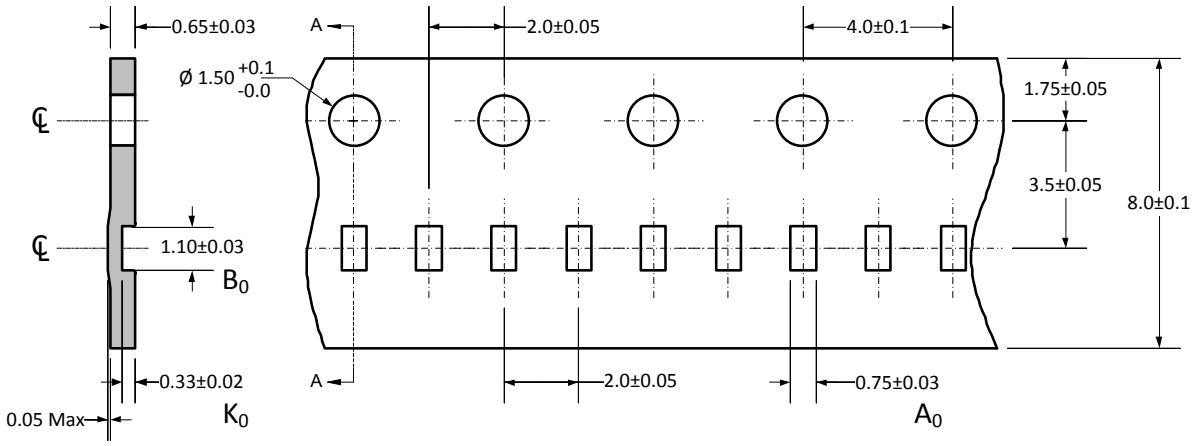
NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.

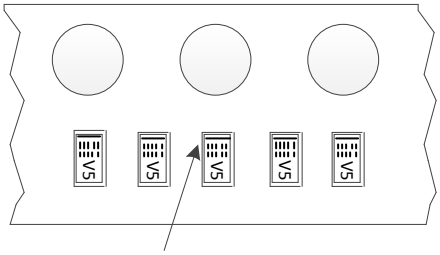
Marking Code



Notes:
1. Marking will also include line matrix date code.
2. Bar indicates Pin 1 location.

Tape and Reel Specification





Marking Code Location
(Bar Towards Sprocket Holes)

Ordering Information

Part Number	Qty per Reel	Reel Size
PClamp0511ZVTFT	15,000	7″

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