Version : 0.1

TECHNICAL SPECIFICATION

MODEL NO. : PD024OX2

☐Customer's Confirmation

Customer

Date

By

☐PVI's Confirmation

Confirmed By

Prepared By

PRIME VIEW INTERNATIONAL CO.,LTD.
3,LI SHIN RD. 1,SCIENCE-BASED INDUSTRIAL PARK,HSINCHU,TAIWAN,R.O.C.
http://www.pvi.com.tw

Date : Jul. 26 , 2004

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TECHNICAL SPECIFICATION

CONTENTS

1. Application

This technical specification applies to 2.37" color TFT-LCD panel. The 2.37” color TFT LCD panel is designed for camcorder, digital camera application and other electronic products which require high quality flat panel displays.

2. Features

. Amorphous silicon TFT-LCD panel with LED Backlight unit

. Support 8-bit digital (RGB) or CCIR656/CCIR601 8 bit format

. Support the SPI commands setting, the operation parameters setting internally

. Support low power control mode (Standby mode)

. PWM function is embedded

. Pixel in delta configuration

. 256K color display simultaneously

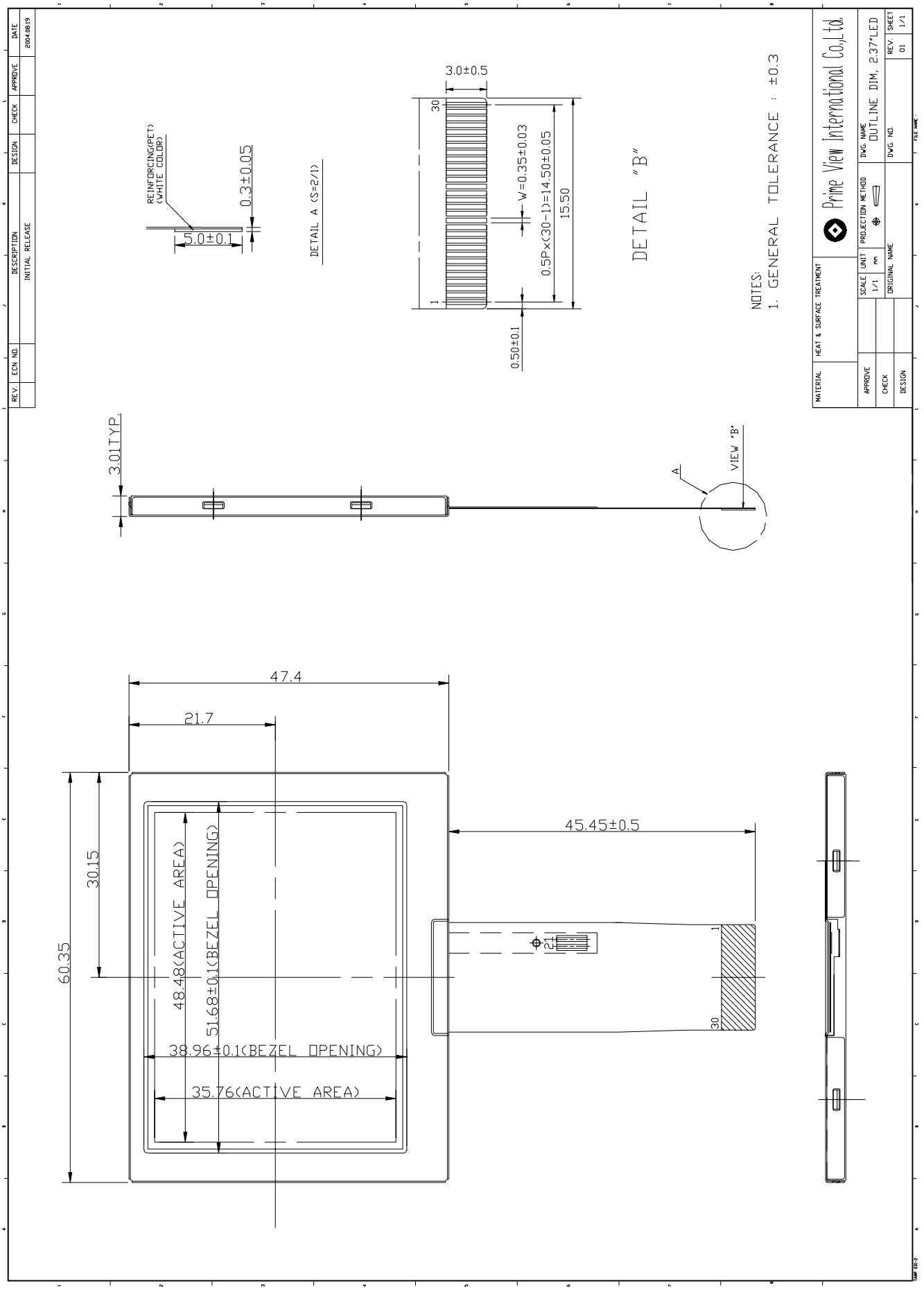
. Slim and compact

. Image Reversion : Up/Down and Left/Right

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	2.37 (diagonal)	inch
Display Format	160×R,G,B×240	dot
Active Area	48.48 (H)×35.76 (V)	mm
Dot Pitch	0.101 (W)×0.149 (H)	mm
Pixel Configuration	Delta	
Outline Dimension	61.35(W) × 47.40(H) × 3.01(D)(typ.)	mm
Surface Treatment	Anti – Glare	
Weight	TBD	g

4. Mechanical Drawing of TFT-LCD Module



5. Input / Output Terminals

TFT-LCD Module Connector
FPC Down Connect , 30Pins , Pitch : 0.5 mm

Pin No	Symbol	I/O	Description	Remark
1	VLED	I	Supply voltage for LED backlight	Note 5-1
2	GLED	I	Ground for LED backlight	
3	VFB	I	PWM feedback reference voltage	
4	DRV	O	PWM drive output signal	
5	V_{COML}	I/O	V_{COM} reference low level voltage	
6	V_{COMH}	I/O	V_{COM} reference high level voltage	
7	V_{COM}	I	V_{COM} input signal	
8	V_{GH}	I	Gate output High voltage	
9	V_{GL}	I	Gate output Low voltage	
10	V_{DDA}	I	Analog power voltage	Note 5-2
11	V_{SSA}	I	Analog power ground	
12	V_{SS}	I	Digital power ground	
13	POL	O	Polarity output signal	
14	RESETB	I	Active low global reset signal input	
15	SPENA	I	Serial port data enable signal	
16	SPCK	I	Serial port clock	
17	SPDA	I/O	Serial port data input / output	
18	HSD	I	Horizontal Sync. Input with negative polarity	
19	VSD	I	Vertical Sync. Input with negative polarity	
20	DEN	I	Input data enable control	
21	DIN7	I	Digital image data input	
22	DIN6	I	Digital image data input	
23	DIN5	I	Digital image data input	
24	DIN4	I	Digital image data input	
25	DIN3	I	Digital image data input	
26	DIN2	I	Digital image data input	
27	DIN1	I	Digital image data input	
28	DIN0	I	Digital image data input	
29	CLKIN	I	Input data sampling clock at rising edge	
30	V_{DD}	I	Digital power voltage	Note 5-3

Note 5-8 : I_{LED} TYP.=20mA

Note 5-2 : V_{DDA} TYP.＝+5V

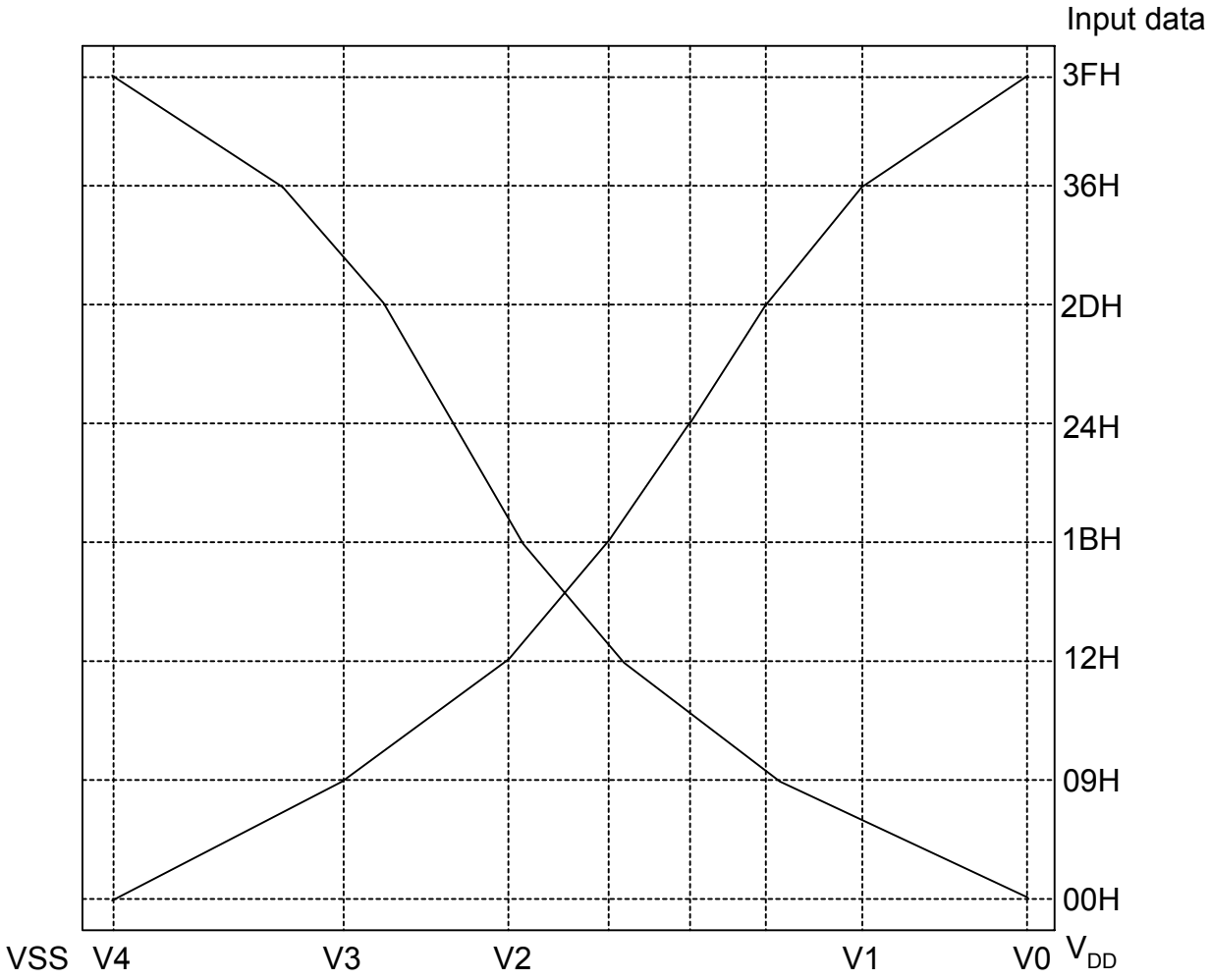
Note 5-3 : V_{DD} TYP.＝+3.3V

6. Operation Description

6.1 Relationship between input data and output voltage

The output voltage to panel is determined by the 6-bit digital input data.

γ correction characteristic curve :



The actual output voltage to panel for all the 64 input data at positive and negative polarity are shown on the following two pages.

Relationship between input data and output voltage to panel

Data	Positive polarity output voltage		Ω
00H	V0	V0	0
01H	V1	V1+ (V0-V1) × 2916 / 3645	729
02H	V2	V1+ (V0-V1) × 2187 / 3645	729
03H	V3	V1+ (V0-V1) × 1458 / 3645	729
04H	V4	V1+ (V0-V1) × 729 / 3645	729
05H	V5	V1	729
06H	V6	V2+ (V1-V2) × 9504 / 10233	729
07H	V7	V2+ (V1-V2) × 8775 / 10233	729
08H	V8	V2+ (V1-V2) × 8046 / 10233	729
09H	V9	V2+ (V1-V2) × 7317 / 10233	729
0AH	V10	V2+ (V1-V2) × 6809 / 10233	508
0BH	V11	V2+ (V1-V2) × 6301 / 10233	508
0CH	V12	V2+ (V1-V2) × 5793 / 10233	508
0DH	V13	V2+ (V1-V2) × 5285 / 10233	508
0EH	V14	V2+ (V1-V2) × 4777 / 10233	508
0FH	V15	V2+ (V1-V2) × 4269 / 10233	508
10H	V16	V2+ (V1-V2) × 3761 / 10233	508
11H	V17	V2+ (V1-V2) × 3253 / 10233	508
12H	V18	V2+ (V1-V2) × 2745 / 10233	508
13H	V19	V2+ (V1-V2) × 2440 / 10233	305
14H	V20	V2+ (V1-V2) × 2135 / 10233	305
05H	V21	V2+ (V1-V2) × 1830 / 10233	305
16H	V22	V2+ (V1-V2) × 1525 / 10233	305
17H	V23	V2+ (V1-V2) × 1220 / 10233	305
18H	V24	V2+ (V1-V2) × 915 / 10233	305
19H	V25	V2+ (V1-V2) × 610 / 10233	305
1AH	V26	V2+ (V1-V2) × 305 / 10233	305
1BH	V27	V2	305
1CH	V28	V3+ (V2-V3) × 4318 / 4572	254
1DH	V29	V3+ (V2-V3) × 4064 / 4572	254
1EH	V30	V3+ (V2-V3) × 3810 / 4572	254
1FH	V31	V3+ (V2-V3) × 3556 / 4572	254
20H	V32	V3+ (V2-V3) × 3302 / 4572	254
21H	V33	V3+ (V2-V3) × 3048 / 4572	254
22H	V34	V3+ (V2-V3) × 2794 / 4572	254
23H	V35	V3+ (V2-V3) × 2540 / 4572	254
24H	V36	V3+ (V2-V3) × 2286 / 4572	254
25H	V37	V3+ (V2-V3) × 2032 / 4572	254
26H	V38	V3+ (V2-V3) × 1778 / 4572	254
27H	V39	V3+ (V2-V3) × 1524 / 4572	254
28H	V40	V3+ (V2-V3) × 1270 / 4572	254
29H	V41	V3+ (V2-V3) × 1016 / 4572	254
2AH	V42	V3+ (V2-V3) × 762 / 4572	254
2BH	V43	V3+ (V2-V3) × 508 / 4572	254
2CH	V44	V3+ (V2-V3) × 254 / 4572	254
2DH	V45	V3	254
2EH	V46	V4+ (V3-V4) × 6237 / 6561	324
2FH	V47	V4+ (V3-V4) × 5913 / 6561	324
30H	V48	V4+ (V3-V4) × 5589 / 6561	324
31H	V49	V4+ (V3-V4) × 5265 / 6561	324
32H	V50	V4+ (V3-V4) × 4941 / 6561	324
33H	V51	V4+ (V3-V4) × 4617 / 6561	324
34H	V52	V4+ (V3-V4) × 4293 / 6561	324
35H	V53	V4+ (V3-V4) × 3969 / 6561	324
36H	V54	V4+ (V3-V4) × 3645 / 6561	324
37H	V55	V4+ (V3-V4) × 3240 / 6561	405
38H	V56	V4+ (V3-V4) × 2835 / 6561	405
39H	V57	V4+ (V3-V4) × 2430 / 6561	405
3AH	V58	V4+ (V3-V4) × 2025 / 6561	405
3BH	V59	V4+ (V3-V4) × 1620 / 6561	405
3CH	V60	V4+ (V3-V4) × 1215 / 6561	405
3DH	V61	V4+ (V3-V4) × 810 / 6561	405
3EH	V62	V4+ (V3-V4) × 405 / 6561	405
3FH	V63	V4	405

Data	Negative polarity output voltage		Ω
00H	V0’	V4	0
01H	V1’	V4+ (V3-V4) × 729 / 6561	729
02H	V2’	V4+ (V3-V4) × 1458 / 6561	729
03H	V3’	V4+ (V3-V4) × 2187 / 6561	729
04H	V4’	V4+ (V3-V4) × 2916 / 6561	729
05H	V5’	V4+ (V3-V4) × 3645 / 6561	729
06H	V6’	V4+ (V3-V4) × 4374 / 6561	729
07H	V7’	V4+ (V3-V4) × 5103 / 6561	729
08H	V8’	V4+ (V3-V4) × 5832 / 6561	729
09H	V9’	V3	729
0AH	V10’	V3+ (V2-V3) × 508 / 4572	508
0BH	V11’	V3+ (V2-V3) × 1016 / 4572	508
0CH	V12’	V3+ (V2-V3) × 1524 / 4572	508
0DH	V13’	V3+ (V2-V3) × 2032 / 4572	508
0EH	V14’	V3+ (V2-V3) × 2540 / 4572	508
0FH	V15’	V3+ (V2-V3) × 3048 / 4572	508
10H	V16’	V3+ (V2-V3) × 3556 / 4572	508
11H	V17’	V3+ (V2-V3) × 4064 / 4572	508
12H	V18’	V2	508
13H	V19’	V2+ (V1-V2) × 305 / 10233	305
14H	V20’	V2+ (V1-V2) × 610 / 10233	305
05H	V21’	V2+ (V1-V2) × 915 / 10233	305
16H	V22’	V2+ (V1-V2) × 1220 / 10233	305
17H	V23’	V2+ (V1-V2) × 1525 / 10233	305
18H	V24’	V2+ (V1-V2) × 1830 / 10233	305
19H	V25’	V2+ (V1-V2) × 2135 / 10233	305
1AH	V26’	V2+ (V1-V2) × 2440 / 10233	305
1BH	V27’	V2+ (V1-V2) × 2745 / 10233	305
1CH	V28’	V2+ (V1-V2) × 2999 / 10233	254
1DH	V29’	V2+ (V1-V2) × 3253 / 10233	254
1EH	V30’	V2+ (V1-V2) × 3507 / 10233	254
1FH	V31’	V2+ (V1-V2) × 3761 / 10233	254
20H	V32’	V2+ (V1-V2) × 4015 / 10233	254
21H	V33’	V2+ (V1-V2) × 4269 / 10233	254
22H	V34’	V2+ (V1-V2) × 4523 / 10233	254
23H	V35’	V2+ (V1-V2) × 4777 / 10233	254
24H	V36’	V2+ (V1-V2) × 5031 / 10233	254
25H	V37’	V2+ (V1-V2) × 5285 / 10233	254
26H	V38’	V2+ (V1-V2) × 5539 / 10233	254
27H	V39’	V2+ (V1-V2) × 5793 / 10233	254
28H	V40’	V2+ (V1-V2) × 6047 / 10233	254
29H	V41’	V2+ (V1-V2) × 6301 / 10233	254
2AH	V42’	V2+ (V1-V2) × 6555 / 10233	254
2BH	V43’	V2+ (V1-V2) × 6809 / 10233	254
2CH	V44’	V2+ (V1-V2) × 7063 / 10233	254
2DH	V45’	V2+ (V1-V2) × 7317 / 10233	254
2EH	V46’	V2+ (V1-V2) × 7641 / 10233	324
2FH	V47’	V2+ (V1-V2) × 7965 / 10233	324
30H	V48’	V2+ (V1-V2) × 8289 / 10233	324
31H	V49’	V2+ (V1-V2) × 8613 / 10233	324
32H	V50’	V2+ (V1-V2) × 8937 / 10233	324
33H	V51’	V2+ (V1-V2) × 9261 / 10233	324
34H	V52’	V2+ (V1-V2) × 9585 / 10233	324
35H	V53’	V2+ (V1-V2) × 9909 / 10233	324
36H	V54’	V1	324
37H	V55’	V1+ (V0-V1) × 405 / 3645	405
38H	V56’	V1+ (V0-V1) × 810 / 3645	405
39H	V57’	V1+ (V0-V1) × 1215 / 3645	405
3AH	V58’	V1+ (V0-V1) × 1620 / 3645	405
3BH	V59’	V1+ (V0-V1) × 2025 / 3645	405
3CH	V60’	V1+ (V0-V1) × 2430 / 3645	405
3DH	V61’	V1+ (V0-V1) × 2835 / 3645	405
3EH	V62’	V1+ (V0-V1) × 3240 / 3645	405
3FH	V63’	V0	405

6.2 Digital RGB data input format

For digital RGB input data format, both SYNC. mode and DE mode are supported. If DEN signal is fixed low, SYNC. mode is used. otherwise , DE mode is used.

6.3 To prevent the device from damage due to latch-up, the power ON/OFF sequence shown below must be followed.

Power ON : V_{DD}, V_{DDA} → V_{EE} → input signals → V_{GH}

Power OFF : V_{GH} → input signals → V_{EE} → V_{DD}, V_{DDA}

7. Register Description

7.1 Function Control Register (R00h) :

D7	D6	D5	D4	D3	D2	D1	D0
COM	RSTB0	STBYB	XAO	VSET	NPC	UID	RIL
0	1	1	1	1	1	0	1

RIL : Control the shift direction of Source Driver. (Right or Left)

If RIL = "H" → Normal Shift. S1→S2→S3→……. →S479→S480

If RIL = "L" → Reverse Shift. S480→S479→……..→S3→S2→S1

UID : Control the scan direction of Gate Driver. (Up or Down)

If UID = "L" → Normal scan. G1→G2→G3→……. →G239→G240

If UID = "H" → Reverse scan. G240→G239→……..→G3→G2→G1

NPC : Control the video signal.

If NPC = "H" → NTSC

If NPC = "L" → PAL

VSET : Control the gamma correction voltage is generated internally

XAO :

If XAO = "H" → Gate driver in normal operation.

If XAO = "L" → Fixed gate driver output to high.

STBYB : Standby mode. Low enable.

If STBYB enable , stop the analog power.

(1) Source Driver : OPA

(2) Bandgap reference

RSTB0 : Reset all registers. Low enable.

COM :

If COM = "L" → The V_{COM} circuit is generated internally.

If COM = "H" → The V_{COM} circuit is generated externally and V_{COM} input pin is used.

7.2 Data Control Register (R01h) :

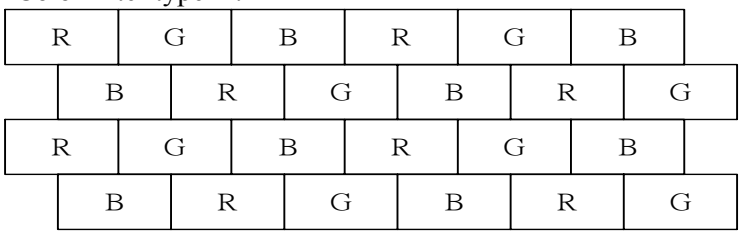
D7	D6	D5	D4	D3	D2	D1	D0
VSDPOL	HSDPOL	SEL1	SEL0	Reserve	DITH	CF2	CF1
0	1	0	0	0	0	1	1

CF2/CF1 :

If Digital RGB input mode is used, input data sequence must be considered according to different color filter type.

→CF2/CF1 = “H, H”→Delta type

Color filter type 1 :



Data sequence :

Scan direction	UID	Low	Low	High	High
Shift direction	RIL	High	Low	High	Low
Data sequence	Even line	BRG	GRB	RGB	BGR
	Odd line	RGB	BGR	BRG	GRB

If CCIR 601/656 input mode is used, the input data sequence is the same and only define as the color filter type.

DITH : Dithering on or off setting

If DITH = “H”→Dithering on, 8 bit resolution.

If DITH = ”L”→Dithering off, 6 bit resolution and truncation last 2 bits of data.

SEL1/SEL0 :

If SEL1/SEL0 = “H, H”→CCIR656

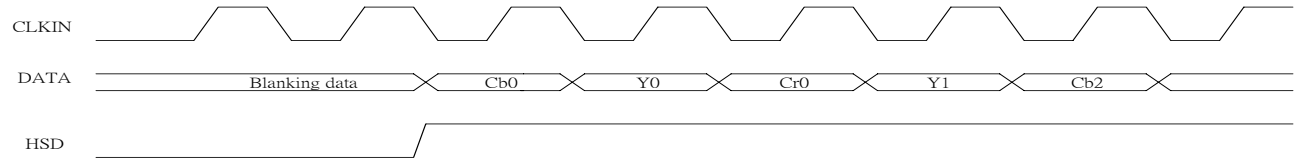
If SEL1/SEL0 = “H, L”→CCIR601

If SEL1/SEL0 = “L, H”→RGB

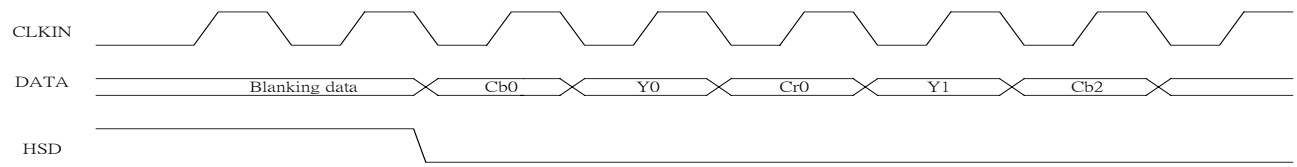
If SEL1/SEL0 = “L, L”→RGB

HSDPOL : define the signal polarity of HSD in CCIR601 input mode

If HSDPOL = "H" -> HSD is high pulse for data



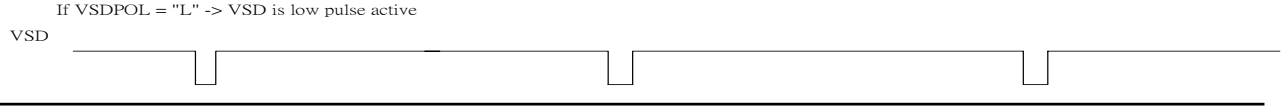
If HSDPOL = "L" -> HSD is low pulse for data valid



VSDPOL : define the signal polarity of VSD in CCIR601 input mode

If VSDPOL = "H" -> VSD is high pulse active

If VSDPOL = "L" -> VSD is low pulse active



7.3 Source Driver Start Pulse Pixel Position Control Register (R02h):

D7	D6	D5	D4	D3	D2	D1	D0
Reserve	Reserve	Reserve	STHST4	STHST3	STHST2	STHST1	STHST0
0	0	0	0	0	0	0	0

STHST〔4：0〕：Used to set the Source Driver Start Pulse Pixel Position. This setting is only effective when DEN is fixed low. The step unit is one pixel clock, not CLKIN.

STHST4	STHST3	STHST2	STHST1	STHST0	Pixel Step
1	0	0	0	0	-16
1	0	0	0	1	-15
1	0	0	1	0	-14
1	0	0	1	1	-13
1	0	1	0	0	-12
1	0	1	0	1	-11
1	0	1	1	0	-10
1	0	1	1	1	-9
1	1	0	0	0	-8
1	1	0	0	1	-7
1	1	0	1	0	-6
1	1	0	1	1	-5
1	1	1	0	0	-4
1	1	1	0	1	-3
1	1	1	1	0	-2
1	1	1	1	1	-1
0	0	0	0	0	0
0	0	0	0	1	+1
0	0	0	1	0	+2
0	0	0	1	1	+3
0	0	1	0	0	+4
0	0	1	0	1	+5
0	0	1	1	0	+6
0	0	1	1	1	+7
0	1	0	0	0	+8
0	1	0	0	1	+9
0	1	0	1	0	+10
0	1	0	1	1	+11
0	1	1	0	0	+12
0	1	1	0	1	+13
0	1	1	1	0	+14
0	1	1	1	1	+15

7.4 Gate Driver Start Pulse Position Control Register (R03h):

D7	D6	D5	D4	D3	D2	D1	D0
Reserve	Reserve	Reserve	Reserve	STVST3	STVST2	STVST1	STVST0
0	0	0	0	0	0	0	0

STHST〔3：0〕：Used to set the Gate Start Position. This setting is only effective when DEN is fixed low.

STHST3	STHST2	STHST1	STHST0	Line Step
1	0	0	0	-8
1	0	0	1	-7
1	0	1	0	-6
1	0	1	1	-5
1	1	0	0	-4
1	1	0	1	-3
1	1	1	0	-2
1	1	1	1	-1
0	0	0	0	0
0	0	0	1	+1
0	0	1	0	+2
0	0	1	1	+3
0	1	0	0	+4
0	1	0	1	+5
0	1	1	0	+6
0	1	1	1	+7

7.5 VCOM Voltage High Level Control Register (R04h)

D7	D6	D5	D4	D3	D2	D1	D0
Reserve	Reserve	Reserve	VCOMH4	VCOMH3	VCOMH2	VCOMH1	VCOMH0
0	0	0	0	0	1	0	1

VCOMH[4:0] : Used to set the VCOMH voltage. The VCOMH voltage must not exceed the VDDA-0.1V voltage.

VCOMH Voltage setting

VCMH4	VCMH3	VCMH2	VCMH1	VCMH0	VCOMH Voltage
1	0	0	0	0	Setting Inhibited
1	0	0	0	1	Setting Inhibited
1	0	0	1	0	Setting Inhibited
1	0	0	1	1	Setting Inhibited
1	0	1	0	0	Setting Inhibited
1	0	1	0	1	Setting Inhibited
1	0	1	1	0	VDDA × 0.60
1	0	1	1	1	VDDA × 0.62
1	1	0	0	0	VDDA × 0.64
1	1	0	0	1	VDDA × 0.66
1	1	0	1	0	VDDA × 0.68
1	1	0	1	1	VDDA × 0.70
1	1	1	0	0	VDDA × 0.72
1	1	1	0	1	VDDA × 0.74
1	1	1	1	0	VDDA × 0.76
1	1	1	1	1	VDDA × 0.78
0	0	0	0	0	VDDA × 0.80
0	0	0	0	1	VDDA × 0.82
0	0	0	1	0	VDDA × 0.84
0	0	0	1	1	VDDA × 0.86
0	0	1	0	0	VDDA × 0.88
0	0	1	0	1	VDDA × 0.9 (default)
0	0	1	1	0	VDDA × 0.92
0	0	1	1	1	VDDA × 0.94
0	1	0	0	0	VDDA × 0.96
0	1	0	0	1	VDDA × 0.98
0	1	0	1	0	Setting Inhibited
0	1	0	1	1	Setting Inhibited
0	1	1	0	0	Setting Inhibited
0	1	1	0	1	Setting Inhibited
0	1	1	1	0	Setting Inhibited
0	1	1	1	1	Setting Inhibited

7.6 VCOM Voltage Swing Control Register (R05h)

D7	D6	D5	D4	D3	D2	D1	D0
Reserve	Reserve	VCOMA4	VCOMA3	VCOMA2	VCOMA1	VCOMA0	VCOMG
0	0	0	1	0	1	0	1

VCOMA [4:0]: Used to set the VCOM swing. The swing must not exceed 6V.

VCOMG :When VCOMG = 0, the low-level voltage of VCOML Is fixed to GND level.

When VCOMG = 1, the low-level voltage of VCOML can be set to following value.

VCOM Swing Voltage setting

VCMA4	VCMA3	VCMA2	VCMA1	VCMA0	VCOM Swing Voltage
1	0	0	0	0	Setting Inhibited
1	0	0	0	1	Setting Inhibited
1	0	0	1	0	Setting Inhibited
1	0	0	1	1	Setting Inhibited
1	0	1	0	0	Setting Inhibited
1	0	1	0	1	Setting Inhibited
1	0	1	1	0	VDDA × 0.80
1	0	1	1	1	VDDA × 0.82
1	1	0	0	0	VDDA × 0.84
1	1	0	0	1	VDDA × 0.86
1	1	0	1	0	VDDA × 0.88
1	1	0	1	1	VDDA × 0.90
1	1	1	0	0	VDDA × 0.92
1	1	1	0	1	VDDA × 0.94
1	1	1	1	0	VDDA × 0.96
1	1	1	1	1	VDDA × 0.98
0	0	0	0	0	VDDA × 1.00
0	0	0	0	1	VDDA × 1.02
0	0	0	1	0	VDDA × 1.04
0	0	0	1	1	VDDA × 1.06
0	0	1	0	0	VDDA × 1.08
0	0	1	0	1	VDDA × 1.10
0	0	1	1	0	VDDA × 1.12
0	0	1	1	1	VDDA × 1.14
0	1	0	0	0	VDDA × 1.16
0	1	0	0	1	VDDA × 1.18
0	1	0	1	0	VDDA × 1.20 (default)
0	1	0	1	1	Setting Inhibited
0	1	1	0	0	Setting Inhibited
0	1	1	0	1	Setting Inhibited
0	1	1	1	0	Setting Inhibited
0	1	1	1	1	Setting Inhibited

7.7 Gamma reference voltage selection register ｜ (R06h) :

D7	D6	D5	D4	D3	D2	D1	D0
GAM13	GAM12	GAM11	GAM10	GAM03	GAM02	GAM01	GAM00
0	0	1	0	0	1	1	0

GAM0[3:0] : Used to set gamma reference voltage V0.

GAM03	GAM02	GAM01	GAM00	V0 voltage
0	0	0	0	VDDA × (7/8 + 6/64)
0	0	0	1	VDDA × (7/8 + 5/64)
0	0	1	0	VDDA × (7/8 + 4/64)
0	0	1	1	VDDA × (7/8 + 3/64)
0	1	0	0	VDDA × (7/8 + 2/64)
0	1	0	1	VDDA × (7/8 + 1/64)
0	1	1	0	VDDA × 7/8(default)
0	1	1	1	VDDA × (7/8 - 1/64)
1	0	0	0	VDDA × (7/8 - 2/64)
1	0	0	1	VDDA × (7/8 - 3/64)
1	0	1	0	VDDA × (7/8 - 4/64)
1	0	1	1	VDDA × (7/8 - 5/64)
1	1	0	0	VDDA × (7/8 - 6/64)
1	1	0	1	VDDA × (7/8 - 7/64)
1	1	1	0	VDDA × (7/8 - 8/64)
1	1	1	1	VDDA × (7/8 - 9/64)

GAM1[3:0] : Used to set gamma reference voltage V1.

GAM13	GAM12	GAM11	GAM10	V1 voltage
0	0	0	0	VDDA × (11/16 + 7/64)
0	0	0	1	VDDA × (11/16 + 6/64)
0	0	1	0	VDDA × (11/16 + 5/64) (default)
0	0	1	1	VDDA × (11/16+ 4/64)
0	1	0	0	VDDA × (11/16 + 3/64)
0	1	0	1	VDDA × (11/16 + 2/64)
0	1	1	0	VDDA × (11/16 + 1/64)
0	1	1	1	VDDA × 11/16
1	0	0	0	VDDA × (11/16 – 1/64)
1	0	0	1	VDDA × (11/16 – 2/64)
1	0	1	0	VDDA × (11/16 – 3/64)
1	0	1	1	VDDA × (11/16 – 4/64)
1	1	0	0	VDDA × (11/16 - 5/64)
1	1	0	1	VDDA × (11/16 – 6/64)
1	1	1	0	VDDA × (11/16 – 7/64)
1	1	1	1	VDDA × (11/16 - 8/64)

7.8 Gamma reference voltage selection register ‖ (R07h) :

D7	D6	D5	D4	D3	D2	D1	D0
GAM33	GAM32	GAM31	GAM30	GAM23	GAM22	GAM21	GAM20
0	1	1	1	0	1	1	1

GAM2[3:0] : Used to set gamma reference voltage V2.

GAM23	GAM22	GAM21	GAM20	V2 voltage
0	0	0	0	VDDA × (29/64 + 7/64)
0	0	0	1	VDDA × (29/64 + 6/64)
0	0	1	0	VDDA × (29/64 + 5/64)
0	0	1	1	VDDA × (29/64 + 4/64)
0	1	0	0	VDDA × (29/64 + 3/64)
0	1	0	1	VDDA × (29/64 + 2/64)
0	1	1	0	VDDA × (29/64 + 1/64)
0	1	1	1	VDDA × 29/64 (default)
1	0	0	0	VDDA × (29/64 - 1/64)
1	0	0	1	VDDA × (29/64 - 2/64)
1	0	1	0	VDDA × (29/64 - 3/64)
1	0	1	1	VDDA × (29/64 - 4/64)
1	1	0	0	VDDA × (29/64 - 5/64)
1	1	0	1	VDDA × (29/64 - 6/64)
1	1	1	0	VDDA × (29/64 - 7/64)
1	1	1	1	VDDA × (29/64 - 8/64)

GAM3[3:0] : Used to set gamma reference voltage V3.

GAM33	GAM32	GAM31	GAM30	V3 voltage
0	0	0	0	VDDA × (5/16 + 7/64)
0	0	0	1	VDDA × (5/16 + 6/64)
0	0	1	0	VDDA × (5/16 + 5/64)
0	0	1	1	VDDA × (5/16 + 4/64)
0	1	0	0	VDDA × (5/16 + 3/64)
0	1	0	1	VDDA × (5/16 + 2/64)
0	1	1	0	VDDA × (5/16 + 1/64)
0	1	1	1	VDDA × 5/16 (default)
1	0	0	0	VDDA × (5/16 - 1/64)
1	0	0	1	VDDA × (5/16 - 2/64)
1	0	1	0	VDDA × (5/16 - 3/64)
1	0	1	1	VDDA × (5/16 - 4/64)
1	1	0	0	VDDA × (5/16 - 5/64)
1	1	0	1	VDDA × (5/16 - 6/64)
1	1	1	0	VDDA × (5/16 - 7/64)
1	1	1	1	VDDA × (5/16 - 8/64)

7.9 Gamma reference voltage selection register III (R08h):

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	GAM43	GAM42	GAM41	GAM40
0	0	0	0	1	0	1	0

GAM4〔3：0〕：used to set gamma reference voltage V4.

GAM43	GAM42	GAM41	GAM40	V4 voltage
0	0	0	0	VDDA*(1/8+9/64)
0	0	0	1	VDDA*(1/8+8/64)
0	0	1	0	VDDA*(1/8+7/64)
0	0	1	1	VDDA*(1/8+6/64)
0	1	0	0	VDDA*(1/8+5/64)
0	1	0	1	VDDA*(1/8+4/64)
0	1	1	0	VDDA*(1/8+3/64)
0	1	1	1	VDDA*(1/8+2/64)
1	0	0	0	VDDA*(1/8+1/64)
1	0	0	1	VDDA*1/8
1	0	1	0	VDDA*(1/8-1/64) (default)
1	0	1	1	VDDA*(1/8-2/64)
1	1	0	0	VDDA*(1/8-3/64)
1	1	0	1	VDDA*(1/8-4/64)
1	1	1	0	VDDA*(1/8-5/64)
1	1	1	1	VDDA*(1/8-6/64)

7.10 Block Control Register (R09h):

D7	D6	D5	D4	D3	D2	D1	D0
Reserve	Reserve	Reserve	Reserve	Reserve	Reserve	PINV	PWM
0	0	0	0	0	0	1	0

PWM: PWM function on or off setting

If PWM = “H” → PWM function is enable.

If PWM = “L” → PWM function is disable.

PINV: Control the polarity of internal generated V_{COM} signal

If PINV = “H” → V_{COM} is the same phase with POL.

If PINV = “L” → V_{COM} is reverse polarity of POL.

7.11 Source Driver Start Pulse Dot Position Control Register (R0Ah):

D7	D6	D5	D4	D3	D2	D1	D0
Reserve	Reserve	Reserve	STHD4	STHD3	STHD2	STHD1	STHD0
0	0	0	0	0	0	0	0

STHD〔4：0〕：Used to set the Source Start Dot Position. This setting is only effective when DEN is fixed low. The step unit is one input clock, CLKIN.

STHD4	STHD3	STHD2	STHD1	STHD0	Pixel Step
1	0	0	0	0	-16
1	0	0	0	1	-15
1	0	0	1	0	-14
1	0	0	1	1	-13
1	0	1	0	0	-12
1	0	1	0	1	-11
1	0	1	1	0	-10
1	0	1	1	1	-9
1	1	0	0	0	-8
1	1	0	0	1	-7
1	1	0	1	0	-6
1	1	0	1	1	-5
1	1	1	0	0	-4
1	1	1	0	1	-3
1	1	1	1	0	-2
1	1	1	1	1	-1
0	0	0	0	0	0
0	0	0	0	1	+1
0	0	0	1	0	+2
0	0	0	1	1	+3
0	0	1	0	0	+4
0	0	1	0	1	+5
0	0	1	1	0	+6
0	0	1	1	1	+7
0	1	0	0	0	+8
0	1	0	0	1	+9
0	1	0	1	0	+10
0	1	0	1	1	+11
0	1	1	0	0	+12
0	1	1	0	1	+13
0	1	1	1	0	+14
0	1	1	1	1	+15

8. Absolute Maximum Ratings

The followings are maximum values , which if exceeded, may cause faulty operation or damage to the unit.

$V_{SS}=V_{SSA}=0$ V，Ta = 25 ℃

Parameter		Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage For Source Driver		V_{DD}	-0.3	+7.0	V	
		V_{DDA}	-0.3	+7.0	V	
	H Level	V_{GH}	-0.3	+32.0	V	
	L Level	V_{GL}	-22.0	+0.3	V	
		V_{GH}-V_{GL}	-0.3	+45.0	V	
Input Signal voltage		V_{IN}	-0.3	V_{DD}+0.3	V	Note 8-1
Storage Temperature			-20	+70	℃	
Operation Temperature			0	+60	℃	Note 8-2

Notes 8-1 : Digital image data input Voltage.

Notes 8-2 : Operating Temperature define that contrast, response time, other display optical character are Ta=+25℃.

9. Electrical Characteristics

9-1) Operating Condition

$V_{SS}=V_{SSA}=0$ V，Ta = 25 ℃

Parameter		Symbol	MIN.	Typ.	MAX.	Unit	Remark
Supply Voltage For Source Driver	Analog	V_{DDA}	+3.8	+5.0	+5.5	V	
	Digital	V_{DD}	+3.0	+3.3	+3.6	V	
Supply Voltage For Gate Driver	H level	V_{GH}	+10	-	+30	V	
	L level	V_{GL}	-17	-	-5	V	DC Component of V_{GL}
		V_{GH}-V_{GL}	+15	-	+40	V_{P-P}	AC Component of V_{GL}
Digital input voltage	H level	V_{IH}	0.7VDD	-	VDD	V	
	L level	V_{IL}	0	-	0.3VDD	V	
V_{COM}		$V_{COM\ AC}$	-	+6.0	-	V_{P-P}	AC Component of V_{COM}
		$V_{COM\ DC}$	-	TBD	-	V	DC Component of V_{COM} Note 9-1

Note 9-1 : PVI strongly suggests that the $V_{COM\ DC}$ level shall be adjustable , and the adjustable level range is TBDV±1V , every module's $V_{COM\ DC}$ level shall be carefully adjusted to show a best image performance.

9-2) Recommended driving condition for LED backlight

GND = 0 V， Ta = 25 ℃

Parameter	Symbol	Min	TYP	MAX	Unit	Remark
Supply voltage of LED backlight	V_{LED}	TBD	TBD	TBD	V	I_L = 20 mA
Supply current of LED backlight	I_{LED}		20		mA	Note 9-2
Backlight Power Consumption	P_{LED}	TBD	TBD	TBD	mW	Note 9-3

Note 9-2 : LED B/L applied information , please refer to the appendix at the end .

Note 9-3 : $P_{LED} = V_{LED} * I_{LED}$.

9-3) Power Consumption

Parameter	Symbol	Conditions	TYP.	MAX.	Unit	Remark
Supply current for Gate Driver (Hi level)	I_{GH}	V_{GH} =+15V	TBD	TBD	mA	
Supply current for Gate Driver (Low level)	I_{GL}	V_{GL} =-15V	TBD	TBD	mA	V_{GL} center voltage
Supply current for Source Driver(Digital)	I_{DD}	V_{DD}=+3.3V	TBD	TBD	mA	
Supply current for Source Driver(Analog)	I_{DDA}	V_{DDA}=+5V	TBD	TBD	mA	
LCD Panel Power Consumption	-	-	TBD	TBD	mW	
Backlight Power Consumption	P_{LED}		TBD	TBD	mW	
Total Power Consumption			TBD	TBD	mW	

9-4) Timing Characteristics Of Input Signals

9.4.1 Digital RGB interface

Characteristics		Symbol	Min.	Typ.	Max.	Unit	Remark
CLK period		T_{OSC}	94	104	114	ns	Note 9-4
Data setup time		T_{SU}	12	-	-	ns	
Data hold time		T_{HD}	12	-	-	ns	
HSD period		T_H	61.5	63.5	65.5	us	
HSD pulse width		T_{HS}	4	4.7	5.4	us	
HSD rising time		T_{Cr}	-	-	700	ns	
HSD falling time		T_{Cf}	-	-	300	ns	
VSD pulse width		T_{VS}	1	3	5	T_H	
VSD rising time		T_{Vr}	-	-	700	ns	
VSD falling time		T_{Vf}	-	-	1.5	us	
HSD falling to VSD falling time for odd field		T_{HVO1}	0.3	-	-	us	
VSD falling to HSD rising time for odd field		T_{HVO2}	1	-	-	us	
HSD rising to VSD falling time for even field		T_{HVE}	1	-	-	us	
VSD-DEN time	NTSC	T_{VSE}	-	15	-	T_H	
	PAL			24			
HSD-DEN time		T_{HE}	75	-	120	T_{OSC}	
DEN pulse width		T_{EP}	-	480	-	T_{OSC}	
VSD period	NTSC	-	-	262.5	-	T_H	
	PAL	-	-	312.5	-	T_H	

Note 9-4 : When SYNC mode is used, the CLK period start from 106 after HSD falling

9.4.2 CCIR601 Interface

Characteristics		Symbol	Min.	Typ.	Max.	Unit	Remark
CLK period		T_{OSC}	-	37	-	ns	
Data setup time		T_{SU}	12	-	-	ns	
Data hold time		T_{HD}	12	-	-	ns	
HSD data blanking pulse width	NTSC	T_{HL}	-	276	-	T_{OSC}	
	PAL	T_{HL}	-	288	-	T_{OSC}	

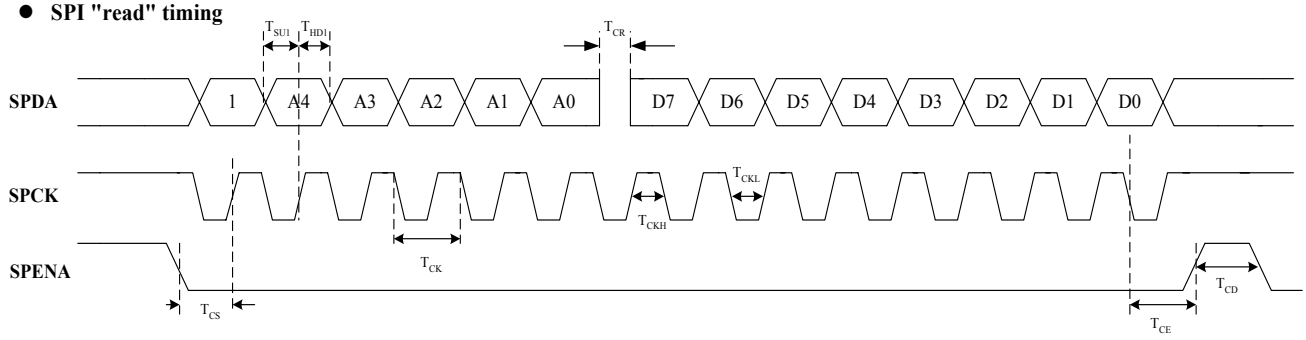
9.4.3 CCIR656 Interface

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
CLK period	T_{OSC}	-	37	-	ns	
Data setup time	T_{SU}	12	-	-	ns	
Data hold time	T_{HD}	12	-	-	ns	

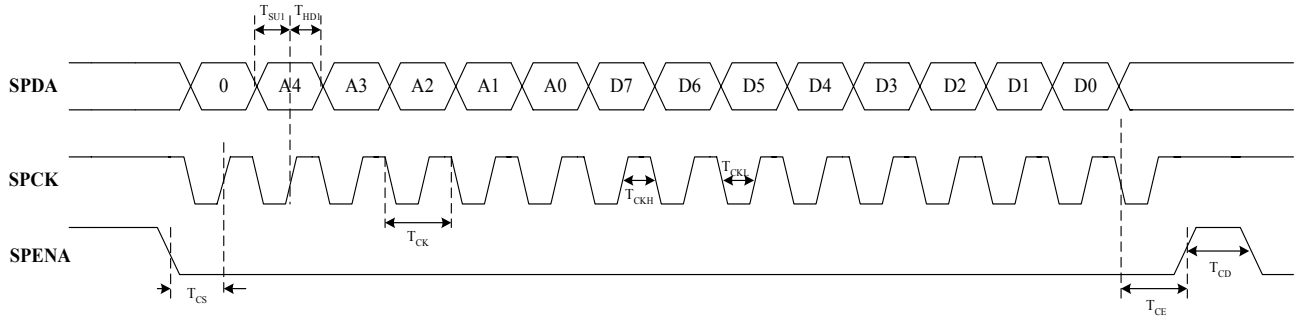
9-6) Timing Characteristics Of SPI

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
SPCK period	T_{CK}	60	-	-	ns	
SPCK high width	T_{CKH}	30	-	-	ns	
SPCK low width	T_{CKL}	30	-	-	ns	
Data setup time	T_{SU1}	12	-	-	ns	
Data hold time	T_{HD1}	12	-	-	ns	
SPENA to SPCK setup time	T_{CS}	20	-	-	ns	
SPENA to SPDA hold time	T_{CE}	20	-	-	ns	
SPENA high pulse width	T_{CD}	50	-	-	ns	
SPDA output latency	T_{CR}	-	1/2	-	T_{CK}	

- **SPI "read" timing**



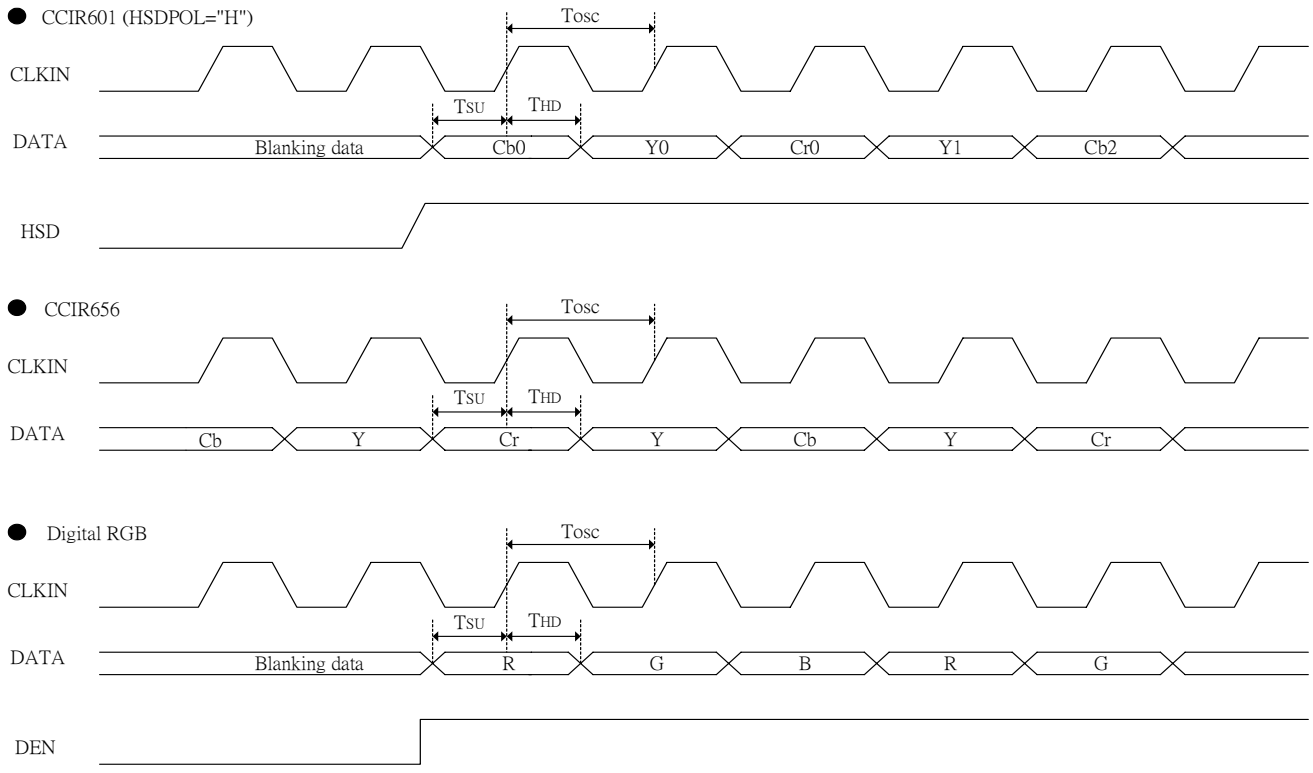
- **SPI "write" timing**



10. Waveform

10.1 Timing Controller Timing Chart

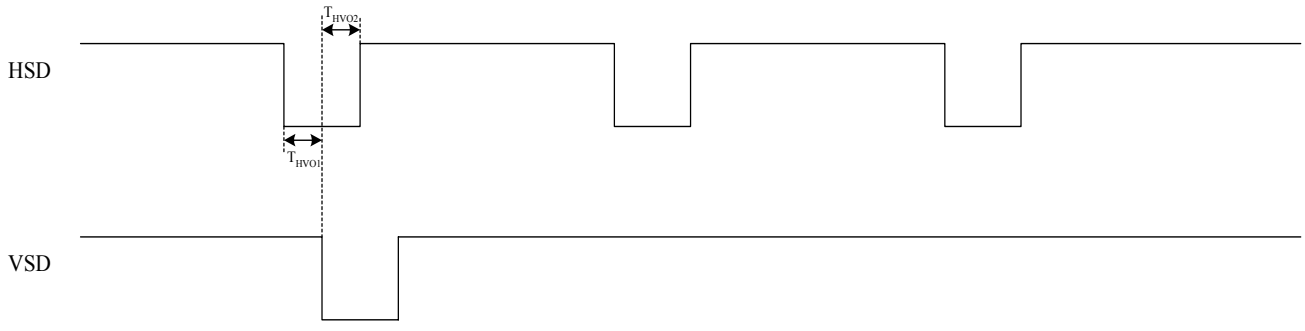
10.1.1 Clock and Data waveform



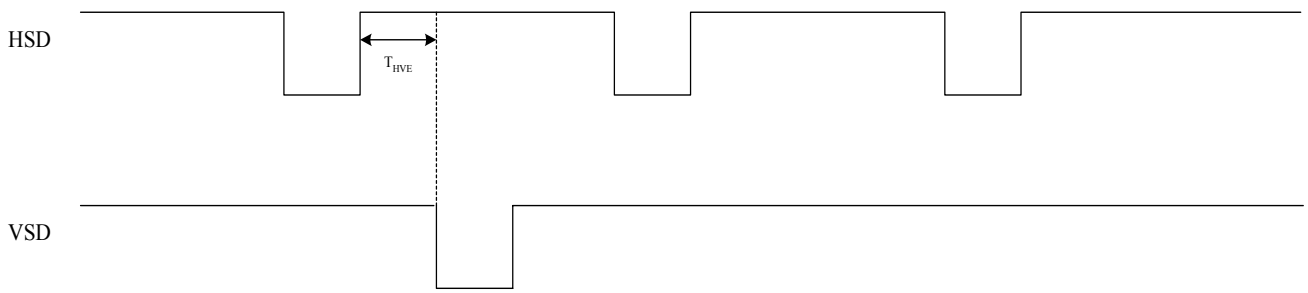
10.1.2 Digital RGB timing waveform

10.1.2.1 HSD and VSD timing relationship

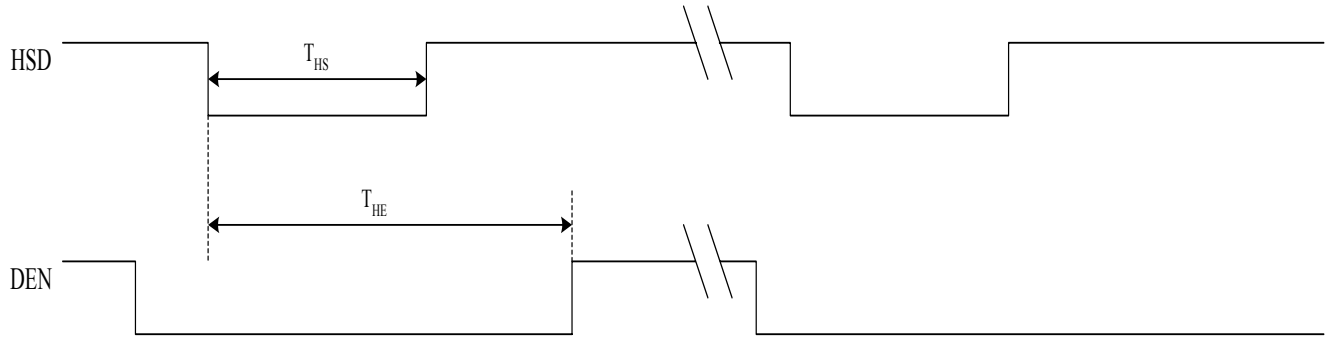
- **Odd field**



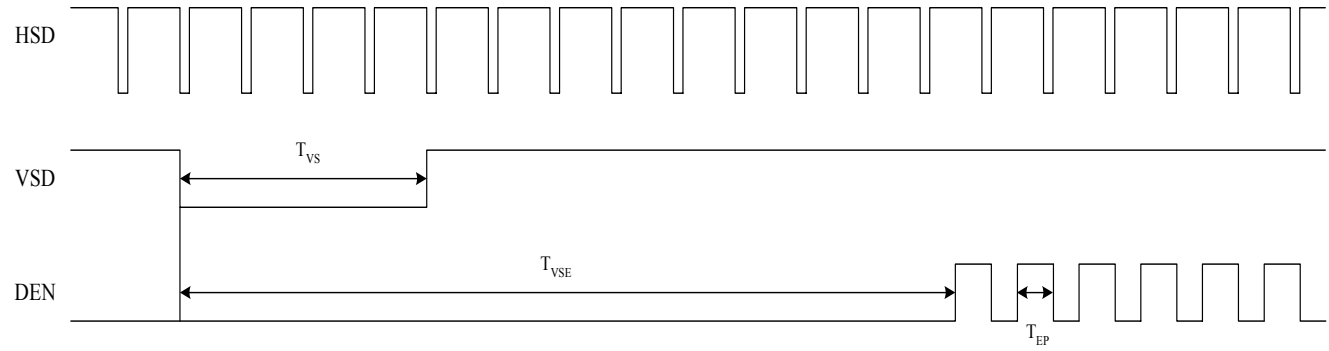
- **Even field**



10.1.2.2 HSD and DEN timing relationship

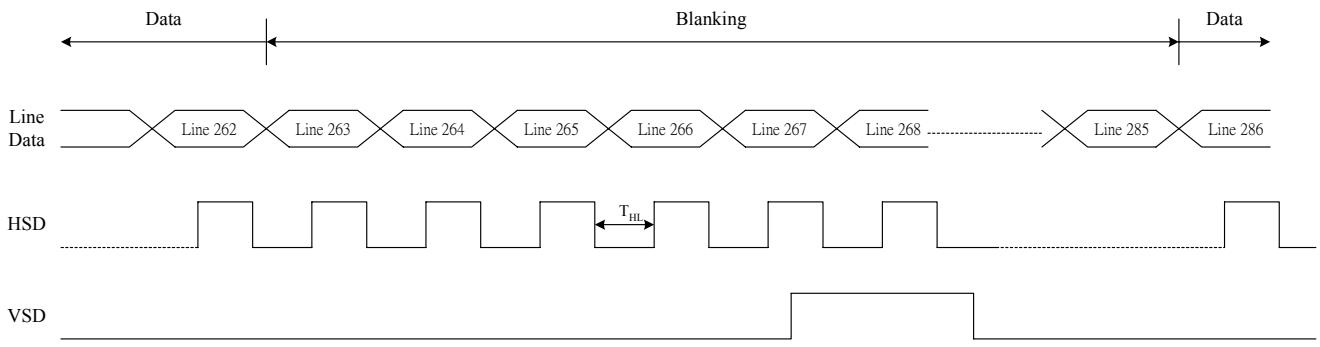


10.1.2.3 HSD, VSD and DEN timing relationship

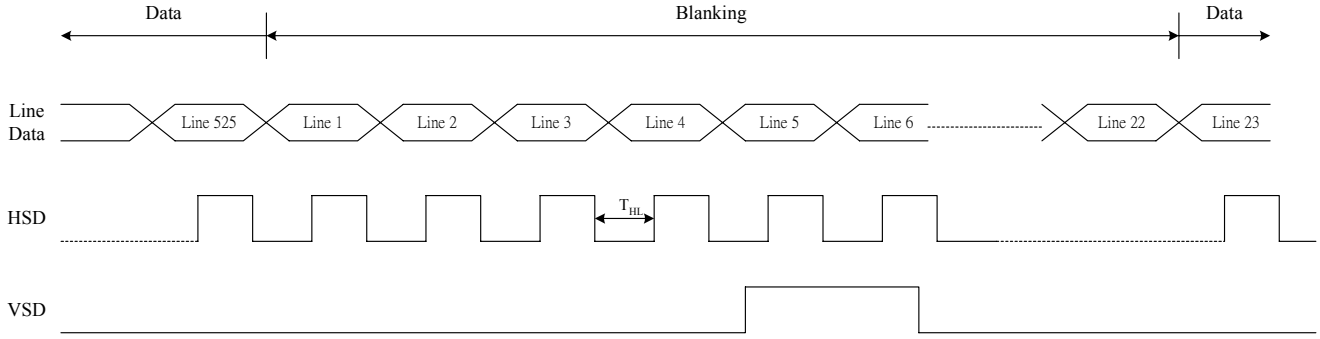


10.1.3 CCIR601 timing waveform

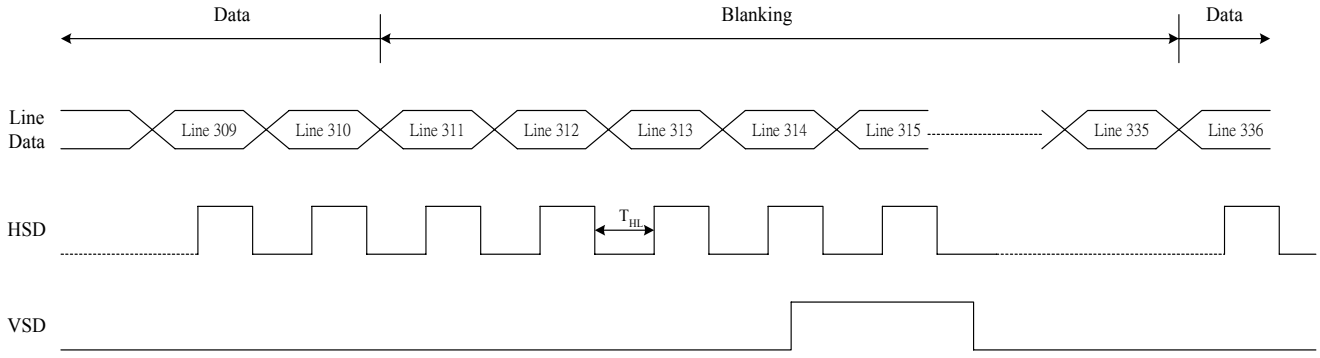
- NTSC Mode , Even field (HSDPOL="H",VSDPOL="H")



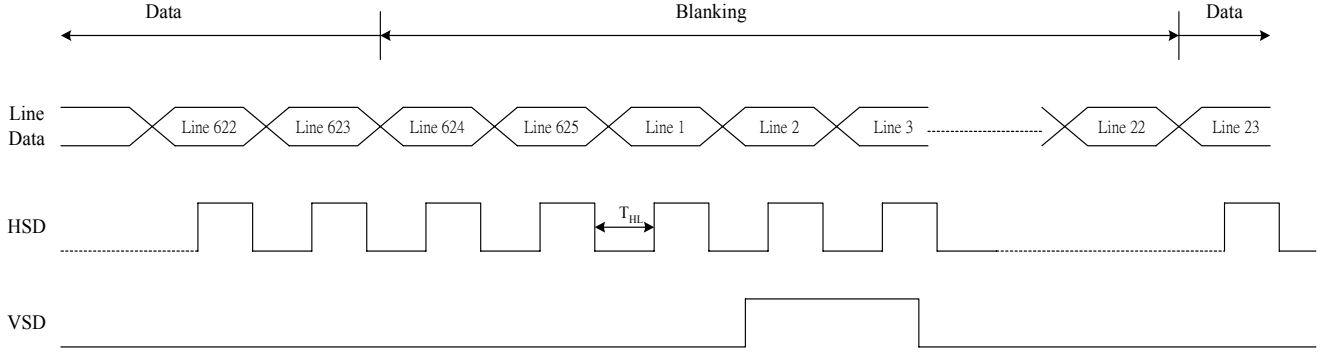
- NTSC Mode , Odd field (HSDPOL="H",VSDPOL="H")



- PAL Mode , Even field (HSDPOL="H",VSDPOL="H")



- PAL Mode , Odd field (HSDPOL="H",VSDPOL="H")



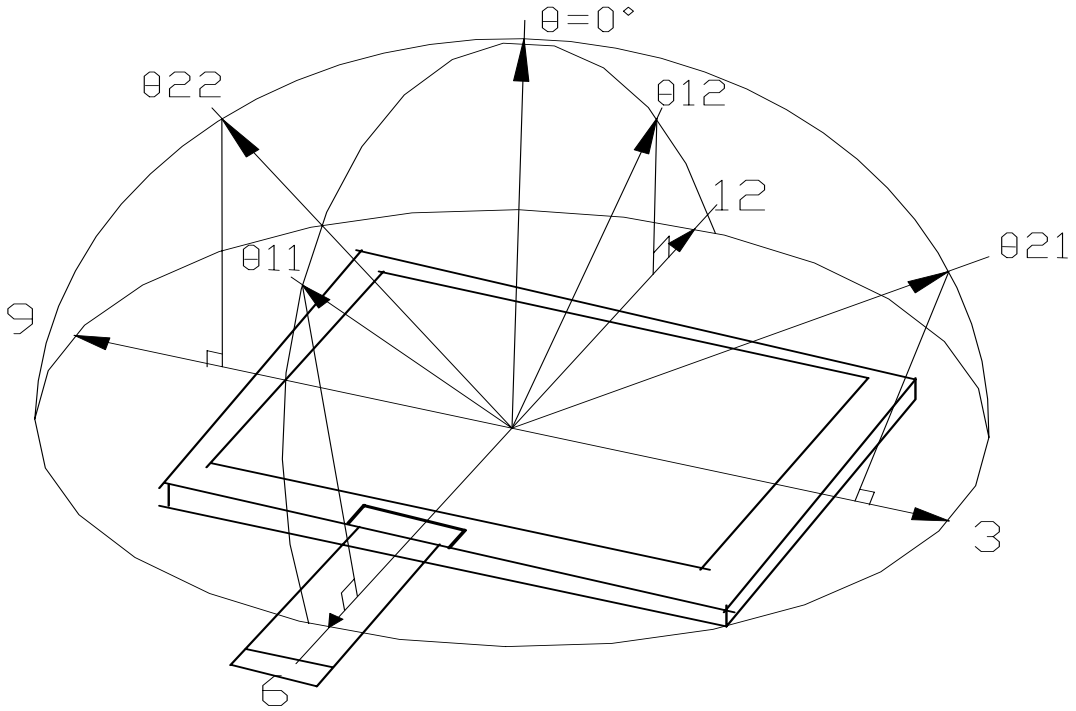
11. Optical Characteristics

11-1) Specification:

Ta = 25℃

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ 21, θ 22	CR≧10	45	50	---	deg	Note 11-1
	Vertical	θ 11		30	35	---	deg	
		θ 12		10	15	---	deg	
Contrast Ratio		CR	At optimized Viewing angle	200	350	---		Note 11-2
Response time	Rise	Tr	θ =0°	---	15	30	ms	Note 11-4
	Fall	Tf		---	25	50	ms	
Uniformity		U		TBD	TBD		%	
Brightness				TBD	TBD		cd/㎡	Note 10-2
White Chromaticity		x	θ =0°	0.28	0.31	0.34		Note 11-3
		y	θ =0°	0.30	0.33	0.36		
LED Life Time Ta=25℃					10000		hrs	

Note 11-1 : The definitions of viewing angles

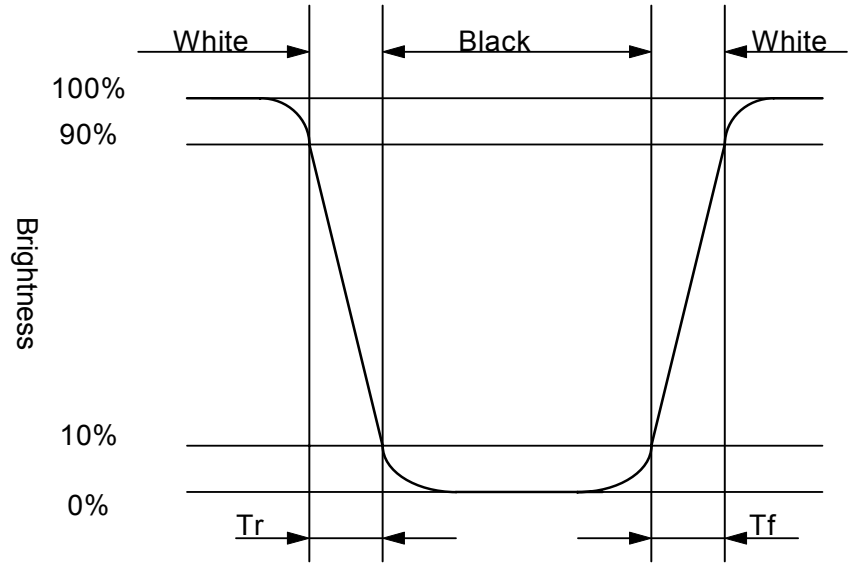


Note 11-2 : CR = $\frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$

Contrast Ratio is measured in optimum common electrode voltage.

Note 11-3 : Topcon BM-7(fast) luminance meter 1.0° field of view is used in the testing (use PVI backlight after 10 minutes operating).

Note 11-4 : The definition of response time :



12. Handling Cautions

12-1) Mounting of module

a) Please power off the module when you connect the input/output connector.

b) Please connect the ground pattern surely. If the connection is not perfect, some following problems may happen possibly.

1.The noise from the backlight unit will increase.

2.In some cases a part of module will heat.

c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.

d) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

12-2) Precautions in mounting

a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.

b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.

c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.

d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

12-3) Others

a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.

b) Store the module at a room temperature place.

c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.

d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.

e) Observe all other precautionary requirements in handling general electronic components.

13. Reliability Test

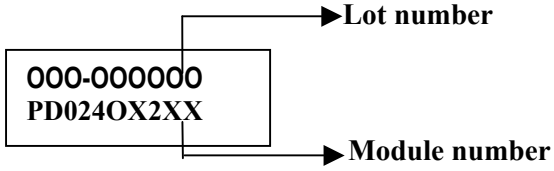
No	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +70℃, 240 hrs
2	Low Temperature Storage Test	Ta = -20℃, 240 hrs
3	Low Temperature Operation Test	Ta = 0℃, 240 hrs
4	High Temperature & High Humidity Operation Test	Ta = +50℃, 80%RH, 240 hrs
5	Thermal Cycling Test (non-operating)	-20℃ ← → +70℃ , 200 Cycles 30 min 30 min
6	Vibration test (non-operating)	Frequency : 10 ~ 55Hz Amplitude : 1mm , sweep time : 11 mins Test period : 6 cycles for each direction of X,Y, Z
7	Shock Test(non-operating)	100G , 6ms , 3cycles for each direction of X,Y,Z
8	Electrostatic Discharge Test (non-operating)	200pF, 0Ω Machine mode = ±200V 1 time / each terminal

Ta: ambient temperature

[Criteria]
Under the display quality test conditions with normal operation state, there should be no change which may affect practical display function.

14. Indication of Lot Number Label

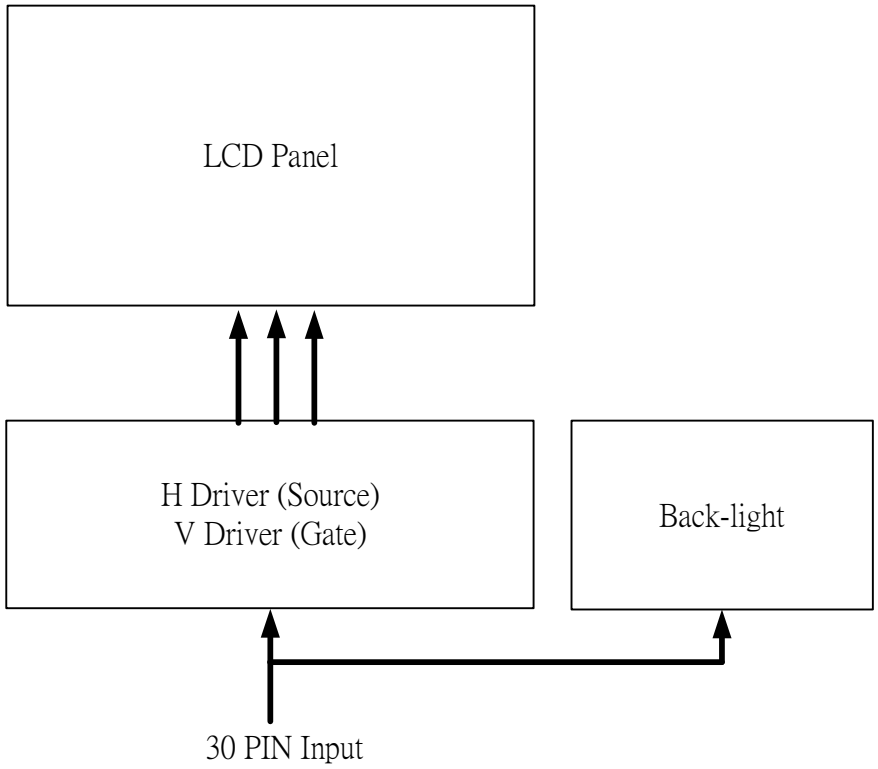
a) Indicated contents of the label



Contents of lot number : 1_{st}~3_{rd}—The OEM product
5_{th}—Production year : 1999⇒9, 2000⇒A, 2001⇒B……..
6_{th}—Production month : 1, 2, 3,….9, A, B, C
7_{th}~8_{th}—Production size : 2.37” ⇒24
9_{th}~10_{th}— Serial numbers : 01~99

15. Block Diagram

15.1 LCD Module Diagram



16. Packing

TBD

Revision History

Rev.	Issued Date	Revised Contents
0.1	Jul. 26 , 2004	NEW

Appendix