Version：2.0

TECHNICAL SPECIFICATION

MODEL NO. : PD024OX8

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☐Customer's Confirmation

Customer _____

Date _____

By _____

☐PVI's Confirmation

Confirmed By Tommy Chang

Prepared By 張昌鋐

Revision History

Rev.	Issued Date	Revised Contents
1.0	June. 7, 2006	New
2.0	Dec. 20, 2007	Modify Packing Drawing

TECHNICAL SPECIFICATION

CONTENTS

1. Application

This technical specification applies to a 2.36” color TFT-LCD panel.
This is designed for printer application and other electronic products which require high quality flat panel display.

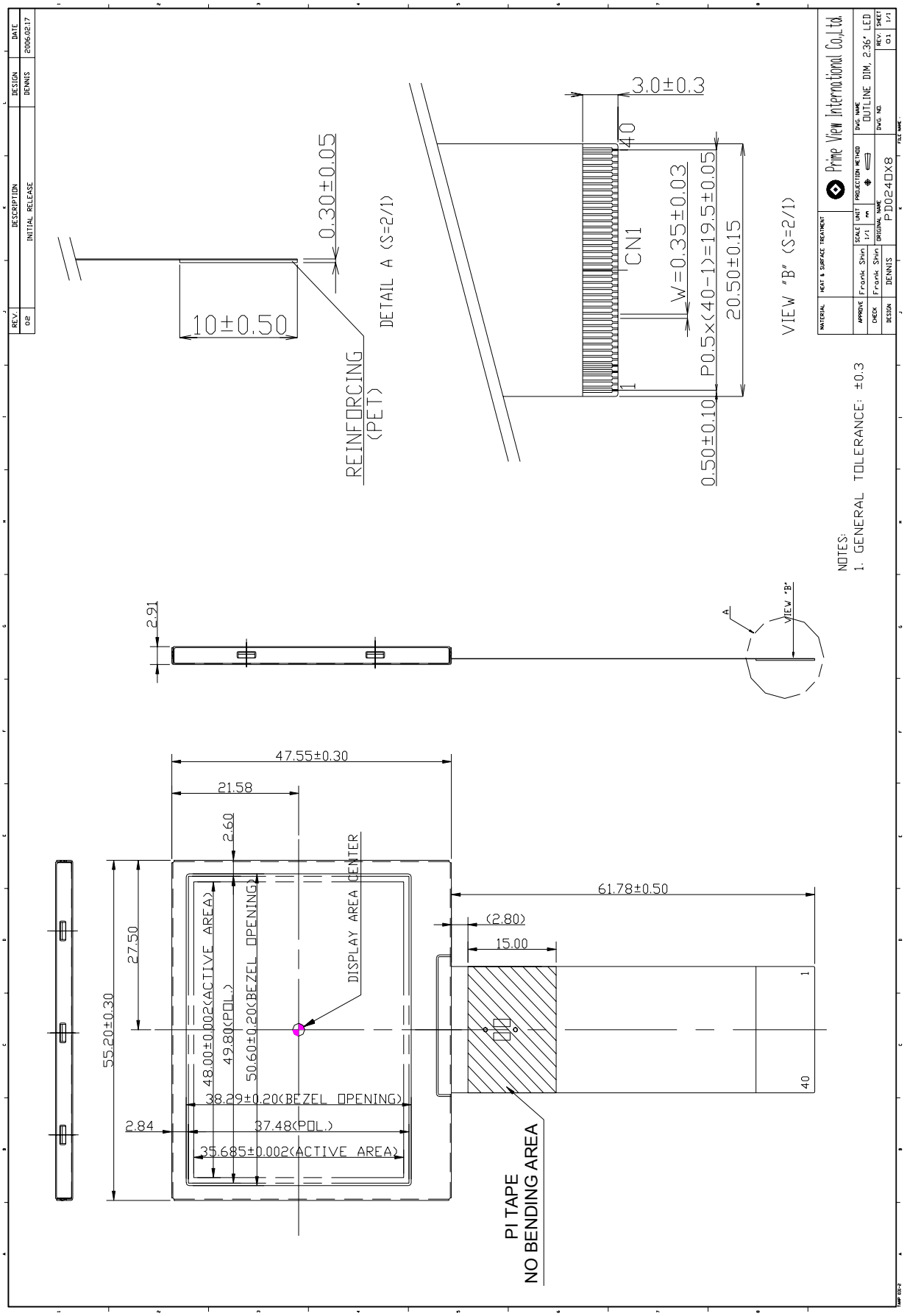
2. Features

. Pixel in delta configuration
. Enables an approximately 16,190,000 color display by approximate 8-bit function.
. Provide a 3-wire clock synchronous serial interface for various operation mode settings.
. Built-in TCON, and support serial RGB mode, YUV mode, CIR656 mode.
. Image reversion : Up/Down and Left/Right.
. Built-in control circuit for LED driving.
. Built-in power-save functions such as the stand-by mode.
. Built-in Vcom amplitude voltage output circuit.

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	2.36 (diagonal)	inch
Display Format	160×(RGB)×234	dot
Display colors	262,144	
Active Area	48.0(H)×35.685(V)	mm
Pixel Pitch	0.3(H)×0.1525 (V)	mm
Pixel Configuration	Delta	
Outline Dimension	55.20(W)×47.55 (V)×2.91(D)(typ.)	mm
Weight	12±1.5	g
Back-light	Three LED	
Surface Treatment	Anti – Glare	
Display model	Normally white	

4. Mechanical Drawing of TFT-LCD Module



5. Input / Output Terminals

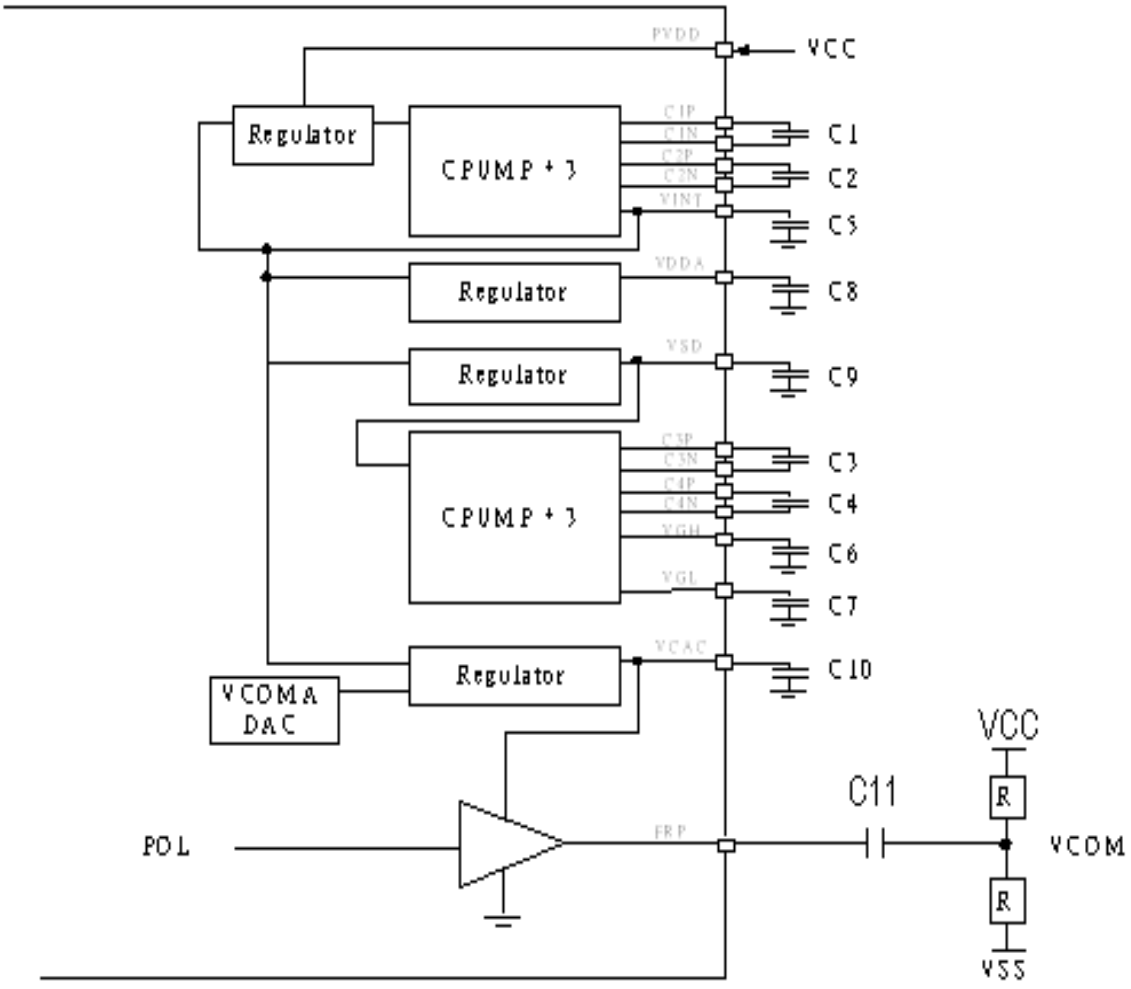
FPC Down Connect , 40Pins , Pitch : 0.5 mm

PGND=GND=0V

Pin No	Symbol	I/O	Description	Remark
1	VCOM	I	Common electrode voltage	Note 5-1
2	N/C	-	-	
3	VGL	I	Negative power supply for gate driver	Note 5-2
4	C4P	C	Pins to connect capacitance for power circuitry	
5	C4N	C	Pins to connect capacitance for power circuitry	
6	VGH	I	Positive power supply for gate driver	
7	FRP	O	Frame polarity output for VCOM	
8	VCAC	C	Define the amplitude of the VCOM swing	
9	VSD	I	Voltage for Source Driver and Reference Voltage	
10	C3P	C	Pins to connect capacitance for power circuitry	
11	C3N	C	Pins to connect capacitance for power circuitry	
12	VDDA	I	Voltage for Source Driver and Reference Voltage	
13	C2P	C	Pins to connect capacitance for power circuitry	
14	C2N	C	Pins to connect capacitance for power circuitry	
15	VINT	I	Voltage for Source Driver and Reference Voltage	
16	C1P	C	Pins to connect capacitance for power circuitry	
17	C1N	C	Pins to connect capacitance for power circuitry	
18	PGND	I	Charge Pump Power GND	
19	PVDD	I	Charge Pump Power VDD	Note 5-3
20	DRV	O	Gate signal for the power transistor of the boost converter	Note 5-4
21	VLED	I	Supply voltage for LED backlight	
22	NC	-	-	
23	FB	I	Main boost regulator feedback input	Note 5-5
24	VCC	I	Digital power supply	Note 5-3
25	GND	I	Digital GND	
26	VCC	I	Digital power supply	Note 5-3
27	CS	I	Serial interface chip select signal	
28	SDA	I	Serial interface data input signal	
29	SCL	I	Serial interface transmission clock	
30	HSYNC	I	Horizontal sync input	
31	VSYNC	I	Vertical sync input	
32	DCLK	I	Clock input	
33	D7	I	Data input	
34	D6	I	Data input	
35	D5	I	Data input	
36	D4	I	Data input	
37	D3	I	Data input	
38	D2	I	Data input	
39	D1	I	Data input	
40	D0	I	Data input	

Note 5-1: V_{COM} = +5.0 Vp-p. (Typ.)
Note 5-2: The external capacitor is required on those pins as following.

Cap No.	Pin name	Capacitor value.(μF)	Recommand breakdown voltage
C1	C1P/C1N	1	16V
C2	C2P/C2N	1	16V
C3	C3P/C3N	1	25V
C4	C4P/C4N	1	25V
C5	VINT	1	16V
C6	VGH	1	25V
C7	VGL	1	25V
C8	VDDA	1	16V
C9	VSD	1	16V
C10	VCAC	1	16V
C11	FRP	1	16V



Note 5-3: PVDD, VCC = +3.3 V (Typ.)
Note 5-4: Outputs the control signal of switching regulator for LED. Duty cycle varies according to FB input voltage.
Note 5-5: Feedback signal of switching signal for LED. It controls DRV output duty cycle with 0.6V input level sense.

6. Absolute Maximum Ratings

The followings are maximum values, which if exceeded, may cause faulty operation or damage to the unit.

PGND=GND=0V , Ta = 25℃

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Power Supply Voltage	Vcc	-0.3	7	V	
	PV_{DD}	-0.3	7	V	
Input Signal Voltage	Vcom	-0.5	6.375	V	
Digital Input Voltage	V_{IN}	-0.3	Vcc+0.3	V	
Maximum clock frequency	Fmax	-	30	MHz	

7. Electrical Characteristics

7-1 Operation condition

PGND=GND=0V , Ta = 25℃

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage for Source Driver	Vcc	3.0	3.3	3.6	V	
Supply Voltage for Gate Driver	PVDD	3.0	3.3	3.6		
	V_{GH}	14.5	15.5	16.5	V	Note 7-1
	V_{GL}	-10.5	-9.5	-8.5	V	Note 7-1
Digital input voltage	V_{IH}	0.7 V_{CC}	-	V_{CC}	V	
	V_{IL}	0	-	0.3 V_{CC}	V	
Digital output voltage	V_{OH}	0.7 V_{CC}	-	V_{CC}	V	
	V_{OL}	0	-	0.3 V_{CC}	V	
V_{COM}	$V_{COM\ AC}$	-	+5.0	-	V_{P-P}	AC Component of V_{COM}
	$V_{COM\ DC}$	-	1.5	-	V	Note 7-2

Note 7-1: V_{GH} and V_{GL} supplied by internal setup-up circuit.

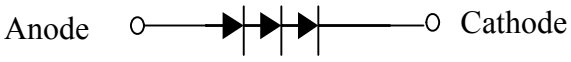
Note 7-2: PVI strongly suggests that the $V_{COM\ DC}$ level shall be adjustable , and the adjustable level range is 1.5±1V , every module's $V_{COM\ DC}$ level shall be carefully adjusted to show a best image performance.

7-2 Power consumption

Parameter	Symbol	Min	TYP	MAX	Unit	Remark
Supply voltage of LED backlight	V_{LED}	9.0	10.0	11.5	V	I_{LED} = 20 mA
Supply current of LED backlight	I_{LED}		20		mA	Note 7-3
Backlight Power Consumption	P_{LED}	180	200	230	mW	Note 7-4

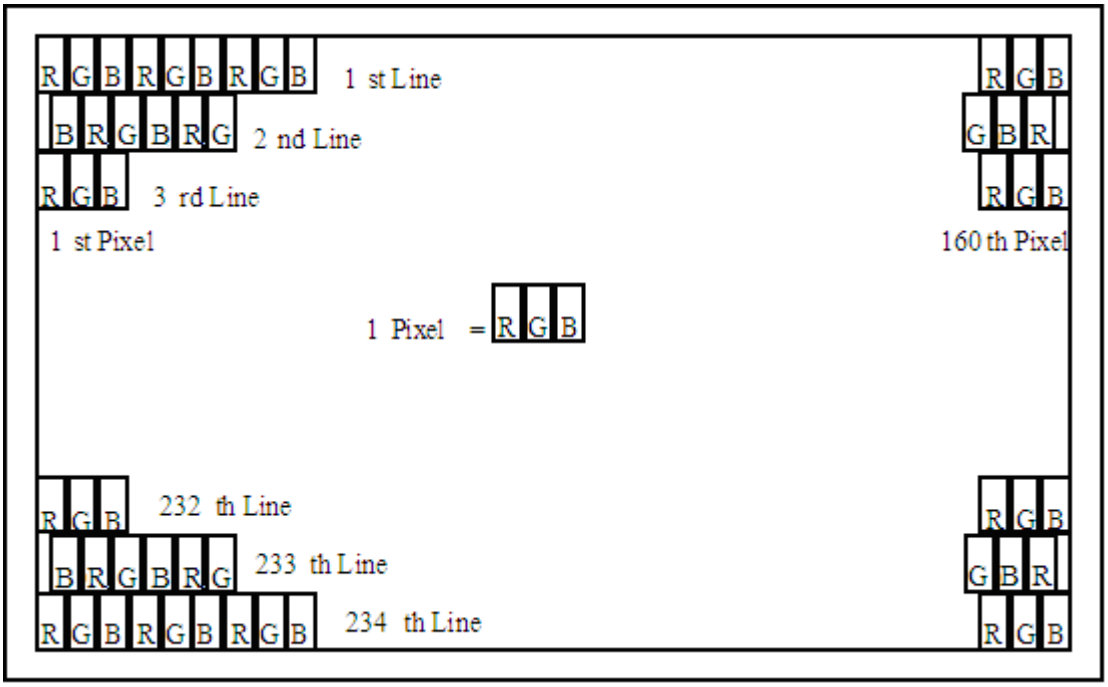
Note 7-3: LED B/L applied information, please refer to the appendix at the end.

Note 7-4: $P_{LED} = V_{LED} * I_{LED}$



Parameter	Symbol	Conditions	TYP.	MAX.	Unit	Remark
Supply current for IC driver	ICC	VCC =+3.3V	5.5	7	mA	
	PVDD	PVDD1=+3.3V	15	20	mA	
Total power consumption			68	90	mW	

8. Pixel arrangement



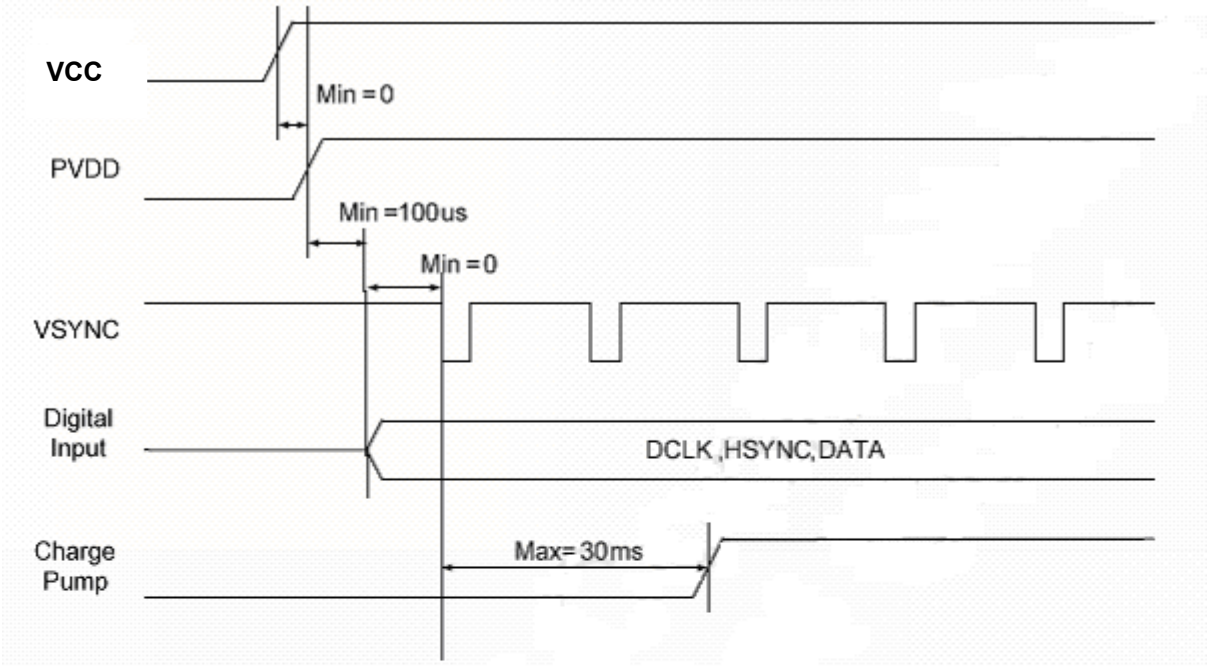
9. Display Color and Gray Scale Reference

Color		Input Color Data																							
		Red								Green								Blue							
		R7	**R6**	**R5**	**R4**	**R3**	**R2**	**R1**	**R0**	**G7**	**G6**	**G5**	**G4**	**G3**	**G2**	**G1**	**G0**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (01)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (02)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (01)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0
	Green (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Blue (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

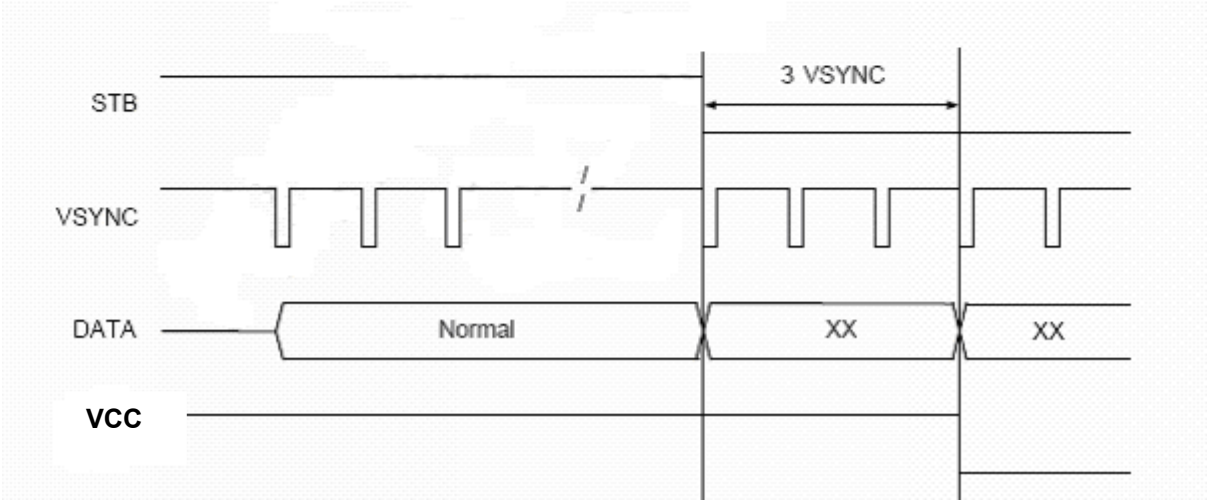
10. Power On/Off Sequence

Specially take care that the large current may cause a permanent damage to the IC when voltage is applied to the charge pump power supply in the condition that the logic power supply is floating.

Please refer to the following timing and command setting, concerning the power supply ON and the power supply OFF.

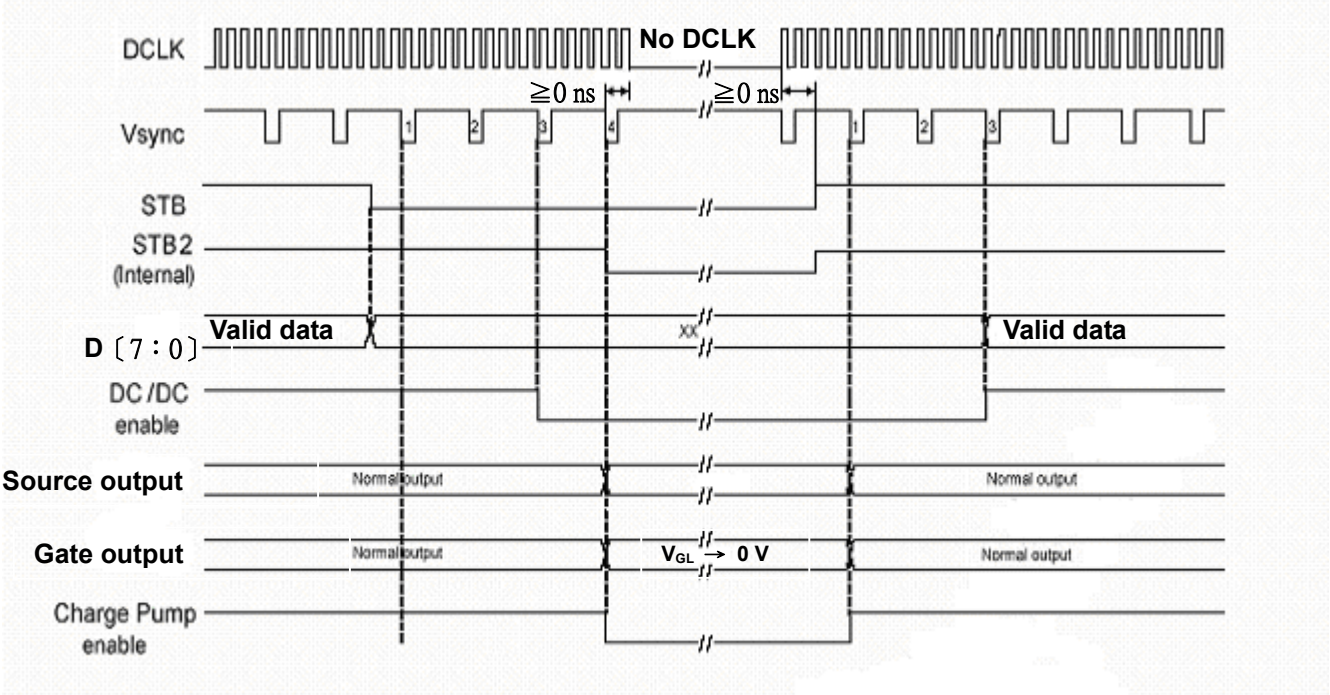


Power on sequence timing diagram



Driver IC will write 3 VSYNC Black pattern to the LCD panel after STB mode.

Power off sequence timing diagram



During No DCLK , Hsync and Vsync can be stopped.
But in all other cases Hysnc and Vsync must be active.

11.Register Description

Register	Function Description
R00	System Setting Register
R01	Timing Control Setting Register
R02	Driver Setting Register
R03	Data format Setting Register
R04	Source Delay Setting Register
R05	Vertical Delay Setting Register
R06	Voltage Level Setting Register
R07	Internal Setting Register

Function Description

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Register Address			Data												
R00	0	0	0	0									GRB	STB	SHDB	SHCB
R01	0	0	1	0							reserved	reserved	reserved	DITB		reserved
R02	0	1	0	0						reserved	reserved	reserved	FPOL		UD	SHL
R03	0	1	1	0								PALM	PAL	SEL2	SEL1	SEL0
R04	1	0	0	0								DDL4	DDL3	DDL2	DDL1	DDL0
R05	1	0	1	0									HDL3	HDL2	HOL1	HDL0
R06	1	1	0	0					VDV 1	VDV 0	LPC1	LPC0		VSCL2	VSCL1	VSCL0
R07	1	1	1	0									DCKS1	DCKS0		

Register Description

Note：(1) D12 must be low.

(2) All the SPI register settings will active at the falling edge of the VSYNC except GRB、STB and SEL〔2：0〕bits.

11-1 Function Control Register (R00h)

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Register Address			Data												
R00	0	0	0	0									GRB	STB	SHDB	SHCB
													1	1	0	1

GRB	Global Reset
L	The Controller is resets, the Charge Pump and DCDC is off.
H	Normal operation; Default setting.

STB	Stand By Mode
L	TCON, SD, Charge Pump and DC-DC are off. All outputs are High-Z.
H	Normal operation; Default setting.

SHDB	DC-DC converter shutdown signal
L	The DC-DC is off. Default Setting.
H	The DC-DC is on.

Note: The function disable, the DRV output be VSS.

SHCB	Charge Pump shutdown signal
L	The Charge Pump is off.
H	The Charge Pump is on. ; Default setting.

11-2 Function Control Register (R01h)

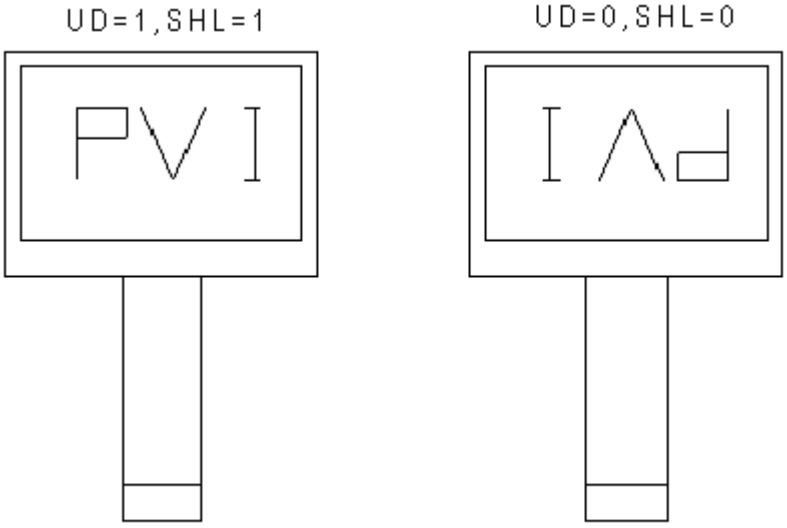
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Register Address			Data												
R01	0	0	1	0							reserved	reserved	reserved	DITB		reserved
											1	0	0	0		1

DITB	Dithering setting
L	Dithering on 8-bit resolution. Default Setting.
H	Dithering off. 6-bit resolution (the last 2-bits truncated).

11-3 Function Control Register (R02h)

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Register Address			Data												
R02	0	1	0	0						reserved	reserved	reserved	FPOL		UD	SHL
										0	0	0	0		1	1

FPOL	Control the inversion of FRP depending on the polarity of the Gamma Correction
L	FRP inverted with respect to the polarity of the gamma correction. Default setting.
H	FRP in phase with the polarity of the gamma correction.



11-4 Function Control Register (R03h)

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Register Address			Data												
R03	0	1	1	0								PALM	PAL	SEL2	SEL1	SEL0
												0	0	0	0	0

PALM	PAL Selection Signal (only available when PAL=H)
L	Input data format is PAL 1/6,8(280 active line). Default Setting.
H	Input data format is PAL 1/6(288 active line).

PAL	NTSC/PAL Selection Signal
L	Input data format is NTSC. Default Setting.
H	Input data format is PAL.

Select Input Data Format, Default Setting=**000.**

SEL2	SEL1	SEL0	Format	Operating Frequency
0	0	0	Serial-RGB data format (HV mode)	9.7MHz
0	0	1		
0	1	0	CCIR 656 data format(640RGB)	24.54MHz
0	1	1	YUV mode A data format	24.54MHz
1	0	0	YUV mode A data format	27MHz
1	0	1	YUV mode B data format	24.54MHz
1	1	0	YUV mode B data format	27MHz
1	1	1	CCIR 656 data format(720RGB)	27MHz

Note : SEL [2:0] =000,010,011,101, only NTSC mode, no support PAL mode.

11-5 Function Control Register (R04h)

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Register Address			Data												
R04	1	0	0	0								DDL4	DDL3	DDL2	DDL1	DDL0
												0	0	0	0	0

Select the data delay timing, Default Setting=00000.

DDL4	DDL3	DDL2	DDL1	DDL0	Delay	Unit
0	0	0	0	0	0	DCLK Period
0	0	0	0	1	1	
0	0	0	1	0	2	
0	0	0	1	1	3	
0	0	1	0	0	4	
0	0	1	0	1	5	
0	0	1	1	0	6	
0	0	1	1	1	7	
0	1	0	0	0	8	
0	1	0	0	1	9	
0	1	0	1	0	10	
0	1	0	1	1	11	
0	1	1	0	0	12	
0	1	1	0	1	13	
0	1	1	1	0	14	
0	1	1	1	1	15	
1	0	0	0	0	-1	
1	0	0	0	1	-2	
1	0	0	1	0	-3	
1	0	0	1	1	-4	
1	0	1	0	0	-5	
1	0	1	0	1	-6	
1	0	1	1	0	-7	
1	0	1	1	1	-8	
1	1	0	0	0	-9	
1	1	0	0	1	-10	
1	1	0	1	0	-11	
1	1	0	1	1	-12	
1	1	1	0	0	-13	
1	1	1	0	1	-14	
1	1	1	1	0	-15	
1	1	1	1	1	-16	

11-6 Function Control Register (R05h)

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Register Address			Data												
R05	1	0	1	0									HDL3	HDL2	HOL1	HDL0
													0	0	0	0

Select the first active line delay timing, Default Setting=00000.

DDL3	DDL2	DDL1	DDL0	Delay	Unit
0	0	0	0	0	HSYNC. Period.
0	0	0	1	1	
0	0	1	0	2	
0	0	1	1	3	
0	1	0	0	4	
0	1	0	1	5	
0	1	1	0	6	
0	1	1	1	7	
1	0	0	0	8	
1	0	0	1	-1	
1	0	1	0	-2	
1	0	1	1	-3	
1	1	0	0	-4	
1	1	0	1	-5	
1	1	1	0	-6	
1	1	1	1	-7	

11-7 Function Control Register (R06h)

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Register Address			Data												
R06	1	1	0	0					VDV 1	VDV 0	LPC1	LPC0		VSCL2	VSCL1	VSCL0
									0	0	0	0		0	1	1

Voltage level control, default setting=00.

VDV1	VDV0	VDDA
0	0	5.0V
0	1	4.8V
1	0	4.6V
1	1	4.4V

Low power control, default setting=00.

LPC1	LPC0	Output driving time	Unit
0	0	30	µs
0	1	20	
1	0	63.5	
1	1	40	

VCOM amplitude control, default setting=011.

VSCL2	VSCL1	VSCL0	VCAC Level	Unit
0	0	0	6.25	V
0	0	1	6.375	
0	1	0	4.75	
0	1	1	5	
1	0	0	5.25	
1	0	1	5.5	
1	1	0	5.75	
1	1	1	6	

11-8 Function Control Register (R07h)

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Register Address			Data												
R07	1	1	1	0									DCKS1	DCKS0		
													0	0		

Charge Pump clock frequency selection. (Default = 00)

DCKS1	DCKS0	CKC1	CKC2	Unit
0	0	150	37.5	KHz
0	1	50	12.5	
1	0	100	25	
1	1	200	50	

12.AC Characteristics

12-1 Timing conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Delay between Hsync and DCLK	Thc	-	-	1	DCLK
Hysnc width	Twh	1	32	-	DCLK
Hysnc period	Th	60	63.5	67	μs
Vsync setup time	Tvst	12	-	-	ns
Vsync hold time	Tvhd	12	-	-	ns
Hsync setup time	Thst	12	-	-	ns
Hsync hold time	Thhd	12	-	-	ns
Data set-up time	Tdsu	12	-	-	ns
Data hold time	Tdhd	12	-	-	ns
Vsync width for RGB mode	Twv	2	4	6	Th
Vsync width for YUV mode	Twv	1.5	1.5	5.5	Th
Vsync period NTSC	Tv	-	262.5	-	Th
Vsync period PAL	Tv	-	312.5	-	Th
Hsync to Vsync time for ODD field	T_{HV_O}	-4	0	+4	DCLK
Hsync to Vsync time for EVEN field	T_{HV_E}	0	0.5	-	Th

Serial communication

Parameter	Symbol	Min.	Typ.	Max.	Unit
Serial clock period	Tsck	320	-	-	ns
Serial clock duty cycle	Tscw	40	50	60	%
Serial clock width	Tssw	120	-	-	μs
Serial data setup time	Tist	120	-	-	ns
Serial data hold time	Tihd	120	-	-	ns
SPENB setup time	Tcst	120	-	-	ns
SPENB data hold time	Tchd	120	-	-	ns
Chip select distinguish	Tcd	1	-	-	μs
Delay between SPCK and Vsync	Tcv	1	-	-	μs

12-2 Operating mode dependent AC characteristic

Serial RGB Mode, SEL〔2:0〕=〔000〕

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	Fclk	-	9.7	-	Mhz
DCLK period	Tcph	-	103	-	ns
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from Hsync to 1,st data input	Ths	84	100	115	DCLK
Delay from Vsync to 1,st data input	Tstv	9	16	24	Th
DRV output frequency		-	303.1	-	KHz

12-3 Operating mode dependent AC characteristic

YUV Mode, SEL〔2:0〕=〔011~110〕

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	Fclk	-	24.54/27	-	Mhz
DCLK period	Tcph	-	40.7/37	-	ns
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from Vsync to 1,st data input (NTSC)	Tstv	13	20	28	Th
Delay from Vsync to 1,st data input (PAL 288Lines)	Tstv	16	23	31	Th
Delay from Vsync to 1,st data input (PAL280Lines)	Tstv	20	27	35	Th
DRV output frequency		-	383.4/ 421.9	-	KHz

12-4 Operating mode dependent AC characteristic

CCIR656 Mode,SEL〔2:0〕=〔111〕

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	Fclk	-	27	-	Mhz
DCLK period	Tcph	-	37	-	ns
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from V to 1,st data input (NTSC)	Tstv	18	25	33	Th
Delay from V to 1,st data input (PAL 288Lines)	Tstv	20	27	35	Th
Delay from V to 1,st data input (PAL280Lines)	Tstv	24	31	39	Th
DRV output frequency	-	-	421.9	-	KHz

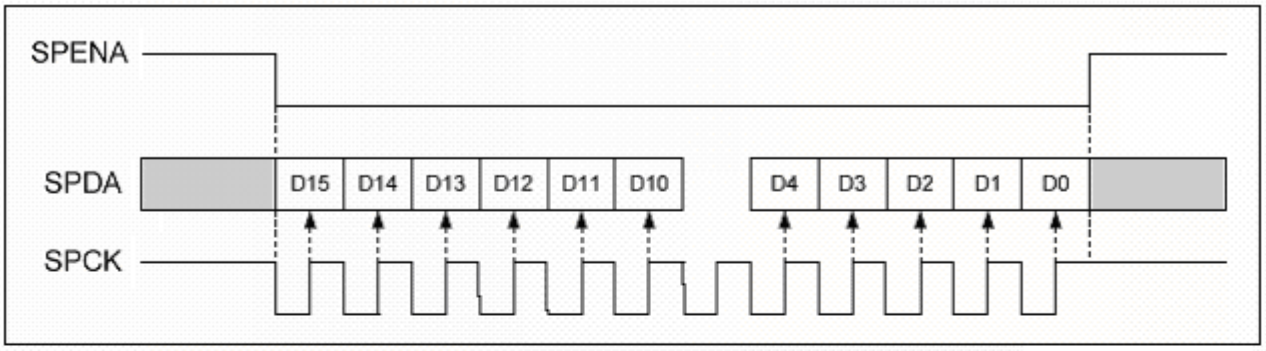
12-5 Operating mode dependent AC characteristic

CCIR656 Mode,SEL〔2:0〕=〔010〕

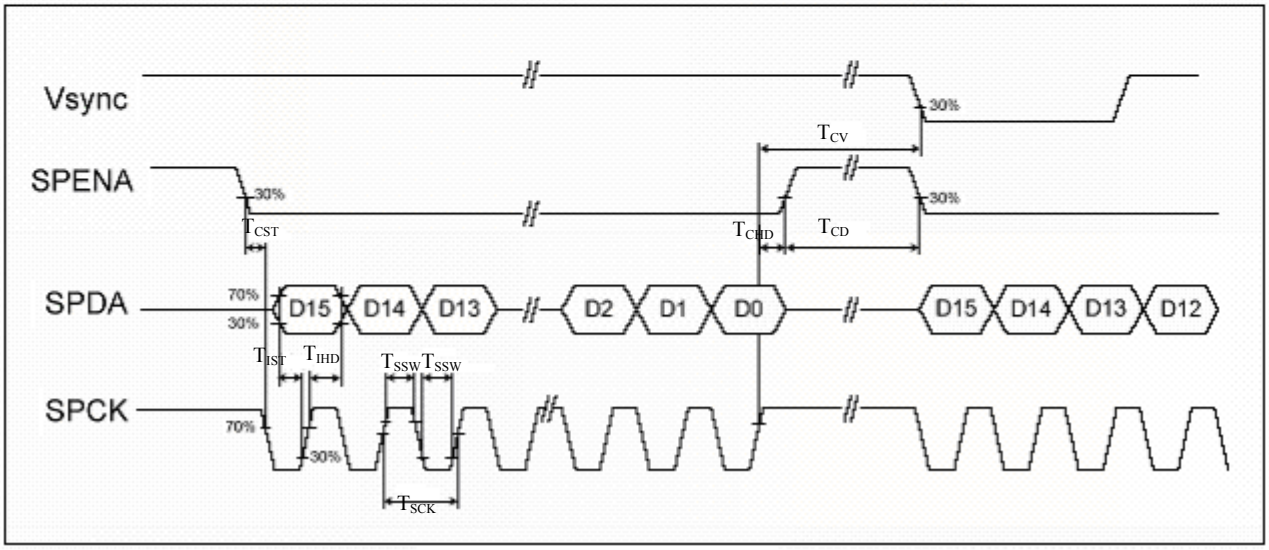
Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	Fclk	-	24.54	-	Mhz
DCLK period	Tcph	-	40.7	-	ns
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay form V to 1, st data input (NTSC)	Tstv	18	25	33	Th
DRV output frequency	-	-	383.4	-	KHz

13.Waveform

13-1 Timing format：Serial communication timing

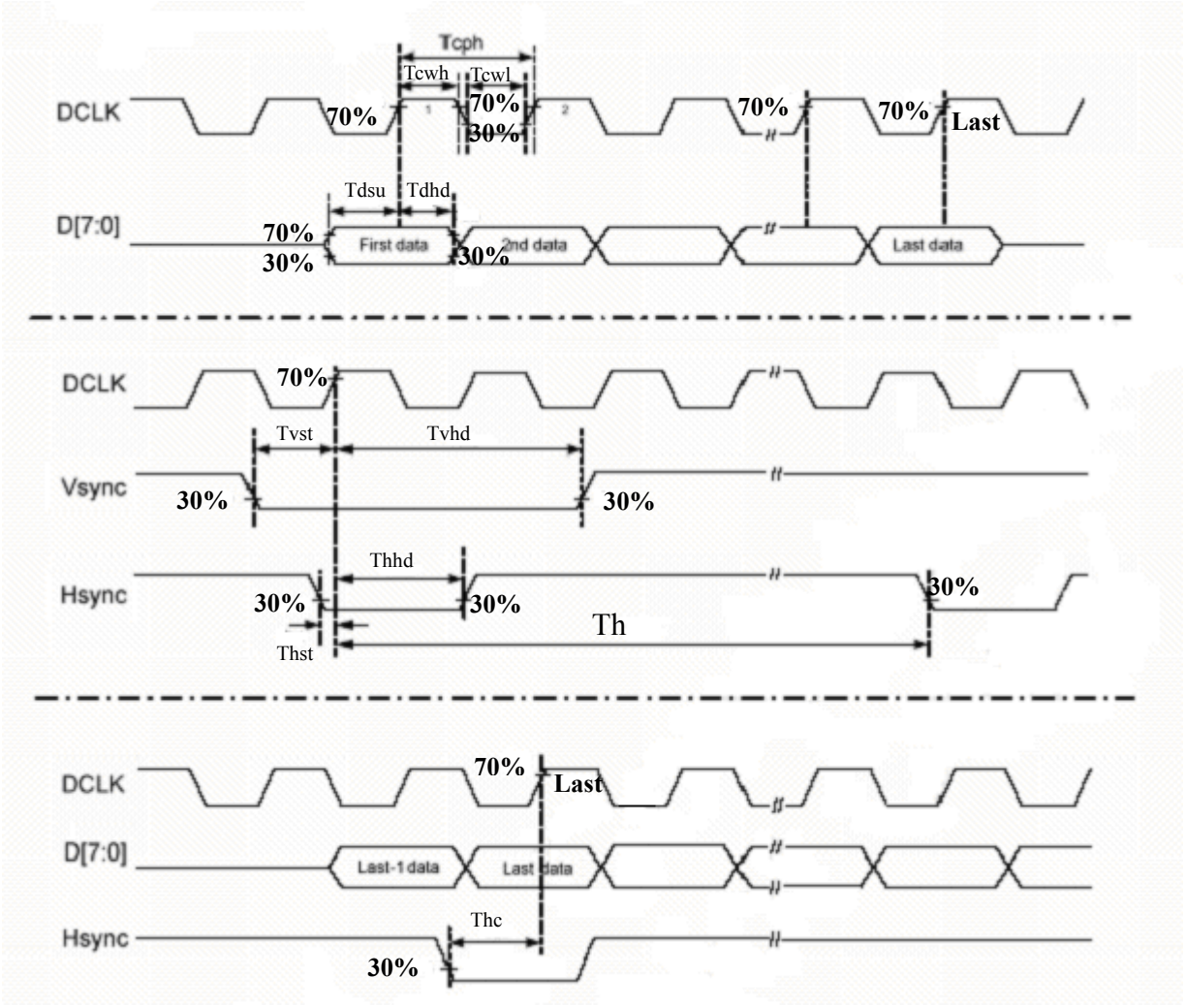


SPI Timing Diagram



SPI Timing Diagram V.S. Vsync

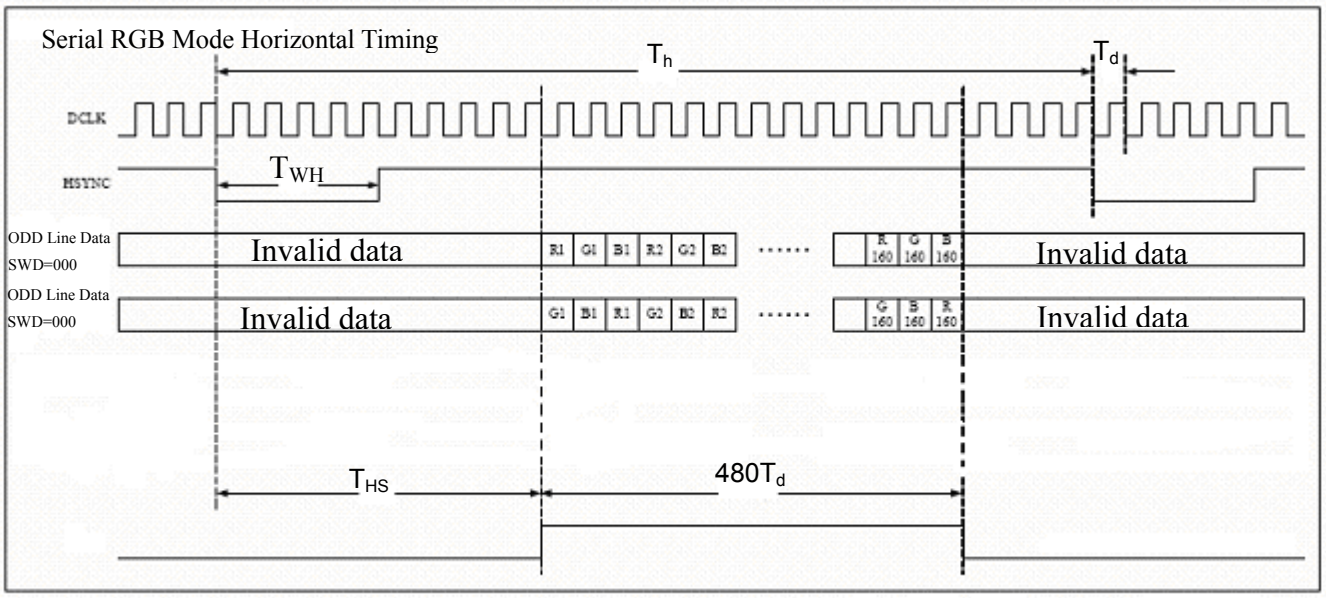
13-2 Clock and Data Input Timing Diagram



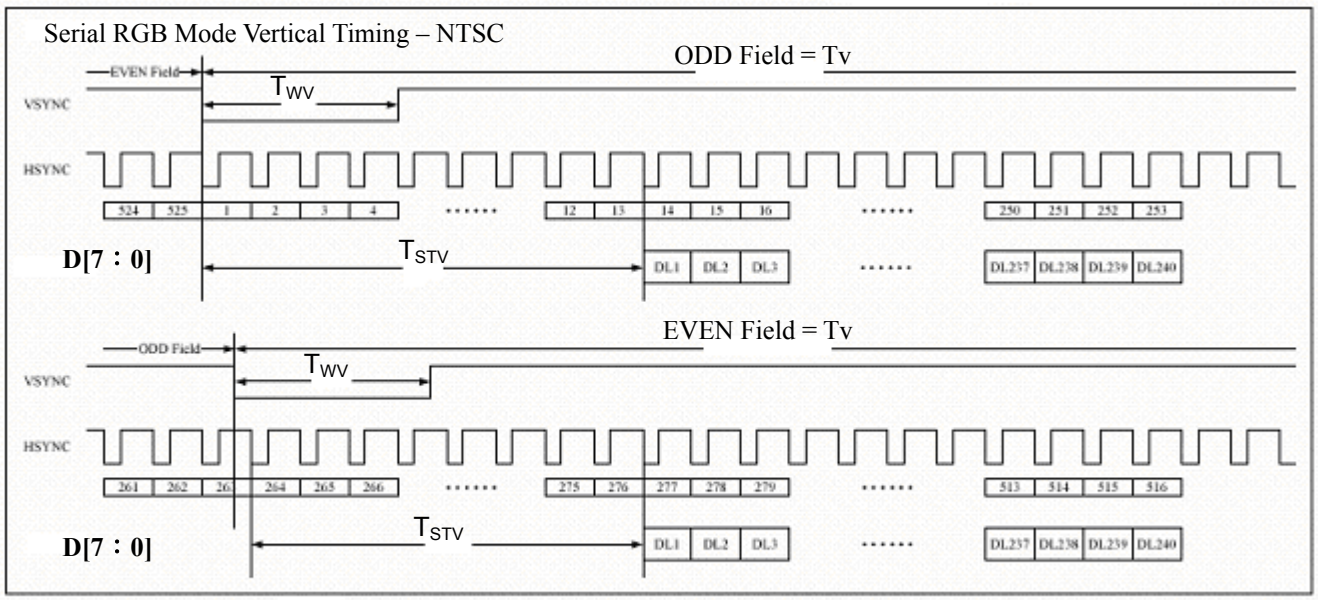
Clock and Data Input Timing Diagram

13-3 Input Data Format Timing

13-3-1 Serial RGB Data Format

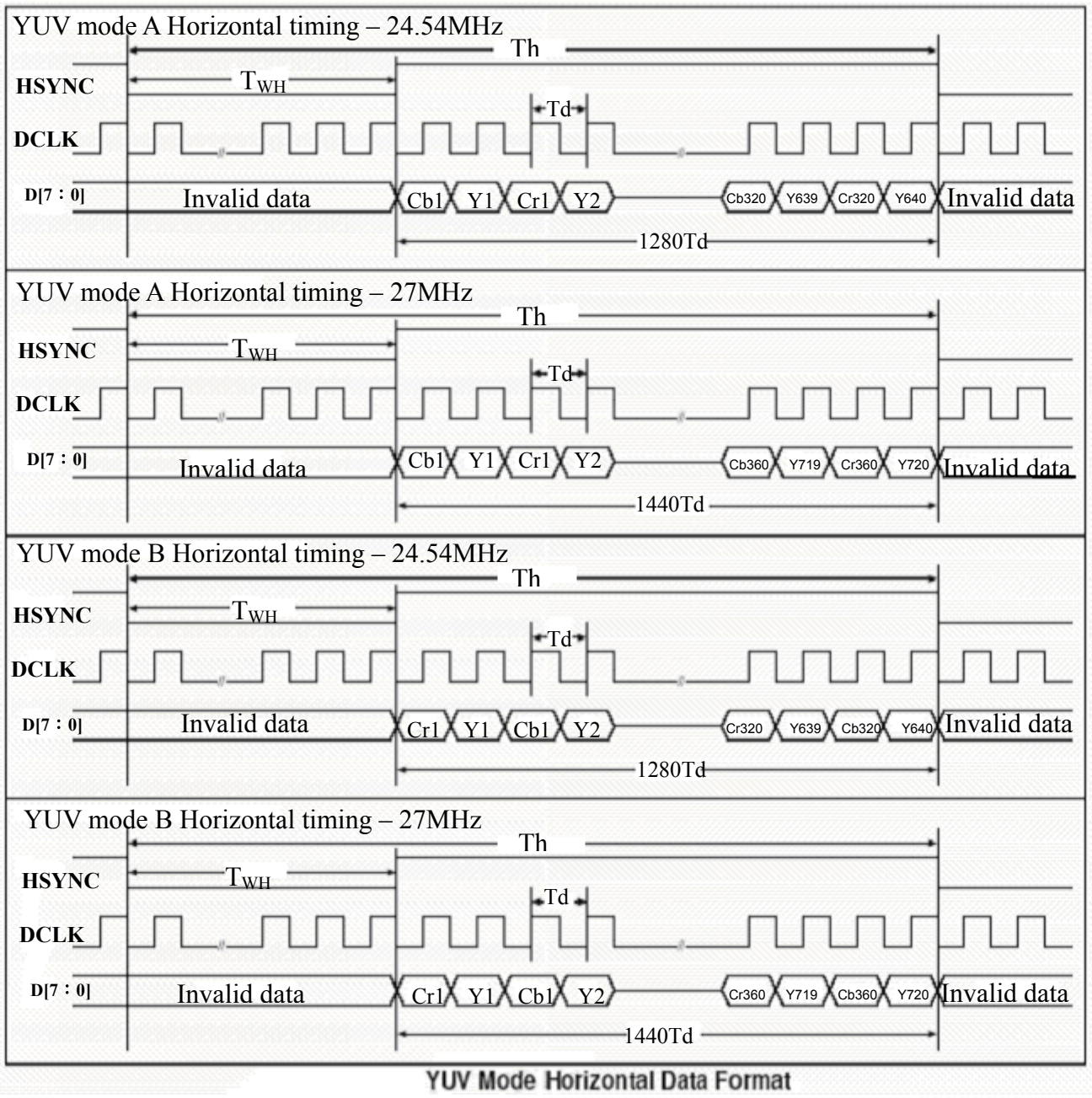


Serial RGB Horizontal Data Format

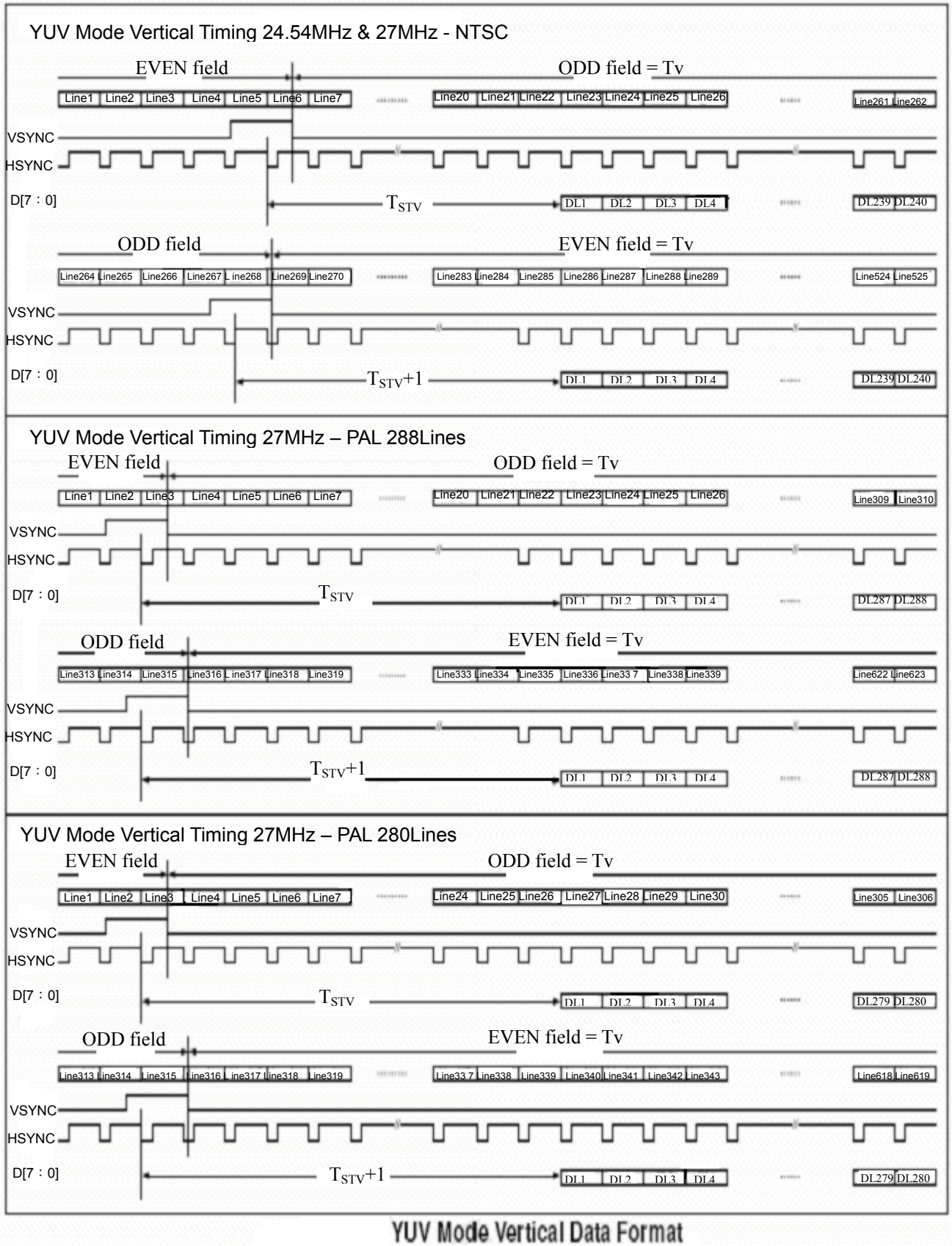


Serial RGB NTSC Mode Vertical Data Format

13-3-2 YUV mode Data Format

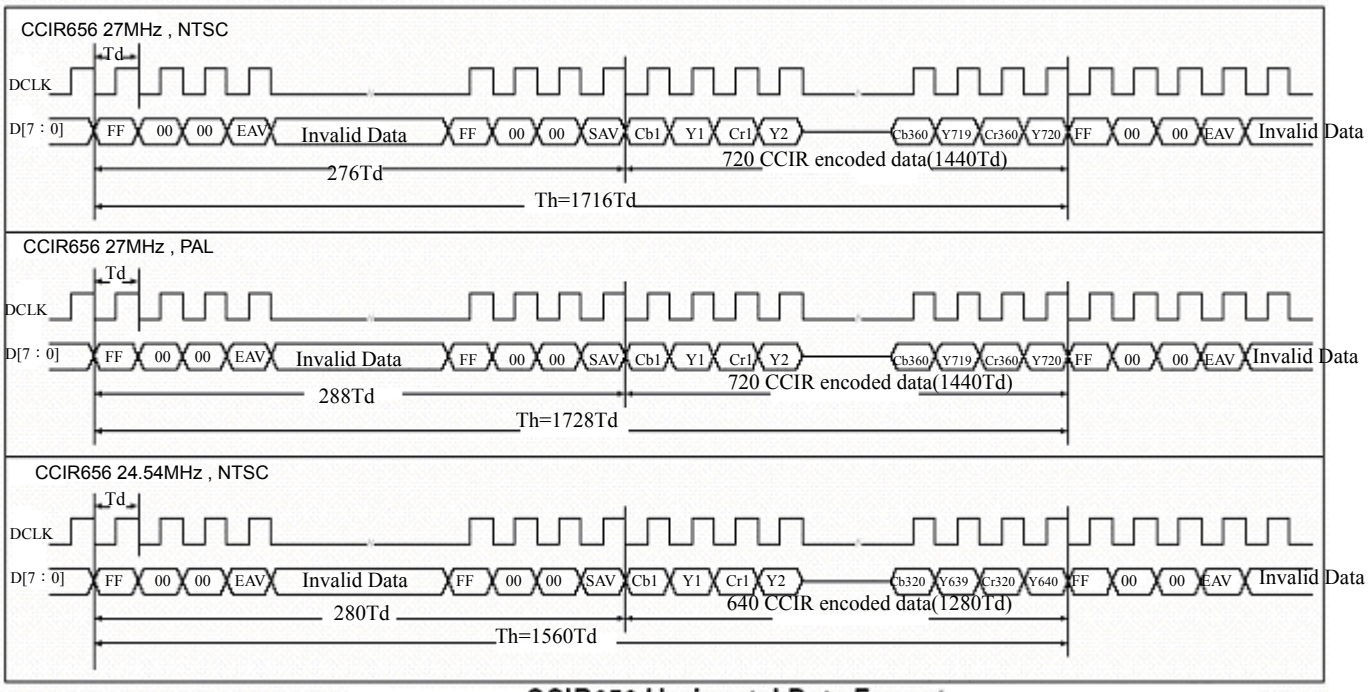


YUV Mode Horizontal Data Format

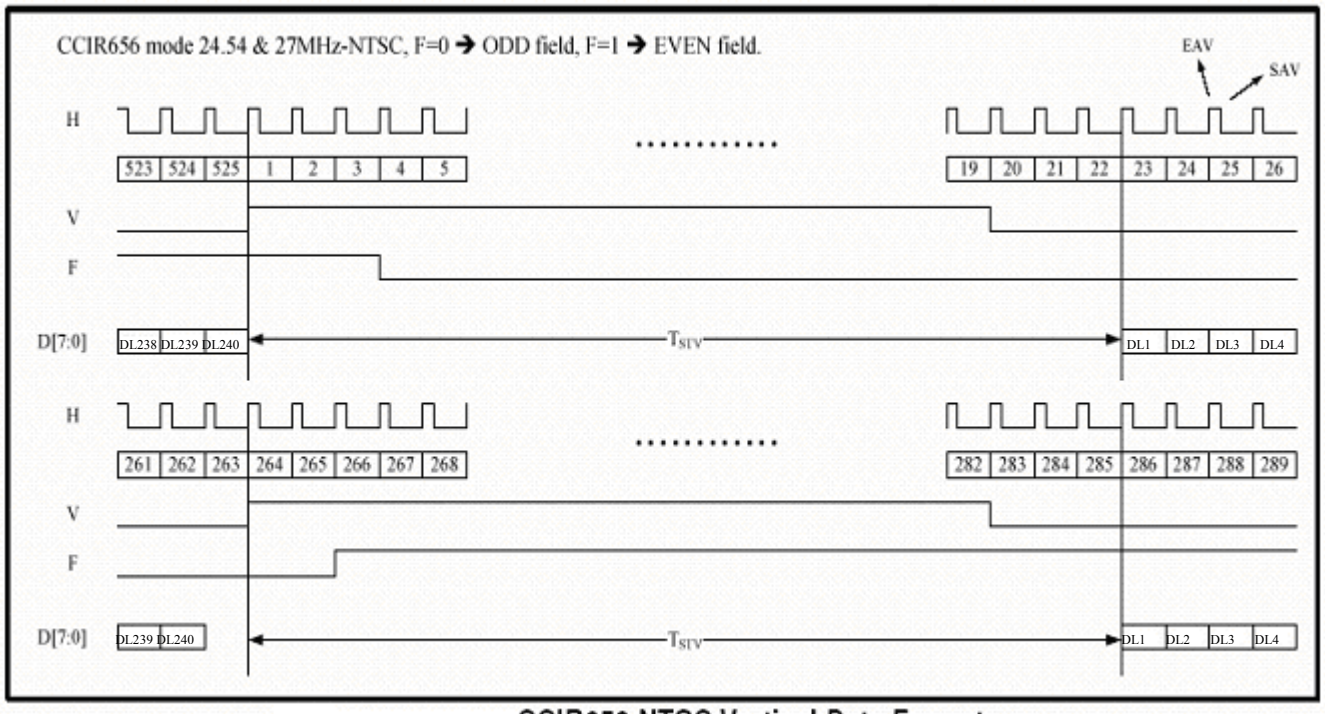


YUV Mode Vertical Data Format

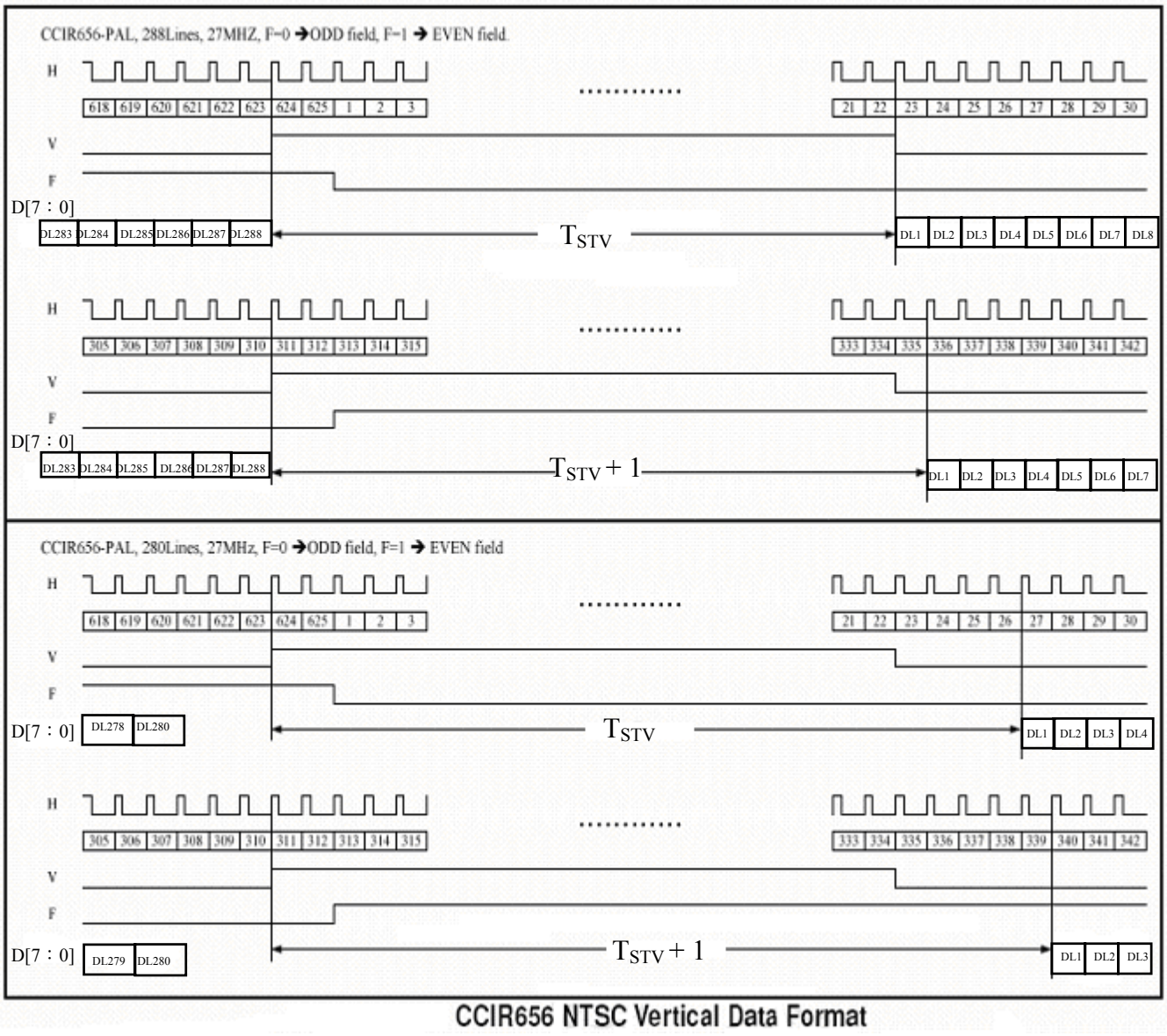
13-3-3 CCIR656 Data Format



CCIR656 Horizontal Data Format

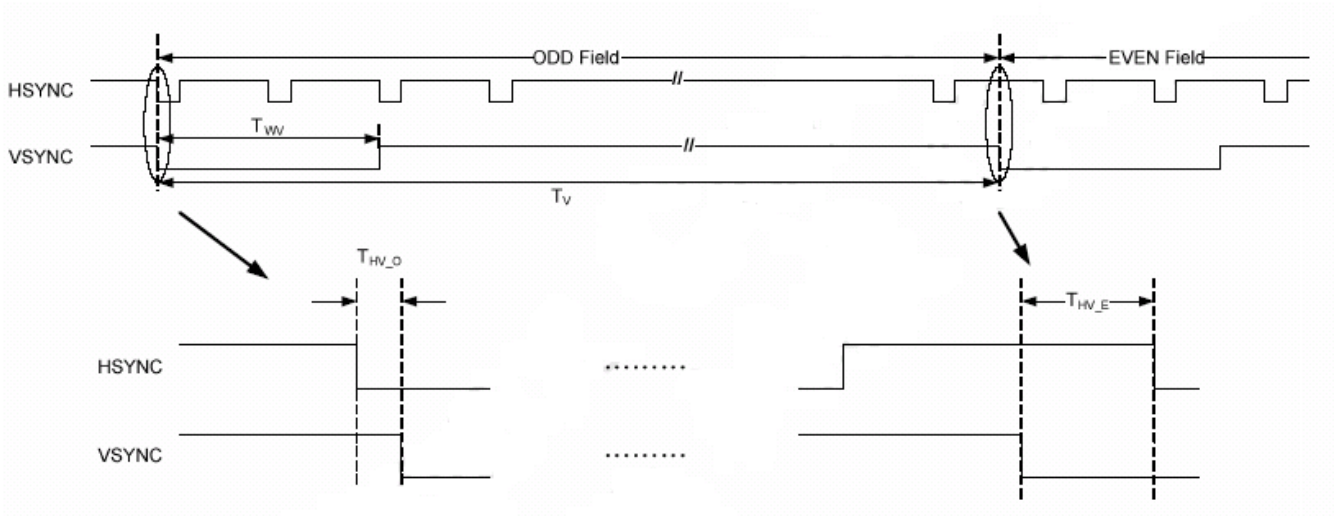


CCIR656 NTSC Vertical Data Format



CCIR656 NTSC Vertical Data Format

13-4 The HSYNC & VSYNC timing of the ODD/EVEN field



Define the HSYNC to VSYNC timing for serial RGB mode

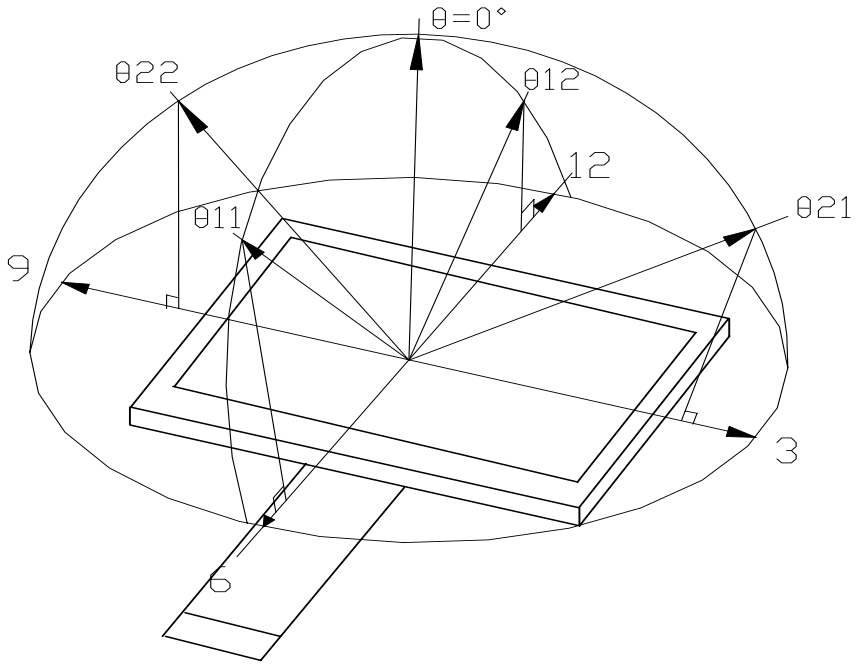
14.Optical Characteristics

14-1 Specification

Ta = 25℃

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ 21, θ 22	CR≧10	45	50	---	deg	Note 14-1
	Vertical	θ 11		30	35	---	deg	
		θ 12		10	15	---	deg	
Contrast Ratio		CR	At optimized Viewing angle	200	400	---		Note 14-2
Response time	Rise	Tr	θ =0°	---	6	12	ms	Note 14-3
	Fall	Tf		---	15	30	ms	
Uniformity		U	---	70	75	---	%	Note 14-4
Brightness		L	θ =0°	200	250	---	cd/㎡	Note 14-5
White Chromaticity		X	θ =0°	0.28	0.31	0.34		Note 14-5
		Y	θ =0°	0.30	0.33	0.36		
LED Life Time			---	---	10000	---	hrs	Note 14-6

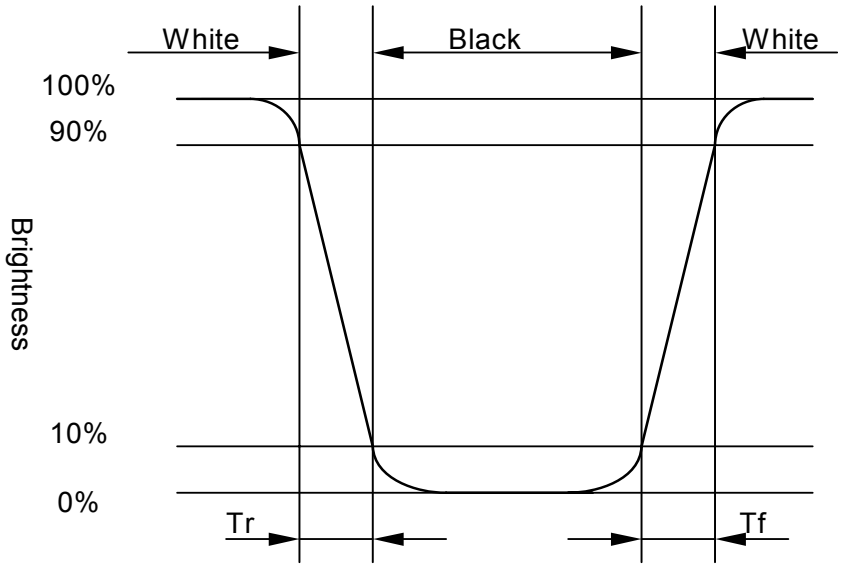
Note 14-1 : The definitions of viewing angles



Note 14-2 : CR $= \dfrac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$

Contrast ratio is measured in optimum common electrode voltage.

Note 14-3 : The definition of response time :

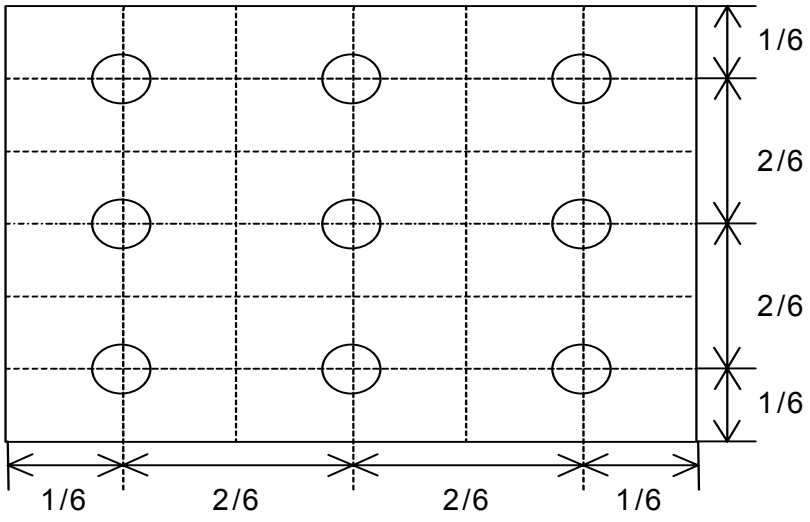


Note 14-4 : The uniformity of LCD is defined as

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

Luminance meter : BM-7 fast (TOPCON)
Measurement distance : 500 mm +/- 50 mm
Ambient illumination : < 1 Lux
Measuring direction : Perpendicular to the surface of module

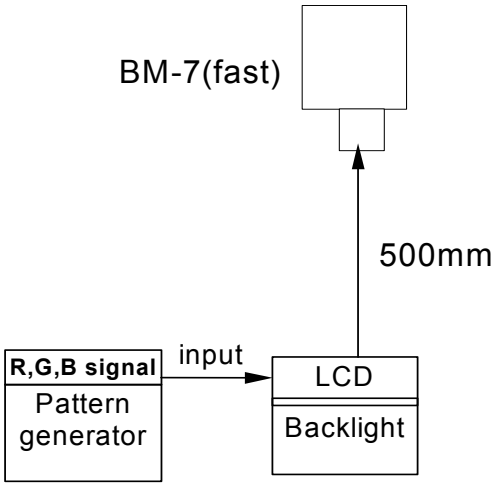
The test pattern is white



Note 14-5 : Topcon BM-7(fast) luminance meter 1.0° field of view is used in the testing (use PVI backlight after 5 minutes operating), ILED = 20mA.

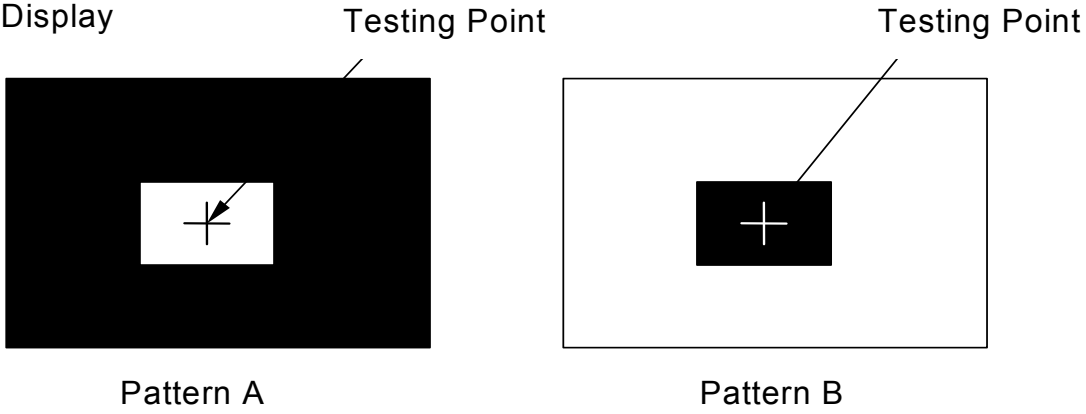
Note 14-6 : Constant current 20mA for each loop , and the center brightness must more than 50% of initial brightness value .

14-2 Testing configuration

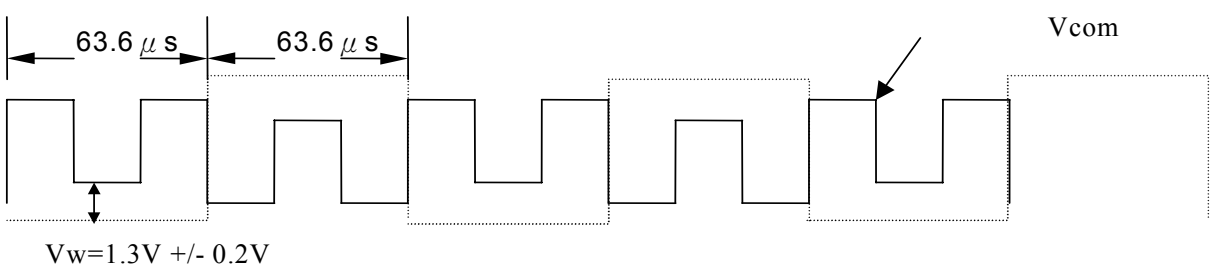


Caution: 1. Environmental illumination ≦ 1 lux
2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

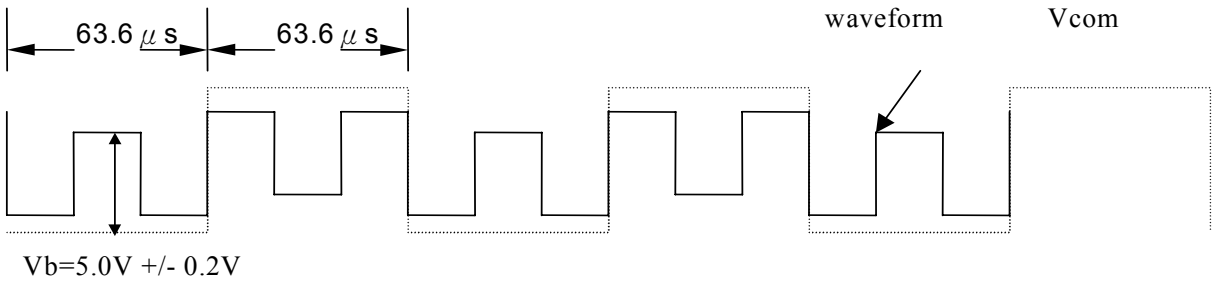
- LCD Display



- R, G, B Waveform of Pattern A at Testing Point



- R, G, B Waveform of Pattern B at Testing Point



15. Handling Cautions

15-1) Mounting of module

a) Please power off the module when you connect the input/output connector.

b) Please connect the ground surely. If the connection is not perfect, some following problems may happen possibly.
1.The noise from the backlight unit will increase.
2.In some cases a part of module will heat.

c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.

d) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

15-2) Precautions in mounting

a) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.

b) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.

c) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

15-3) Others

a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.

b) Store the module at a room temperature place.

c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.

d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.

e) Observe all other precautionary requirements in handling general electronic components.

16. Reliability Test

No.	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +70℃ , 240 hrs
2	Low Temperature Storage Test	Ta = -20℃ , 240 hrs
3	High Temperature Operation Test	Ta = +60℃ , 240 hrs
4	Low Temperature Operation Test	Ta = 0℃ , 240 hrs
5	High Temperature & High Humidity Operation Test	Ta = +60℃ , 90%RH , 240 hrs
6	Thermal Cycling Test (non-operating)	-20℃ → +70℃, 200 Cycles 30 min 30 min
7	Vibration Test (non-operating)	Frequency : 10 ~ 55 H_Z Amplitude : 1.0 mm Sweep time : 11 mins Test Period : 6 Cycles for each direction of X, Y, Z
8	Shock Test (non-operating)	100G , 6ms Direction : ±X , ±Y , ±Z Cycle : 3 times
9	Electrostatic Discharge Test (non-operating)	200pF , 0Ω ±200V 1 time / each terminal

Ta: ambient temperature

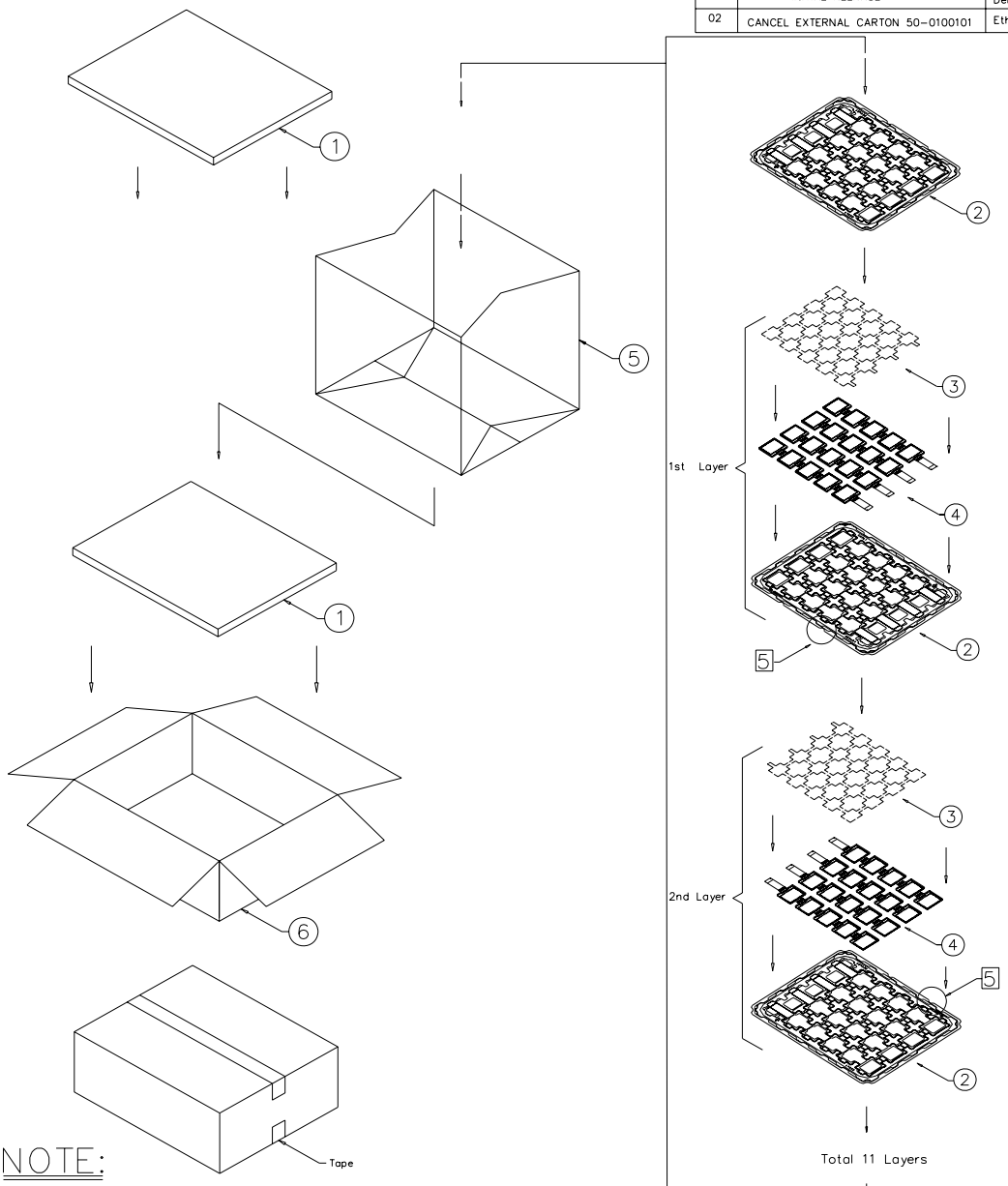
Note : The protective film must be removed before temperature test.

[Criteria]

In the standard conditions, there is not display function NG issue occurred. (Including：line defect, no image) All the cosmetic specification is judged before the reliability stress.

17. Packing Diagram

REV	DESCRIPTION	DESIGN	DATE
01	INITIAL RELRASE	Dennis chen	2005.05.19
02	CANCEL EXTERNAL CARTON 50-0100101	Ethan chen	2007.12.05



NOTE:

1. One layer include: 1 piece of cushion sheet, 20pcs panel & 1 piece of tray.
2. Q'TY: 220 pcs panel/carton.
3. Dimension: 455*375*190mm
4. Weight: 6.0 KG

5. tray需180°交又堆疊, 堆疊後可從側邊檢視圓弧防呆方向是否正確

ITEM	PART NO.	DESCRIPTION	QTY	REMARK
6	50-0100091	CARTON INTERNAL	1	
5	50-0500041	摺口袋450*380*700mm	1	抗靜電
4		PD024OX8	220	
3	50-0200071	EPE CUSHION SHEET	11	抗靜電
2	50-0301331	TRAY	12	抗靜電
1	50-0300491	EPE FOAM	2	

MTL.SPEC.	UNSPECIFIED TOL'S ±5.0mm ANGLE ROUGHNESS	REMARK	元太科技股份有限公司 Prime View Internation Co.,ltd.

APPROVE	Frank Shin	'05.05.19	SCALE 1:1	UNIT mm	SHEET 1 OF 1	DWG.TITLE PD024OX8 PACKING Dim
CHECK	Frank Shin	'05.05.19				
DESIGN	Dennis	'05.05.19	MTL.NO.	DWG.NO.	REV. 01	A4 SIZE

