

Version: 7.0

TECHNICAL SPECIFICATION  
MODEL NO : PD035OX1

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Customer's Confirmation


Customer \_\_\_\_\_

Date \_\_\_\_\_

By \_\_\_\_\_

PVI's Confirmation

  
Confirmed By \_\_\_\_\_

  
Prepared By \_\_\_\_\_

## Revision History

Rev.	Eng	Issued Date	Revised Contents
0.1		Jan .03 , 2005	Preliminary
0.2		Feb .02 , 2005	Modify: Page07: Note5-2 V <sub>GH</sub> Typ.= +15V. Page16: Register R2 – bit D5, D4 change to reserved, Register R3 – bit D6,D5,D4 change to reserved. Page18: Absolute Max. ratings – storage and operation temperature. Delete: Page21: 9.4.4 Output signal character for Digital/Analog RGB mode.
0.3		Apr. 15, 2005	Modify: Page04: Mechanical Drawing of TFT-LCD Module (FPC Outline Drawing) Add: Appendix ( LED B/L driving reference circuit)
0.4		May.17, 2005	Modify: Page05: POL I/O condition to output. Page25: Uniformity Typ. From 80% to 75%.
1.0		Jun. 07, 2005	Modify: Page31: Packing
2.0		Jul. 22, 2005	Modify: Page20:9.4.1 Serial 8 bit RGB interface Page21:9.4.2Parallel 24 bits RGB interface Page22: 9.5.1Clock and Data waveform Page23: 9.5.2Digital/Analog RGB timing waveform
3.0		Sep.19,2005	Modify: Page6:5. Input / Output Terminals(CON2) Pin15 Symbol from IF1 change to IF2 Pin16 Symbol from IF2 change to IF1 Page18:11.1 Function Control Register Register R0 : Register R1 : Register R2 : Register R3 : ↓ change to Register R0 :Address(A3~A0)→0000 Register R1 :Address(A3~A0)→0001 Register R2 :Address(A3~A0)→0010 Register R3 :Address(A3~A0)→0011 Page21 11-2 SPI timing characteristic 8SPI write timing 8SPI read timing Add: Page16: 9. Display Color and Gray Scale Reference Page26:.15.Reliability test

			High Temperature Operation Test
4.0		Mar.8,2006	Modify Page3:3.Mechanical Specification Outline Dimension from 84.15 (W)×65.3 (H)×3.45 (D) change to 84.03 (W)×65.24(H)×3.43 (D) Page4: Mechanical Drawing of TFT-LCD Module Page10:7-4 Timing characteristics of input signals→7.4.1 Serial 8 bits RGB interface→VS-DEN time from 18T <sub>H</sub> change to 21 T <sub>H</sub> Page11: 7.4.2 Parallel 24 bits RGB interface VS-DEN time from 18T <sub>H</sub> change to 21 T <sub>H</sub>
5.0		June,22,2006	Page 26: 15. Reliability Test High Temperature Storage Test: From Ta = +70°C, 240 hrs modify to Ta = +80°C, 240 hrs. Low Temperature Storage Test: From Ta = -20°C, 240 hrs modify to Ta = -30°C, 240 hrs. High Temperature Operation Test From Ta = +60°C, 240 hrs modify to Ta = +70°C, 240 hrs. Low Temperature Operation Test From Ta = 0°C, 240 hrs modify to Ta = -30°C, 240 hrs.
6.0	耀霆	July,24,2006	Modify Page 24 13. Optical Characteristics LED Life Time 10000 hrs modify to 30000 hrs
7.0	愷崑	Nov,12,2007	Modify Page 27 14. Delete carton and change packing

# TECHNICAL SPECIFICATION

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**1.Application**

This data sheet applies to a color TFT LCD module, PD035OX1. The module applies to OA product, GPS, which require high quality flat panel display. If you must use in high reliability environment can't over reliability test condition. If you use PD035OX1, Prime View advises your system sides must use PVI-2002A(2005/8 new product change to PVI-2003A) which one generates signal to control PD035OX1.

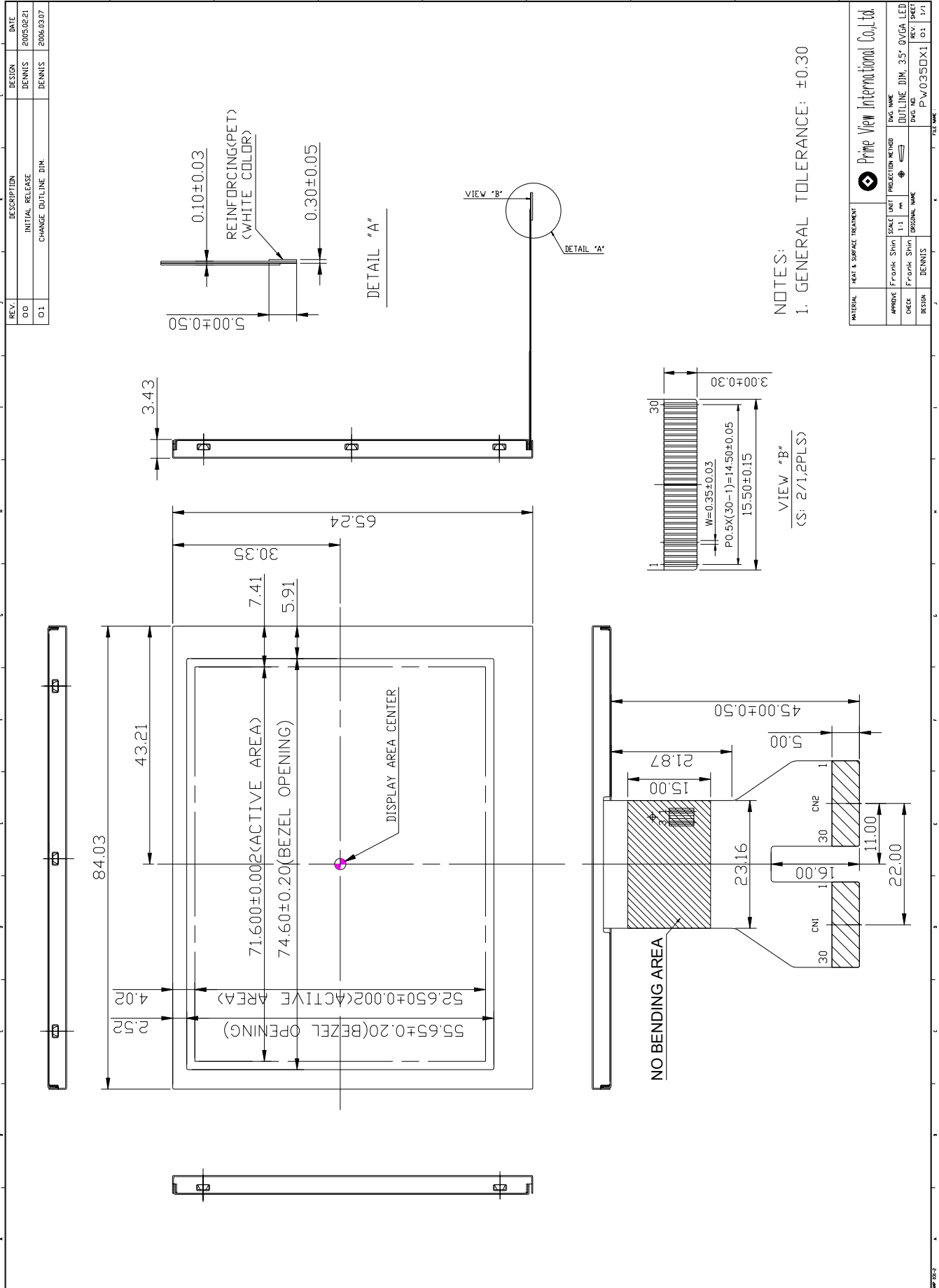
**2. Features**

- . Amorphous silicon TFT LCD panel with back-light unit
- . Pixel in Delta configuration
- . Display Colors : 262,144 colors
- . Optimum Viewing Direction : 6 o'clock
- . TTL transmission interface

**3.Mechanical Specifications**

<b>Parameter</b>	<b>Specifications</b>	<b>Unit</b>
Screen Size	3.5 (diagonal)	inch
Display Format	320x(RGB) x 234	dot
Display colors	262,144	
Active Area	71.6 (H)x52.65 (V)	mm
Pixel Pitch	0.22375 (H)x0.225 (V)	mm
Pixel Configuration	Delta	
Outline Dimension	84.03 (W)x65.24(H)x3.43 (D)	mm
Surface Treatment	Anti – Glare	
Back-light	6-LED	
Weight	42±5	g
Display model	Normally white	
Gray scale inversion direction	6 o'clock [Note13-1]	

4.Mechanical Drawing of TFT-LCD Module



NOTES:  
1. GENERAL TOLERANCE: ±0.30

REV.	DESCRIPTION	DESIGN	DATE
00	INITIAL RELEASE	DENNIS	2005.02.21
01	CHANGE OUTLINE DIM.	DENNIS	2006.03.07

MATERIAL		HEAT & SURFACE TREATMENT		PRIME VIEW INTERNATIONAL CO., LTD.	
APPROVE	FRONT SHIP	SCALE	UNIT	DWG. NAME	DWG. NO.
DRAW	FRONT SHIP	1:1	mm	OUTLINE DIM. 35" DVGA LED	PW0350X1
DESIGN	DENNIS	PROJECTION METHOD	ORIGINAL NAME	REV.	SHEET
		1st		01	1/1

**5. Input / Output Terminals**
**CON1**

FPC Down Connect , 30Pins , Pitch : 0.5 mm

Pin No	Symbol	I/O	Description	Remark
1	D15(G5)	I	Green Data	Note 5-1
2	D14(G4)	I	Green Data	
3	D13(G3)	I	Green Data	
4	D12(G2)	I	Green Data	
5	D11(G1)	I	Green Data	
6	D10(G0)	I	Green Data(LSB)	
7	V <sub>DD2</sub>	I	Analog power supply for source driver	Note 5-2
8	V <sub>8</sub>	I	Gamma correction voltage 8	Note 5-3
9	V <sub>7</sub>	I	Gamma correction voltage 7	
10	V <sub>6</sub>	I	Gamma correction voltage 6	
11	V <sub>5</sub>	I	Gamma correction voltage 5	
12	V <sub>4</sub>	I	Gamma correction voltage 4	
13	V <sub>3</sub>	I	Gamma correction voltage 3	
14	V <sub>2</sub>	I	Gamma correction voltage 2	
15	V <sub>1</sub>	I	Gamma correction voltage 1	
16	V <sub>SS2</sub>	I	Analog ground for source driver	
17	D07(R7)	I	Red Data(MSB)	Note 5-1
18	D06(R6)	I	Red Data	
19	D05(R5)	I	Red Data	
20	D04(R4)	I	Red Data	
21	D03(R3)	I	Red Data	
22	D02(R2)	I	Red Data	
23	D01(R1)	I	Red Data	
24	D00(R0)	I	Red Data(LSB)	
25	CLK	I	Clock signal. Latching data at the rising edge	
26	HS	I	Horizontal sync input in RGB mode and CCIR601	Note 5-4
27	VS	I	Vertical sync input in RGB mode and CCIR601	Note 5-5
28	DEN	I	Input data enable control.(Normally pull low)	Note 5-6
29	V <sub>CC</sub>	I	Digital power supply for source driver IC	Note 5-7
30	V <sub>COM</sub>	I	Voltage for common electrode	Note 5-8

**CON2**

FPC Down Connect , 30Pins , Pitch : 0.5 mm

Pin No	Symbol	I/O	Description	Remark
1	VLED	I	Power supply for LED	Note 5-9
2	GLED1	I	Ground for LED	
3	GLED2	I	Ground for LED	
4	NC	-	NC	
5	VGH	I	Positive power for gate driver	Note 5-10
6	VDD1	I	Power supply for gate logic circuit	Note 5-11
7	VSS1	I	Ground for gate driver	
8	VEE	I	Negative power for gate driver	Note 5-12
9	VDD1	I	Power supply for gate logic circuit	Note 5-11
10	GND	I	Digital ground for source driver IC	
11	RESETB	I	Hardware global reset, (low active)	
12	VSET	I	Externally/Internally gamma voltage setup	
13	U/D	I	Up/Down control for gate driver	Note 5-13
14	L/R	I	Left/Right control for source driver	
15	IF2	I	Select the input data format (Serial RGB, Parallel RGB, CCIR601/656)	Note 5-14
16	IF1	I		
17	SPENA	I	Serial port data enable signal (normally pull high)	
18	SPCK	I	Serial port clock. (Normally pull high)	
19	SPDA	I/O	Serial port data input/output	
20	POL	O	Polarity select for the line inversion control signal	Note 5-15
21	D27(B7)	I	Blue Data(MSB)	Note 5-1
22	D26(B6)	I	Blue Data	
23	D25(B5)	I	Blue Data	
24	D24(B4)	I	Blue Data	
25	D23(B3)	I	Blue Data	
26	D22(B2)	I	Blue Data	
27	D21(B1)	I	Blue Data	
28	D20(B0)	I	Blue Data(LSB)	
29	D17(G7)	I	Green Data(MSB)	
30	D16(G6)	I	Green Data	



Note 5-1 : Digital data input. DX0 is LSB and DX7 is MSB.

If parallel RGB input mode is used, D0X, D1X, and D2X indicate R, G and B data in turn.  
 If serial RGB or CCIR601/656 input mode is selected, only D07~D00 are used, and others short to Vss.

Note 5-2 : V<sub>DD2</sub> Typ. = +5V

Note 5-3 : The output voltage is determined by the digital input data. If digital RGB or CCIR601/656 input mode is selected, The 8 gamma correction reference voltages can be set to externally or generate internally.

If VSET = "H", the gamma correction voltage generated externally

If VSET = "L", the default value is as below : (When V<sub>DD</sub> =+5V)

	V1	V2	V3	V4	V5	V6	V7	V8
Default Voltage(V)	4.29	3.73	3.33	2.94	2.62	2.22	1.51	0.48

Note 5-4 : Horizontal sync input in digital RGB mode. Or HREF input in CCIR601 mode.  
 ( Short to Vss if not used )

Note 5-5 : Vertical sync input in digital RGB mode. Or V123 input in CCIR601 mode.  
 ( Short to Vss if not used )

Note 5-6 : Digital RGB data input format  
 For digital RGB input data format, both SYNC. Mode and DEN mode are supported. If DEN signal is fixed low, SYNC. Mode is used. Otherwise , DEN mode is used.

Note 5-7 : V<sub>CC</sub> Typ. = +3.3V

Note 5-8 : V<sub>COM</sub> Typ. =+6.0Vpp

Note 5-9 : I<sub>LED</sub> Typ. = 20mA., V<sub>LED</sub> Typ. = 9V

Note 5-10 : V<sub>GH</sub> Typ. =+15V.

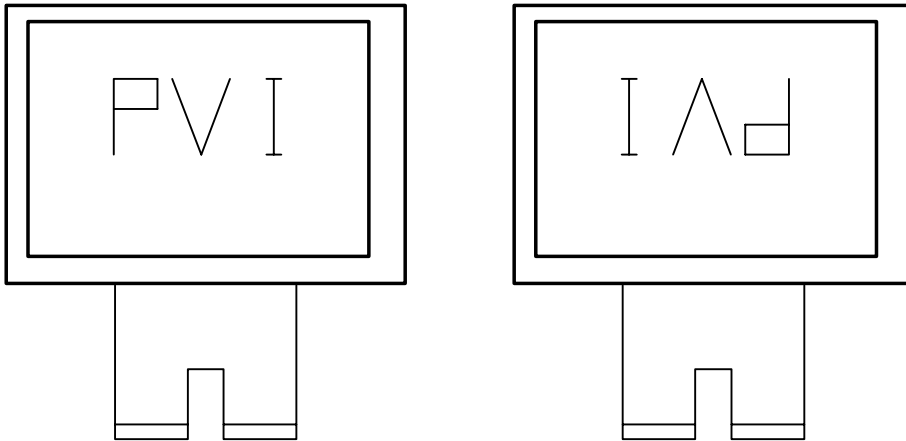
Note 5-11 : V<sub>DD1</sub> Typ. =+3.3V.

Note 5-12 : V<sub>EE</sub> Typ. = -15V.

Note 5-13 : The definition of L/R , U/D

U/D(PIN 13)=Low L/R(PIN 14)=High

U/D(PIN 13)=High L/R(PIN 14)=Low



Note 5-14 : IF1,IF2 control the input data format.

IF2,IF1	Input data format
L,L (default)	Serial RGB
L,H	Parallel RGB
H,L	CCIR601
H,H	CCIR656

Note 5-15 : When POL=L, output voltage is negative polarity.  
When POL=H, output voltage is positive polarity.

6. Absolute Maximum Ratings

V<sub>SS1</sub>=V<sub>SS2</sub>=0 V , Ta = 25 °C

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Supply voltage for source driver	V <sub>CC</sub>	-0.3	+7.0	V	
	V <sub>DD2</sub>	-0.3	+7.0	V	
Supply voltage for gate driver	V <sub>DD1</sub>	-0.3	+7.0	V	
	H Level V <sub>GH</sub>	-0.3	+32.0	V	
	L Level V <sub>EE</sub>	-22.0	+0.3	V	
	V <sub>GH</sub> -V <sub>EE</sub>	-0.3	+45.0	V	
Input signal voltage	V <sub>IN</sub>	-0.3	V <sub>DD</sub> +0.3	V	

7. Electrical Characteristics

7-1 Operating condition

$V_{SS1}=V_{SS2}=0\text{ V}$  ,  $T_a = 25\text{ }^\circ\text{C}$

Parameter		Symbol	MIN.	Typ.	MAX.	Unit	Remark
Supply voltage for source driver	Logic	V <sub>CC</sub>	+3.0	+3.3	+3.6	V	
	Analog	V <sub>DD2</sub>	+3.8	+5.0	+5.5	V	
Supply voltage for gate driver	Logic	V <sub>DD1</sub>	+3.0	+3.3	+3.6	V	
	H level	V <sub>GH</sub>	+10	+15	+30	V	
	L level	V <sub>EE</sub>	-17	-15	-5	V	
Signal input voltage	H level	V <sub>IH</sub>	0.7V <sub>CC</sub>	-	V <sub>CC</sub>	V	
	L level	V <sub>IL</sub>	0	-	0.3V <sub>CC</sub>	V	
Signal output voltage	H level	V <sub>OH</sub>	0.8V <sub>CC</sub>	-	V <sub>CC</sub>	V	
	L level	V <sub>OL</sub>	0	-	0.2V <sub>CC</sub>	V	
V <sub>COM</sub>		V <sub>COMAC</sub>	-	+6.0	-	V <sub>P-P</sub>	AC Component of V <sub>COM</sub>
		V <sub>COMDC</sub>	-	1.0	-	V	DC Component of V <sub>COM</sub> Note 7-1

Note 7-1 : PVI strongly suggests that the V<sub>COMDC</sub> level shall be adjustable , and the adjustable level range is 1V±1V , every module's V<sub>COMDC</sub> level shall be carefully adjusted to show a best image performance.

7-2 Recommended driving condition for LED backlight

$T_a = 25\text{ }^\circ\text{C}$

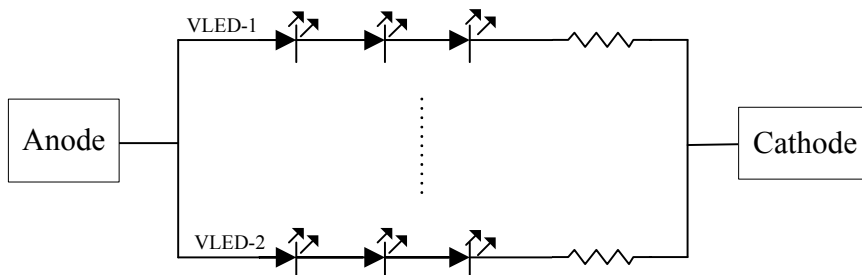
Parameter	Symbol	Min	TYP	MAX	Unit	Remark
Supply voltage of LED backlight	V <sub>LED</sub>	-	-	(11.0)	V	Note 7-1
Supply current of LED backlight	I <sub>LED</sub>	-	20	-	mA	Note 7-2
Backlight Power Consumption	P <sub>LED</sub>	-	-	440	mW	Note 7-3

Note 7-1 I<sub>LED</sub>=20mA, Constant Current

Note 7-2 : The LED driving condition is defined for each LED module. (3 LED Serial)

Input current = 20mA \* 2

Note 7-3 :  $P_{LED} = 2 * I_{LED} * V_{LED}$  .



**7-3 Power consumption**
 $V_{SS1}=V_{SS2}=0\text{ V}$  ,  $T_a = 25\text{ }^\circ\text{C}$ 

Parameter	Symbol	Conditions	TYP.	MAX.	Unit	Remark
Supply current for gate driver (Hi level)	I <sub>GH</sub>	V <sub>GH</sub> = +15V	0.2	0.5	mA	
Supply current for gate driver (Logic)	I <sub>DD1</sub>	V <sub>DD1</sub> = +3.3V	0.05	0.1	mA	
Supply current for gate driver (Low level)	I <sub>EE</sub>	V <sub>EE</sub> = -15V	0.2	0.5	mA	V <sub>EE</sub> center voltage
Supply current for source driver (Analog)	V <sub>DD2</sub>	V <sub>DD2</sub> = +5V	5.0	8.0	mA	
Supply current for source driver (Logic)	V <sub>CC</sub>	V <sub>CC</sub> = +3.3V	4.5	7.0	mA	
LCD panel power consumption	-		48	80	mW	
Backlight power consumption	P <sub>LED</sub>		400	440	mW	
Total power consumption	-		0.45	0.52	W	

\* Above data measured on serial mode:

If on parallel mode, I<sub>CC</sub> Typ.= 3.0mA, Max.=5.0mA ;

panel power consumption Typ.= 41.5mW      Max.= 72.8mW.

If on CCIR601/656 mode, I<sub>CC</sub> Typ.= 6.0mA, Max.=10.0mA ;

panel power consumption Typ.= 51.4mW      Max.= 89.3mW.

**7-4 Timing characteristics of input signals**
**7.4.1 Serial 8 bits RGB interface**

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
CLK period	T <sub>OSC</sub>	-	52	-	ns	Note 7-4
Data setup time	T <sub>SU</sub>	12	-	-	ns	
Data hold time	T <sub>HD</sub>	12	-	-	ns	
HS period	T <sub>H</sub>	-	1224	-	T <sub>OSC</sub>	
HS pulse width	T <sub>HS</sub>	5	90	-	T <sub>OSC</sub>	
HS rising time	T <sub>Cr</sub>	-	-	700	ns	
HS falling time	T <sub>Cf</sub>	-	-	300	ns	
VS pulse width	T <sub>VS</sub>	1	3	5	T <sub>H</sub>	
VS rising time	T <sub>Vr</sub>	-	-	700	ns	
VS falling time	T <sub>Vf</sub>	-	-	1.5	us	
HS falling to VS falling time for odd field	T <sub>HVO</sub>	0	3	-	T <sub>OSC</sub>	
VS falling to HS falling time for even field	T <sub>HVE</sub>	0	3	-	T <sub>OSC</sub>	
VS-DEN time	T <sub>VSE</sub>	-	21	-	T <sub>H</sub>	
HS-DEN time	T <sub>HE</sub>	108	204	264	T <sub>OSC</sub>	
DEN pulse width	T <sub>EP</sub>	-	960	-	T <sub>OSC</sub>	
VS period		-	262	-	T <sub>H</sub>	

Note 7-4 : When SYNC mode is used, 1<sup>st</sup> data start from 204<sup>th</sup> CLK after HS fallings.

**7.4.2 Parallel 24 bits RGB interface**

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
CLK period	$T_{OSC}$	-	156	-	ns	Note 7-5
Data setup time	$T_{SU}$	12	-	-	ns	
Data hold time	$T_{HD}$	12	-	-	ns	
HS period	$T_H$	-	408	-	$T_{OSC}$	
HS pulse width	$T_{HS}$	5	30	-	$T_{OSC}$	
HS rising time	$T_{Cr}$	-	-	700	ns	
HS falling time	$T_{Cf}$	-	-	300	ns	
VS pulse width	$T_{VS}$	1	3	5	$T_H$	
VS rising time	$T_{Vr}$	-	-	700	ns	
VS falling time	$T_{Vf}$	-	-	1.5	us	
HS falling to VS falling time for odd field	$T_{HVO}$	0	3	-	$T_{OSC}$	
VS falling to HS falling time for even field	$T_{HVE}$	0	3	-	$T_{OSC}$	
VS-DEN time	$T_{VSE}$	-	21	-	$T_H$	
HS-DEN time	$T_{HE}$	36	68	88	$T_{OSC}$	
DEN pulse width	$T_{EP}$	-	320	-	$T_{OSC}$	
VS period		-	262	-	$T_H$	

Note 7-5 : When SYNC mode is used, 1<sup>st</sup> data start from 68<sup>th</sup> CLK after HS fallings.

**7.4.3 CCIR601/656 Interface**

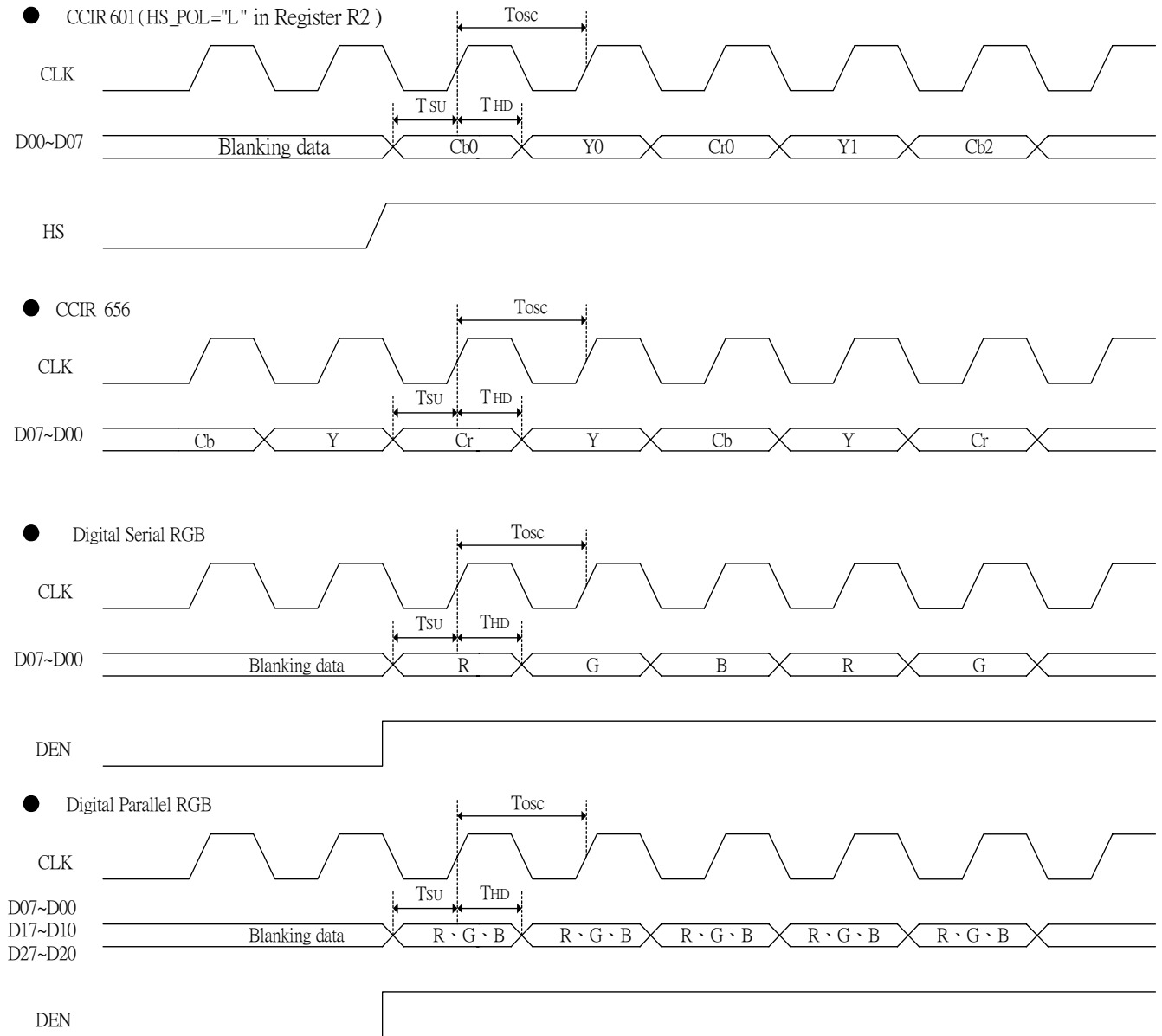
Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
CLK period	$T_{OSC}$	-	37	-	ns	
Data setup time	$T_{SU}$	12	-	-	ns	
Data hold time	$T_{HD}$	12	-	-	ns	

**7.4.4 Hardware reset timing**

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
RESETB low pulse width	$T_{RSB}$	200	-	-	ns	

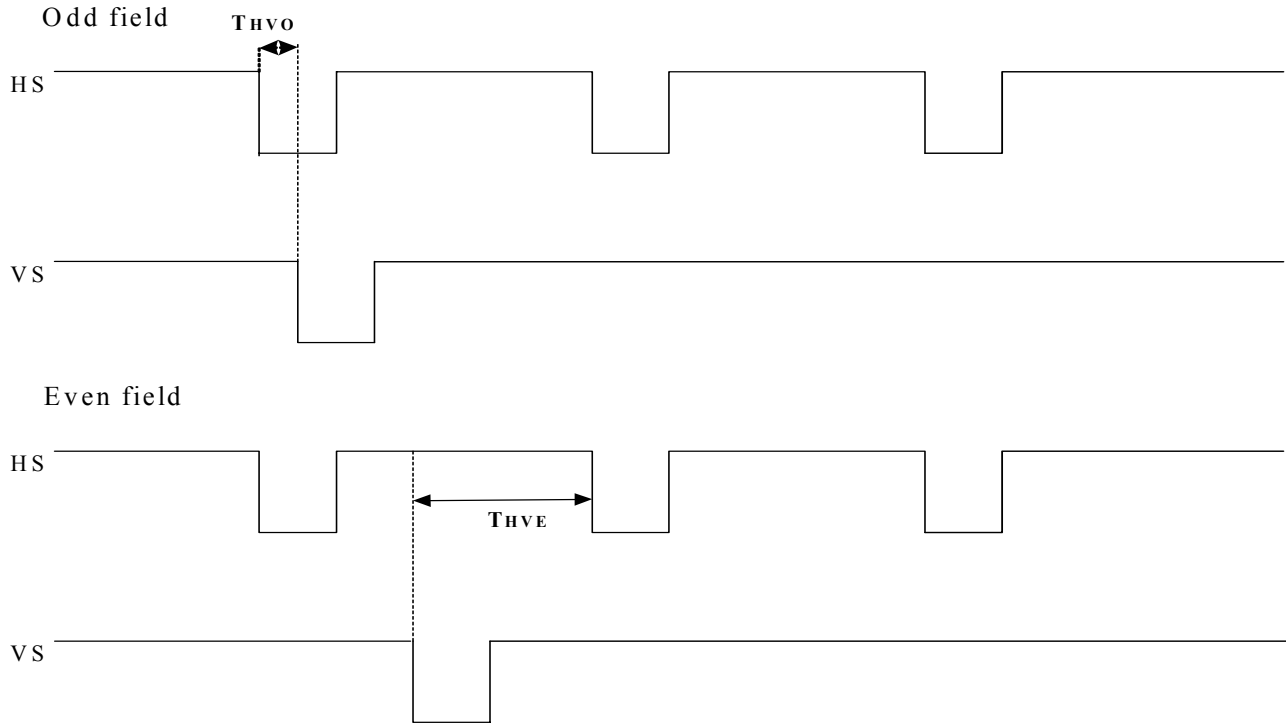
7.5 Timing controller timing chart

7.5.1 Clock and Data waveform

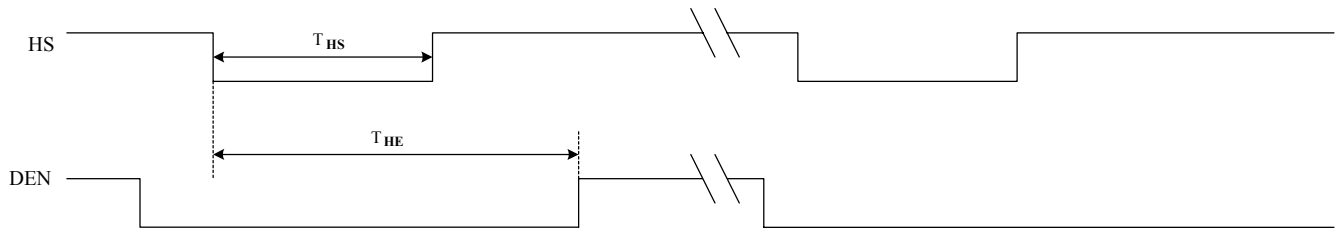


7.5.2 HS,VS,DEN timing waveform

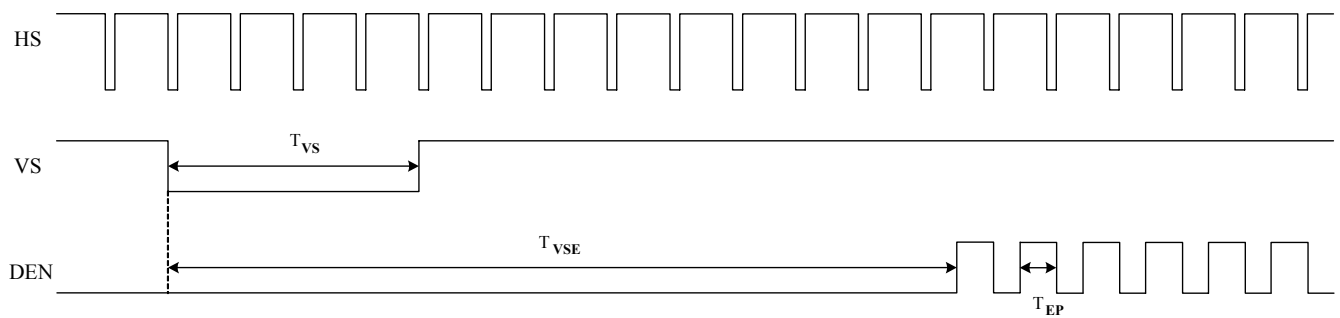
**HS and VS timing relationship**



**HS and DEN timing relationship**

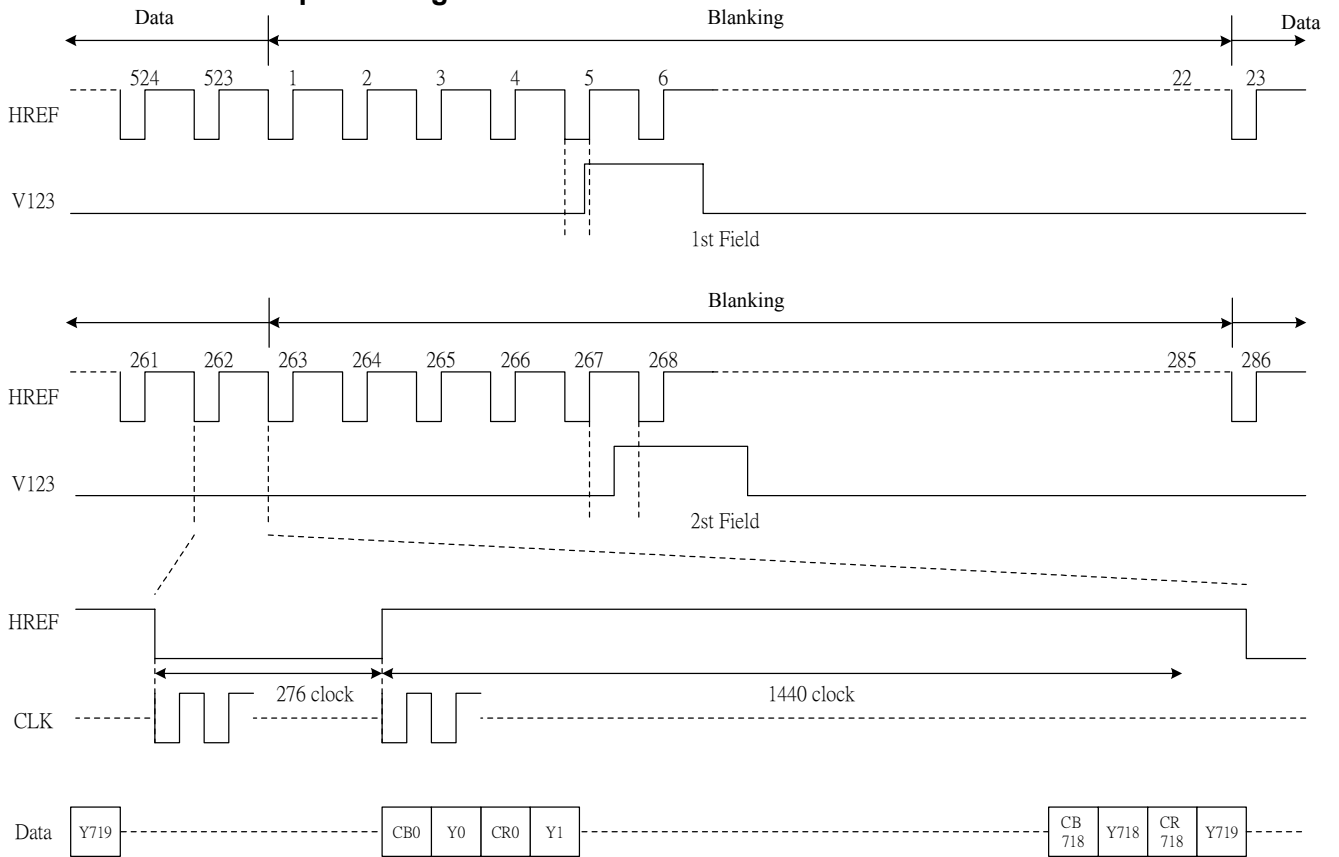


**HS, VS and DEN timing relationship**

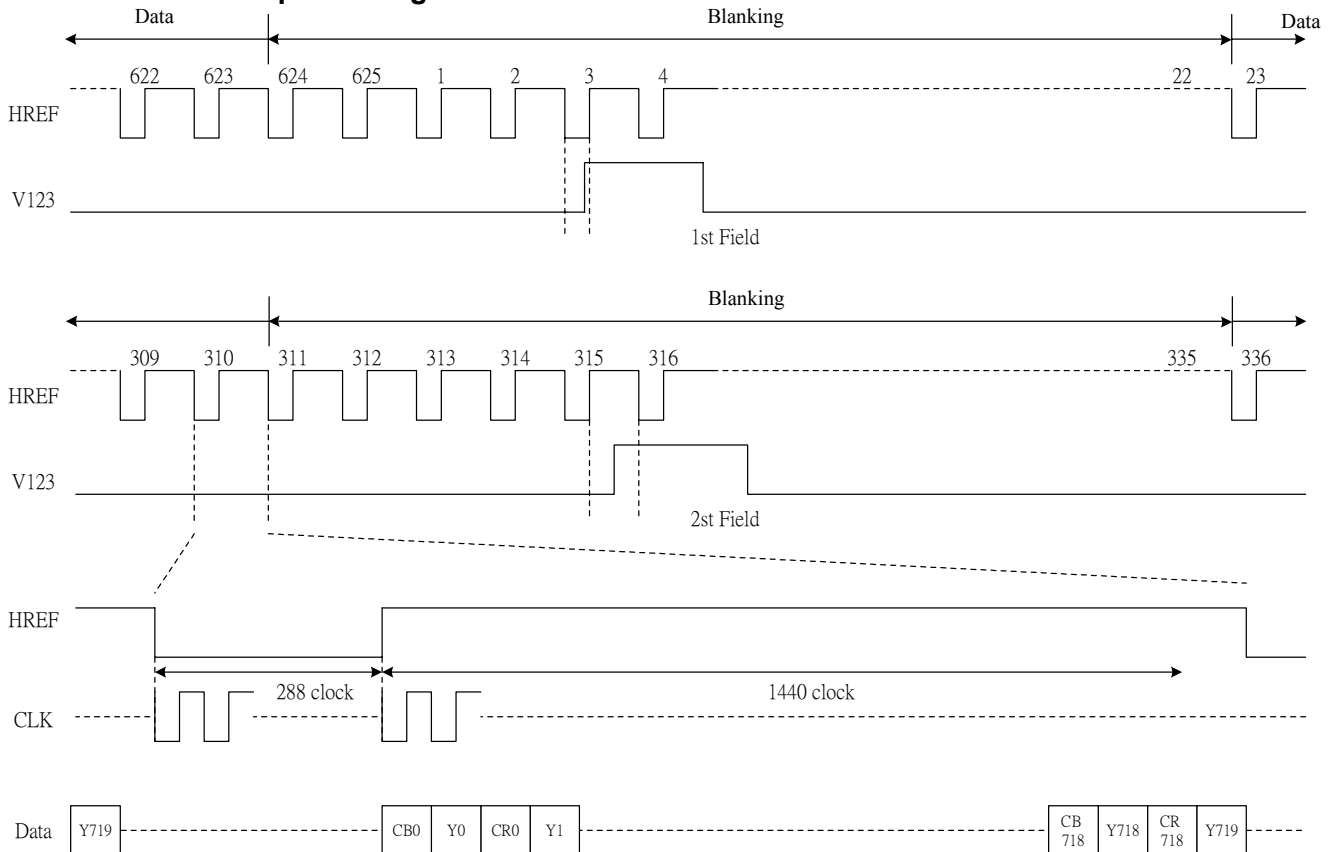


7.5.3 CCIR601 timing waveform (VS\_POL="H", HS\_POL="L" in Register R2)

**ITU-R BT.601 NTSC Input Timing**

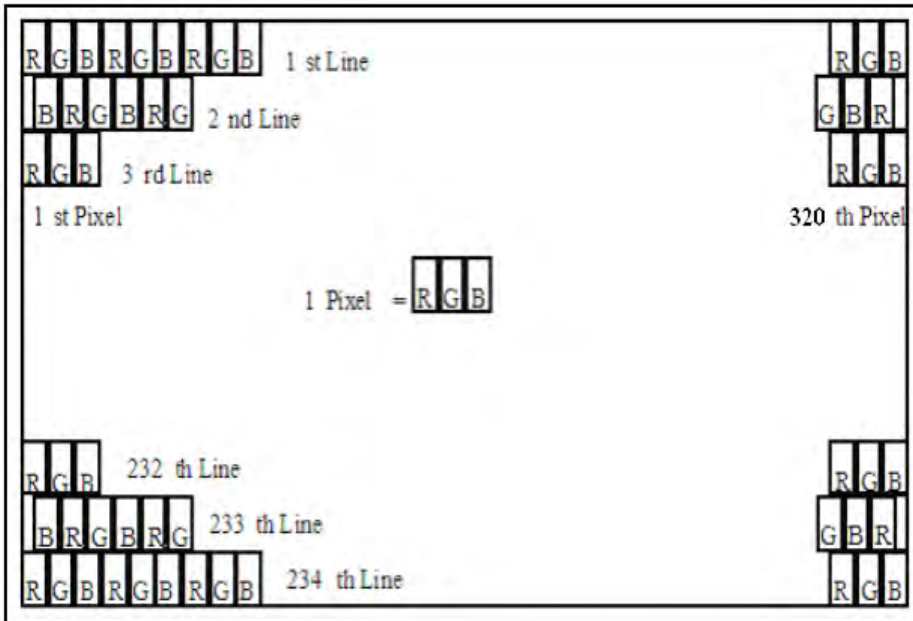


**ITU-R BT.601 PAL Input Timing**





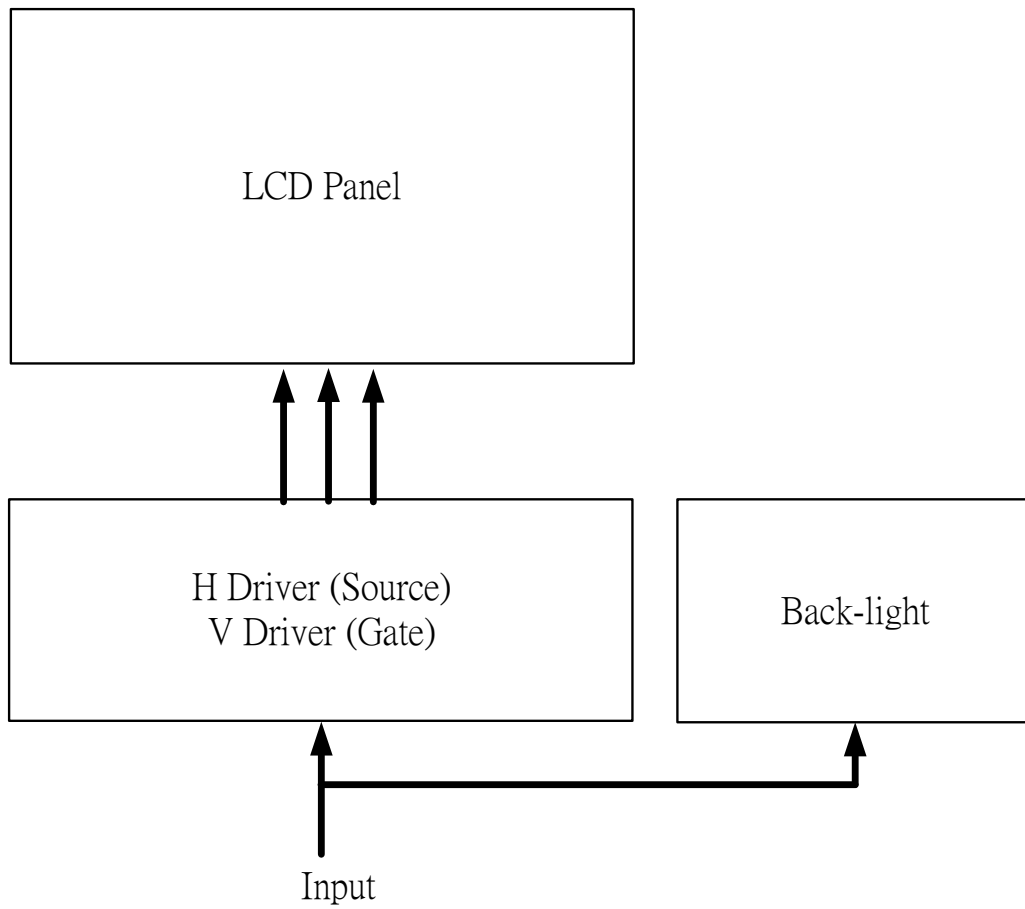
8. Pixel Arrangement



9. Display Color and Gray Scale Reference

Color		Input Color Data																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (01)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (02)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Green	Green (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Blue	Blue (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

10. Block Diagram



## 11. SPI Register Description and Timing Characteristics

### 11.1 Function Control Register

**Register R0 :Address(A3~A0)→0000**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserve d	STHD1	STHD0	STHP4	STHP3	STHP2	STHP1	STHP0
Default	0	0	0	0	0	0	0	0

STHD [1:0] : adjust start pulse position by dot

STHD1	STHD0	STH position adjust by dot
1	1	-1
1	0	-2
0	0	0
0	1	+1

STHP [4:0] : adjust start pulse position by pixel

STHP4	STHP3	STHP2	STHP1	STHP0	STH position adjust by pixel
1	1	1	1	1	-1
1	1	1	1	0	-2
1	1	1	0	1	-3
1	1	1	0	0	-4
1	1	0	1	1	-5
1	1	0	1	0	-6
1	1	0	0	1	-7
1	1	0	0	0	-8
1	0	1	1	1	-9
1	0	1	1	0	-10
1	0	1	0	1	-11
1	0	1	0	0	-12
1	0	0	1	1	-13
1	0	0	1	0	-14
1	0	0	0	1	-15
1	0	0	0	0	-16
0	0	0	0	0	0
0	0	0	0	1	+1
0	0	0	1	0	+2
0	0	0	1	1	+3
0	0	1	0	0	+4
0	0	1	0	1	+5
0	0	1	1	0	+6
0	0	1	1	1	+7
0	1	0	0	0	+8
0	1	0	0	1	+9
0	1	0	1	0	+10
0	1	0	1	1	+11
0	1	1	0	0	+12
0	1	1	0	1	+13
0	1	1	1	0	+14
0	1	1	1	1	+15

**Register R1 :Address(A3~A0)→0001**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	STVP3	STVP2	STVP1	STVP0	STVNT1	STVNT0	STVPAL1	STVPAL0
Default	0	0	0	0	0	0	0	1

**STVP [3:0] : adjust first line position by line**

STVP3	STVP2	STVP1	STVP0	STV position adjust by line
1	1	1	1	-1
1	1	1	0	-2
1	1	0	1	-3
1	1	0	0	-4
1	0	1	1	-5
1	0	1	0	-6
1	0	0	1	-7
1	0	0	0	-8
0	0	0	0	0
0	0	0	1	+1
0	0	1	0	+2
0	0	1	1	+3
0	1	0	0	+4
0	1	0	1	+5
0	1	1	0	+6
0	1	1	1	+7

**STVNT[1:0]:** When NTSC mode, the relationship of first line in Even field and Odd field.

00: First line in Even field = First line in Odd field.

01: First line in Even field = First line in Odd field +1.

10: No use.

11: First line in Even field = First line in Odd field -1.

**STVPAL[1:0]:** When PAL mode, the relationship of first line in Even field and Odd field.

(Only for CCIR601/656 mode)

00: First line in Even field = First line in Odd field.

01: First line in Even field = First line in Odd field +1.

10: No use.

11: First line in Even field = First line in Odd field -1.

**Register R2 :Address(A3~A0)→0010**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	reserved	reserved	HS_POL	VS_POL	NPC_IN	NPC_SET
Default	0	0	0	1	0	0	1	0

HS\_POL: HS polarity setting.

HS\_POL = “L”, negative polarity.

HS\_POL = “H”, positive polarity.

VS\_POL: VS polarity setting.

VS\_POL = “L”, negative polarity.

VS\_POL = “H”, positive polarity.

NPC\_IN: Define the NTSC/PAL mode by SPI.

NPC\_IN = “L”, PAL. (Only for CCIR601/656 mode)

NPC\_IN = “H”, NTSC.

NPC\_SET: Set the NTSC/PAL auto detection or define by NPC\_IN.

NPC\_SET = “L”, auto detection.

NPC\_SET = “H”, define by SPI.

**Register R3 :Address(A3~A0)→0011**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	reserved	reserved	PWD_EN	OSDCLK P	OSDHSP	OSDVSD
Default	0	0	1	0	1	0	1	1

PWD\_EN: Set DAC power saving function.

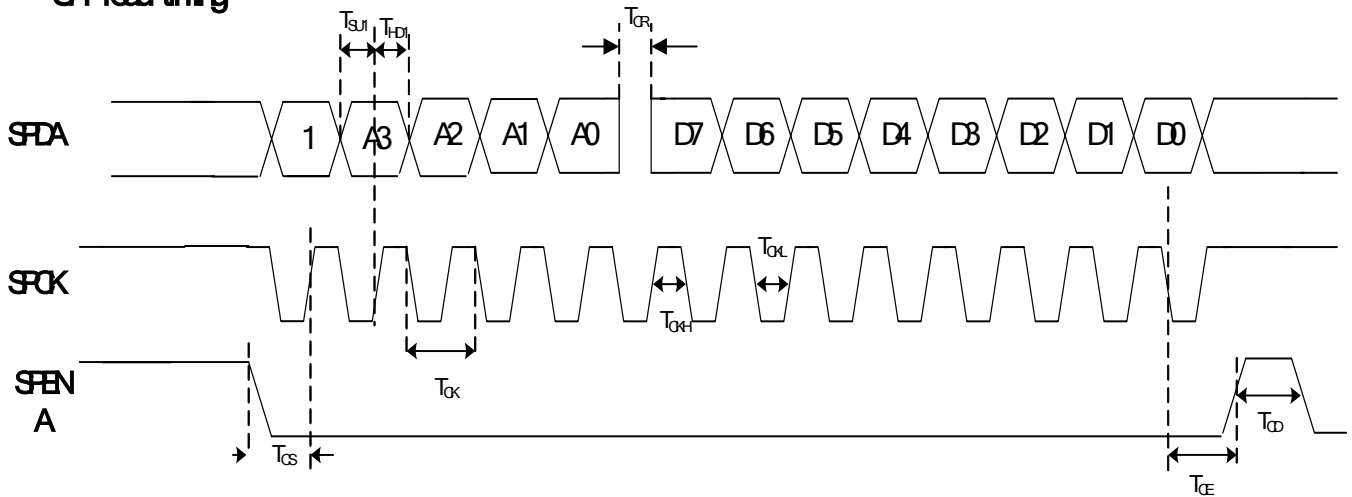
PWD\_EN = “L”, disable. The DAC is always power on.

PWD\_EN = “H”, enable.

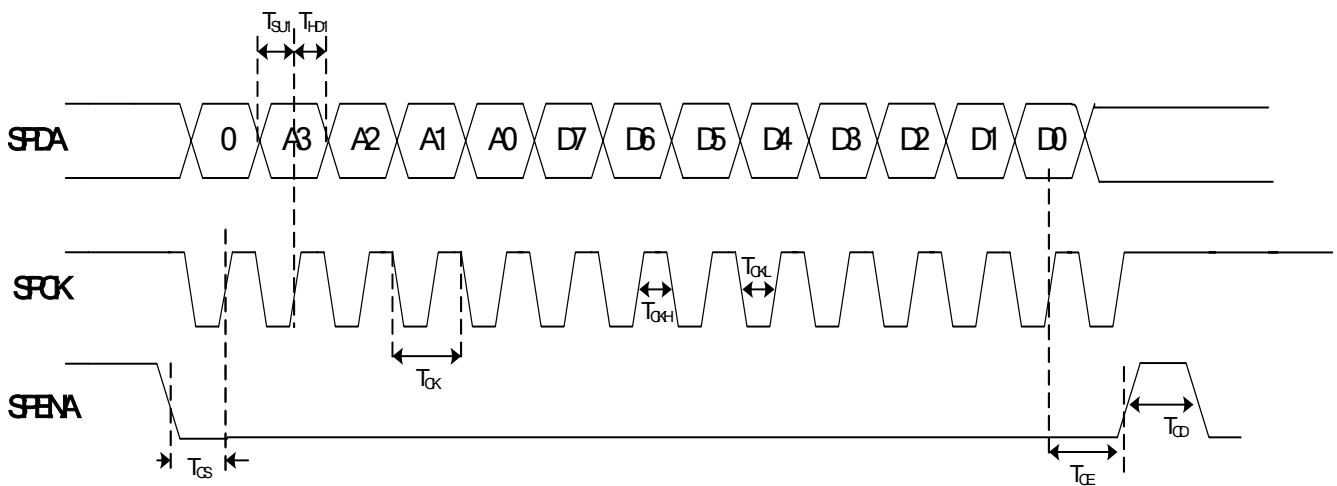
11-2 SPI timing characteristic

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
SPCK period	$T_{CK}$	60	-	-	ns	
SPCK high width	$T_{CKH}$	30	-	-	ns	
SPCK low width	$T_{CKL}$	30	-	-	ns	
Data setup time	$T_{SU1}$	12	-	-	ns	
Data hold time	$T_{HD1}$	12	-	-	ns	
SPENA to SPCK setup time	$T_{CS}$	20	-	-	ns	
SPENA to SPDA hold time	$T_{CE}$	20	-	-	ns	
SPENA high pulse width	$T_{CD}$	50	-	-	ns	
SPDA output latency	$T_{CR}$	-	1/2	-	$T_{CK}$	

· SPI 'read' timing

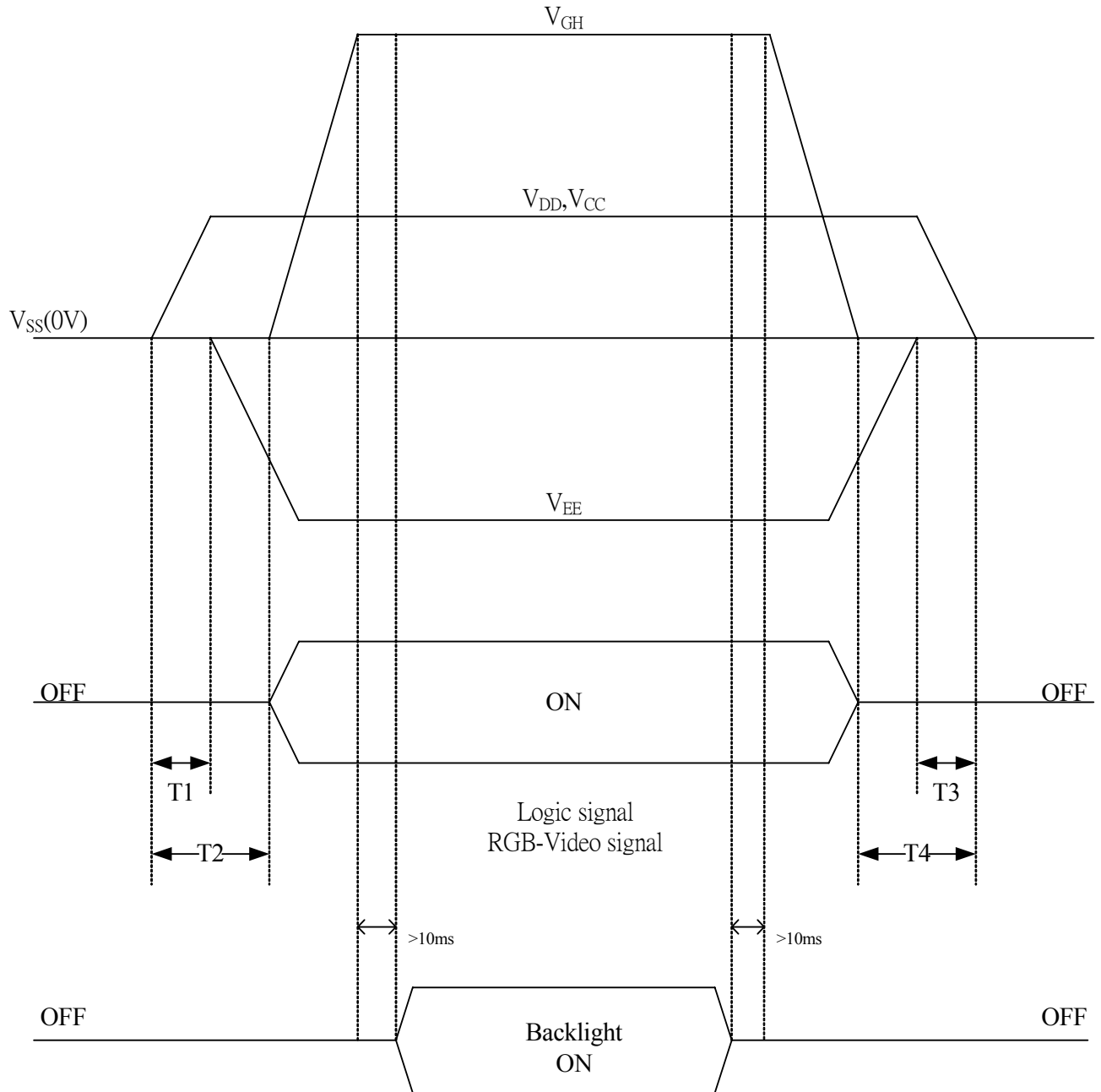


· SPI 'write' timing



12. Power On Sequence

The Power on sequence only effect by  $V_{CC}$ ,  $V_{SS}$ ,  $V_{DD}$ ,  $V_{EE}$  and  $V_{GH}$ , the others do not care.



- 1)  $10ms \leq T1 < T2$
- 2)  $0ms < T3 \leq T4 \leq 10ms$

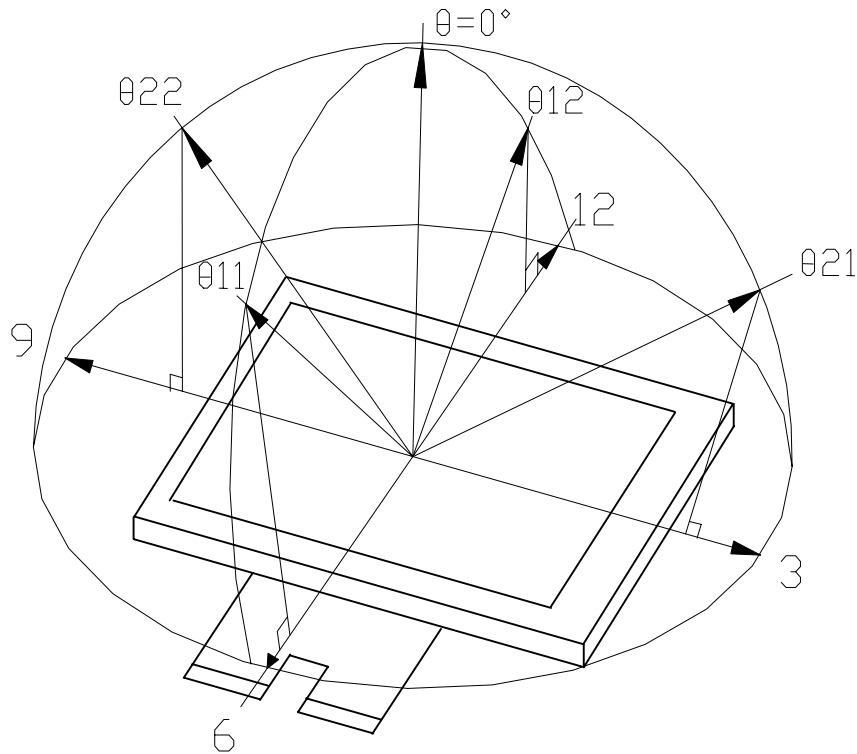


13. Optical Characteristics

Ta = 25°C

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	$\theta 21, \theta 22$	$CR \geq 10$	45	50	---	deg	Note 13-1
	Vertical	$\theta 11$		30	35	---	deg	
		$\theta 12$		10	15	---	deg	
Contrast Ratio		CR	At optimized Viewing angle	200	400	---		Note 13-2
Response time	Rise	Tr	$\theta = 0^\circ$	---	15	30	ms	Note 13-3
	Fall	Tf		---	25	50	ms	
Uniformity		U	9 point	70	75	-	%	Note 13-4
Brightness		-	Center point	200	250	-	cd/m <sup>2</sup>	Note 13-5
White		x	$\theta = 0^\circ$	0.28	0.31	0.34	-	Note 13-5
Chromaticity		y	$\theta = 0^\circ$	0.30	0.33	0.36	-	
LED Life Time		-	25°C	-	30000	-	hrs	Note 13-6

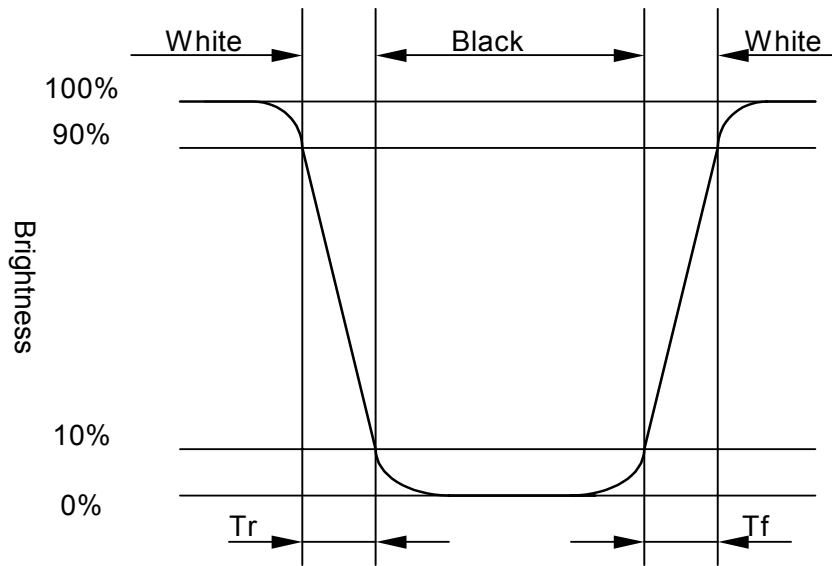
Note 13-1 : The definitions of viewing angles



Note 13-2 :  $CR = \frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$

Contrast ratio is measured in optimum common electrode voltage.

Note 13-3 : The definition of response time :



Note 13-4 : The uniformity of LCD is defined as

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

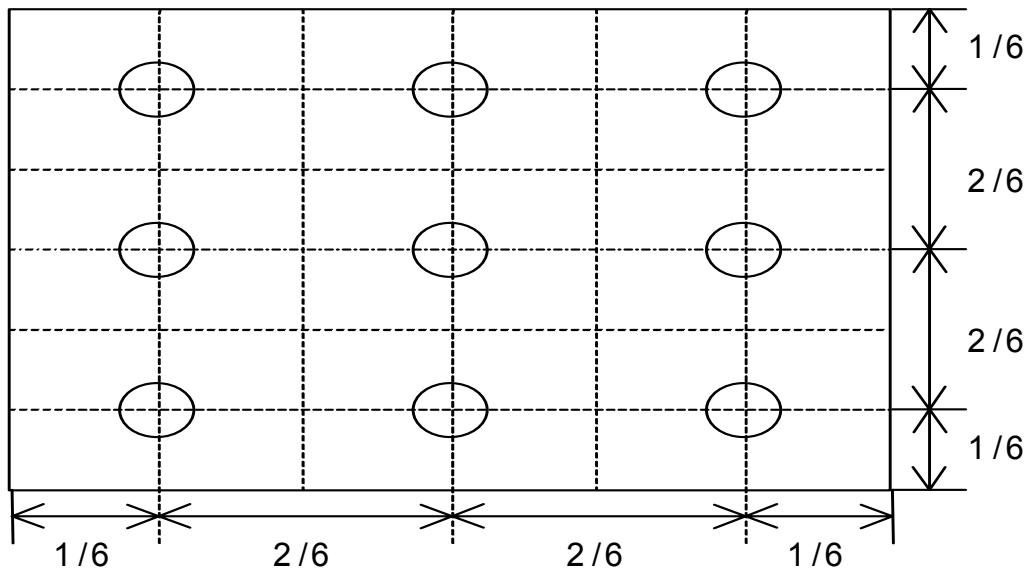
Luminance meter : BM-5A or BM-7 fast (TOPCON)

Measurement distance : 500 mm +/- 50 mm

Ambient illumination : < 1 Lux

Measuring direction : Perpendicular to the surface of module

The test pattern is white (Gray Level 63).



Note 13-5 : Topcon BM-7(fast) luminance meter 1.0° field of view is used in the testing (use PVI backlight after 5 minutes operating), I<sub>LED</sub> = 20mA.

Note 13-6 : The “LED Life time “ is defined as the module brightness decrease to 50% original Brightness that the ambient temperature is 25°C and I<sub>LED</sub> =20mA.

## 14. Handling Cautions

### 14-1) Mounting of module

- a) Please power off the module when you connect the input/output connector.
- b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.
  - 1. The noise from the backlight unit will increase.
  - 2. The output from inverter circuit will be unstable.
  - 3. In some cases a part of module will heat.
- c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
- d) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

### 14-2) Precautions in mounting

- a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
- b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

### 14-3) Adjusting module

- a) Adjusting volumes on the rear face of the module have been set optimally before shipment.
- b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

### 14-3) Others

- a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
- b) Store the module at a room temperature place.
- c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
- e) Observe all other precautionary requirements in handling general electronic components.
- f) Please adjust the voltage of common electrode as material of attachment by 1 module.

**15. Reliability Test**

No	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +80°C, 240 hrs
2	Low Temperature Storage Test	Ta = -30°C, 240 hrs
3	Low Temperature Operation Test	Ta = -30°C, 240 hrs
4	High Temperature Operation Test	Ta = +70°C, 240hrs
5	High Temperature & High Humidity Operation Test	Ta = +60°C, 90%RH, 240 hrs
6	Thermal Cycling Test (non-operating)	-20°C ← → +70°C , 200 Cycles 30 min            30 min
7	Vibration test (non-operating)	Frequency : 10 ~ 55Hz Amplitude : 1mm , sweep time : 11 mins Test period : 6 cycles for each direction of X,Y, Z
8	Shock Test(non-operating)	100G , 6ms , 3cycles for each direction of X,Y,Z
9	Electrostatic Discharge Test (non-operating)	200pF, 0Ω Machine mode = ±200V 1 time / each terminal

Ta: ambient temperature

Note : The protective film must be removed before temperature test.

[Criteria]

In the standard conditions, there is not display function NG issue occurred. (Including: line defect ,no image). All the cosmetic specification is judged before the reliability stress.

16. Packing

REV.	DESCRIPTION	DESIGN	DATE
△	Cancel the carton(50-0100101)	Ethan	2007.11.5

**NOTE:**

1. One layer include: 1 piece of cushion sheet, 12 pcs panel & 1 piece of tray.
2. Q'TY: 120 pcs panel/carton.
3. Dimension: 455\*375\*190mm
4. Weight: 7.7 KG
5. tray需180°交叉堆疊, 堆疊後可從側邊檢視圓弧防呆方向是否正確

6	50-0100091	CARTON INTERNAL	1	
5	50-0500041	摺口袋450*380*700mm	1	抗靜電
4		PD035VX2	120	
3	50-0200059	EPE CUSHION SHEET	10	抗靜電
2	50-0301181	TRAY	11	抗靜電
1	50-0300491	EPE FOAM	2	
ITEM	PART NO.	DESCRIPTION	QTY	REMARK

MTL.SPEC.		UNSPECIFIED TOL'S ±5.0mm		REMARK	
		ANGLE			
		ROUGHNESS			
APPROVE	Frank Shin	'05.01.21	SCALE	UNIT	SHEET
CHECK	Frank Shin	'05.01.21	1:1	mm	1 OF 1
DESIGN	Dennis	'05.01.21	MTL.NO.		DWG.NO.

**元太科技股份有限公司**  
Prime View Internation Co.,ltd.

DWG.TITLE  
PD035OX1 PACKING Dim

								REV.	A4
								01	SIZE

**Appendix**

**CON 2**

