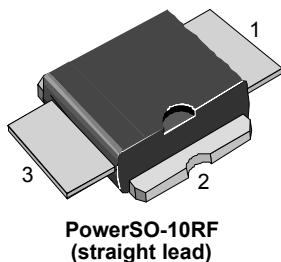


35 W, 12.5 V, HF to 1 GHz RF power LDMOS transistor



Features

Order code	Frequency	V _{DD}	P _{OUT}	Gain	Efficiency
PD55035STR1-E	500 MHz	12.5 V	35 W	16.9 dB	62%

- Excellent thermal stability
- Common source configuration
- P_{OUT} = 35 W with 16.9 dB at 500 MHz, 12.5 V
- New RF plastic package

Pin connection	
Pin	Connection
1	Drain
2	Source
3	Gate

Description

The device is a common source N-channel, enhancement-mode lateral field-effect RF power transistor. It is designed for high gain, broad band commercial and industrial applications. It operates at 12 V in common source mode at frequencies of up to 1 GHz. The device boasts the excellent gain, linearity and reliability of ST's latest LDMOS technology mounted in the first true SMD plastic RF power package, PowerSO-10RF. Device's superior linearity performance makes it an ideal solution for car mobile radio. The PowerSO-10 plastic package, designed to offer high reliability, is the first ST JEDEC approved, high power SMD package. It has been specially optimized for RF needs and offers excellent RF performance and ease of assembly.



Product status link									
PD55035STR1-E									
Product summary									
<table border="1"> <tbody> <tr> <td>Order code</td> <td>PD55035STR1-E</td> </tr> <tr> <td>Marking</td> <td>PD55035S</td> </tr> <tr> <td>Package</td> <td>PowerSO-10RF (straight lead)</td> </tr> <tr> <td>Packing</td> <td>Tape and reel</td> </tr> </tbody> </table>		Order code	PD55035STR1-E	Marking	PD55035S	Package	PowerSO-10RF (straight lead)	Packing	Tape and reel
Order code	PD55035STR1-E								
Marking	PD55035S								
Package	PowerSO-10RF (straight lead)								
Packing	Tape and reel								

1 Electrical data

Table 1. Absolute maximum ratings ($T_C = 25^\circ\text{C}$)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current	7	A
P_{TOT}	Total power dissipation at $T_C = 70^\circ\text{C}$	95	W
T_J	Maximum operating junction temperature	165	$^\circ\text{C}$
T_{stg}	Storage temperature range	-65 to 150	$^\circ\text{C}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.0	$^\circ\text{C}/\text{W}$

2 Electrical characteristics

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Zero gate voltage drain leakage current	$V_{GS} = 0 \text{ V}, V_{DS} = 28 \text{ V}$			1	μA
I_{GSS}	Gate-source leakage current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			± 100	nA
$V_{GS(Q)}$	Gate quiescent voltage	$V_{DS} = 28 \text{ V}, I_D = 100 \text{ mA}$	2.0		5.0	V
$V_{GS(th)}$	Gate threshold voltage	$I_D = 250 \mu\text{A}$	2.05		2.65	V
$V_{DS(on)}$	Static drain-source on-voltage	$V_{GS} = 10 \text{ V}, I_D = 3 \text{ A}$			510	mV
G_{FS}	Forward transconductance	$V_{DS} = 10 \text{ V}, I_D = 3 \text{ A}$	2.5			S
C_{iss}	Input capacitance	$V_{DS} = 12.5 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0 \text{ V}$		92		pF
C_{oss}	Output capacitance			73		
C_{rss}	Reverse transfer capacitance			6.1		

Table 4. Gate threshold voltage range groups

Symbol	Parameter	Test conditions	Group	Min.	Max.	Unit
$V_{GS(th)}$	Gate threshold voltage	$I_D = 250 \mu\text{A}$	A	2.05	2.20	V
			B	2.20	2.35	
			C	2.35	2.50	
			D	2.50	2.65	

Note: PD55035STR1-E is preselected in four groups of gate threshold voltage ranges as per table: the letter identifying the group to which it belongs is printed on the label of the cardboard box.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	Output power	$V_{DD} = 12.5 \text{ V}, I_{DQ} = 200 \text{ mA}, P_{OUT} = 35 \text{ W}, f = 500 \text{ MHz}$	35		-	W
G_P	Power gain		13	16.9	-	dB
η_D	Drain efficiency			62	-	%
$VSWR$	Load mismatch	$P_{OUT} = 35 \text{ W}$, all phases	20:1		-	

Table 6. Moisture sensitivity level

Test methodology	Rating
J-STD-020B	MSL 3

3 Impedance data

Figure 1. Impedance data

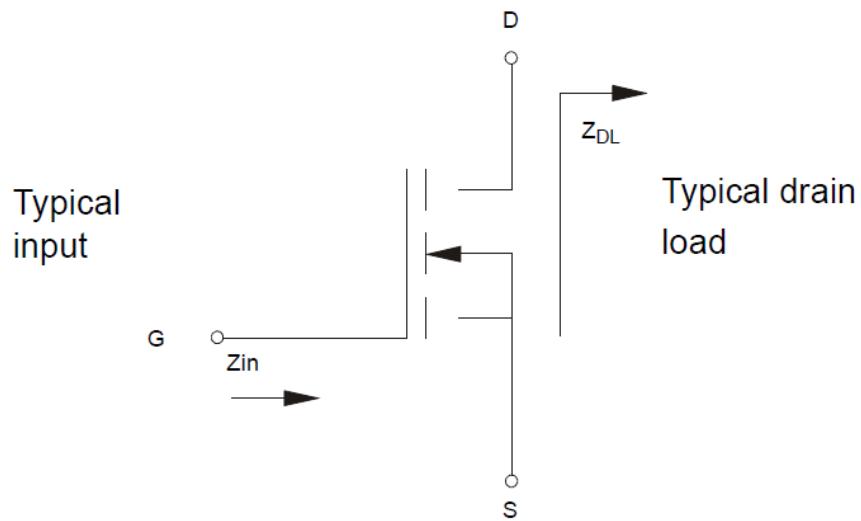


Table 7. Impedance data

Frequency (MHz)	Z_{in} (Ω)	Z_{DL} (Ω)
175	$3.34 - j 5.84$	$1.67 + j 1.45$
480	$0.53 - j 1.08$	$0.86 + j 0.25$
500	$0.45 - j 1.21$	$1.05 + j 0.03$
520	$0.42 - j 1.20$	$1.04 + j 0.15$

4 Typical performances

Figure 2. Capacitance vs supply voltage

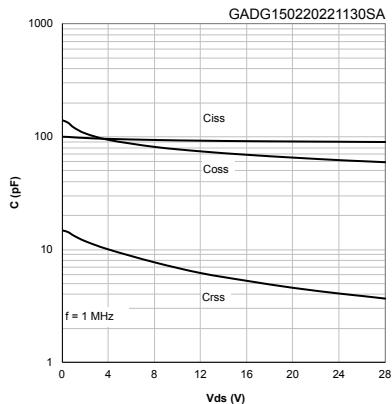


Figure 3. Drain current vs gate source voltage

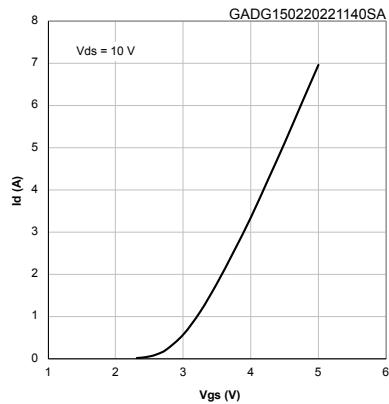


Figure 4. Gate-source voltage vs case temperature

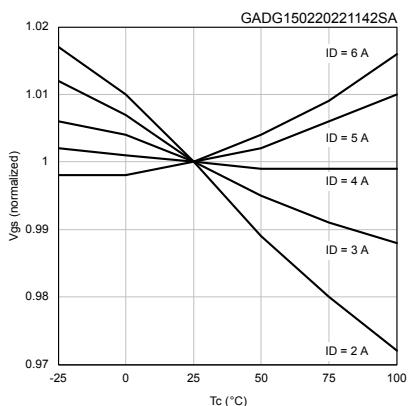


Figure 5. Output power vs input power

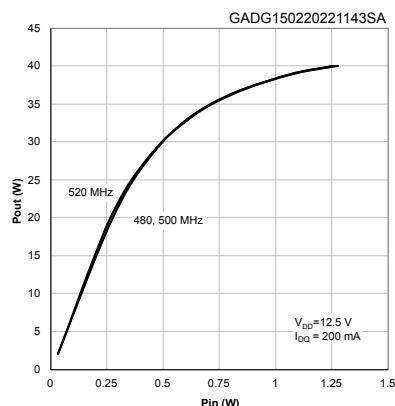


Figure 6. Power gain vs output power

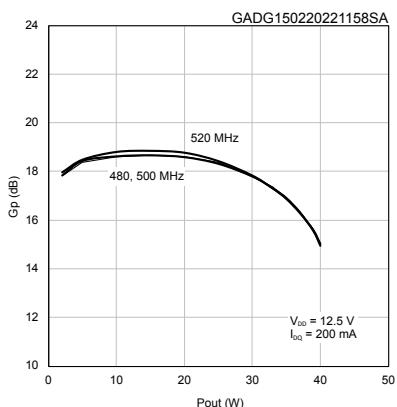


Figure 7. Efficiency vs output power

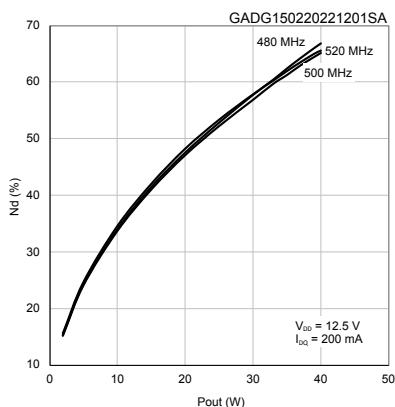
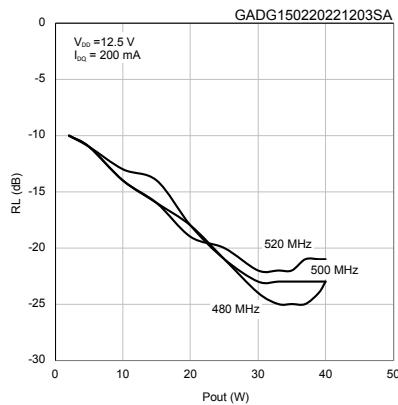
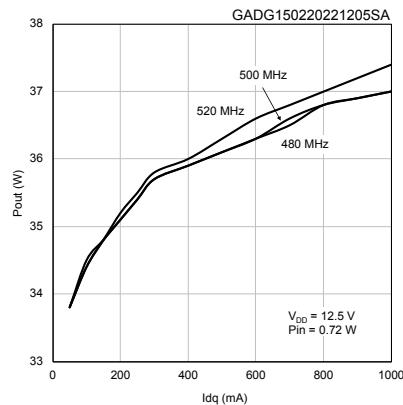
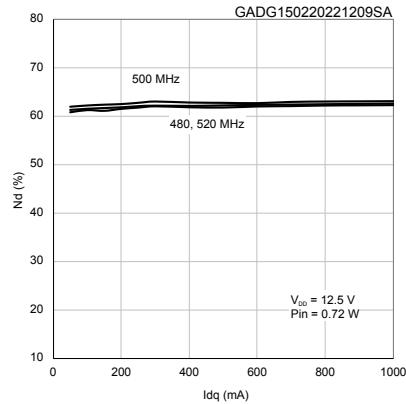
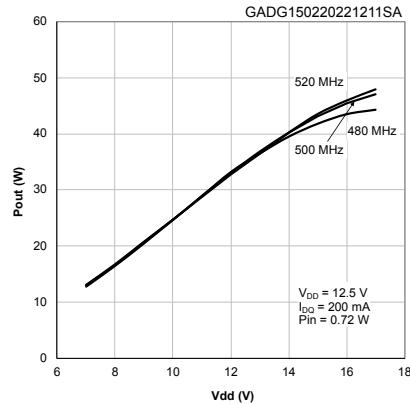
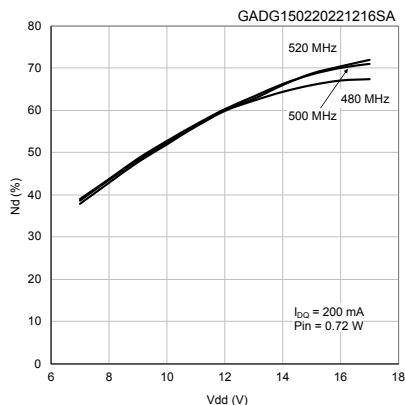
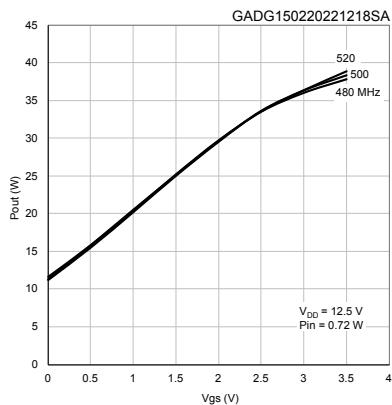
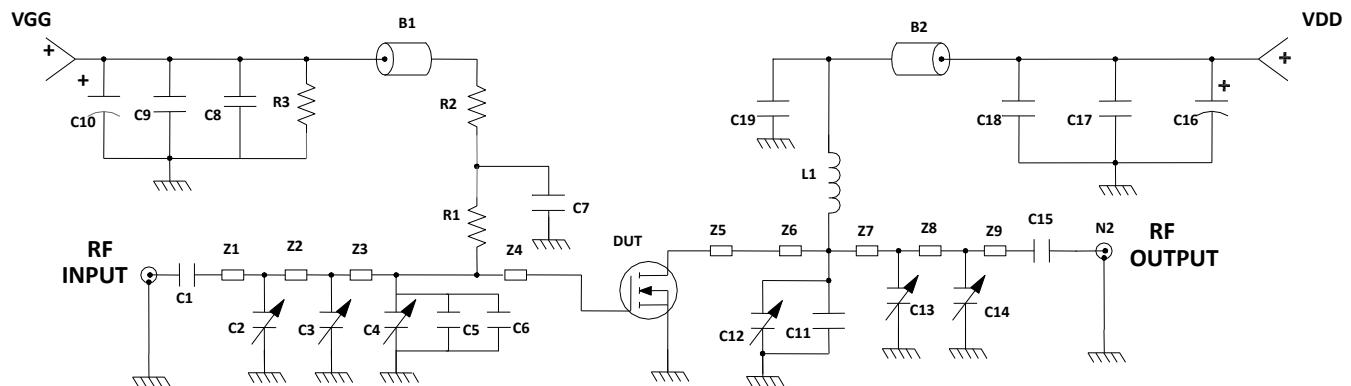


Figure 8. Input return loss vs output power

Figure 9. Output power vs bias current

Figure 10. Efficiency vs bias current

Figure 11. Output power vs supply voltage

Figure 12. Efficiency vs supply voltage

Figure 13. Output power vs gate voltage


5 Test circuit

Figure 14. 500 MHz test circuit schematic (engineering)



GADG150220221307SA

Table 8. Test circuit component part list

Component	Description
B1,B2	Ferrite bead
C1,C13	300 pF, 100 mil chip capacitor
C2,C3,C4,C12,C13,C14	1 to 20 pF trimmer capacitor
C6	39 pF ATC 100B surface mount ceramic chip capacitor
C7, C19	120 pF100 mil chip capacitor
C10, C16	10 µF, 50 V electrolytic capacitor
C9, C17	0.1 mF, 100 mil chip cap
C8, C18	1.000 pF 100 mil chip cap
C5, C11	33 pF, 100 mil chip cap
L1	56 nH, 7 turn, Coilcraft
N1, N2	Type N flange mount
R1	15 Ω,1 W chip resistor
R2	1 kΩ,1 W chip resistor
R3	33 kΩ,1 W chip resistor
Z1	0.471" X 0.080" microstrip
Z2	1.082" X 0.080" microstrip
Z3	0.372" X 0.080" microstrip
Z4,Z5	0.260" X 0.223" microstrip
Z6	0.050" X 0.080" microstrip
Z7	0.551" X 0.080" microstrip
Z8	0.825" X 0.080" microstrip
Z9	0.489" X 0.080" microstrip
Board	Roger, ultra lam 2000 THK 0.030", $\epsilon_r = 2.55$ 2oz. EDcu 2 sides.

6 Typical performances 175 MHz

Figure 15. Output power vs input power

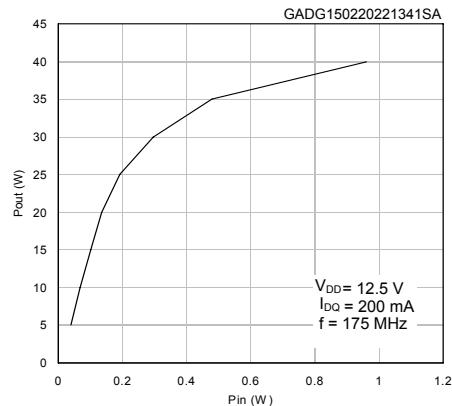


Figure 16. Power gain vs output power

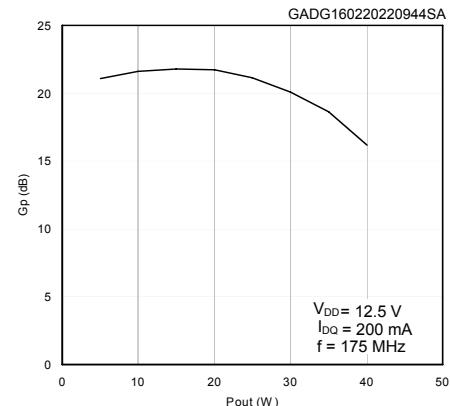


Figure 17. Efficiency vs output power

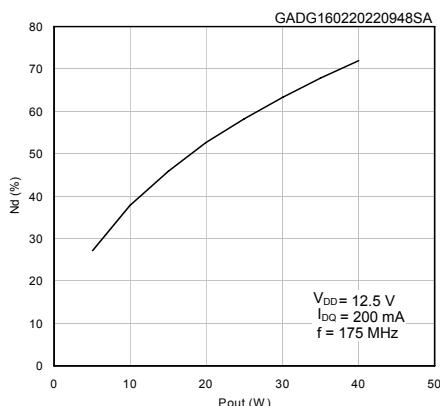
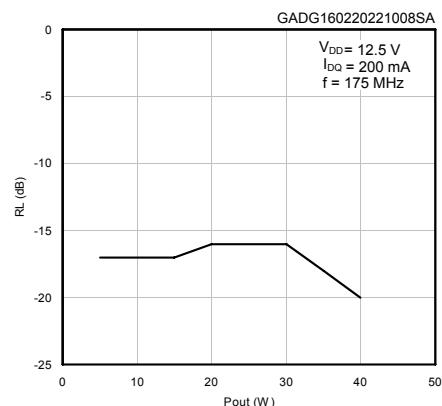


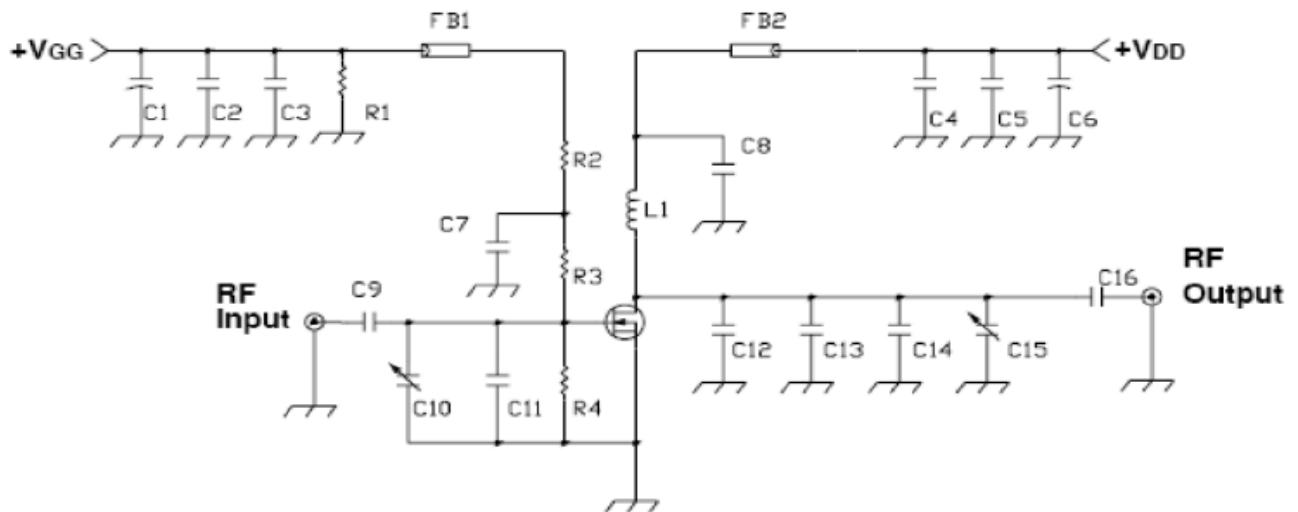
Figure 18. Input return loss vs output power



7

Test circuit 175 MHz

Figure 19. 175 MHz test circuit schematic (engineering)



GADG160220221105SA

Table 9. Test circuit component part list

Component	Description
C1,C6	10 μ F electrolytic capacitor
C2,C5	0.1 μ F chip capacitor
C3, C4	0.01 μ F chip capacitor
C7, C8	1200 pF chip capacitor
C9, C16	1000 pF chip capacitor
C10	ARCO 406 trimmer capacitor
C11	62 pF chip capacitor
C12	15 pF chip capacitor
C13	20 pF chip capacitor
C14	75 pF chip capacitor
C15	Johanson 1-20 pF trimmer capacitor
R1	33 k Ω chip resistor
R2	18 Ω chip resistor
R3	27 Ω chip resistor
R4	47 Ω chip resistor
L1	5 turn, 16 AWG magnetwire, ID = 0.25", inductor
FB1, FB2	Ferrite bead
Board	Roger, ultra lam 2000 THK 0.030", ϵ_r = 2.55 2oz. ED Cu 2 sides

8 Common source s-parameter

Table 10. S-parameter for $V_{DS} = 12.5$ V, $I_D = 500$ mA

Frequency (MHz)	S ₁₁	S ₁₁ <Φ	S ₂₁	S ₂₁ <Φ	S ₁₂	S ₁₂ <Φ	S ₂₂	S ₂₂ <Φ
50	0.823	-162	14.28	86	0.015	-3	0.782	-168
100	0.855	-169	6.87	75	0.015	-11	0.798	-171
150	0.875	-172	4.50	68	0.014	-17	0.813	-172
200	0.891	-173	3.18	60	0.013	-24	0.835	-172
250	0.902	-174	2.42	53	0.012	-29	0.856	-172
300	0.918	-175	1.90	47	0.011	-32	0.876	-173
350	0.924	-176	1.52	42	0.010	-36	0.890	-173
400	0.934	-176	1.25	37	0.008	-37	0.903	-174
450	0.940	-177	1.03	33	0.007	-38	0.918	-175
500	0.949	-177	0.87	29	0.007	-40	0.928	-175
550	0.956	-178	0.74	26	0.005	-40	0.935	-176
600	0.958	-179	0.65	23	0.004	-36	0.946	-177
650	0.963	-180	0.56	20	0.004	-36	0.952	-178
700	0.968	180	0.49	18	0.003	-27	0.955	-178
750	0.971	179	0.44	15	0.003	-21	0.959	-179
800	0.970	179	0.39	13	0.002	-5	0.962	-179
850	0.973	178	0.35	12	0.002	11	0.967	-180
900	0.975	178	0.32	10	0.002	24	0.967	179
950	0.974	177	0.29	8	0.002	27	0.971	179
1000	0.976	177	0.26	7	0.003	47	0.972	178
1050	0.977	176	0.24	5	0.002	61	0.976	178
1100	0.976	176	0.22	4	0.003	69	0.976	177
1150	0.978	176	0.20	2	0.003	72	0.974	177
1200	0.979	175	0.19	1	0.004	78	0.975	176
1250	0.980	175	0.18	-1	0.004	87	0.977	176
1300	0.979	174	0.16	-2	0.005	86	0.976	176
1350	0.977	174	0.15	-3	0.006	88	0.975	175
1400	0.975	174	0.14	-3	0.006	91	0.977	174
1450	0.974	173	0.13	-3	0.006	97	0.975	174
1500	0.972	173	0.12	-4	0.007	117	0.969	174

Table 11. S-parameter for $V_{DS} = 12.5$ V, $I_D = 1$ A

Frequency (MHz)	S ₁₁	S ₁₁ <Φ	S ₂₁	S ₂₁ <Φ	S ₁₂	S ₁₂ <Φ	S ₂₂	S ₂₂ <Φ
50	0.845	-165	14.89	87	0.012	0	0.818	-171
100	0.877	-171	7.23	78	0.011	-8	0.829	-174
150	0.894	-174	4.81	72	0.011	-12	0.836	-175
200	0.905	-175	3.46	65	0.010	-17	0.849	-175
250	0.909	-176	2.69	59	0.010	-20	0.863	-175
300	0.920	-176	2.15	54	0.009	-23	0.877	-175
350	0.924	-177	1.75	48	0.008	-27	0.887	-175
400	0.933	-177	1.46	44	0.007	-28	0.898	-176
450	0.937	-178	1.22	39	0.007	-28	0.910	-176
500	0.946	-178	1.05	36	0.006	-28	0.919	-177
550	0.951	-179	0.90	32	0.005	-26	0.925	-177
600	0.953	-180	0.79	29	0.004	-23	0.936	-178
650	0.959	180	0.69	26	0.004	-19	0.942	-178
700	0.963	179	0.61	24	0.003	-13	0.946	-179
750	0.965	179	0.55	21	0.003	-4	0.951	-179
800	0.964	178	0.49	19	0.003	6	0.954	-180
850	0.967	178	0.44	17	0.003	14	0.960	180
900	0.970	177	0.40	15	0.003	31	0.960	179
950	0.971	177	0.37	13	0.003	39	0.965	179
1000	0.972	176	0.34	11	0.003	55	0.964	178
1050	0.972	176	0.31	9	0.003	53	0.970	178
1100	0.973	176	0.29	8	0.003	64	0.969	177
1150	0.975	175	0.26	6	0.004	70	0.966	179
1200	0.976	175	0.25	4	0.004	75	0.971	176
1250	0.975	174	0.22	3	0.005	85	0.972	176
1300	0.975	174	0.21	2	0.005	81	0.970	175
1350	0.974	174	0.19	1	0.005	85	0.970	175
1400	0.973	174	0.18	0	0.006	89	0.971	174
1450	0.972	173	0.17	-1	0.006	95	0.971	174
1500	0.970	173	0.16	-1	0.008	110	0.965	174

Table 12. S-parameter for $V_{DS} = 12.5$ V, $I_D = 2$ A

Frequency (MHz)	S ₁₁	S ₁₁ <Φ	S ₂₁	S ₂₁ <Φ	S ₁₂	S ₁₂ <Φ	S ₂₂	S ₂₂ <Φ
50	0.863	-165	15.03	88	0.010	0	0.841	-173
100	0.892	-171	7.33	80	0.009	-5	0.848	-176
150	0.909	-174	4.91	74	0.009	-9	0.853	-176
200	0.916	-176	3.56	68	0.009	-11	0.860	-176
250	0.920	-177	2.81	63	0.008	-12	0.872	-177
300	0.927	-177	2.26	58	0.008	-15	0.880	-177
350	0.929	-178	1.86	52	0.007	-18	0.889	-177
400	0.935	-178	1.57	48	0.006	-20	0.896	-177
450	0.938	-179	1.33	44	0.006	-20	0.906	-178
500	0.944	-179	1.14	40	0.005	-16	0.914	-177
550	0.950	-180	0.99	37	0.005	-15	0.918	-178
600	0.952	180	0.87	33	0.004	-14	0.929	-179
650	0.956	179	0.77	30	0.004	-9	0.935	-179
700	0.960	179	0.69	28	0.003	4	0.940	-179
750	0.964	179	0.61	25	0.003	11	0.946	180
800	0.964	178	0.55	23	0.003	20	0.949	180
850	0.965	177	0.50	21	0.003	32	0.955	179
900	0.968	177	0.46	18	0.003	38	0.954	179
950	0.969	177	0.42	17	0.003	46	0.959	178
1000	0.971	176	0.39	14	0.003	47	0.959	177
1050	0.971	176	0.36	12	0.004	57	0.967	177
1100	0.970	176	0.33	11	0.004	60	0.964	177
1150	0.973	175	0.30	9	0.004	69	0.964	176
1200	0.975	175	0.28	7	0.004	72	0.966	176
1250	0.973	174	0.26	5	0.005	78	0.971	175
1300	0.971	174	0.24	4	0.006	80	0.968	175
1350	0.973	174	0.23	3	0.006	83	0.970	174
1400	0.971	173	0.21	2	0.006	83	0.971	174
1450	0.969	173	0.20	1	0.006	91	0.970	174
1500	0.968	173	0.18	1	0.008	112	0.969	173

Table 13. S-parameter for $V_{DS} = 12.5$ V, $I_D = 3$ A

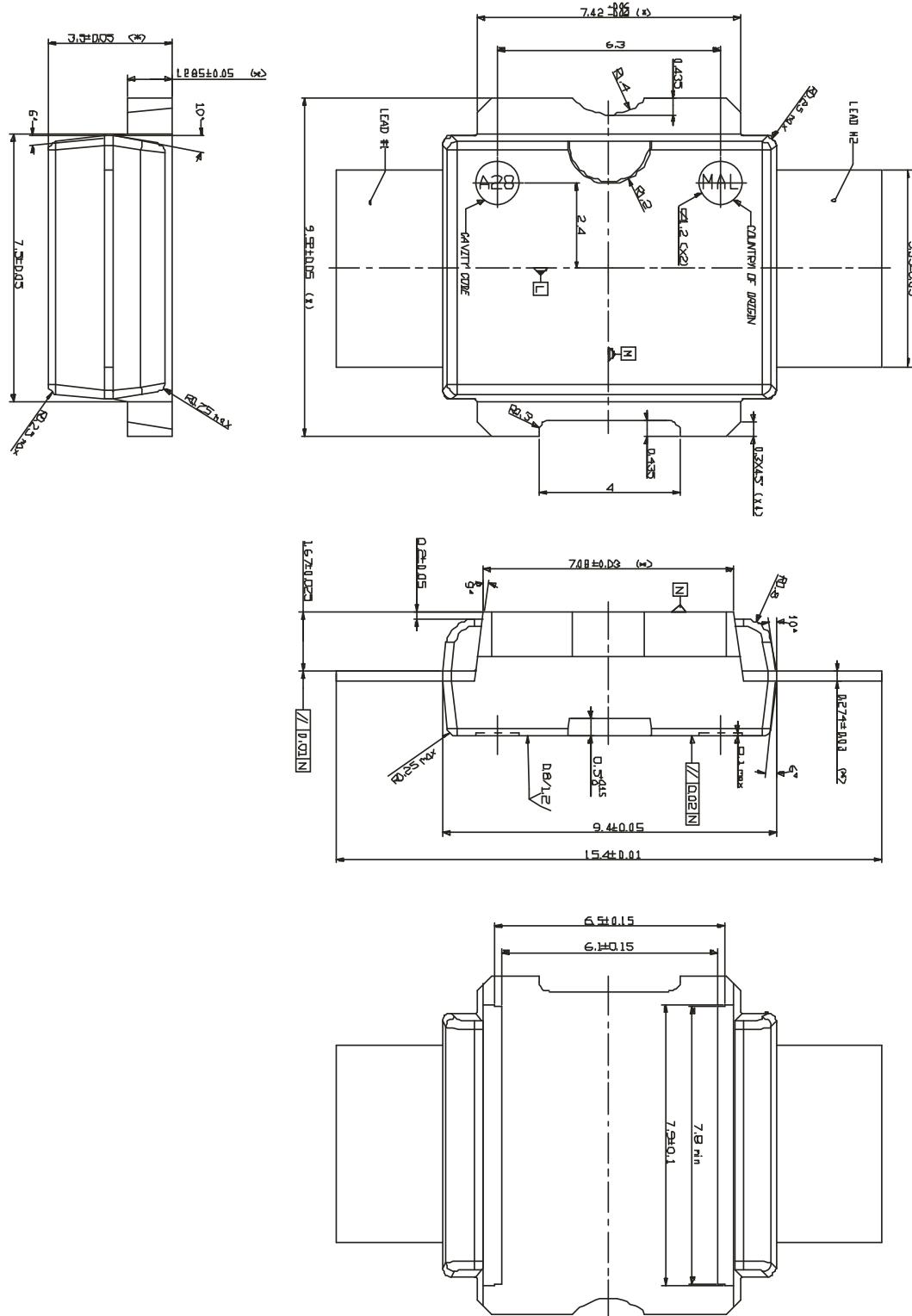
Frequency (MHz)	S ₁₁	S ₁₁ <Φ	S ₂₁	S ₂₁ <Φ	S ₁₂	S ₁₂ <Φ	S ₂₂	S ₂₂ <Φ
50	0.867	-165	14.95	88	0.009	2	0.848	-174
100	0.896	-171	7.31	80	0.009	-4	0.856	-177
150	0.913	-175	4.92	75	0.008	-7	0.861	-177
200	0.921	-176	3.57	69	0.008	-9	0.866	-177
250	0.921	-177	2.82	64	0.008	-13	0.874	-177
300	0.929	-178	2.28	59	0.007	-12	0.882	-177
350	0.930	-178	1.90	54	0.007	-14	0.888	-178
400	0.936	-178	1.59	50	0.006	-16	0.896	-177
450	0.938	-179	1.36	45	0.005	-14	0.904	-178
500	0.947	-179	1.17	42	0.005	-11	0.915	-178
550	0.950	180	1.02	38	0.004	-10	0.917	-178
600	0.951	180	0.90	35	0.004	-6	0.927	-179
650	0.956	179	0.79	32	0.004	-3	0.934	-179
700	0.960	179	0.71	29	0.003	4	0.935	-179
750	0.963	178	0.64	26	0.003	17	0.943	180
800	0.962	178	0.58	24	0.003	21	0.948	179
850	0.964	177	0.52	22	0.004	32	0.951	179
900	0.967	177	0.48	20	0.003	41	0.949	178
950	0.969	177	0.44	18	0.003	36	0.958	178
1000	0.969	176	0.40	15	0.004	53	0.956	178
1050	0.969	176	0.37	14	0.004	58	0.963	177
1100	0.969	175	0.34	12	0.004	64	0.963	177
1150	0.971	175	0.32	10	0.004	69	0.961	176
1200	0.973	175	0.30	8	0.004	71	0.965	176
1250	0.971	174	0.27	6	0.005	77	0.967	175
1300	0.971	174	0.26	5	0.006	78	0.970	174
1350	0.973	174	0.24	4	0.006	80	0.965	175
1400	0.970	173	0.22	2	0.007	87	0.973	174
1450	0.968	173	0.21	3	0.006	91	0.967	174
1500	0.968	173	0.19	1	0.008	111	0.965	173

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 PowerSO-10RF (straight lead) package information

Figure 20. PowerSO-10RF (straight lead) package outline (dimensions in millimeters)



7221039_REV_6

Revision history

Table 14. Document revision history

Date	Revision	Changes
08-Mar-2022	1	First release.

Contents

1	Electrical data	2
2	Electrical characteristics.....	3
3	Impedance data.....	4
4	Typical performances.....	5
5	Test circuit	7
6	Typical performances 175 MHz.....	8
7	Test circuit 175 MHz	9
8	Common source s-parameter	10
9	Package information.....	14
9.1	PowerSO-10RF (straight lead) package information	15
	Revision history	16

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