PD64012

12-channel PoE Manager

Preliminary Datasheet

Description

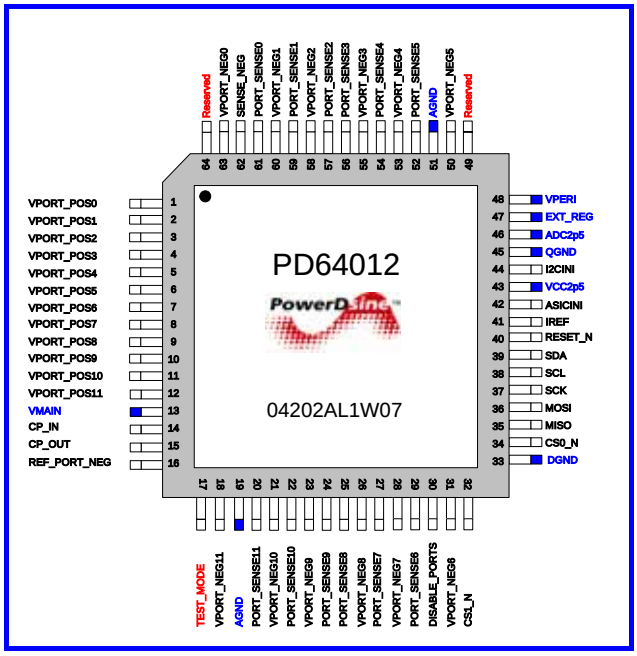
PowerDsine's™ PD64012 Power over Ethernet (PoE) Manager chip integrates power, analog and logic functions into a single 64-pin, plastic pack. It is used in Ethernet switches and Midspans to allow next generation network devices to share power and data over the same cable.

The device is a twelve-port, mix-signal, high-voltage Power over Ethernet driver. The PoE Manager allows the detection of IEEE 802.3af-2003 compliant terminals, referred to as powered devices or PDs, ensuring safe power feeding and removal over Ethernet ports. With full digital control via a serial communication interface and a minimum of external components, the device integrates in multi-port and highly populated Ethernet switches.

The PD64012 implements all real time functions according to IEEE 802.3af-2003, including: detection, classification, and port status monitoring; as well as system level activities such as: power management and MIB support, for system management. The PoE Manager is designed to detect and disable disconnected ports, using both DC and AC disconnect methods, as defined in IEEE 802.3af-2003.

The PD64012 has two possible working configurations: an Auto mode (stand-alone topology) for basic PoE functions and an Enhanced mode for extended functions.

Pin Configuration



Features

- IEEE 802.3af-2003 compliant
- Drives 12 independent power ports
- Can be cascaded for up to 48 ports, using a master/slave architecture
- Supports IETF Power Ethernet MIB (RFC 3621)
- Thermal protection per port
- Thermal monitoring capabilities
- Multi-point resistor detection
- Supports DC modulation method under-current detection according to IEEE 802.3af-2003
- AC & DC disconnect functions
- PD classification function
- Operates from single input (44 to 57 V)
- I^2C bus interface
- Supports foldback current limiting
- Digitally programmable overcurrent protection per port
- Digitally programmable timers
- Power management algorithm for up to 48 ports
- Internal power-on reset
- Power soft-start algorithm
- Fast power shutdown, in case of power supply failure
- Automatic on/off sequencer for up to 48 ports
- Disable/enable power feeding
- Continuous port current monitoring
- Supports back-off feature for Midspan implementation
- Additional features for Enhanced mode:
  - UART interface
  - Pre-standard PD detection
  - Supports non-standard terminals
  - Advanced power management
  - Programmable port matrix

Ordering Information

PART	TEMP. RANGE	PIN PACKAGE
PD64012	-20 to +85 °C	LQFP-64

Date code: see the bottom line (*04202AL1W07*) in the Pin Configuration drawing. "*0420*" is the date code. "*04*" the year (2004), while "*20*" is the week.

Maximum Ratings

V_{main}..... -0.3 to 80 V(1)
DGND, AGND, QGND, SENSE_NEG.....-0.3 to 0.3 V(2)

V_{PORT_POSx} ..... -0.3 to 80 V(1)
V_{PORT_NEGx}, REF_PORT_NEG
V_{PORT_POSx} - V_{PORT_NEGx}

PORT_SENSEx..... -0.3 to 15 V
VCC_{2p5}, ADC_{2p5}.....-0.3 to 3 V
V_{PERI}..... 4 V
EXT_REG.....-0.3 to 6 V
I2CINI, ASICINI..... -0.3 to 3 V

MISO, MOSI, SCK, SCL, SDA,
CLK, RESETN, CS0_N, CS1_N..... -0.3 to (V_{PERI} + 0.3) V

ESD (Human Body Model)..... -2 to 2 kV(3)
Max junction temperature (T_{junc}).....+150 °C
Junction-ambient thermal resistance (θ_{JA})..... 25 °C/W
Junction-case thermal resistance (θ_{JC}).....16 °C/W
Lead temperature (soldering, 10 s)..... 300 °C
Storage temperature.....-40 to +125 °C

Notes: "x" defines port numbers, 0 thru 11, inclusive.
(1) 80 V is the transient voltage that can be applied for at most one minute.
(2) Maximum value between grounds.
(3) ESD testing is performed in accordance with the Human Body Model (C_{Zap} = 100 pF, R_{Zap} = 1500 Ω).

Stresses beyond those listed above, may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods, may affect device reliability.

Operating Conditions

PARAMETER	MIN.	NOM.	MAX.	UNIT
Operating temperature	-20		+85	°C
Operational limitations (1)	15 to 44	44 to 55	55 to 57	V

(1) Operating functions depend on the input voltage, as shown in the distribution of Figure 1.

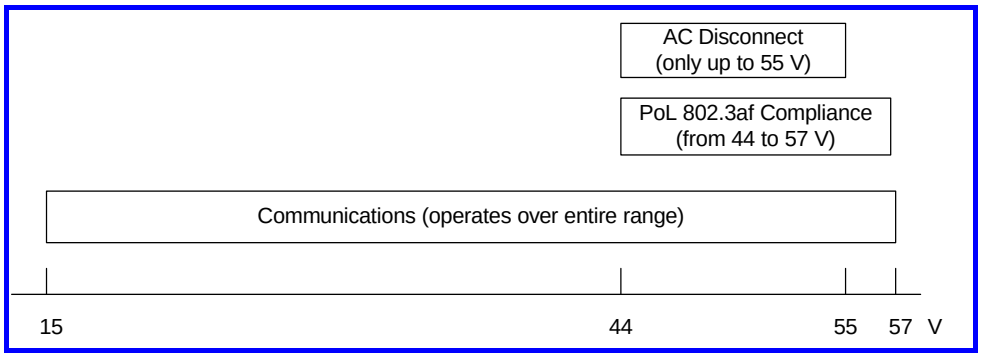


Figure 1 - Operational Ranges

Electrical Characteristics

DC Characteristics for Digital Inputs and Outputs

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	REMARKS
Pin Name	DISABLE_PORTS				
Type	Schmitt Trigger CMOS input, TTL level with internal pullup				
High level input voltage	V_{IH}	2.0		V	
Low level input voltage	V_{IL}		0.8	V	
Input voltage hysteresis		0.3		V	
Input high current	I_{IH}	+10	+150	µA	
Input low current	I_{IL}	NA	NA	µA	

DC Characteristics for Digital Inputs and Outputs (continued)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	REMARKS
Pin Name	SCL				
Type	Schmitt Trigger CMOS input, TTL level with internal pullup				
High level input voltage	V_{IH}	2.0		V	
Low level input voltage	V_{IL}		0.8	V	
Input voltage hysteresis		0.3		V	
Input high current	I_{IH}	NA	NA	µA	
Input low current	I_{IL}	-150	-10	µA	
Pin Name	MOSI, MISO, CS0_N, CS1_N, SCK				
Type	CMOS I/O, TTL level with no internal pull up/pull down resistor				
High level input voltage	V_{IH}	2.0		V	
Low level input voltage	V_{IL}		0.8	V	
Input voltage hysteresis		0.3		V	
Input high current	I_{IH}	-1	+1	µA	
Input low current	I_{IL}	-1	+1	µA	
High level output voltage		V_{PERI}-0.4V		V	I_{out} = 3 mA
Low level output voltage			0.4	V	I_{out} = 3 mA
Tri state output current		-1	+1	µA	
Pin Name	RESET_N, SDA				
Type	CMOS open drain output with Schmitt Trigger input, TTL level				
High level input voltage			0.4	V	I_{out} = 3mA
Low level input voltage	V_{IL}		0.8	V	
Input voltage hysteresis		0.3		V	
OFF state output current		-1	+1	µA	

Electrical Characteristics for Analog I/O Pads

PARAMETER	MIN.	MAX.	UNIT	REMARKS
Pin Name	VPORT_POSx, VPORT_NEGx, REF_PORT_NEG			
Operating voltage	44	62	V	
Pin current consumption	-5	+5	µA	Port driver off, V_{port} differential measurement off, AC generator off
Pin Name	PORT_SENSEx			
Operating voltage	0	1.48	V	With external 2 ohms (1%) to ground
Internal current consumption		20	µA	
Pin Name	VMAIN			
Operating voltage	44	57	V	
V_{main} current consumption		20	mA	Total on V_{main}
Pin Name	CP out			
Operating voltage	44	67	V	
Pin current consumption		5	mA	
Pin Name	ADC_{2p5}, VCC_{2p5}, V_{PERI}, EXT_REG			
ADC_{2p5} output voltage	2.45	2.55	V	
ADC_{2p5} internal current consumption		6	mA	Recommended external cap. = 47 to 135 nF
VCC_{2p5} output voltage	2.37	2.62	V	Recommended external cap. = 47 to 135 nF
VCC_{2p5} internal current consumption		5	mA	
V_{PERI} output voltage	3.13	3.46	V	Recommended external cap. = 1 to 4.7 µF
V_{PERI} external current load		6	mA	Without external NPN
EXT_REG output current		6	mA	When using external NPN for V_{PERI}

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Electrical Characteristics for Analog I/O Pads (continued)

PARAMETER	MIN.	MAX.	UNIT	REMARKS
Pin Name	ASICINI, I2CINI			
Operating voltage	0	ADC_{2p5}	V	
Current consumption	-1	+1	µA	
Pin Name	I_{REF}			
Output voltage	1.21	1.34	V	With external 24.9 kΩ resistor to ground

Dynamic Characteristics

The PD64012 is an advanced power-limiting device that uses three programmable current level thresholds (I_{min}, I_{cut}, I_{lim}) and two timers (T_{min}, T_{cut}), to operate as shown in Figure 2. Loads that dissipate more than I_{cut} for longer than T_{cut} (OVL_S to OVL) are classified as overloads and are automatically shutdown. Output power dissipation below I_{min} for during more than T_{min} (UDL_S to UDL) will be classified as no-load and will also be shutdown. Automatic recovery from overload and no-load conditions are attempted every T_{OVLREC} and T_{UDLREC} periods (typically 5 and 1 seconds, respectively). In any case, output power is limited to $I_{lim,}$ which is a maximum peak power allowed at the port.

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Automatic recovery from overload shutdown	T_{OVLREC} value, measured from port shutdown (can be modified through control port)			5		s
Automatic recovery from no-load shutdown	T_{UDLREC} value, measured from port shutdown (can be modified through control port)			1		s
Cutoff timers accuracy	Typical accuracy of T_{cut}			10		ms
Inrush current	I_{Inrsh}	*For t=50 ms, C_{load}=180 uF max.*	400		450	mA
Output current operating range	I_{port}	*Continuous operation after startup period.*	10		350	mA
Output power available, operating range	P_{port}	Continuous operation after startup period, at port output.	0.57		15.4	W
Off mode current	I_{min1}	Must disconnect for t greater than T_{UVL}	0		5	mA
	I_{min2}	May or may not disconnect for t greater than T_{UVL}	5	7.5	10	mA
PD power maintenance request drop-out time limit	T_{PMDO}	Buffer period to handle transitions	300		400	ms
Over load current detection range	I_{cut}	Time limited to T_{OVL}	350		400	mA
Over load time limit	T_{OVL}		50		75	ms
Turn on rise time	T_{rise}	From 10% to 90% of V_{port} (specified for PD load consisting of 100 uF capacitor in parallel to 200 Ω).	15			us
Turn off time	Toff	From V_{port} to 5 Vdc			500	ms

Thermal Data

Power consumption – the internal power consumption of a single device from the DC input is based on:

Input voltage range……. 44 to 57 VDC
Input current…….. 10 mA typ.; 15 mA max.

$P_{main} = V_{main} \times I_{main}$
P_{main} typ. = 48 VDC x 10 mA = 0.480 W
P_{main} max. = 57 VDC x 15 mA = 0.855 W

Device Power Dissipation – the PD64012 incorporates 12 power MOSFETs, each characterized by:

Resistance from drain-source $R_{ds(on)}$ = 0.3 Ω typ. ; 0.5 Ω max.
Drain-source current I_{ds} = 360 mA max.

Maximum power dissipation P_{MOSFET} max. of a single PD64012 device (for 12 MOSFETs) :

$[(I_{ds})^2 \times R_{ds(on)}] \times 12 = [(0.36\ A)^2 \times 0.5\ \Omega] \times 12 = 0.78\ W$

Charge pump (see Analog Section of Block Diagram Description, hereafter) power dissipation P_{CP} is 0.21 W.

Total power dissipation P_{total} by device, under maximum conditions:

$P_{total} = P_{main}$ max. + P_{MOSFET} max. + P_{CP} = 0.855 W + 0.78 W + 0.21 W = 1.845 W

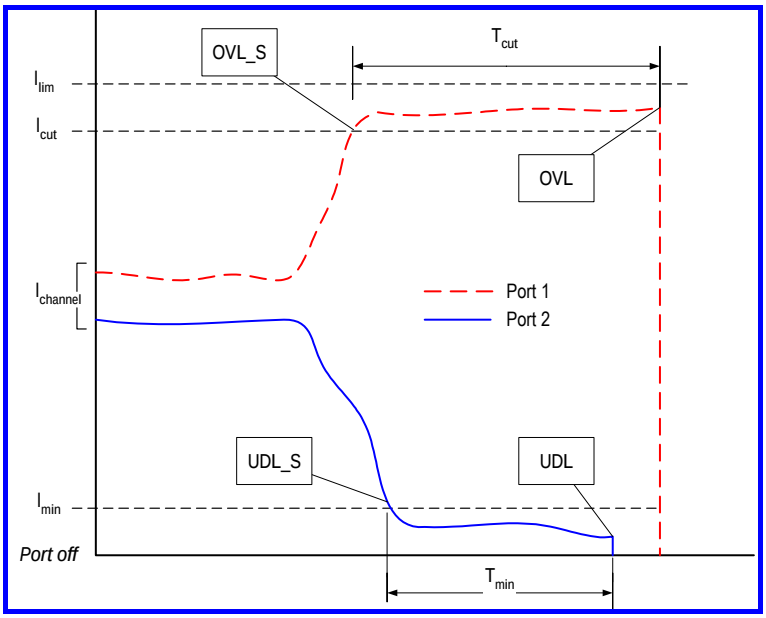

Figure 2: Power Limits

Protection Mechanism

The PD64012 includes internal thermal protection to avoid junction overheat. Three types of temperature sensors are integrated into the device: two are used for protection and one for temperature monitoring.

Hi-temp protection – the device contains thermal shutdowns. This protection system is activated in extreme conditions.

Lo-temp protection – there are thermal sensors that are intended to protect the functionality of the device, in cases of temperature rise.

Indicator sensors – four temperature sensors monitor the local temperature in the device. Their average is also calculated by the PD64012. All values are stored in internal registers for data retrieval. The register values are calculated by:

Decimal value = 684 - 1.514 x [(T_{junc})+ 40 °C].

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Pins Descriptions

PIN	PIN NAME	PIN TYPE	PIN DESCRIPTION
1.	V_{PORT_POS0}	Analog I/O	Port 0 positive voltage feeding
2.	V_{PORT_POS1}	Analog I/O	Port 1 positive voltage feeding
3.	V_{PORT_POS2}	Analog I/O	Port 2 positive voltage feeding
4.	V_{PORT_POS3}	Analog I/O	Port 3 positive voltage feeding
5.	V_{PORT_POS4}	Analog I/O	Port 4 positive voltage feeding
6.	V_{PORT_POS5}	Analog I/O	Port 5 positive voltage feeding
7.	V_{PORT_POS6}	Analog I/O	Port 6 positive voltage feeding
8.	V_{PORT_POS7}	Analog I/O	Port 7 positive voltage feeding
9.	V_{PORT_POS8}	Analog I/O	Port 8 positive voltage feeding
10.	V_{PORT_POS9}	Analog I/O	Port 9 positive voltage feeding
11.	V_{PORT_POS10}	Analog I/O	Port 10 positive voltage feeding
12.	V_{PORT_POS11}	Analog I/O	Port 11 positive voltage feeding
13.	V_{main}	Supply	Main Voltage supply
14.	CP_IN	Analog I/O	Charge Pump input, 48V+5V
15.	CP_OUT	Analog I/O	Charge Pump Pulse Output
16.	REF_PORT_NEG	Analog I/O	Port negative reference
17.	TEST_MODE	Analog I/O	Test Mode Pin (connect to ground)
18.	V_{PORT_NEG11}	Analog I/O	Port 11 negative voltage feeding
19.	AGND	Supply	Analog ground
20.	PORT_SENSE11	Analog I/O	Channel current monitoring
21.	V_{PORT_NEG10}	Analog I/O	Port 10 negative voltage feeding
22.	PORT_SENSE10	Analog I/O	Channel current monitoring
23.	V_{PORT_NEG9}	Analog I/O	Port 9 negative voltage feeding
24.	PORT_SENSE9	Analog I/O	Channel current monitoring
25.	PORT_SENSE8	Analog I/O	Channel current monitoring
26.	V_{PORT_NEG8}	Analog I/O	Port 8 negative voltage feeding
27.	PORT_SENSE7	Analog I/O	Channel current monitoring
28.	V_{PORT_NEG7}	Analog I/O	Port 7 negative voltage feeding
29.	PORT_SENSE6	Analog I/O	Channel current monitoring
30.	DISABLE_PORTS_N	Digital input	Disable all ports power (active low)
31.	V_{PORT_NEG6}	Analog I/O	Port 6 negative voltage feeding
32.	CS1_N	Digital I/O	SPI bus, Chip Select 1
33.	DGND	Supply	Digital ground
34.	CS0_N	Digital I/O	SPI bus, Chip Select 0
35.	MISO	Digital I/O	SPI bus, Master in/slave out
36.	MOSI	Digital I/O	SPI bus, Master out/slave in
37.	SCK	Digital input	SPI bus, Serial clock I/O
38.	SCL	Digital input	I2C bus, Serial Clock Input
39.	SDA	Digital I/O	I2C bus, open drain
40.	RESET_N	Digital I/O	Active Low Reset I/O
41.	IREF	Analog I/O	Current reference
42.	ASICINI	Analog input	Analog input for ASIC initialization
43.	VCC_{2p5}	Supply	Internal 2.5 V supply (do not use!)
44.	I2CINI	Analog input	Analog input for I2C initialization
45.	QGND	Supply	Quiet analog ground
46.	ADC_{2p5}	Supply	ADC reference (do not use!)
47.	EXT_REG	Analog out	External regulation
48.	V_{PERI}	Analog out	Regulated 3.3 V power source
49.	Reserved	Digital input	(Connect to ground)
50.	V_{PORT_NEG5}	Analog I/O	Port 5 negative voltage feeding

PIN	PIN NAME	PIN TYPE	PIN DESCRIPTION
51.	AGND	Supply	Analog ground
52.	PORT_SENSE5	Analog I/O	Channel current monitoring
53.	V_{PORT_NEG4}	Analog I/O	Port 4 negative voltage feeding
54.	PORT_SENSE4	Analog I/O	Channel current monitoring
55.	V_{PORT_NEG3}	Analog I/O	Port 3 negative voltage feeding
56.	PORT_SENSE3	Analog I/O	Channel current monitoring
57.	PORT_SENSE2	Analog I/O	Channel current monitoring
58.	V_{PORT_NEG2}	Analog I/O	Port 2 negative voltage feeding
59.	PORT_SENSE1	Analog I/O	Channel current monitoring
60.	V_{PORT_NEG1}	Analog I/O	Port 1 negative voltage feeding
61.	PORT_SENSE0	Analog I/O	Channel current monitoring
62.	SENSE_NEG	Analog I/O	Port sense reference
63.	V_{PORT_NEG0}	Analog I/O	Port 0 negative voltage feeding
64.	Reserved	TBD	Not connected

Functional Description

Operational Modes

The PD64012 supports two main modes of operation, based on two different architectures, as described hereafter. The two modes are: Enhanced mode and Automatic mode.

Enhanced mode – in this mode of operation, the PD64012s communicate with the PD63000 PoE MCU (dedicated MCU for Power over Ethernet tasks), through a Serial Parallel Interface (SPI) bus. In this mode, all PD64012s are directly connected to the PD63000 through the SPI, in slave mode. The MCU is used for additional Power over Ethernet features, such as:

- Legacy PDs detection (including Cisco discovery)
- Enhanced power management algorithms
- LED indicators support
- Port matrix control
- Communication protocol translator.

The switch host CPU communicates with the PD63000, via an isolated I^2C or UART bus, as shown in Figure 3.

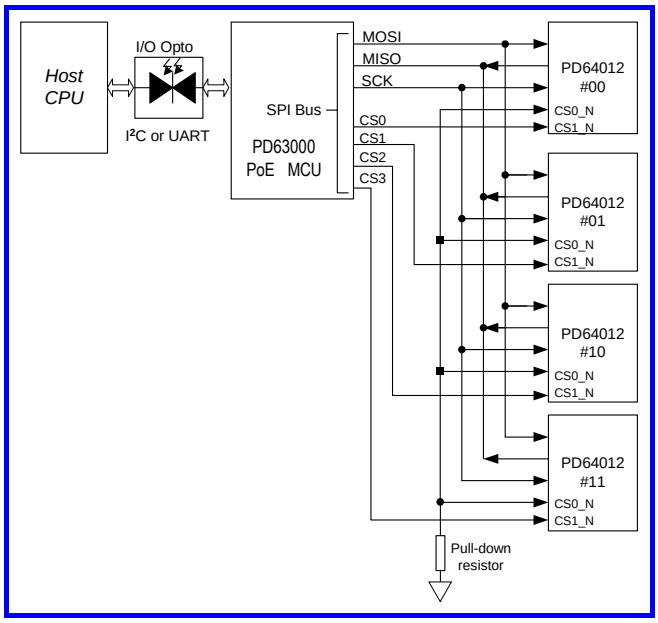

Figure 3: Enhanced Mode

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Automatic mode – in this mode the PD64012 PoE Managers communicate with the host CPU, through an isolated I^2C bus. The PD64012 SPI bus is dedicated for internal communication among PD64012s (for power management), as illustrated in Figure 4.

Anyone of the devices (for example, PD64012 #00) may be configured as Master, while the others are Slaves. This Master/Slave configuration only affects the Serial Peripheral Interface (SPI) bus. It is critical that only one of them be set-up as a Master, with the others acting as Slaves, in order to avoid SPI clock and data I/Os contentions.

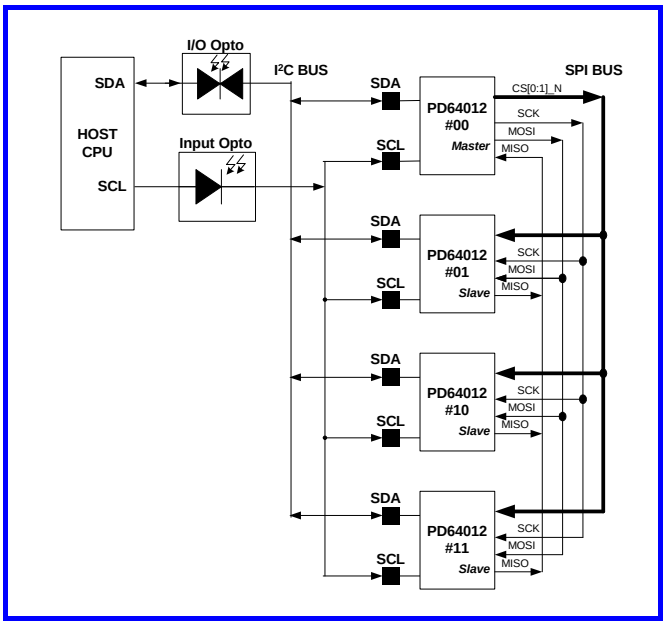

Figure 4: Automatic Mode

Mode Configuration Method

The PoE Manager's configuration is done via the ASIC_INI pin, according to the following table.
The ASIC_INI analog signal is converted into a 10-bit register (A/D). Once a hard Reset pulse is detected, the data is latched into an internal mode register.

MODE NAME	ASIC_INI VOLTAGE LEVEL	ASIC_INI INTERNAL A/D REGISTER	I^2C 2 LSB ADDRESS (set internally)
Enhanced mode	0.31 to 0.63 V	001	00
Auto mode – Slave 1	0.63 to 0.94 V	010	01
Auto mode – Slave 2	0.94 to 1.25 V	011	10
Auto mode – Slave 3	1.25 to 1.56 V	100	11
Auto mode - Master	2.19 to 2.5 V	111	00

Notes:
In the Auto mode – the PD64012 is communicating with the host via I^2C.
In the Enhanced mode – the PD64012 is communicating with the controller via SPI.

Block Diagram Description (see Figure 5)

The PD64002 PoE Manager complies with all requirements of IEEE standard 802.3af-2003, for detection. The device has been designed around two major sections:

1. A common Digital section, that serves all 12 channels
2. Twelve separate and identical channels for driving ports.

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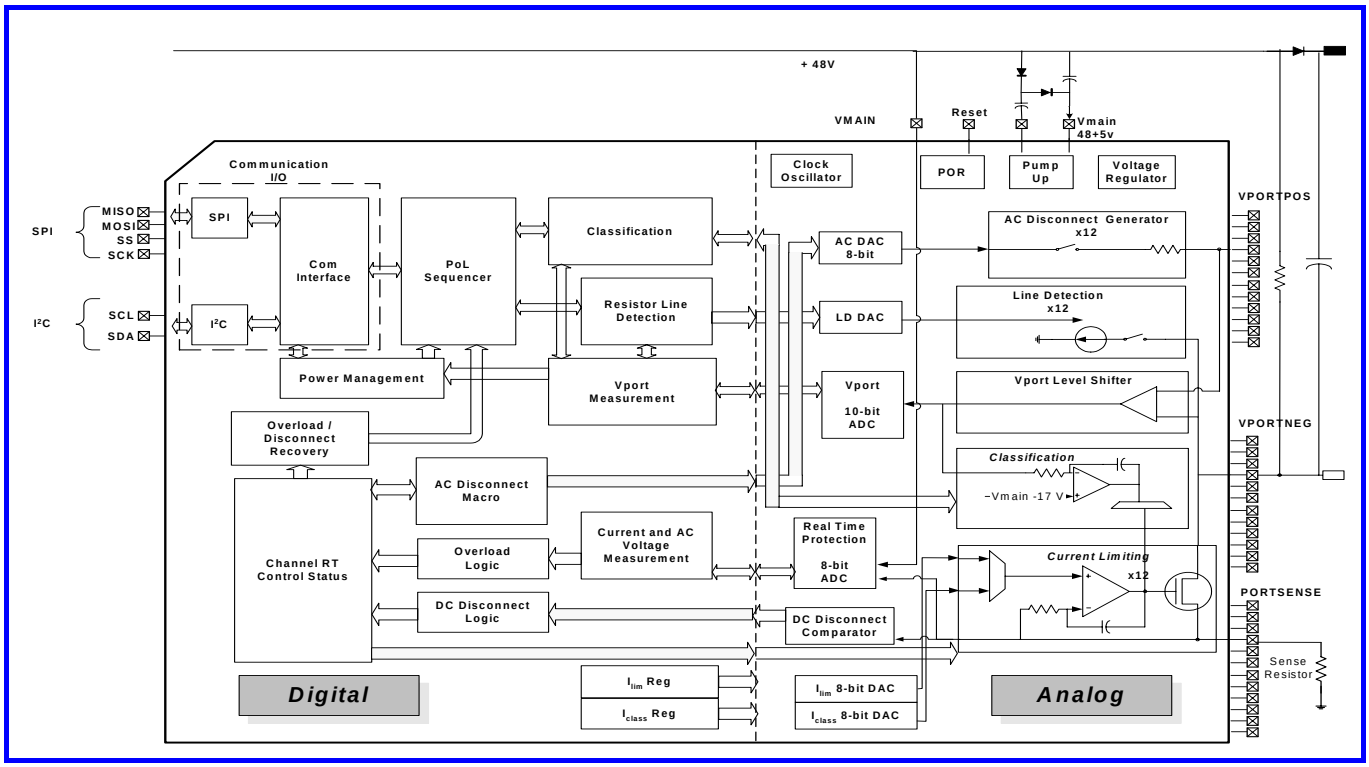

Figure 5: Internal Block Diagram

Digital Section

Communication I/O

The PD64012 incorporates two communication interfaces. When operating in the Enhanced mode, an SPI bus connects the PD63000 MCU to the PD64012s. The second interface is the I^2C, used in the Automatic mode (with the host).

Both interfaces are used to communicate the contents of internal registers between the PD64012 logic and the MCU.

PoE Sequencer

This central block of the Digital section includes a combination of internal state machines (macros). It is fed from the Overload/Disconnect Recovery circuit and from the Power Management block.

Power Management

Receives data from the Vport Measurement block and receives commands and controls from the Communication Interface. This, in order to control the power allocated to the system, as defined by the host. Power Management receives requests to enable ports and decides, by communicating with the Sequencer, whether power is to be allocated.

Overload /Disconnect Recovery

There is a number of macros which decide on port enable and some on port disconnect.

Port enabling: Classification, Resistor Line Detection and Vport Measurement.

Port disable: AC Disconnect, DC Disconnect and Overload Logic. These macros are connected to the Channel RT Control Status block. Based on the inputs from these macros, the Channel RT controller starts the shutdown operation or the recovery process. This is done according to preprogrammed parameters for different time windows, as shown in Figure 2, Power Limits.

Macros (802.3 Standard)
Classification – upon request from the MCU, a state machine applies a regulated 18 V on the port output. The internal current is measured by a metering circuit, compared with a number of preset ranges and in this manner, the classification is established.

Line Detection – the MCU generates a request to have four separate voltage levels applied to the output port. A unique measurement circuit monitors the delta between the second and third levels, and between the third and fourth levels. The voltage differences are compared with values stored in registers. By comparing the values, the system can decide whether or not to enable the port.

AC Disconnect – the system applies a sinusoidal signal to the positive terminal of the port. The voltage developed on the port terminals is proportional to the value of the load. If the load is high, the AC component riding on the port terminals, will be small and reversed. If the load low, the AC component will be large. A special circuit measures the level of the AC component and compares it with a value stored in a register. Based on the comparison results, the system decides to disable the port or not.

DC Disconnect for DC Modulation: senses if the port current falls below 7.5 mA. If so, a flag is raised and timers in the Channel RT Controller are enabled. The Channel RT Controller acts according to pre-programmed limits for thresholds and time windows, prior to initiating a disconnect status for that port. The circuitry takes into account PD's that modulate their current consumption, disconnecting them only if necessary.

Analog Section

Clock Oscillator
A 4 MHz oscillator, used for internal logic and timers.

Power on Reset (POR)
Monitors the internal regulated +3.3 V and generates a Reset signal, if this value drops below 2.8 V. The Reset signal resets the ASIC's logic and generates an output flag to the other PD64012 ASICs, via the RESET_N pin.

Charge Pump
This circuit block generates a voltage which increases the main input voltage by 10 VDC (approx.). This potential is used to operate the AC Disconnect circuits.

Current Limit
This circuit continuously checks the current for enabled ports. Once the current exceeds a specific level, the system starts to measure the elapsed time. If this period is greater than a preset threshold, the port is disabled. In all cases, the output current will not exceed a pre-established maximum.

Real Time Protection
This circuit receives flags from two locations in the PD64012: from the sense resistor and from the main input voltage (48 V). A 10-bit A/D Converter feeds the Digital section, at the Current and AC Voltage Measurement block. From there on, the system handles the levels according to pre-programmed limits.

DC Disconnect Comparator
Once the port current drops below a set limit, the comparator provides an indication to the DC Disconnect Logic to that effect.

PD-IM-7348 Evaluation Board

The performance features of the PD64012 PoE Manager can be fully appreciated with the PD-IM-7348 Evaluation Board. This board allows to investigate all functions accessible to the designer. The evaluation board supports up to 48 ports, has both I^2C and UART interfaces and can demonstrate the Enhanced and Auto modes.

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I²C Interface

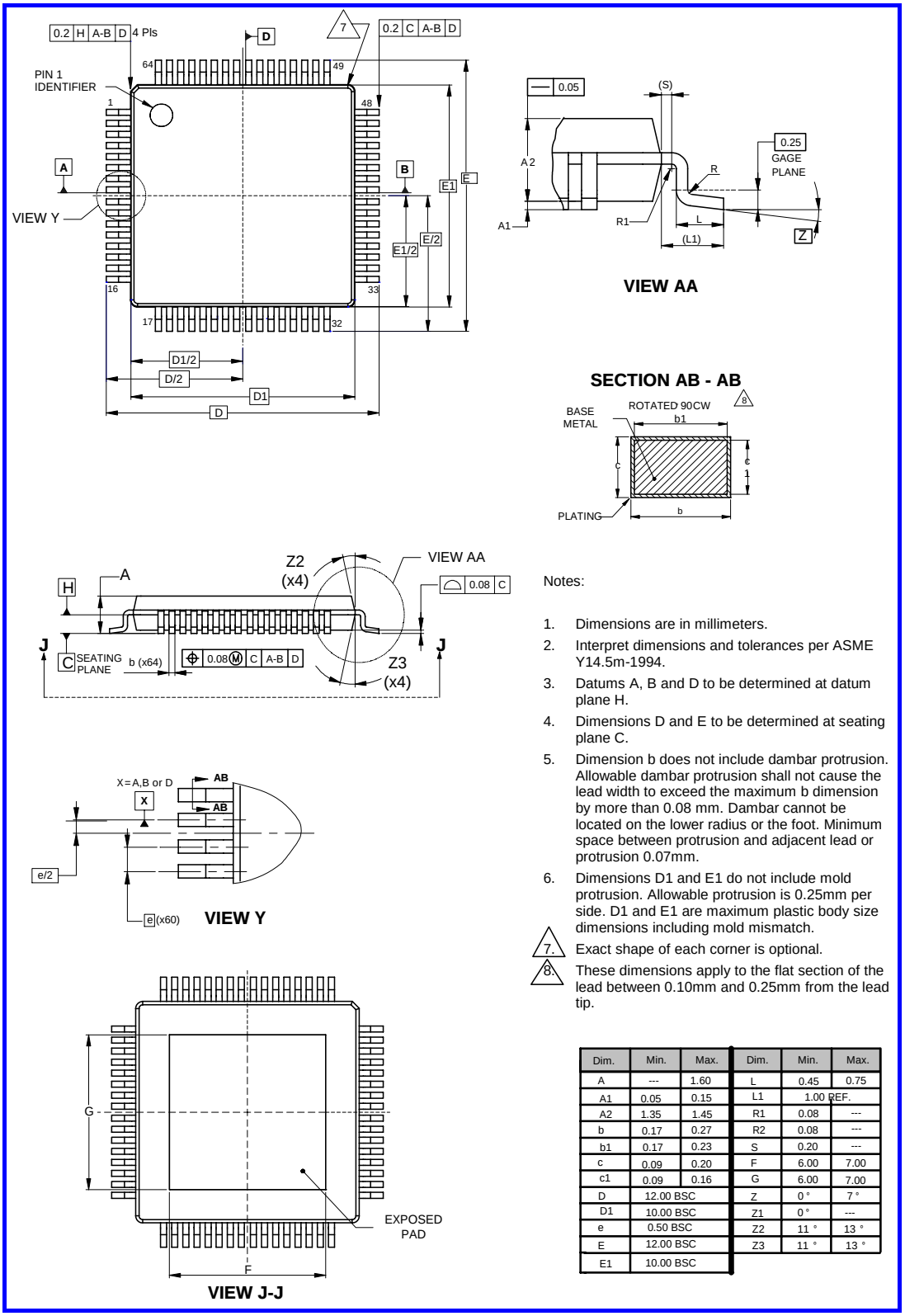
A standard I²C interface is used to communicate between the PD64012 and the host controller.
The PD64012's I²C interface is designed to support the following features:

- SLAVE mode only
- Normal-mode and Fast-mode data rate (0 to 400 kb/s)
- 7-bit addressing - the 7-bit addressing (128 addresses) uses the following address code:
  - First MSB = "0" (forced by internal logic)
  - 4 MSB address bits are set via the I2C_INI pin, according to the following table
  - "*mm*" bits are set through the ASIC_INI pin (Enhanced mode = "00"; Automatic mode Master ="00"; Automatic mode Slave = "01", "10", "11")
  - "*xxx*" - 3 LSB are ignored.

I²C ADDRESS	I2C_INI VOLTAGE LEVEL	I2C_INI INTERNAL A/D REGISTER	NOTES
Address #0	0 to 0.15 V	0,0000,*mm,xxx*	*General call addresses; not to be used*
Address #1	0.16 to 0.31 V	0,0001,*mm,xxx*	
Address #2	0.32 to 0.47 V	0,0010,*mm,xxx*	
Address #3	0.48 to 0.62 V	0,0011,*mm,xxx*	
Address #4	0.63 to 0.77 V	0,0100,*mm,xxx*	
Address #5	0.78 to 0.93 V	0,0101,*mm,xxx*	
Address #6	0.94 to 1.09 V	0,0110,*mm,xxx*	
Address #7	1.10 to 1.24 V	0,0111,*mm,xxx*	
Address #8	1.25 to 1.40 V	0,1000,*mm,xxx*	
Address #9	1.41 to 1.55 V	0,1001,*mm,xxx*	
Address #10	1.56 to 1.71 V	0,1010,*mm,xxx*	
Address #11	1.72 to 1.87	0,1011,*mm,xxx*	
Address #12	1.88 to 2.02 V	0,1100,*mm,xxx*	
Address #13	2.03 to 2.18 V	0,1101,*mm,xxx*	
Address #14	2.19 to 2.33 V	0,1110,*mm,xxx*	
Address #15	2.34 to 2.5 V	1,1111,*mm,xxx*	

Package Information

The PD64012 is housed in a 64-pin plastic package, 10 x 10 x 1.4 mm, meeting JEDEC's MS-026 package outline and dimensions. Exposed pad (for heat-sinking purposes) dimensions are 6.00 by 7.00 mm.



Notes:

1. Dimensions are in millimeters.
2. Interpret dimensions and tolerances per ASME Y14.5m-1994.
3. Datums A, B and D to be determined at datum plane H.
4. Dimensions D and E to be determined at seating plane C.
5. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and adjacent lead or protrusion 0.07mm.
6. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
7. Exact shape of each corner is optional.
8. These dimensions apply to the flat section of the lead between 0.10mm and 0.25mm from the lead tip.

Dim.	Min.	Max.	Dim.	Min.	Max.
A	---	1.60	L	0.45	0.75
A1	0.05	0.15	L1	1.00 REF.	
A2	1.35	1.45	R1	0.08	---
b	0.17	0.27	R2	0.08	---
b1	0.17	0.23	S	0.20	---
c	0.09	0.20	F	6.00	7.00
c1	0.09	0.16	G	6.00	7.00
D	12.00 BSC		Z	0 °	7 °
D1	10.00 BSC		Z1	0 °	---
e	0.50 BSC		Z2	11 °	13 °
E	12.00 BSC		Z3	11 °	13 °
E1	10.00 BSC				

Figure 6: PD64012 Mechanical Dimensions

Applications

The PD64012 may be integrated into a number of applications, ranging from daughter boards to full integration into Ethernet switches. Examples of such applications are:

Integrated directly in a switch – facilitates the entire PoE concept, by including the ASIC(s) on the main switch PCB.
Daughter board add-on – in which the ASIC is integrated into a small PCB for PoE, mounted on top of the switch's main PCB.
Midspan units – stand alone devices, installed between the Ethernet switch and powered devices (telephone, camera, wireless LAN, etc..). These Midspan units include the PD64012 ASIC as a PoE control element, to inject power over the communication lines.

Figures 7 thru 10 provide detailed schematic diagrams for various applications of the PD64012.

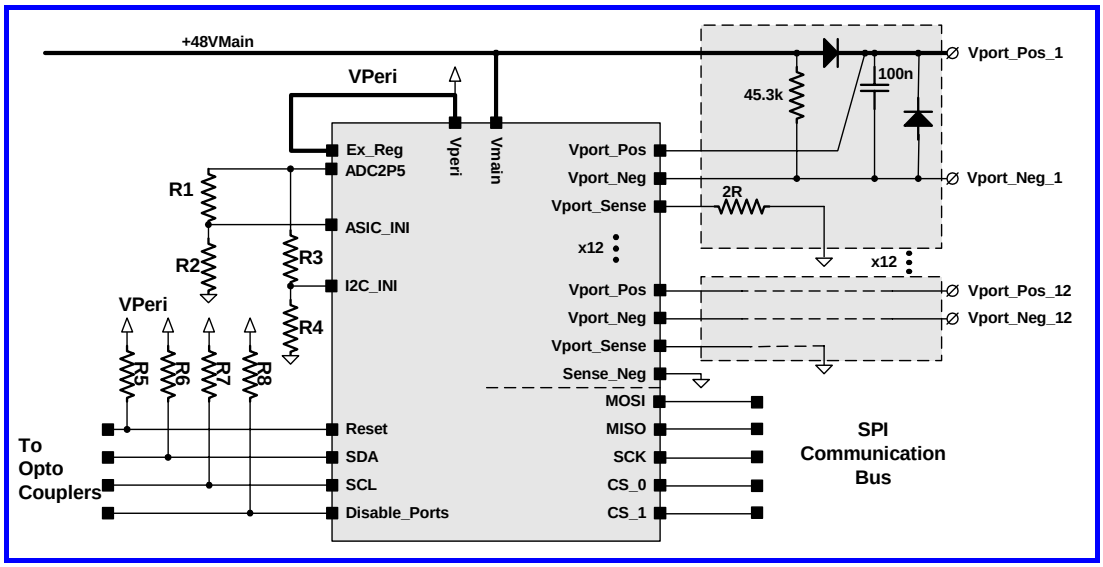


Figure 7 - Single-port Application with AC Disconnect Support

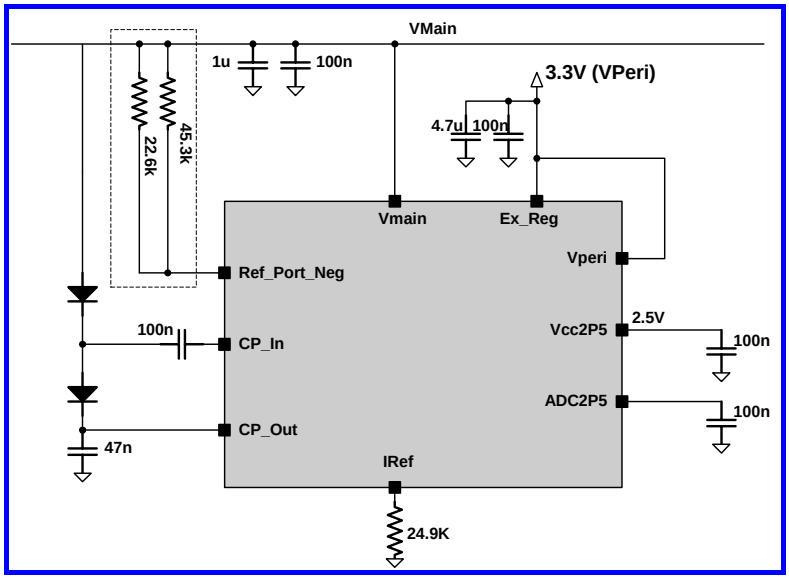


Figure 8 - Typical Power Filtering

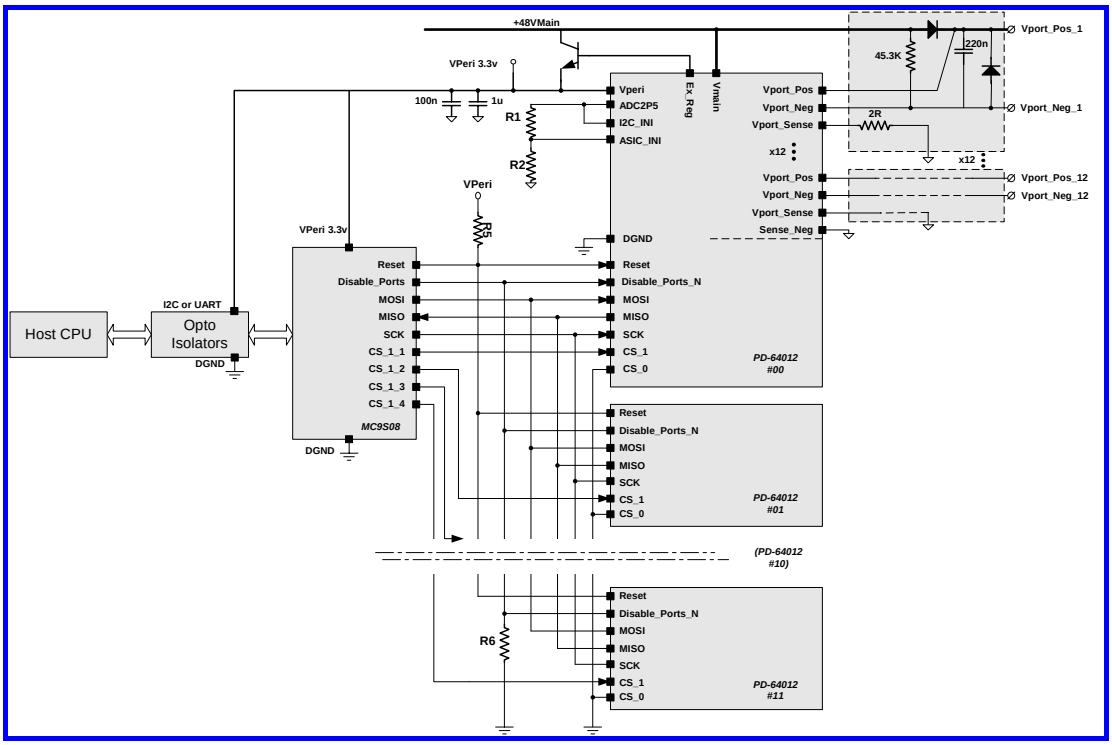


Figure 9 - Enhanced Mode Application

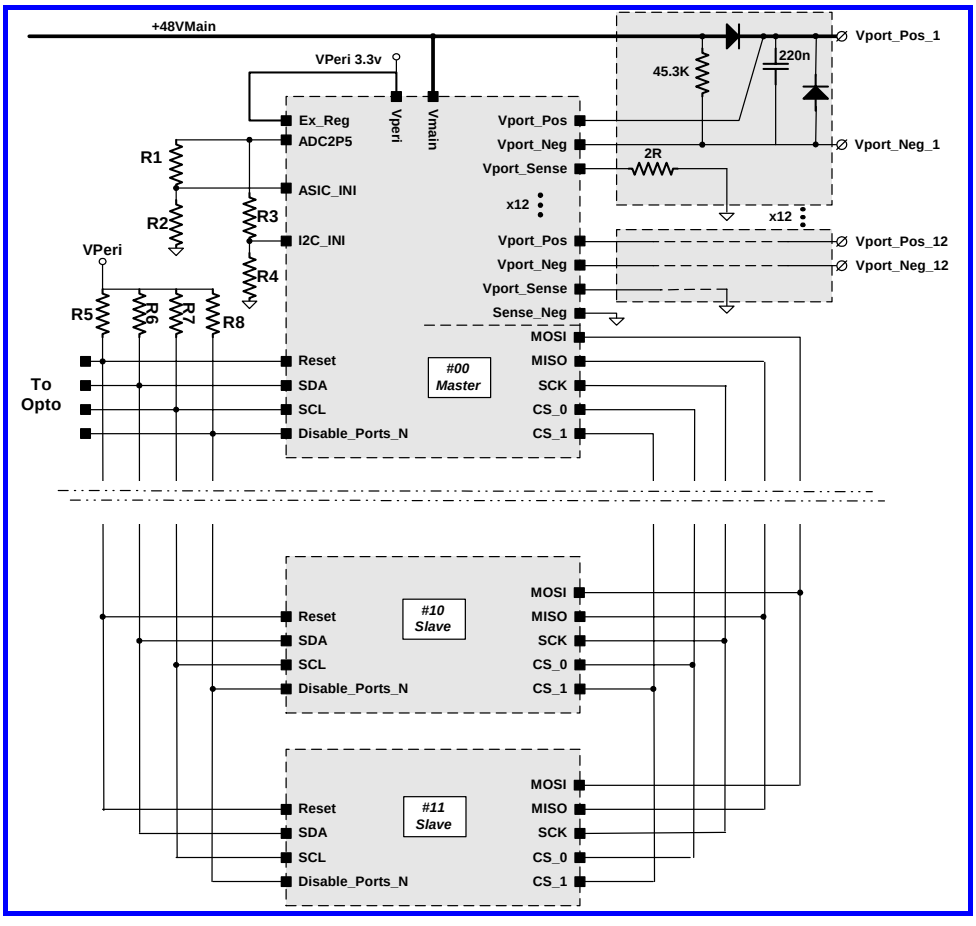


Figure 10 - Automatic Mode Application

Reader Notes

06-0003-058 (Rev. 2.8) / 5 August 2004

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Revision History

Revision Level / Date	Para. Affected/page	Description
2.3 / 10 Dec. 03	Ordering Information/page 1	Lower temperature range deleted. Remains single range only: -20 to +85 °C.
2.4 / 18 Dec. 03	Mode Configuration Method/page 8 I²C Interface/page 11	Deleted extreneous values for ASIC_INI and deleted default Mode value. Deleted primary default value in the table column for Notes.
2.41 / 10 Jan. 04	Features/page 1	Changed MIB from draft to RFC 3621.
2.5 / 9 Feb. 04	Front & back pages	Added policy statements and disclaimers.
2.6 / 10 Mar. 04	Several	Added temp. of junction-case, under max ratings; added thermal data on page 4; added protection mechanism on page 5.
2.7 / 1 Aug. 04	Macros/page 8 Analog section/page 9	Corrected inacuracies in descriptions.
2.8 / 5 Aug. 04	Pin Configuration/1	Added part number and associated description.