

**PD69101**  
**Datasheet**  
**1-Port PSE PoE Controller**  
March 2018



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# 1 Revision History

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The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 2.0

Revision 2.0 was published in March 2018. The following is a summary of changes in revision 2.0 of this document.

- Document format was updated.
- MSL level was updated from 1 to 3.
- 4-pair application was removed.
- Tape and Reel—Packaging Information section was added. For more information, see [Tape and Reel—Packaging Information \(see page 20\)](#).
- Part marking is updated. For more information, see [Ordering Information \(see page 22\)](#).

## 1.2 Revision 1.9

Revision 1.9 was published in March 2014. The following is a summary of changes in revision 1.9 of this document.

- TETA JB was added.
- A typo in the ESD parameter was corrected.
- Vmain out-of-range information was corrected.

## 1.3 Revision 1.8

Revision 1.8 was published in October 2013. In revision 1.8 of this document, the extended input voltage range was updated to 32 V–57 V.

## 1.4 Revision 1.7

Revision 1.7 was published in July 2013. In revision 1.7 of this document, TETA JC data was added.

## 1.5 Revision 1.6

Revision 1.6 was published in July 2013. In revision 1.6 of this document, the IC marking was updated.

## 1.6 Revision 1.5

Revision 1.5 was published in December 2010. In revision 1.5 of this document, parameters were updated.

## 1.7 Revision 1.4

Revision 1.4 was published in September 2010. In revision 1.4 of this document, parameters were updated.

## 1.8 Revision 1.3

Revision 1.3 was published in June 2010. In revision 1.3 of this document, parameters were updated.

## 1.9 Revision 1.2

Revision 1.2 was published in June 2010. In revision 1.2 of this document, the package drawing was updated.

## 1.10 Revision 1.1

Revision 1.1 was published in March 2010. In revision 1.1 of this document, the wave forms and functionality were updated according to evaluation results.

## **1.11 Revision 1.0**

Revision 1.0 was published in March 2010. It was the first publication of this document.

## 2 Product Overview

Microsemi's PD69101 is a single-port, mixed-signal, high-voltage Power over Ethernet (PoE) driver. Utilized in Ethernet switches, it enables network devices to share power and data over the same cable. It enables detection of IEEE 802.3af-2003-compliant powered devices (PDs) and IEEE 802.3at high-power devices, ensuring safe power feeding and disconnection of ports, with full digital control and a minimum of external components. A "plug-and-play" device, the PD69101 executes all real-time functions as specified in the IEEE 802.3af-2003 (AF) and IEEE 802.3at high-power (AT) standards, including load detection, AF and AT classification, and multiple classification attempts (MCA).

Integrating power, analog, and state-of-the-art logic, the PD69101 fits into a single 24-pin plastic QFN package. The chip includes built-in internal thermal protection, and two LEDs provide port state and port type (AF/AT) indication.

The PD69101:

- Is designed to detect and disable disconnected ports, utilizing DC disconnection methods as specified in the AF and IEEE 802.3ar-2009 standards.
- Is a low-power device using an internal 0.34  $\Omega$  MOSFET and an external 0.5  $\Omega$  sense resistor.
- Can optionally detect legacy/pre-standard PD devices.
- Provides over-load, under-load, over-voltage, over-temperature, and short-circuiting PD protection.
- Supports supply voltages ranging from 32 V to 57 VDC with no need for additional power supply sources.

### 2.1 Features

PD69101 has the following key features.

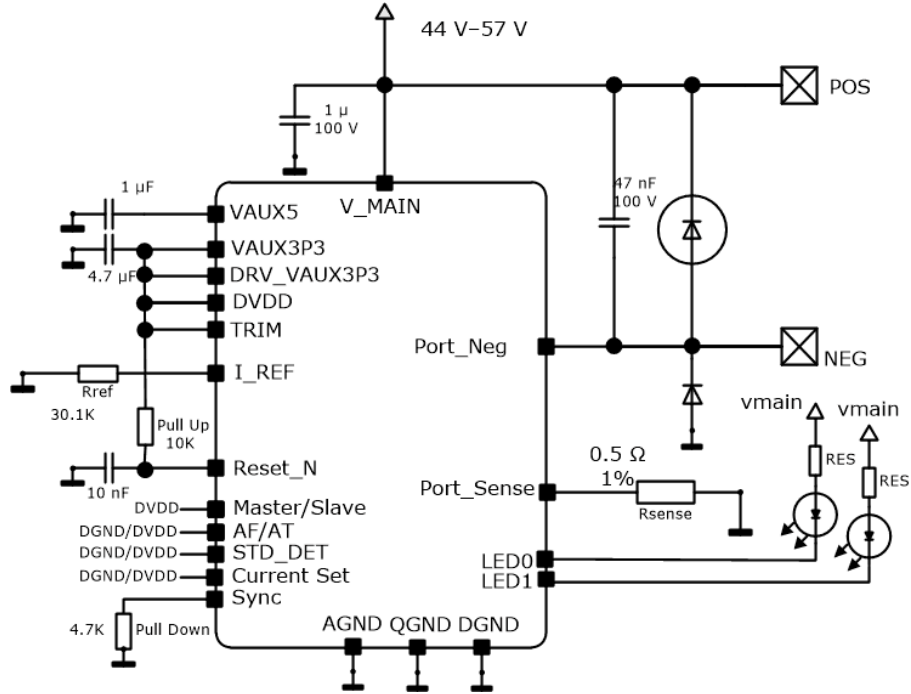
- Fully AF and AT compliant
- Includes two-event classification
- Supports pre-standard PD detection
- Supports Cisco device detection
- Single DC voltage input (32 V–57 VDC)
- Supports two pairs
- $V_{MAIN}$  out-of-range protection
- Wide temperature range:  $-40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$
- Over-temperature protection
- Low thermal dissipation (0.5  $\Omega$  sense resistor)
- Includes on/off command pin
- 2 $\times$  direct LEDs drive
- Continuous port monitoring and system data
- Configurable load current setting
- Configurable AT/AF modes
- Configurable standard and legacy detection mode
- Power soft-start mechanism
- On-chip thermal protection
- Voltage monitoring and protection
- Built-in 3.3 VDC regulator
- Internal power-on reset
- RoHS compliant
- Low  $R_{dson}$  FET: 0.3  $\Omega$
- MSL3

## 2.2 Typical 2-Pairs Application

This typical application illustrates a simple plug-and-play PoE solution for a single Ethernet port switch or hub.

POS and NEG signals should be connected to the switch RJ45 jack. AF and AT modes of operations are set through AF/AT and current-set pins (DGND or DVDD).

Figure 1 • Typical 2-Pair Application

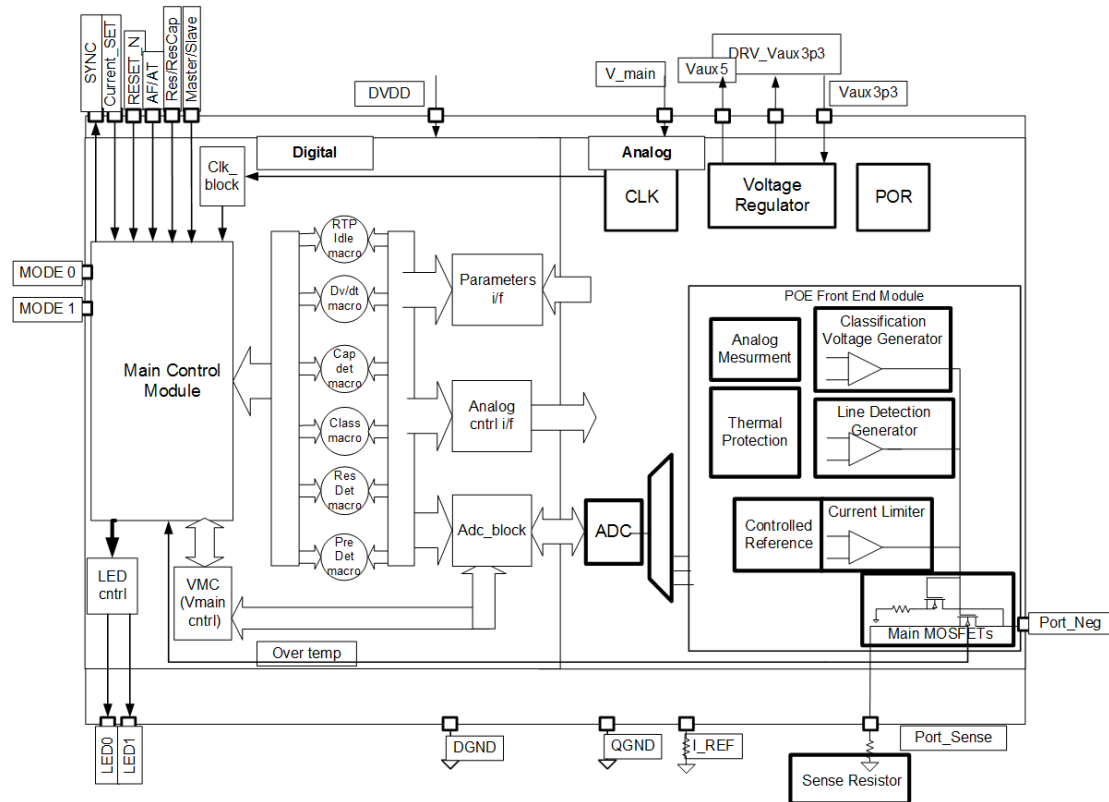


## 3 Functional Descriptions

The PD69101 has two major sections: a digital section that controls and monitors the logical PoE functions (state machines, timings, and so on) and an analog section that performs the front-end analog PoE functionality.

The following illustration shows the internal functional blocks of the PD69101 device.

Figure 2 • PD69101 Internal Block Diagram



### 3.1 Logic Main Control Module

The logic main control block includes the digital timing mechanisms and state machines, synchronizing and activating the PoE functions, such as:

- Real-time protection (RTP)
- Start-up macro (DVDT)
- Load signature detection (RES DET)
- Classification macro (CLASS)
- Voltage and current monitoring registers (VMC)
- LEDs stream out control indications
- ADC interfacing
- Direct digital signals with analog block

#### 3.1.1 Line Detection Generator

Upon request from the main control module, four different voltage levels are generated by the line detection generator, ensuring robust AF/AT line detection functionality.



### **3.1.2 Classification Generator**

Upon request from the main control module, the state machine applies a regulated class event and mark event voltage to the ports, as required by the IEEE standard.

### **3.1.3 Current Limiter**

This circuit continuously monitors the current of powered ports and limits the current to a specific value, according to pre-defined limits as set by AF/AT and current\_set pins. In cases where the current exceeds this specific level, the system starts measuring the elapsed time. If this time period is greater than a preset threshold, the port is disconnected.

### **3.1.4 Main MOSFET**

Main power switching FET, used to control PoE current into the load.

### **3.1.5 Analog-to-Digital Converter (ADC)**

A 10-bit analog-to-digital converter, used to convert analog signals into digital registers for the logic control module.

### **3.1.6 Power on Reset (POR)**

This circuit monitors the internal 3.3 VDC levels. If this voltage drops below specific thresholds, a reset signal is generated and the PD69101s are reset.

### **3.1.7 Voltage Regulator**

The voltage regulator generates 3.3 VDC and 5 VDC for the internal circuitry. These voltages are derived from the Vmain supply.

### **3.1.8 CLK**

CLK is an internal 8 MHz clock oscillator.

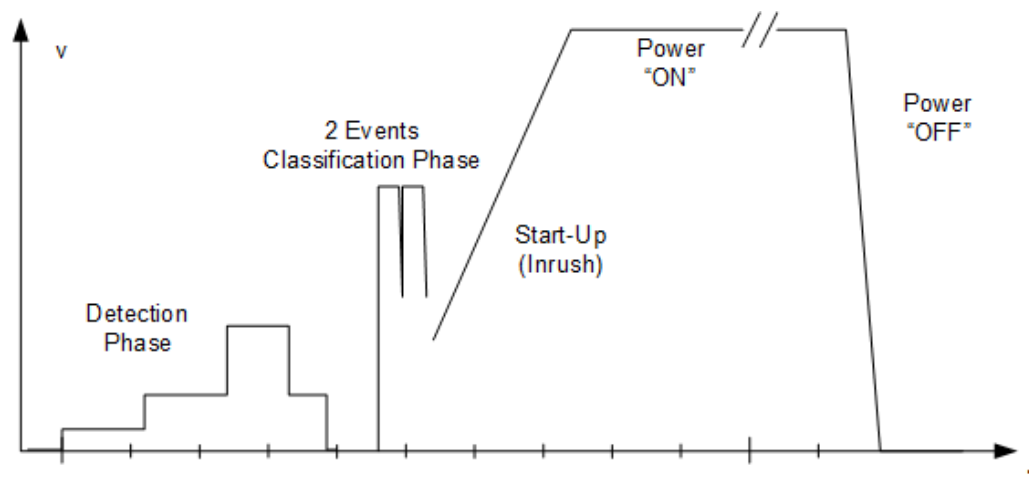
## **3.2 Application Information**

The PD69101 performs IEEE 802.3af and IEEE 802.3at functionality as well as legacy (capacitor) and Cisco PD detection, in addition to protections such as short circuit and dV/dT protection upon startup.

### 3.2.1 Line Detection

The line detection feature detects a valid AF or AT load, as specified in the AF/AT standard. The resistor value should range from 19K  $\Omega$  to 26.5K  $\Omega$ . Line detection is based on four different voltage levels generated over the PD (the load), as shown in the following illustration.

**Figure 3 • Typical PoE Voltage Timing Diagram**



### 3.2.2 Legacy (Capacitor) Detection

In cases where pin 24 is set to 0, the PD69101's detection mechanism is configured to detect and power up legacy PDs, as well as AF/AT-compliant. This mechanism also detects and powers up Cisco legacy PDs.

### 3.2.3 Classification

The classification process takes place right after the resistor detection, when the resistor detection has completed successfully. The main goal of the classification process is to detect the PD class, as specified in the IEEE 802.3AF and AT standards. In AF mode, the classification mechanism is based on a single voltage level (single class event). In AT mode, the classification mechanism is based on two voltage levels (dual class event) as defined in IEEE 802.3at-2009. In AT mode, when the PD is class 0–3, the PD69101 generates a single class event. When the PD is class 4, the PD69101 generates two class events.

### 3.2.4 Port Start Up

Upon a successful detection and classification process, power is applied to the load through a controlled start-up mechanism. During this period, current is limited to 425 mA for a typical duration of 65 mS, which enables the PD load to charge and enter a steady state power condition.

### 3.2.5 Over-Load Detection and Port Shut Down

After power up, the PD69101 automatically initializes its internal protection mechanisms to monitor and disconnect power from the load in cases where extreme conditions (such as over-current or short port terminal scenarios) occur, as specified in the IEEE 802.3AF/AT standard.

### 3.2.6 Disconnect Detection

The PD69101 supports the DC disconnect function as per the IEEE 802.3AF/AT standard. This mechanism continuously monitors the load current and disconnects power in cases where the load current is below 7.5 mA (typical) for more than 322 mS.

### 3.2.7 Over-Temperature Protection

The PD69101 has internal temperature sensors that continuously monitor junction temperature and disconnect load power when the junction temperature exceeds 200 °C. This mechanism protects the device from extreme events such as high ambient temperature or other thermo-mechanical failures that may damage the PD69101.

### 3.2.8 V MAIN Out-of-Range Protection

The PD69101 automatically disconnects port power when Vmain exceeds 57.5 VDC ±0.5 VDC. This is an extremely valuable feature that protects the load if the main power source is faulty or damaged.

### 3.2.9 Serial Communication: Monitoring Mode

When MODE0 and MODE1 input pins are configured to serial monitoring mode (01), the PD69101 continuously and repeatedly transmits out the content of nine internal registers.

- Data out stream is transmitted through LED1 (pin 14)
- Clock out stream is transmitted through LED0 (pin 13)
- Data stream is shifted out with a 1 MHz clock (1 μsec)
- Total transaction packet length is 116 μsec
- The transmission is repeated every 1 μsec
- Between transactions, the clock is held low while the data stream out is stable high/low.

**Note:** To exploit LED1 and LED0 to communicate and monitor transmissions, use a 1K Ω pull-up resistor to the DVDD.

The following table shows the stream out data transmits of 116 bits, starting from MSB to LSB.

**Table 1 • Serial Monitoring Mode**

MSB					LSB			
Internal 0	Internal 1	Internal 2	Internal 3	Internal 4	VPORT	VMAIN	IPOINT	Port Status
13 bits	10 bits	23 bits	16 bits	16 bits	10 bits	10 bits	13 bits	5 bits
78 internal signals used for internal tests					Port voltage measurement	Vmain voltage measurement	Port current measurement	Real-time port status indication
					LSB= 58 mV		LSB= 238 μA	For more information, see <a href="#">Port Status Coding (see page 8)</a> .
					V= Decimal × 58 mV	LSB= 58 mV	I= Decimal × 238 μA	
						V= Decimal × 58 mV		

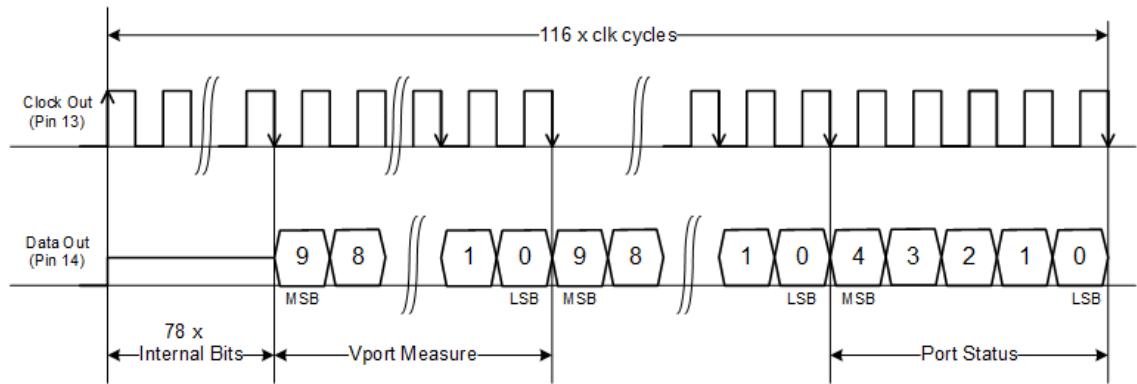
The following table lists the port status coding.

**Table 2 • Port Status Coding**

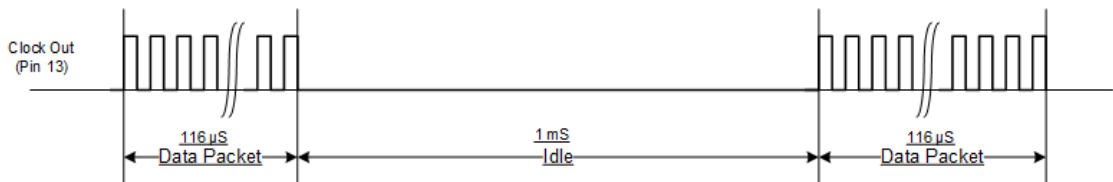
Binary MSB to LSB	Decimal Value	Description
00000	0	PoE idle state
00001	1	
00010	2	
00011	3	Searching phase
00100	4	Res detection phase
00101	5	Back off phase
00110	6	

Binary MSB to LSB	Decimal Value	Description
00111	7	Class phase
01000	8	
01001	9	Wait for start up
01010	10	
01100	12	
01011	11	Cap detection
01101	13	Start up
01110	14	Ongoing
01111	15	
10000	16	UDL
10001	17	
10010	18	Overload or short circuit
10011	19	Vmain out of range
10100	20	

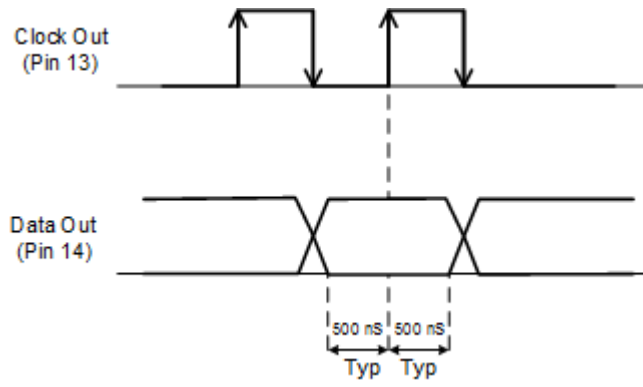
**Figure 4 • Data Stream Out**



**Figure 5 • Multi-Packet Idle Time (Between Packets)**



**Figure 6 • Data/Clock Typical Timing**



## 4 Electrical Specifications

Unless otherwise specified, the following specifications apply to the operating ambient temperature ( $T_{AMB}$ ):  $-40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$ .

**Table 3 • Power Supply**

Parameter	Symbol	Test Conditions/ Comment	Min.	Typ.	Max.	Unit
Input voltage	$V_{MAIN}$	Supports full IEEE 802.3 functionality	32	55	57	VDC
Power supply current at operating mode		$V_{MAIN} = 55\text{ V}$			10	mA

**Table 4 • Digital I/O**

Parameter	Symbol	Test Conditions/ Comment	Min.	Typ.	Max.	Unit
Input logic, high threshold	$V_{IH}$		2.2			VDC
Input logic, low threshold	$V_{IL}$				0.8	VDC
Input hysteresis voltage			0.4	0.6	0.8	VDC
Input high current	$I_{IH}$		-10		10	$\mu\text{A}$
Input low current	$I_{IL}$		-10		10	$\mu\text{A}$
Output high voltage	$V_{OH}$	For $I_{OH} = -1\text{ mA}$	2.4			VDC
Output low voltage	$V_{OL}$	$I_{OH} = 1\text{ mA}$			0.4	VDC

**Table 5 • PoE Load Currents**

Parameter	Symbol	Test Conditions /Comment	Min.	Typ.	Max.	Unit
AT, high limit mode	AT_LIM_HIGH (high current level, for future use)	$R_{SENSE} = 0.5\ \Omega$ 1%, connected at Port_Sense pin	1.18	1.2	1.28	A
AT, medium limit mode	AT_LIM_MID (medium current level, for future use)		847	874	919	mA
AT, low limit mode	AT_LIM_LOW		706	722	767	mA
AF, limit mode	AF_LIM		410	425	448	mA

**Table 6 • Main Power Switching FET**

Parameter	Symbol	Typ.	Unit
On resistance	$R_{DSON}$	0.3	$\Omega$
Internal thermal protection threshold		200	$^{\circ}\text{C}$

**Table 7 • LED0 and LED1 Drivers**

Parameter	Symbol	Typ.	Max.	Unit
Current sink	$I_{SINK}$ (from $V_{main}$ to AGND)	3	5	mA

## 4.1 Dynamic Characteristics

The PD69101 utilizes three current level thresholds ( $I_{MIN}$ ,  $I_{CUT}$ ,  $I_{LIM}$ ) and three timers ( $T_{MIN}$ ,  $T_{CUT}$ ,  $T_{LIM}$ ).

- Loads that consume  $I_{LIM}$  current for more than  $T_{LIM}$  are labeled as "short circuit state" and shut down.
- Loads that dissipate more than  $I_{CUT}$  for longer than  $T_{CUT}$  are labeled as overloads and are shut down.
- If output power is below  $I_{MIN}$  for more than  $T_{MIN}$ , the PD is labeled as "no load" and is shut down.

Automatic recovery from overload and no load conditions is attempted every  $T_{OVLREC}$  periods (typically one second). Output power is limited to  $I_{LIM}$ , which is a maximum peak current allowed at the port.

**Table 8 • IEEE 802.3 AF Mode Parameters**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Automatic recovery from no load shutdown		$T_{UDLREC}$ value, measured from port shutdown point (can be modified through control port)		1		sec
Cutoff timer accuracy		Typical accuracy of $T_{cut}$		2		ms
Inrush current	$I_{Inrsh}$	For $t = 50$ ms, $C_{load} = 180 \mu F$ (max)	400		450	mA
Output current operating range	$I_{PORT}$	Continuous operation after startup period	10		375	mA
Output power available operating range	$P_{PORT}$	Continuous operation after startup period, at port output	0.57		15.4	W
Off-mode current	$I_{MIN1}$	Must disconnect for T greater than $T_{UVL}$	0		5	mA
	$I_{MIN2}$	May or may not disconnect when T is greater than $T_{UVL}$	5	7.5	10	mA
PD power maintenance request drop-out time limit	$T_{PMDO}$	Buffer period to handle transitions	300		400	ms
Over-load current detection range	$I_{CUT}$	Time limited to $T_{OVL}$	350		400	mA
Over-load time limit	$T_{OVL}$		50		75	ms
Turn-on rise time	$T_{RISE}$	From 10% to 90% of $V_{port}$ (specified for PD load consisting of 100 $\mu F$ capacitor in parallel to 200 $\Omega$ )	15			$\mu s$
Turn-off time	$T_{OFF}$	From $V_{port}$ to 2.8 VDC			500	ms
Time maintain power signature	$T_{MPS}$	DC modulation time for DC disconnect		49		ms

**Table 9 • IEEE 802.3 AT Mode Parameters**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Automatic recovery from no load shutdown		$T_{UDLREC}$ value, measured from port shutdown point (can be modified through control port)		1		sec
Cutoff timer accuracy		Typical accuracy of $T_{cut}$		2		ms
Inrush current	$I_{INRSH}$	For $t = 50$ ms, $C_{load} = 180$ $\mu$ F (max)	400		450	mA
Output current operating range	$I_{PORT}$	Continuous operation after startup period	10		725	mA
Output power available operating range	$P_{PORT}$	Continuous operation after startup period, at port output	0.57		36.25	W
Off-mode current	$I_{MIN1}$	Must disconnect for T greater than $T_{UVL}$	0		5	mA
	$I_{MIN2}$	May or may not disconnect when T is greater than $T_{UVL}$	5	7.5	10	mA
PD power maintenance request drop-out time limit	$T_{PMDO}$	Buffer period to handle transitions	300		400	ms
Over-load current detection range	$I_{CUT}$	Time limited to $T_{OVL}$			600	mA
Over-load time limit	$T_{OVL}$		50		75	ms
Turn-on rise time	$T_{RISE}$	From 10% to 90% of $V_{port}$ (specified for PD load consisting of 100 $\mu$ F capacitor in parallel to 200 $\Omega$ ).	15			$\mu$ s
Turn-off time	$T_{OFF}$	From $V_{port}$ to 2.8 VDC			500	ms
Time maintain power signature	$T_{MPS}$	DC modulation time for DC disconnect		49		ms

## 4.2 Absolute Maximum Ratings

The following table lists the absolute maximum ratings for the PD69101. Exceeding these ratings can cause damage to the device. Pin Port\_Sense is ESD sensitive and passes 500 V HBM. All voltages are with respect to ground. Currents are marked positive when flowing into a specified terminal and marked negative when flowing out of a specified terminal.

**Table 10 • Absolute Maximum Ratings**

Parameter	Rating
Supply input voltage ( $V_{MAIN}$ )	-0.3 VDC to 74 VDC
Port_Neg pin, LED0, LED1	-0.3 VDC to 74 VDC
Port_Sense pin	-0.3 VDC to 3.6 VDC
QGND, AGND pins	-0.3 VDC to 0.3 VDC
VAUX5	-0.3 V to 5.5 V
All other pins	-0.3 VDC to 3.6 VDC
Operating ambient temperature range	-40 °C to 85 °C
Maximum operating junction temperature	150 °C
Storage temperature range	-65 °C to 150 °C
ESD protection at all I/O pins	$\pm 2$ KV (HBM)



### 4.3 Moisture Sensitivity

This device is rated moisture sensitivity level 3 or better as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

### 4.4 Power Dissipation Information

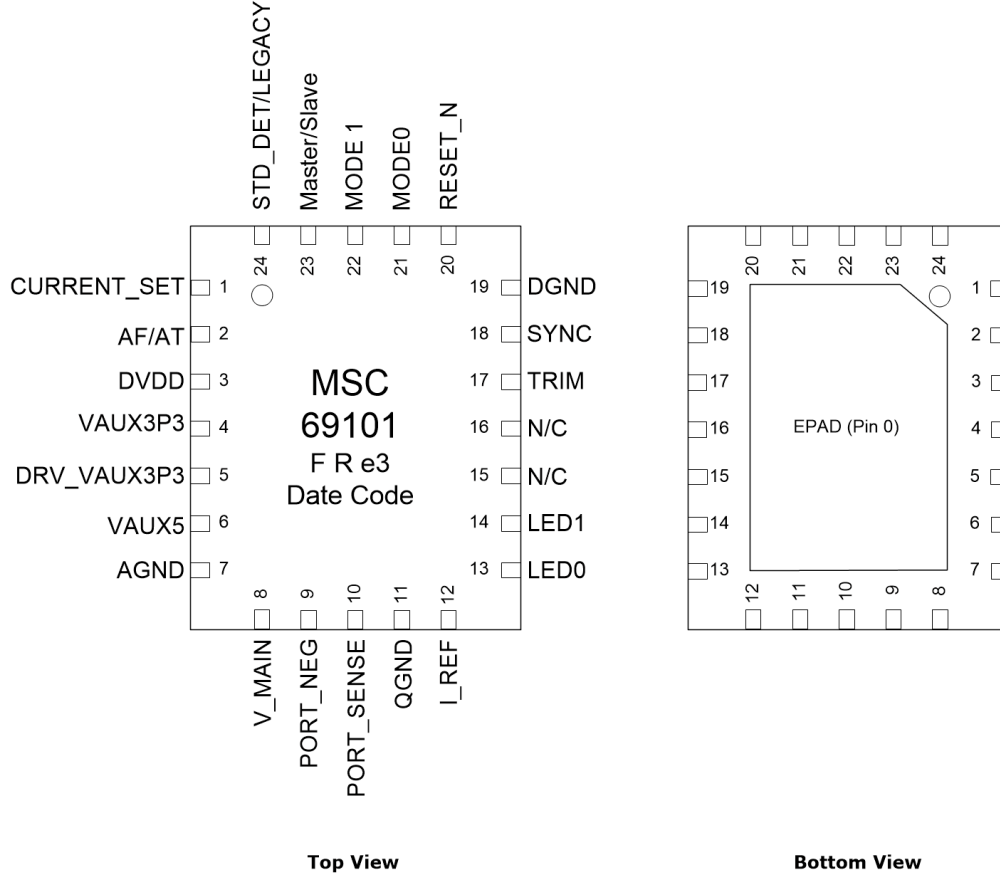
**Table 11 • Power Dissipation**

Parameter	Value
Rsense power dissipation	$0.5 \Omega \times I_{PORT}^2$
Rds_ON power dissipation	$0.3 \Omega \times I_{PORT}^2$
Pport_AF = 15.4 W	PRsense = 51 mW (320 mA)
PRds_ON	31 mW (320 mA)
Pport_AT = 30 W	PRsense = 180 mW (600 mA)
PRds_ON	108 mW (600 mA)
Typical PD69101 self power dissipation (including internal regulations)	0.5 W (50 VDC)
Typical PD69101 2-pairs AF application power dissipation	$0.5 \text{ W} + 51 \text{ mW} + 31 \text{ mW} = 0.582 \text{ W}$
Typical PD69101 2-pairs AT application power dissipation	$0.5 \text{ W} + 180 \text{ mW} + 108 \text{ mW} = 0.788 \text{ W}$

## 5 Pin Descriptions

The following illustration shows the device pin diagram from the top and bottom views.

Figure 7 • PD69101 Pinout



The following table lists the pin descriptions for the PD69101 device.

Table 12 • Pin Descriptions

Number	Name	Type	Description
0	Exposed PAD	Analog ground	Exposed pad; metal plate on the IC bottom side connected to analog ground. A high-quality ground plane (about 500 mil. inch over 500 mil. inch) should be deployed around this pin whenever possible.
1	CURRENT_SET	Digital input	User input to set AF/AT and maximum current limit.
2	AF/AT		Use pull-up resistors to DVDD or pull-down resistors to DGND to set the mode of operation according to <a href="#">CURRENT_SET and AF/AT Pins</a> (see page 17).
3	DVDD	Power in	Regulated input voltage (3.3 V) for internal digital circuitry. Should be externally connected to pin 4.
4	VAUX3P3	Power in	Voltage regulation in, 3.3 VDC.  Connect to pin 5. A 4.7 $\mu$ F capacitor to AGND is recommended.

Number	Name	Type	Description
5	DRV_VAUX3P3	Power out	Internal voltage regulator out, 3.3 VDC. Should be externally connected to pin 4.
6	VAUX5	Power	Regulated 5 VDC voltage filter. A 1 $\mu$ F capacitor to AGND is recommended.
7	AGND	Power	Analog ground.
8	V_MAIN	Power	Supply voltage for the internal analog circuit. Place a low-ESR bypass capacitor with low impedance trace as close as possible to AGND and this pin (not less than 1 $\mu$ F).
9	PORT_NEG	Analog I/O	Negative output of the port.
10	PORT_SENSE	Analog input	Sense resistor port input (connected to 0.5, 1% $\Omega$ resistor to GND).
11	QGND	Power	Quiet analog ground; used for sensitive analog cells.
12	I_REF	Analog I/O	Resistor reference. Connect 30.1K 1% resistor to QGND.
13	LED0	Open-drain I /O	Port status direct LED indications. For details, see <a href="#">2-Pair Behavior (see page 17)</a> . This is a high-voltage, open-drain, active low (SINK) output pin. Connection to LED and Vmain through a $\sim$ 18.2K $\Omega$ ( $\sim$ 3 mA) resistor is recommended.
14	LED1		
15	N/C	Analog I/O	Test pin (for production use only); keep open (not connected).
16	N/C		
17	TRIM	Analog input	Zapping input for IC production trimming. Should be connected to DVDD.
18	SYNC	Digital I/O	Synchronization open-drain I/O pin between master and slave.  In 2-pair mode (switch), this pin should be pulled down to DGND through a 4.7K $\Omega$ resistor.
19	DGND	Digital I/O	Digital ground.
20	RESET_N	Digital input	Reset input/on-off command (active low).
21	MODE 0	Test I/O	Configuration input pins.  Used to set mode of operation and test mode at production. Typically connected to DGND. For details, see <a href="#">Configuration Coding (see page 17)</a> .
22	MODE 1		
23	Master/Slave	Digital input	If connected to DVDD (3.3 VDC): master mode. If connected to GND: slave mode.
24	STD_DET /LEGACY	Digital input	User input pin to set the chip mode of operation.  1: DVDD= IEEE 802.3af-compliant resistor detection only. 0: DGND= IEEE 802.3AF/AT detection and legacy (non-standard) line detection.

**Note:** 0= Connect to DGND, 1= connect to DVDD.

## 5.1 CURRENT\_SET and AF/AT

These pins determine the typical PD load output current as listed in the following table.

**Table 13 • CURRENT\_SET and AF/AT Pins**

AT/AF Pin	Current_Set Pin	Max. Current I <sub>cur</sub> [mA]	Typical I <sub>um</sub> [mA]	IEEE 802.3
0	0	350	425	AF mode (standard)
1	0	600	722	AT mode (standard)
1	1	720	874	AT mode (high power)
0	1	1000	1200	AT mode (extra high power)

## 5.2 Mode of Operation Coding

The following table lists the mode of operation coding options related to pins 21 and 22.

**Table 14 • Configuration Coding**

Mode 0	Mode 1	Mode	Description
0	0	Normal operation mode	Standard operation PoE mode.  LED0 and LED1 outputs are used for direct LED drive as described in <a href="#">LED I/Os Behavior (see page 17)</a> .
0	1	Serial monitoring mode	Standard operation PoE mode.  LED0 and LED1 are used to continuously stream out internal logic signals for PoE monitoring.
1	0	Test mode	Internal IC test mode; used in production only.
1	1	Test mode	Internal IC test mode; used in production only.

## 5.3 LED I/Os Behavior

The following tables list the LED I/Os behavior related to pins 13 and 14 in 2-pair application. In both application types, the LED pin is a high-voltage open-drain output pin and an active low (sink) pin. That is, LED is “ON” when the I/O is pulled low.

**Table 15 • 2-Pair Behavior**

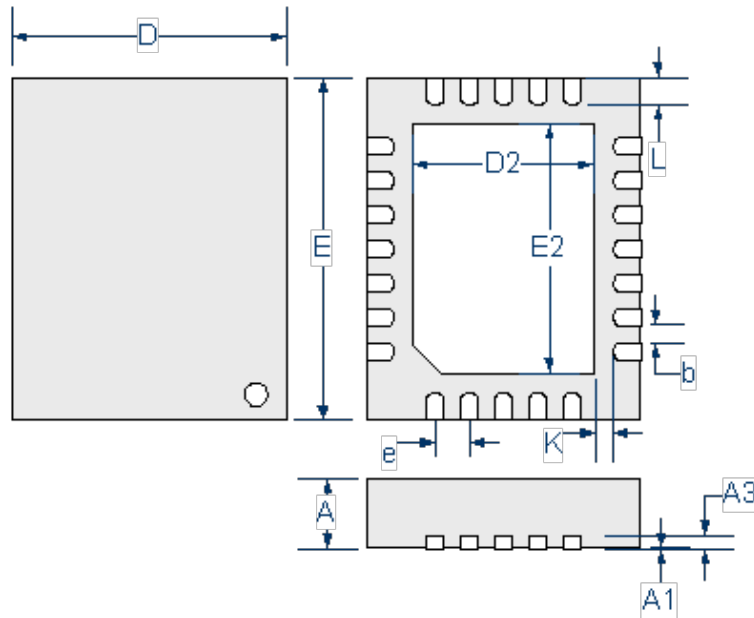
Status Indications	LED0	LED1	Notes
AF mode—port ON	ON	OFF	Useful for bi-color LED connected from LED0 to LED1.
AT mode (class AT was detected)—port ON	ON	ON	
AF mode—over-load or short	Blink 1 Hz	OFF	Blinking continues for ~2 sec.
AT mode—over-load or short	Blink 1 Hz	Blink 1 Hz	Blinking continues for ~2 sec.
Vmain voltage is out of range or IC over-temperature	Blink 4 Hz	OFF	Blinking continues as long as over-voltage or over-temperature state exists.
AF mode—port OFF	OFF	ON	Useful for bi-color LED connected from LED0 to LED1.
AT mode—port OFF	OFF	OFF	

## 6 Package Specifications

This section provides the package drawing, RoHS and solder reflow information, and thermal specifications for the PD69101 device.

The PD69101 package is a 4 mm × 5 mm, 24-pin QFN, as shown in the following illustration.

**Figure 8 • QFN Package**



Dimensions do not include protrusions; these shall not exceed 0.155 mm (.006”) on any side. Lead dimension shall not include solder coverage.

The following table lists the dimensions for the QFN package.

**Table 16 • Package Dimensions**

Dimension	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
K	0.20 MIN		0.008 MIN	
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	2.50	2.75	0.098	0.108
E2	3.50	3.75	0.138	0.148
D	4.00 BSC		0.158 BSC	
E	5.00 BSC		0.197 BSC	

## 6.1 RoHS and Solder Reflow Information

The PD69101 device is rated RoHS 6/6. The package is lead(Pb)-free, with a 100% matte tin finish. The package peak temperature for solder reflow (40 seconds maximum exposure) is 260 °C (0 °C, -5 °C).

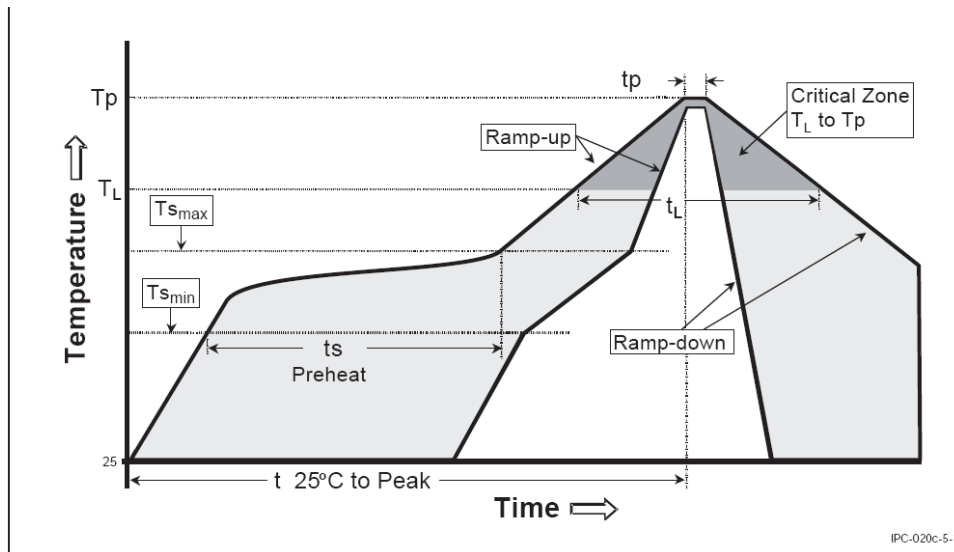
The following table lists the classification reflow profile information.

**Table 17 • Classification Reflow Profiles**

Profile Feature	Pb-Free Assembly
Average ramp-up rate ( $T_{S_{max}}$ to $T_p$ )	3 °C/second max.
Preheat:	150 °C
Temperature minimum ( $T_{S_{min}}$ )	200 °C
Temperature maximum ( $T_{S_{max}}$ )	60–180 seconds
Time ( $T_{S_{min}}$ to $T_{S_{max}}$ )	
Time maintained above:	217 °C
Temperature ( $T_L$ )	60–150 seconds
Time ( $t_L$ )	
Peak/classification temperature	See <a href="#">Package Classification Reflow Temperatures (see page )</a> .
Time within 5 °C of actual peak temperature ( $t_p$ )	20–40 seconds
Ramp-down rate	6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.

**Note:** All temperatures refer to the top-side of the package, measured on the package body surface.

**Figure 9 • Classification Reflow Profile Diagram**



**Note:** Exceeding these ratings can damage the device.

## 6.2 Thermal Specifications

The following table lists the thermal specifications for the PD69101 device.

**Table 18 • Thermal Specifications**

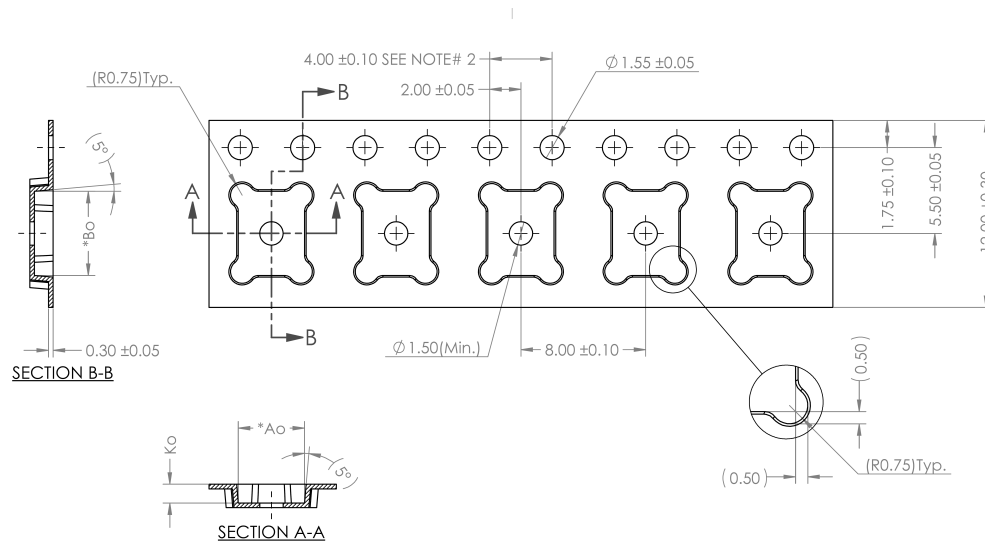
Parameter	Value
Typical thermal resistance: junction to ambient	25 °C/W
Typical thermal resistance: junction to case	4 °C/W
Typical thermal resistance: junction to board	2 °C/W

The  $\theta_{JA}$  numbers are guidelines for the thermal performance of the device/pc-board system. All specifications assume no ambient airflow.

## 6.3 Tape and Reel—Packaging Information

The following section provides the tape and reel packaging information. The following illustration represents tape specification.

**Figure 10 • Tape Specification**



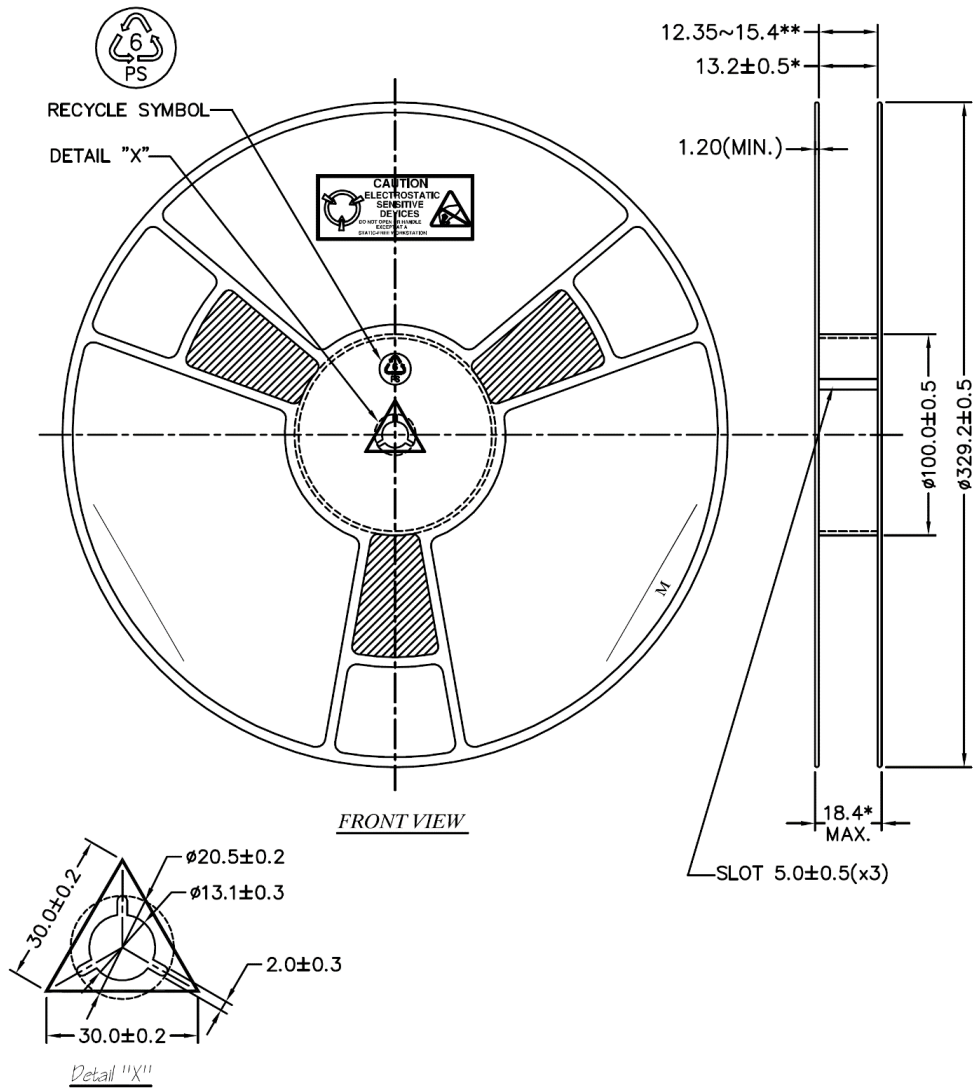
The following table lists the tape mechanical data.

**Table 19 • Tape Mechanical Data**

Dimension	Millimeters
A0	4.25 ±0.10
B0	5.40 ±0.10
K0	1.20 ±0.10
K1	-
Pitch	8.00 ±0.10
Width	12.00 ±0.30

The following illustration represents reel specification.

**Figure 11 • Reel Specification**





## 7 Ordering Information

The following table lists the ordering information for the PD69101 device.

**Table 20 • Ordering Information**

Part Number	Package	Packaging Type	Temperature	Part Marking
PD69101ILQ-TR	Plastic 24-pin QFN: 4 mm × 5 mm	Tape and reel	– 40 °C to 85 °C	MSC 69101 FR e3 <sup>1</sup> YYWWTZZ <sup>2</sup>

1. FR e3: F = FAB Code, R = Product revision code, and e3 = 2nd level interconnect.
2. YY = Year, WW = Week, A = Assembly location, and ZZ = Assembly lot sequence code.

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