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NEW INFORMATION

NEC

MOS INTEGRATED CIRCUIT

μPD78F9189/9188CT

8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD78F9189 is NEW Subseries (small, general-purpose) in the 78K/0S Series.

The μPD78F9189 replaces the internal ROM of the μPD789188 with flash memory.

Because flash memory allows the program to be written and erased electrically with the device mounted on the board, this product is ideal for the evolution stages of system development, small-scale production and rapid development of new products.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD789167, 789177, 789167Y, 789177Y Subseries User's Manual: U14186E
78K/0S Series User's Manual Instruction: U11047E

FEATURES

- Pin compatible with mask ROM version (except V_{PP} pin)
- Flash memory: 24 Kbytes ,Masked Version:16 Kbytes
- High-speed RAM: 512 bytes
- High-speed (0.4 μs: @5.0-MHz operation with main system clock)
- 8-bit resolution A/D converter: 4 channels
- I/O ports: 22
- Serial interface: 1 channel
  - 3-wire serial I/O mode / UART mode: 1 channel
- Timers: 6 channels
  - 16-bit timer: 1 channel
  - 8-bit timer/event counter: 2 channels
  - 8-bit timer: 1 channel
  - Watch timer: 1 channel
  - Watchdog timer: 1 channel
- On-chip 16-bit multiplier
- Power supply voltage: V_{DD} = 4.5 to 5.5 V

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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APPLICATIONS

Air-conditioner, White goods, etc

ORDERING INFORMATION

μPD78F9189CT/789188CT

Part Number	Package
μPD78F9189CT	32-pin plastic SDIP(400 mil)
μPD789188CT-xxx	32-pin plastic SDIP(400 mil)

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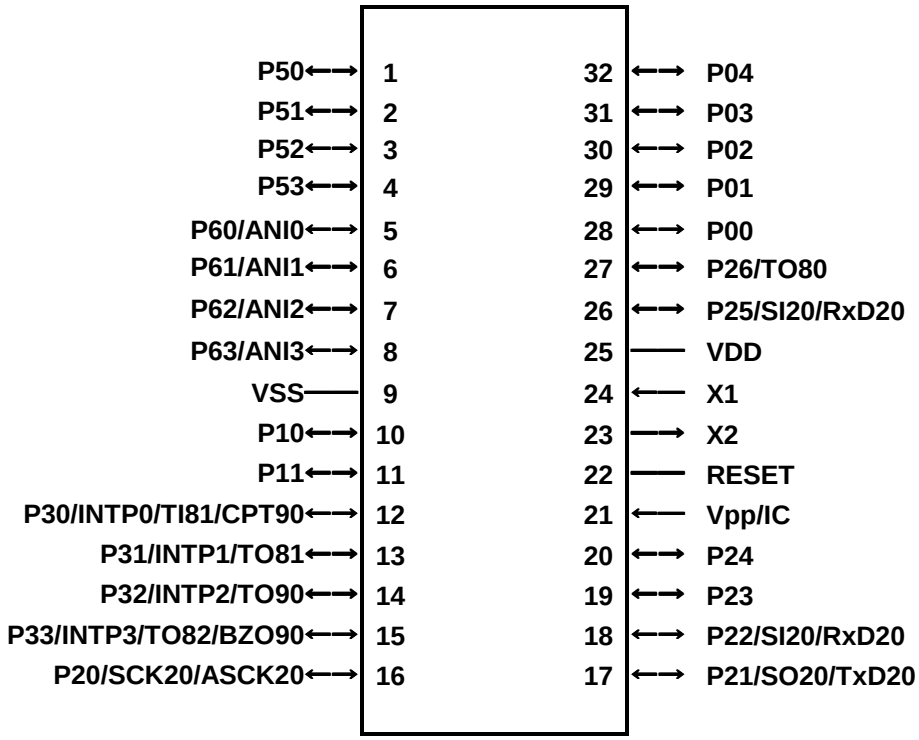
OVERVIEW OF FUNCTIONS

Item		μPD78F9189CT	μPD789188CT-xxx
Internal memory	Flash memory	24 Kbytes	16 Kbytes
	High-speed RAM	512 bytes	
Minimum instruction execution time		• 0.4/1.6 μs (@5.0-MHz operation with main system clock)	
General-purpose registers		8 bits × 8 registers	
Instruction set		• 16-bit operations • Bit manipulations (set, reset, test)	
Multiplier		8 bits × 8 bits = 16 bits	
I/O ports		Total: 26 • CMOS I/O: 17 • CMOS Input: 4(Shared with A/D converter) • N-ch open drain: 5	
A/D converters		8-bit resolution × 4 channels	
Serial interfaces		3-wire serial I/O/UART : 1 channel	
Timers		• 16-bit timer:1 channel • 8-bit timer/event counter:2 channels • 8-bit timer:1 channel • Watch timer:1 channel • Watchdog timer:1 channel	
Timer output		4 output	
Buzzer output		1	
Vectored interrupt sources	Maskable	Internal: 10, External: 4	
	Non-maskable	Internal: 1	
Power supply voltage		V_{DD} = 4.5 to 5.5 V	
Operating ambient temperature		T_A = –40°C to +85°C	
Package		32-pin plastic SDIP (400 mil)	

D a t a S h e

1. PIN CONFIGURATION (TOP VIEW)

- **32-pin plastic shrink DIP (400mil)**
  μPD78F9189CT
  μPD789188CT-xxx



Note: The information of pin assign is subject to change without notice.

Cautions 1. Connect the V_{PP}/IC pin directly to V_{SS}.

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3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P04	I/O	Port 0 5-bit input/output port Input/output mode can be specified in 1-bit units When used as an input port, an on-chip pull-up resistor can be specified by software.	Input	–
P10, P11	I/O	Port 1 2-bit input/output port Input/output mode can be specified in 1-bit units When used as an input port, an on-chip pull-up resistor can be specified by software.	Input	–
P20	I/O	Port 2 7-bit input/output port Input/output mode can be specified in 1-bit units For P20 to P22, P25, and P26, an on-chip pull-up resistor can be specified by software. Only P23 and P24 can be used as N-ch open-drain input/output port pins.	Input	$\overline{\text{SCK20}}$/ASCK20
P21				SO20/TxD20
P22				SI20/RxD20
P23				
P24				
P25				SI20/$\overline{\text{RxD20}}$
P26				TO80
P30	I/O	Port 3 4-bit input/output port Input/output mode can be specified in 1-bit units On-chip pull-up resistor can be specified by software.	Input	INTP0/TI81/CPT90
P31				INTP1/TO81
P32				INTP2/TO90
P33				INTP3/TO82/BZO90
P50 to P53	I/O	Port 5 4-bit N-ch open-drain input/output port Input/output mode can be specified in 1-bit units	Input	–
P60 to P63	Input	Port 6 4-bit input port	Input	ANI0 to ANI3

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3.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P30/TI81/CPT90
INTP1				P31/TO81
INTP2				P32/TO90
INTP3				P33/TO82/BZO90
SI20	Input	Serial data input to serial interface	Input	P22/RxD20
$\overline{SO20}$	Output	Serial data output from serial interface	Input	P21/TxD20
$\overline{SCK20}$	I/O	Serial clock input/output for serial interface	Input	P20/ASCK20
SS20	Input	Chip select input to serial interface	Input	P25/TI80
ASCK20	Input	Serial clock input for asynchronous serial interface	Input	P20/$\overline{SCK20}$
RxD20	Input	Serial data input for asynchronous serial interface	Input	P22/SI20
TxD20	Output	Serial data output for asynchronous serial interface	Input	P21/SO20
TI80	Input	External count clock input to 8-bit timer/event counter (TM80)	Input	P25/$\overline{SS20}$
TI81	Input	External count clock input to 8-bit timer/event counter (TM81)	Input	P30/INTP0/CPT90
TO80	Output	8-bit timer/event counter (TM80) output	Input	P26
TO81	Output	8-bit timer/event counter (TM81) output	Input	P31/INTP1
TO82	Output	8-bit timer (TM82) output	Input	P33/INTP3/BZO90
TO90	Output	16-bit timer (TM90) output	Input	P32/INTP2
BZO90	Output	16-bit timer (TM90) Buzzer output	Input	P33/INTP3/TO82
CPT90	Input	Capture edge input	Input	P30/INTP0/TI81
ANI0 to ANI3	Input	A/D converter analog input	Input	P60 to P63
X1	Input	Connecting crystal resonator for main system clock oscillation	–	–
X2	–		–	–
V_{DD}	–	Positive power supply	–	–
V_{SS}	–	Ground potential	–	–
$\overline{RESET}$	Input	System reset input	Input	–
V_{PP}	–	Sets flash memory programming mode. Applies high voltage when a program is written or verified. Connect directly to V_{SS} in normal operation mode.(μ PD78F9189CT)	–	–
IC	–	Sets test mode. Applies Vdd voltage when test mode. Connect directly to V_{SS} in normal operation mode. (μ PD789188CT)	–	–

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Ordering information
- Product release schedule
- Availability of related technical literature
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