PD81101

RPF PSE Manager

Introduction

Microchip's PD81101 Reverse Power Feeding (RPF) manager is a mixed-signal, high-voltage IC, which integrates power, analog, and logic into a single 56-pin, plastic QFN package. It allows Customer Premises Equipment (CPE) devices and Distribution Point Units (DPU) to share and deliver power and data over the same cable.

Microchip's PD81000 RPF controller is a cost-effective, re-programmed Micro-Controller Unit (MCU) designed to support monitor and control of RPF features, implemention of RPF macros required to perform line analysis, safe power feeding, and disconnection of ports in case of error, all with minimum external components.

The PD81101 and PD81000 chipset is designed to comply with ETSI's TS 101 548 Metallic Detection Startup (MDSU) protocol and supports detection and classification prior to power-up, provides continuous protection from Error Line Conditions (ELC) prior to power-up and afterwards, in accordance with the standard.

The RPF chipset provides real-time protection against overload, under-load, over-voltage, short-circuit, foreign DC voltage, and off-hook phone. This chipset allows the CPE host to receive telemetry data through I^2C communication of RPF line status. The same communication can be used for software download and field upgrades.

The PD81101 device operates from a wide supply voltage range (32 V–60 V), with no need for additional power supply sources. This is a low-power dissipation device that uses internal MOSFET and sense resistor, and is available in a 56-pin, 8 mm × 8 mm QFN package.

The PD81000 device is available in a 32-pin, 5 mm × 5 mm QFN package.

The firmware supports detection and classification, RPF power-up requirements, monitor and control of RPF features, and implementation of RPF macros required to perform line analysis, safe power feeding, and disconnection of ports in case of an error.

Features and Benefits

This section lists the main features and benefits of the PD81101 and PD81000 chipset.

- DPU detection and classification in the presence of MELT signatures, according to ETSI TS 101 548.
- Foreign DC voltage detection
- Off-Hook phone detection and line disconnection
- Support for error lineconditions
- I^2C communication with CPE host
- Supports signaling indication to DPU through RPF voltage modulation (DGL/ACM/BAT)
- PD81000—programmable I^2C address
- UDL/OVL indication andline-disconnection
- Single DC voltage input (32 V to 60 V)
- Input voltage out-of-range protection
- PD81101—over-temperature protection and thermal monitoring
- Low-Power dissipation (0.1 Ω sense resistor and 0.2 Ω MOSFET $R_{DS(on)}$)
- 4x direct address configuration pins
- Continuous port monitoring and system data
- Configurable load current setting
- Power soft start mechanism
- Internal power on reset
- LED indication
- On-Board software download
- Internal flash
- Interrupt output pin for system and port events
- Wide ambient temperature range: –40 °C to 85 °C
- RoHS compliant

Typical Applications

The following figure shows a typical application of the PD81101 and PD81000 chipset.

Figure 1. Typical Application

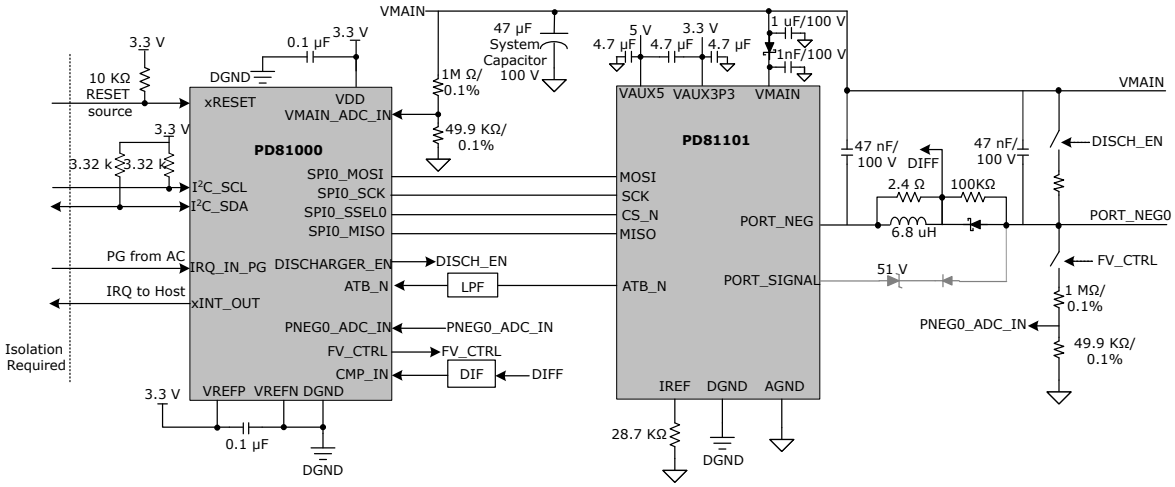

Table of Contents

1. Electrical Specifications

This section describes the electrical specifications and stress ratings for the PD81101 device.

1.1 PD81101 Electrical Characteristics

Unless otherwise specified, the minimum and maximum values in the following tables apply over the entire specified operating ratings of the device. Typical (Typ) values stated are either by design or by production testing at 25 °C ambient.

The following table lists the electrical characteristics for the PD81101 device.

Table 1-1. PD81101 Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Main supply voltage (V_{MAIN})	—	32		60	V
V_{PORT}	V_{MAIN}–V_{PORT_NEGx}	0		60	V
I_{MAIN}	Main power supply current at operating mode. V_{MAIN} = 55 V	—	14		mA
5 V output voltage (V_{AUX5})	V_{AUX5}–AGND	4.5	5	5.5	V
3.3 V output voltage (V_{AUX3P3})	V_{AUX3P3}–AGND	3	3.3	3.6	V
3.3 V output current (I_{AUX3P3})	Without external NPN	—	—	5	mA
	With external NPN transistor on V_{AUX5}	—	—	30	mA
3.3 V input voltage (V_{AUX3P3_INT})	V_{AUX3P3}–AGND	3	3.3	3.6	V
Digital 3.3 V input voltage (DV_{DD})	DV_{DD}–DGND	3	3.3	3.6	V
Power on reset DV_{DD} trip point (POR_{TP})	DV_{DD}–DGND	2.575	2.775	2.975	V
Power on reset DV_{DD} hysteresis (POR_{HYS})	POR_{TP}–DGND	0.2	0.25	0.3	V
Total channel resistance (R_{CH_ON}) between PORT_NEG0 (pins 3 and 4) and AGND (pin 21)	R_{ds_on} + R_{sense} + $R_{bonding}$	—	0.34	—	Ω
Clock frequency (F_{CLK})	Internal clock oscillator frequency	—	8	—	MHz
IREF output voltage	Loaded with a 28.7 KΩ resistor	1.176	1.2	1.224	V

Note: IREF is an output pin. Do not apply voltage or current.

1.2 Detection

The following table lists the detection thresholds for the PD81101 device.

Table 1-2. Detection

Parameter	Conditions	Min	Typ	Max	Units
Pre-Detection voltage, open circuit voltage (V_{OC})	V_{MAIN}–V_{PORT_NEGx}, open port.	—	—	20.5	V
Detection voltage (V_{VALID})	V_{MAIN}–V_{PORT_NEGx}, (R_{SIG} < 33 K)	—	—	9.3	V
Short circuit current (I_{SC})	V_{MAIN}–V_{PORT_NEGx}= 0 V	—	388	408	µA

1.3 Classification

The following table lists the classification signal conditions for the PD81101 device.

Table 1-3. Classification

Parameters	Conditions	Min	Typ	Max	Units
Class event output voltage (V_{CLASS})	V_{MAIN}–V_{PORT_NEGx}; 0 mA ≤ I_{PORT} ≤ 50 mA	15.5	18	20.5	V
Class event current limitation (I_{CLASS_LIM})	V_{MAIN}–V_{PORT_NEGx} = 0 V	51	70	100	mA

1.4 Real-Time Port Protection

The following table lists the real-time port protection of the PD81101 device.

Note: Class SR4 is not defined in RPF standard ETSI TS 101 548 version 2.0.1. The PD81101 device is designed to support class 4 levels for future use.

1.4.1 Port Current Monitoring

Table 1-4. Real-Time Port Protection

Parameter	Conditions	Min	Typ	Max	Units
Turn on rise time (T_{RISE})	From 10 % to 90 % of the voltage difference at the V_{PORT_NEGx} in POWER_ON state from the beginning of POWER_UP	15	—	—	µs
Output currentin POWER_UP state (I_{INRUSH})	C_{LOAD} ≤ 180 µF	—	425	450	mA
In-Rush time limit (T_{INRUSH})	—	50	65		ms
Overload time limit (T_{CUT})	—	50	64	75	ms
Port current limit (I_{LIM})	SR1, SR2, SR3, and SR4	702	720	792	mA
Port current limittime (T_{LIM})	V_{MAIN}–V_{PORT_NEGx} < 30 V	1	2	3	ms
DC disconnect under-load current (I_{UDL})	—	2.5	3.75	5	mA
Turn off time (T_{OFF})	From V_{MAIN} to 2.8 V	—	—	500	ms

The following table lists the port current monitoring of the PD81101 device.

Table 1-5. Port Current Monitoring

Parameter	Min	Typ	Max	Units	Conditions
Resolution	—	10	—	Bits	Reported as 14 bits
LSB	—	122.07	—	µA	—
Measurement period	—	16	—	ms	—
Accuracy	—	—	±4	%	< 250 mA
			±3	%	≥ 250 mA

1.4.2 Port Voltage Monitoring

The following table lists the port voltage monitoring of the PD81101 device.

Table 1-6. PD81101 Port Voltage Monitoring

Parameter	Typ	Max	Units
Resolution	12	—	Bits
LSB	16.7	—	mV
Measurement period	5	—	ms
Accuracy	—	3.2	%

1.4.3 Main Voltage Monitoring

The following table lists the main voltage monitoring of the PD81101 device.

Table 1-7. PD81101 Main Voltage Monitoring

Parameter	Typ	max	Units
Resolution	12	—	Bits
LSB	16.7	—	mV
Measurement period	5	—	ms
Accuracy	—	3.2	%

1.4.4 Temperature Monitoring

The following table lists the temperature monitoring of the device.

Table 1-8. Temperature Monitoring

Parameter	Min	Typ	Max	Units	Conditions
Resolution	—	8	—	Bits	—
LSB	—	1.9384	—	°C	Temperature = (DATA x 1.92)–277
Measurement period	—	3	—	mS	—
Accuracy	–3	—	3	°C	—

1.5 DC Characteristics

The following table lists the DC characteristics of the PD81101 device.

Table 1-9. DC Characteristics

Paramter	Condition	Min	Typ	Max	Units
Input logic high voltage (V_{IH})	RESET_N, MOSI, MISO,SCK, CS_N, ADDR[0..3]	2.2	—	—	V
Input logic low voltage (V_{IL})	RESET_N, MOSI, MISO,SCK, CS_N, ADDR[0..3]	—	—	0.8	V
Input logic hysteresis voltage (Hyst)	RESET_N, MOSI, MISO,SCK, CS_N, ADDR[0..3]	0.4	0.6	0.8	V
Input logic high current (I_{IH})	RESET_N, MOSI, MISO,SCK, CS_N, ADDR[0..3]	–10	—	10	V
Input logic low current (I_{IL})	RESET_N, MOSI, MISO,SCK, CS_N, ADDR[0..3]	–10	—	10	µA
Output logic high voltage (V_{OH})	RESET_N, MOSI, MISO,SCK, CS_N, ADDR[0..3] (I_{OH} = –1 mA)	2.4	—	—	V
Output logic low voltage (V_{OL})	RESET_N, MOSI, MISO,SCK, CS_N, ADDR[0..3] (I_{OH} = –1 mA)	—	—	0.4	V
LED output low voltage (LED1_OD,LED2_OD LED3_OD)	Sink current from V_{MAIN} I_{SINK} = 5 mA	—	—	1	V

1.6 PD81101 Absolute Maximum Ratings

RPF performance is not guaranteed when it exceeds the recommended rating. Exposure to any stress in the range between the recommended rating, as listed in the PD81101 Electrical Characteristics table, and the absolute maximum rating must be limited to a short time period.

Stresses beyond the absolute maximum ratings in the following table may cause permanent damage to the device. Exposure to absolute-maximum-rated voltage for extended periods of time may affect device reliability.

The following table lists the absolute maximum ratings of the PD81101 device.

Table 1-10. PD81101 Absolute Maximum Rating

Parameter	Min	Max	Units
Supply input voltage (V_{MAIN})[1, 2]	–0.3	72	V
Port_Neg, Port_signal	–0.3	V_{MAIN} + 0.5	V
LED0_OD-LED3_OD	–0.3	72	V
V_{AUX5}	–0.3	6	V
DRV_V_{AUX5}[3]	–0.3	V_{MAIN}	V
V_{AUX3P3}, DV_{DD}	–0.3	4	V
Digital pins: MISO, MOSI, SCK, CS_N, ADDR[3:0], RESET_N, TRIM, and TST	–0.3	DV_{DD} + 0.3 and < 4.0	V
Junction temperature	—	150	°C
Lead soldering temperature (40 s, reflow)	—	260	°C

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Parameter	Min	Max	Units
Storage temperature	–65	150	°C
ESD rating ($_{HBM}$)	JESD22 Class 1C Compliant		

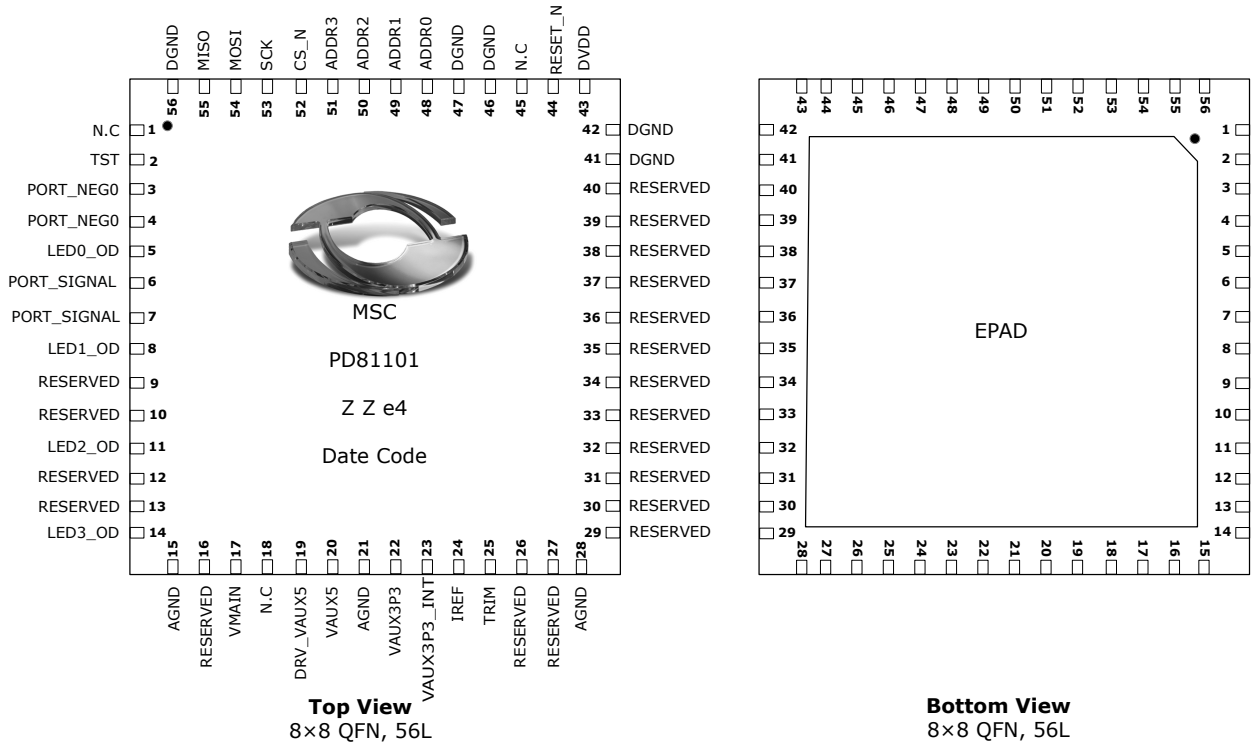
1. Power sequence requirement: $V_{MAIN} > V_{AUX5} > V_{AUX3P3}$ = TRIM, DV_{DD}.
2. PD81101 EPAD is connected by a copper plane on PCB to AGND. AGND is ground for IC.
3. $D_{RV}\_V_{AUX5}$ is an output pin. Do not apply voltage or current. It can be left open when not used.

2. Pins

The following sections describe the functional pin descriptions of the PD81101 device.

The following figure shows the pin diagram of the PD81101 device.

Figure 2-1. PD81101 Pin Diagram



2.1 Pin Descriptions

The following table lists the pin descriptions of the PD81101 device.

Table 2-1. PD81101 Pin Description

Number	Name	Type	Description
0	EPAD	Power	Exposed pad: connect to analog ground. Use an adequate ground plane to ensure the required thermal performance.
1	N.C	N/A	Not connected, do not connect externally (leave floating).
2	TST	Digital input	Test pin for production use only. Keep connected to DGND.
3	PORT_NEG0	Analog I/O	Negative port 0 output.
4	PORT_NEG0	Analog I/O	Negative port 0 output.
5	LED0_OD	Analog I/O	Open drain output for LED indication. LED-ON: PSE port is on (PSE delivers power) LED-Blink: Overload current
6	PORT_SIGNAL	Analog I/O	Signaling port: If function is used, connect according to the Typical Application figure. If unused, leave floating.

.....continued

Number	Name	Type	Description
7	PORT_SIGNAL	Analog I/O	Signaling port: If function is used, connect according to the Typical Application figure. If unused, leave floating.
8	LED1_OD	Analog I/O	Open drain output for LED indication. LED-ON: Open tip-to-ring LED-Blink: POTS exchange (foreign) DC voltage
9	RESERVED	Analog I/O	Reserved pin. Do not connect externally.
10	RESERVED	Analog I/O	Reserved pin. Do not connect externally.
11	LED2_OD	Analog I/O	Open-drain output for LED indication. LED-ON: Off-Hook phone LED-Blink: Short circuit
12	RESERVED	Analog I/O	Reserved pin. Do not connect externally.
13	RESERVED	Analog I/O	Reserved pin. Do not connect externally.
14	LED3_OD	Analog I/O	Open-drain output for LED indication. LED-ON: Wrong class detected. LED-Blink: Wrong resistor signature detected
15	AGND	Power	Analog ground.
16	RESERVED	N/A	Reserved pin. Do not connect externally.
17	V_{MAIN}	Power	Main high voltage supply.
18	N.C	N/A	Not connected. Do not connect externally.
19	D_{RV_VAUX5}	Power	Driven output for 5 V external regulation. If internal regulation is used, connect to pin 20. If an external NPN is used to regulate the voltage, connect this pin to “Base” and use 4.7 mF capacitor to AGND. Leave unconnected (floating) if external 5 V regulator is used.
20	V_{AUX5}	Power	Regulated 5 V output source. A 4.7 mF or higher filtering capacitor must be connected between this pin and AGND. If an external NPN is used to regulate the voltage, connect this pin to the emitter (the collector must be connected to V_{MAIN}).
21	AGND	Power	Analog ground.
22	V_{AUX3P3}	Power	Regulated 3.3 V output source. A 4.7 mF or higher filtering capacitor must be connected between this pin and AGND and this pin and V_{AUX5}. When an external 3.3 V regulator is used, connect it to this pin to supply the chip.
23	V_{AUX3P3_INT}	Power	Connected to V_{AUX3P3} (pin 22) if internal 3.3 V regulator is used (recommended). Leave unconnected (floating) if external 3.3 V regulator is used.
24	IREF	Analog output	Reference resistor pin. Connect a 28.7 KΩ 0.1 % resistor to AGND. Do not apply voltage or current.
25	TRIM	Test input	Test input pin. Keep connected to V_{AUX3P3}.
26	RESERVED	N/A	Reserved pin. Do not connect externally.
27	ATB_N	Analog output	ATB_N

.....continued

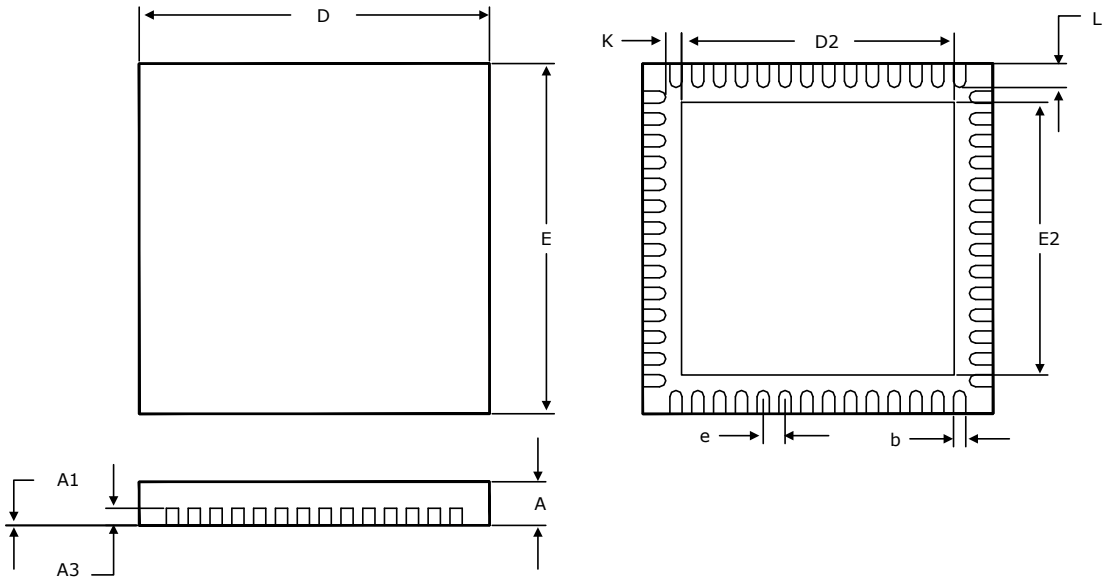
Number	Name	Type	Description
28	AGND	Power	Analog ground.
29	RESERVED	N/A	Reserved pin. Do not connect externally.
30	RESERVED	N/A	Reserved pin. Do not connect externally.
31	RESERVED	N/A	Reserved pin. Do not connect externally.
32	RESERVED	N/A	Reserved pin. Do not connect externally.
33	RESERVED	N/A	Reserved pin. Do not connect externally.
34	RESERVED	N/A	Reserved pin. Do not connect externally.
35	RESERVED	N/A	Reserved pin. Do not connect externally.
36	RESERVED	N/A	Reserved pin. Do not connect externally.
37	RESERVED	N/A	Reserved pin. Do not connect externally.
38	RESERVED	N/A	Reserved pin. Do not connect externally.
39	RESERVED	N/A	Reserved pin. Do not connect externally.
40	RESERVED	N/A	Reserved pin. Do not connect externally.
41	DGND	Power	Digital ground.
42	DGND	Power	Digital ground.
43	DV_{DD}	Power in	Regulated 3.3 V for digital circuitry. Connect voltage from pin V_{AUX3P3}, or from external voltage from pin V_{AUX3P3}, or from external power supply source, if used. A 1 mF or higher filtering capacitor must be power supply source if used. A 1 mF or higher filtering capacitor must be connected between this pin and DGND.
44	RESET_N	Digital input	Reset input-active low. An external 10 K pull-up resistor must be connected between this pin and DV_{DD}. Connect 1 nF capacitor between this pin and DGND.
45	N.C	N/A	Not connected. Do not connect externally.
46	DGND	Power	Digital ground
47	DGND	Power	Digital ground.
48	ADDR0	Digital input	SPI address bit 0 to set chip address. Connect to DGND.
49	ADDR1	Digital input	SPI address bit 1 to set chip address. Connect to DGND.
50	ADDR2	Digital input	SPI address bit 2 to set chip address. Connect to DGND.
51	ADDR3	Digital input	SPI address bit 3 to set chip address. Connect to DGND.
52	CS_N	Digital input	SPI bus, chip select.
53	SCK	Digital input	SPI bus, serial clock input.
54	MOSI	Digital input	SPI bus, master data out/slave in.
55	MISO	Digital output	SPI bus, master data in/slave out.
56	DGND	Power	Digital ground.

3. Package Information

The following sections provide the packaging information of the PD81101 device.

The following figure shows the package outline drawing of the PD81101 device.

Figure 3-1. PD81101 Package Outline Drawing



The following table lists the package dimensions of the PD81101 device.

Table 3-1. PD81101 Package Dimensions

Dimension[1]	Millimeters		Inches[2]	
	Min	Max	Min	Max
A	0.08	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF	—	0.008 REF	—
K	0.20 MIN	—	0.008 MIN	—
e	0.50 BSC	—	0.02 BSC	—
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	6.50	6.75	0.256	0.267
E2	6.50	6.75	0.256	0.267
D	8.00 BSC		0.315 BSC	
E	8.00 BSC		0.315 BSC	

1. Dimensions do not include protrusions—they must not exceed 0.155 mm (0.006 in.) on any side. Lead dimension must not include solder coverage.
2. Dimensions are in millimeters—inches are only for reference.

3.1 Thermal Properties

The following table lists the thermal properties of the PD81101 device.

Table 3-2. PD81101 Thermal Properties

Thermal Resistance	Typical	Units	Notes
Θ_{JA}	19.0	°C/W	Junction-To-Ambient thermal resistance.
Ψ_{JT}	0.05	°C/W	Junction-To-Top thermal characterization parameter. A thermal metric derived from the difference in junction temperature (T_j) and package top temperature (T_t) divided by total heating power (P_h).
Θ_{JC}	4.9	°C/W	Junction-To-Case thermal resistance with heat flow through package top.
Θ_{JB}	2.2	°C/W	Junction-To-Board thermal resistance.

Note: All parameters are as per JEDEC JESD-51.

3.2 Recommended PCB Layout

The following figures show the recommended PCB layout pattern of the PD81101 device (units are in mm).

Figure 3-2. PD81101 Top Copper Layer

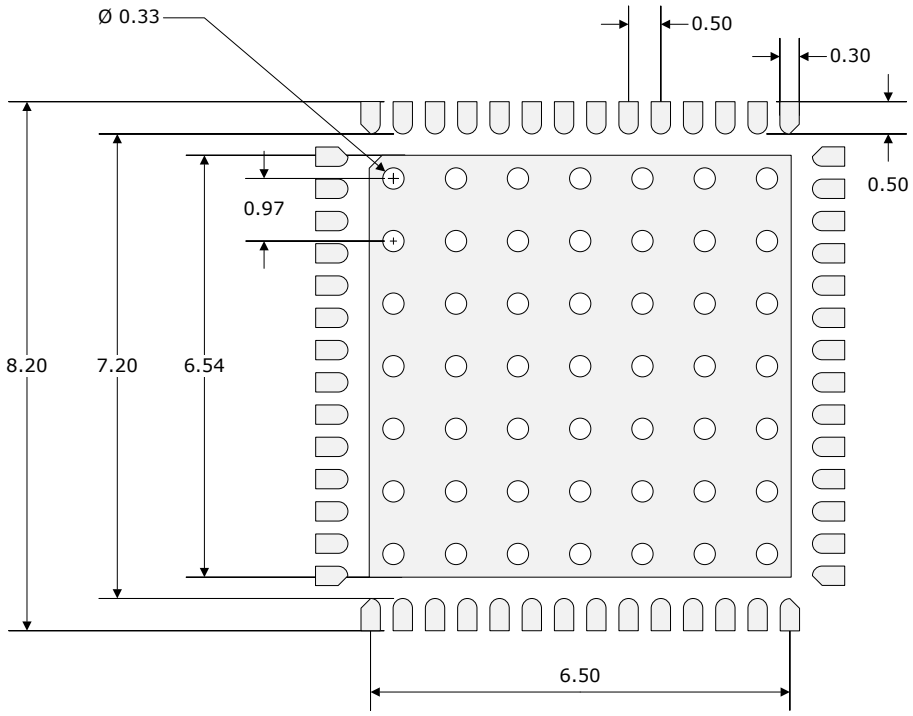


Figure 3-3. PD81101 Top Solder Paste Layer

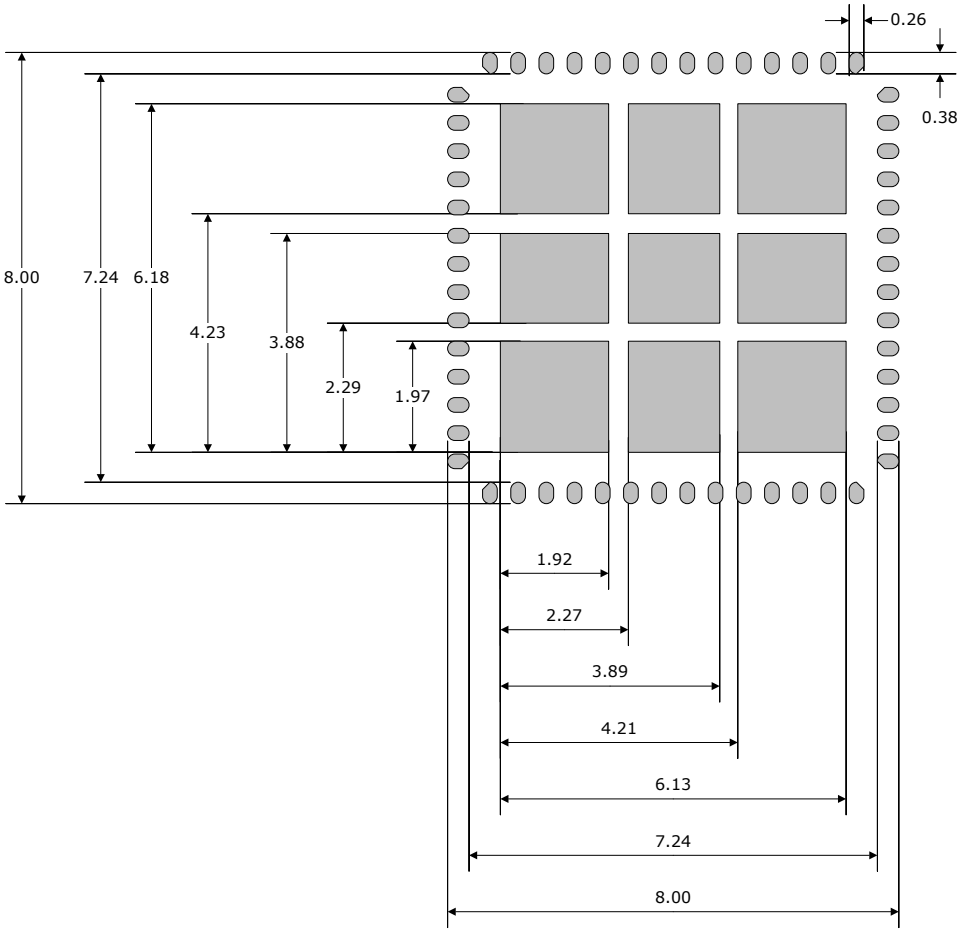


Figure 3-4. PD81101 Top Layer Solder Mask

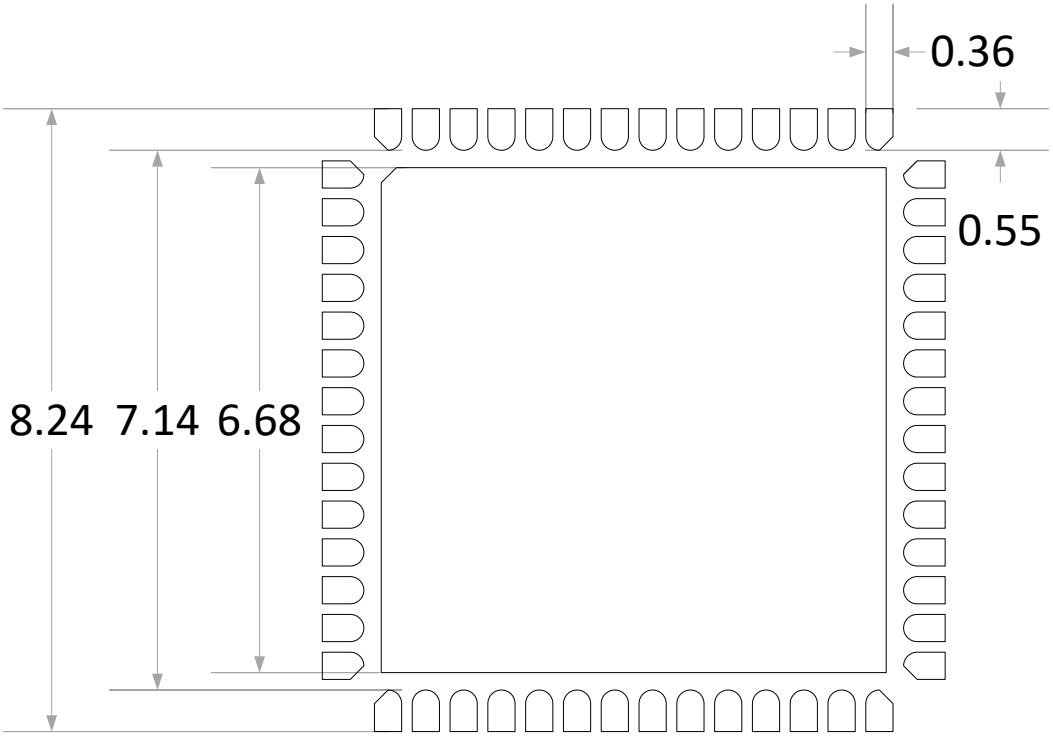


Figure 3-5. PD81101 Bottom and Internal Layer Copper Plane

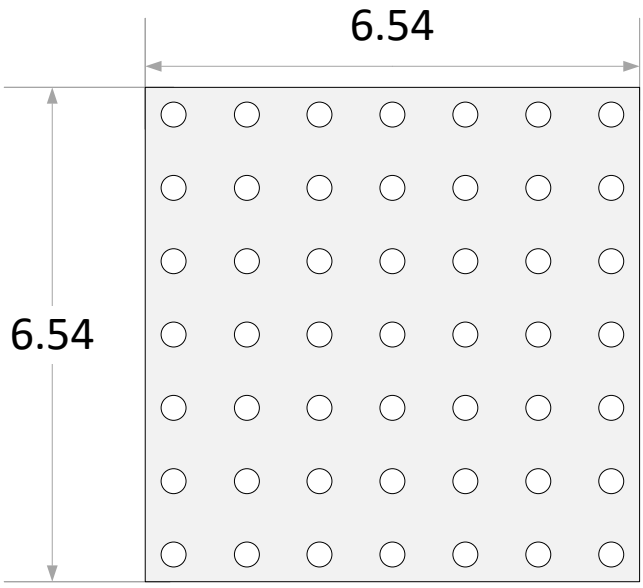
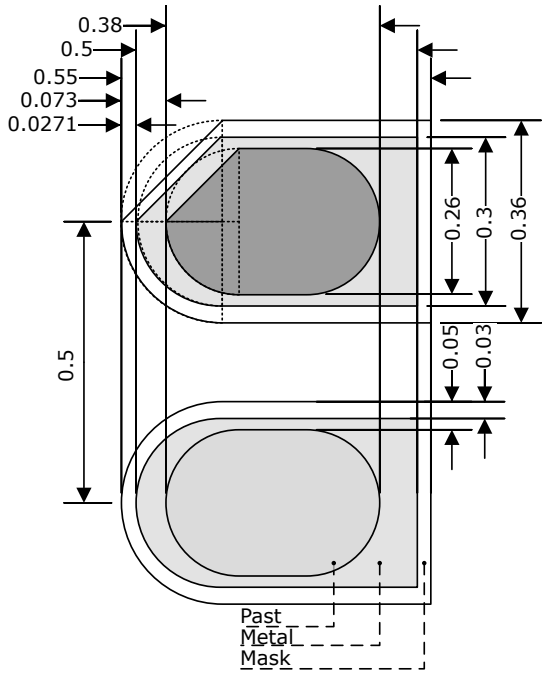


Figure 3-6. PD81101 Top Layer Pin Geometry

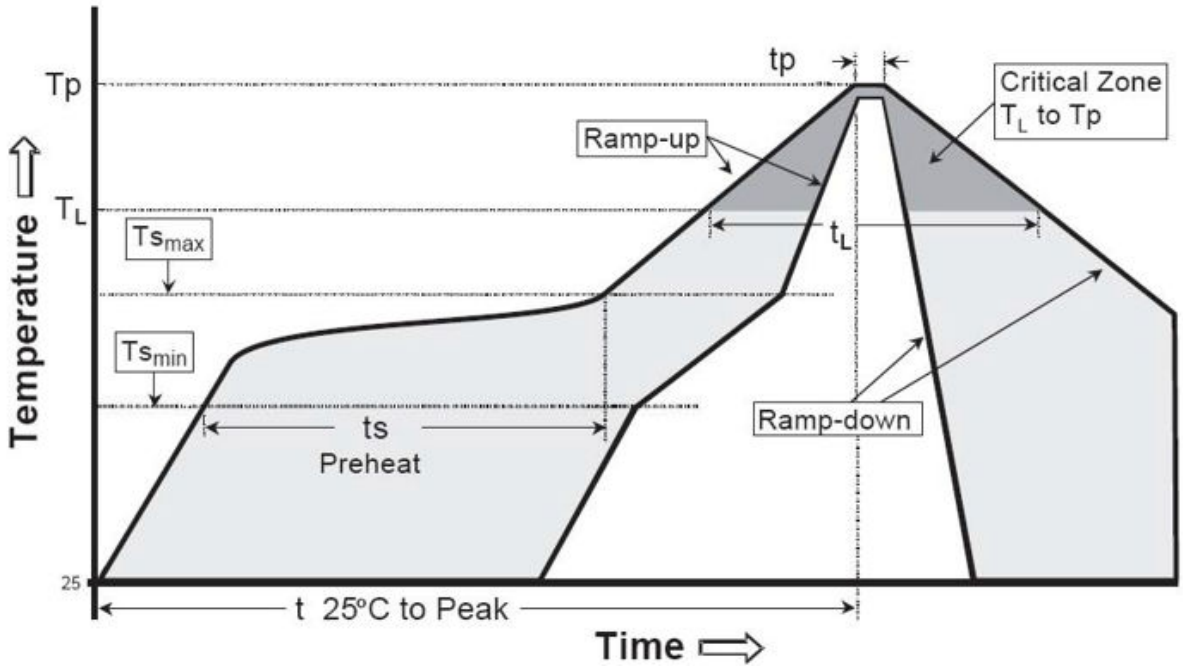


Note: The contract manufacturer has latitude to modify the solder paste stencil for manufacturability reasons. The solder paste stencil must cover 65 % to 80 % of the thermal pad, and must not allow solder to be applied to the thermal vias under the QFN package (using any method deemed appropriate). Any design must be subjected to system validation and qualification prior to committing to mass production or field deployment.
Use a 5 mil stencil.

3.3 Recommended Solder Reflow Information

The following figure shows the recommended solder reflow information of the PD81101 device.

Figure 3-7. Solder Reflow Information

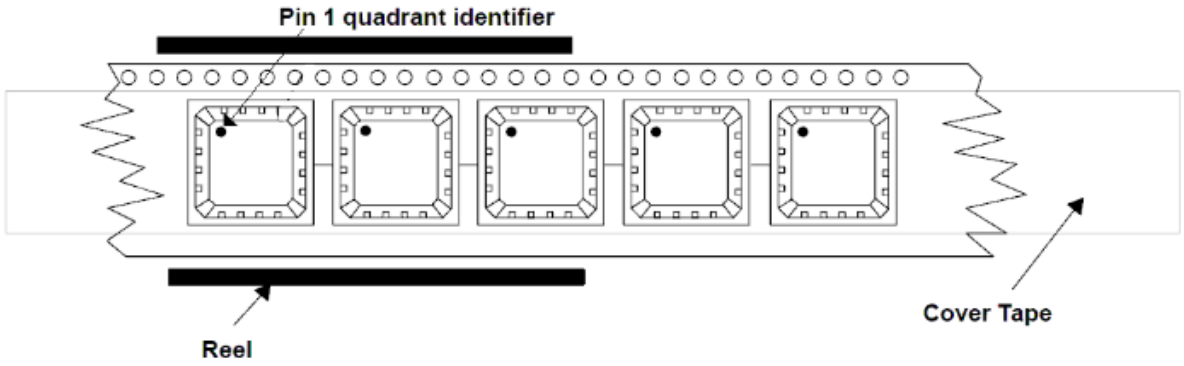


Note: Exceeding these ratings may cause damage to the device.
The finish is a lead-free, 100 % matte tin. The RoHS rating is 6/6. The package peak temperature for solder reflow is 260 °C (0 °C, –5 °C) with 40 seconds maximum exposure. Exceeding these ratings may cause damage to the device.

3.4 Tape-And-Reel Packaging Information

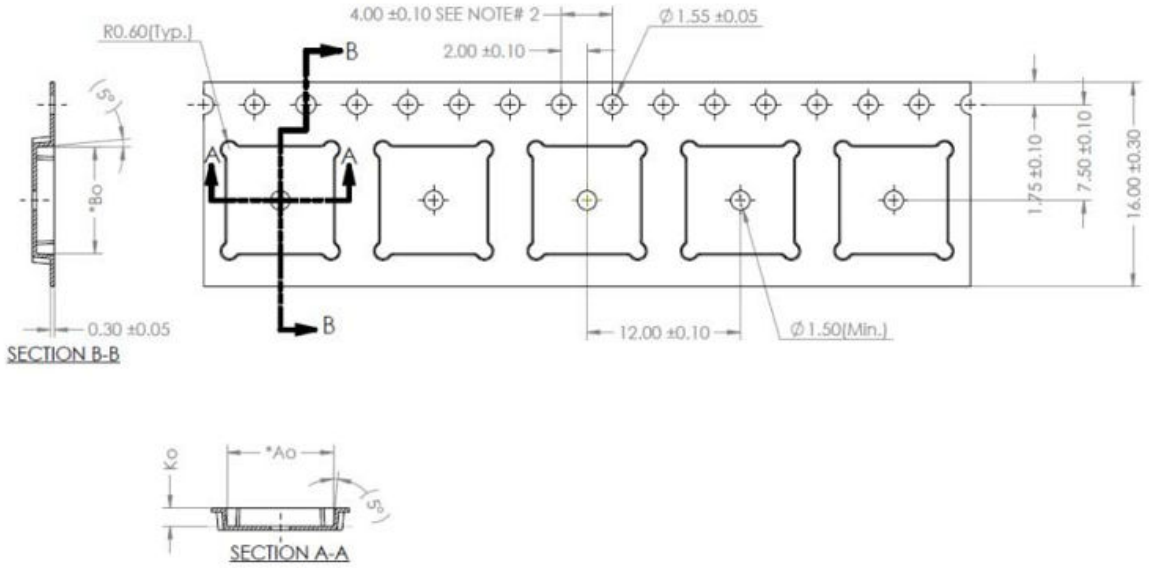
The following figure shows the tape-and-reel pin-1 orientation of QFN packages of the PD81101 device.

Figure 3-8. Tape-And-Reel Pin-1 Orientation



The following figure shows the tape specifications of the PD81101 device.

Figure 3-9. Tape Specifications



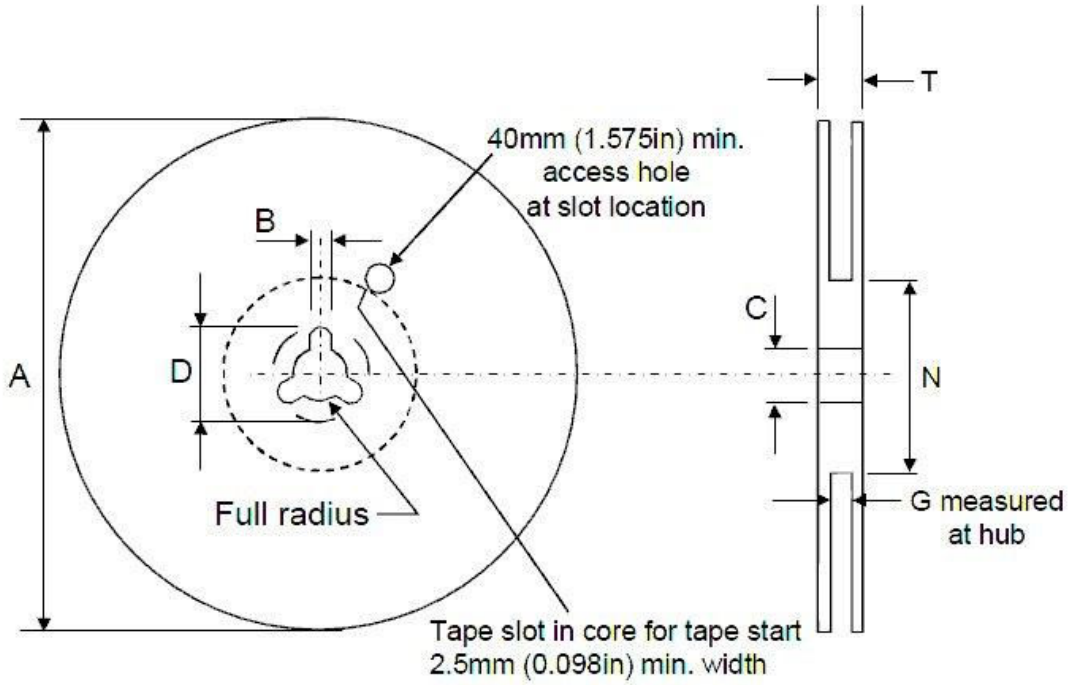
The following table lists the tape mechanical data.

Table 3-3. Tape Mechanical Data

Dimension	Value (mm)
A0	8.35 ±0.10
B0	8.35 ±0.10
K0	1.40 ±0.10
K1	N/A
Pitch	12.00 ±0.10
Width	16.00 ±0.30

The following figure shows the tape-and-reel shipment information and specifications of the PD81101 device.

Figure 3-10. Reel Specifications



The following table lists the reel mechanical data of the PD81101 device. The base quantity is 2000 pieces.

Table 3-4. Reel Mechanical Data

	Millimeters	Inches
Tape size	16.00 ±0.3	0.630 ±0.012
A maximum	330	13
B maximum	1.5	0.059
C	13.0 ±0.20	0.512 ±0.008
D minimum	20.2	0.795
N minimum	50	1.968
G	16.4 + 2.0/–0.0	0.645 + 0.079/–0.0
T maximum	29	1.142

4. Ordering Information

The following table lists the ordering information for the device.

Table 4-1. Ordering Information

Part Order	Number Description
PD81101ILQ-TR-LE	Lead-Free, MSL3, RoHS-compliant, 56-lead device with a plastic QFN8 mm × 8 mm body size, and tape and reel packaging. The operating temperature is –40 °C ambient to 85 °C junction. Microsemi Logo PD811010 Z Z e4[1] YYWWNNN[2]

1. Z = Hardcoded random character, Z = Hardcoded random character, and e4 = 2nd level interconnect.
2. YY = Year, WW = Week, NNN = Trace code.

5. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
3.0	May 2020	• Part order number changed from PD81101ILQ-TR to PD81101ILQ-TR-LE in the Ordering Information section. • Updated number description of part order number in the Ordering Information section. • Updated the PD81101 Pin Diagram figure in the Pins section. • Updated the Typical Application figure in the Typical Applications section. • Updated the datesheet as per Microchip standards.
2.1	February 2018	• Pins 41, 46, 47, and 56 were updated from N.C. to DGND. For more information, see the 2. Pins section.
2.0	February 2018	• PD81101, PD81000, and software information were separated into different documents. • The quiescent current specification was removed. • The V_{MAIN} supply voltage increased from 57 V to 60 V. For more information, see the PD81101 Electrical Characteristics table. • The port current monitoring accuracy specification was modified per PD81101 errata (document number 158599, November 2017). For more information, see the 1.4.1 Port Current Monitoring section. • The LED output low voltage was added. For more information, see the DC Characteristics table. • Storage temperature maximum changed from 130 °C to 150 °C. For more information, see the PD81101 Absolute Maximum Ratings table.

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