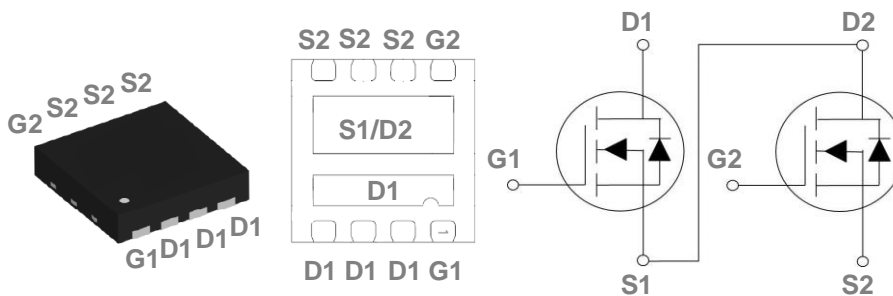


### General Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

	BVDSS	RDSON	ID
Q1	30V	10.5mΩ	19.5A
Q2	30V	10.5mΩ	19.5A

### DFN3x3 Asymmetric Dual Pin Configuration



### Features

- Improved dv/dt capability
- Fast switching
- 100% EAS Guaranteed
- Halogen free

### Applications

- MB / VGA / Vcore
- POL Buck Applications
- SMPS 2<sup>nd</sup> SR

### Absolute Maximum Ratings $T_c=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
$V_{DS}$	Drain-Source Voltage	30	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	$\pm 20$	V
$I_D$	Drain Current – Continuous ( $T_c=25^\circ\text{C}$ )	19.5	19.5	A
	Drain Current – Continuous ( $T_c=100^\circ\text{C}$ )	12.3	12.3	A
	Drain Current – Continuous ( $T_A=25^\circ\text{C}$ )	10.8	10.8	A
	Drain Current – Continuous ( $T_A=100^\circ\text{C}$ )	6.8	6.8	A
$I_{DM}$	Drain Current – Pulsed <sup>1</sup>	78	78	A
EAS	Single Pulse Avalanche Energy <sup>2</sup>	13	13	mJ
IAS	Single Pulse Avalanche Current <sup>2</sup>	16	16	A
$P_D$	Power Dissipation ( $T_c=25^\circ\text{C}$ )	27	27	W
	Power Dissipation – Derate above $25^\circ\text{C}$	0.01	0.01	W/ $^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150		$^\circ\text{C}$

### Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$ Q1	Thermal Resistance Junction to ambient	---	62	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$ Q2		---	62	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$ Q1	Thermal Resistance Junction to Case	---	4.6	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$ Q2		---	4.6	$^\circ\text{C}/\text{W}$

**Static State Characteristics**

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	Q1	30	---	---	V
			Q2	30	---	---	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25°C , I <sub>D</sub> =1mA	Q1	---	0.04	---	V/°C
			Q2	---	0.04	---	V/°C
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =30V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C	Q1	---	---	1	uA
			Q2	---	---	1	uA
		V <sub>DS</sub> =24V , V <sub>GS</sub> =0V , T <sub>J</sub> =125°C	Q1	---	---	10	uA
			Q2	---	---	10	uA
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±20V , V <sub>DS</sub> =0V	Q1	---	---	±100	nA
			Q2	---	---	±100	nA
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>3</sup>	V <sub>GS</sub> =10V , I <sub>D</sub> =10A	Q1	---	8.5	10.5	mΩ
		V <sub>GS</sub> =10V , I <sub>D</sub> =10A	Q2	---	8.5	10.5	mΩ
		V <sub>GS</sub> =4.5V , I <sub>D</sub> =5A	Q1	---	11	14	mΩ
		V <sub>GS</sub> =4.5V , I <sub>D</sub> =5A	Q2	---	11	14	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	Q1	1.2	1.6	2.5	V
			Q2	1.2	1.6	2.5	V
ΔV <sub>GS(th)</sub>	V <sub>GS(th)</sub> Temperature Coefficient	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	Q1	---	-4	---	mV/°C
			Q2	---	-4	---	mV/°C
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =5V , I <sub>D</sub> =5A	Q1	---	12	---	S
		V <sub>DS</sub> =5V , I <sub>D</sub> =5A	Q2	---	12	---	S

**Dynamic Characteristics**

Q <sub>g</sub>	Total Gate Charge <sup>3, 4</sup>		Q1	---	15.6	31	nC
			Q2	---	15.6	31	
Q <sub>gs</sub>	Gate-Source Charge <sup>3, 4</sup>	V <sub>DS</sub> =15V , V <sub>GS</sub> =10V , I <sub>D</sub> =5A	Q1	---	2.3	5	
			Q2	---	2.3	5	
Q <sub>gd</sub>	Gate-Drain Charge <sup>3, 4</sup>		Q1	---	3	6	
			Q2	---	3	6	
T <sub>d(on)</sub>	Turn-On Delay Time <sup>3, 4</sup>		Q1	---	3.8	7	ns
			Q2	---	3.8	7	
T <sub>r</sub>	Rise Time <sup>3, 4</sup>	V <sub>DD</sub> =15V , V <sub>GS</sub> =10V , R <sub>G</sub> =6Ω	Q1	---	10	19	
			Q2	---	10	19	
T <sub>d(off)</sub>	Turn-Off Delay Time <sup>3, 4</sup>	I <sub>D</sub> =1A	Q1	---	22	42	
			Q2	---	22	42	
T <sub>f</sub>	Fall Time <sup>3, 4</sup>		Q1	---	6.6	13	
			Q2	---	6.6	13	

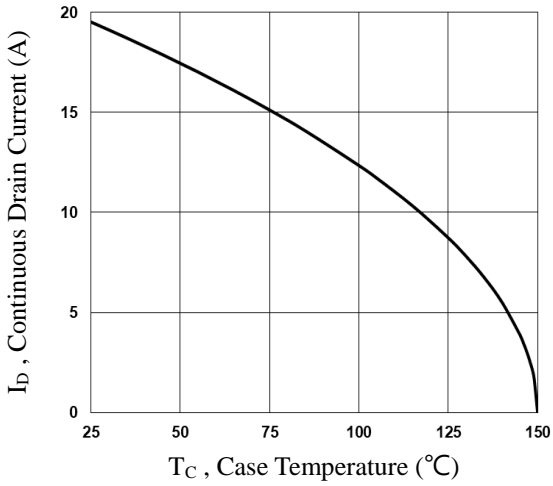
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =25V , V <sub>GS</sub> =0V , F=1MHz	Q1	---	620	900	pF		
			Q2	---	620	900			
C <sub>oss</sub>	Output Capacitance		Q1	---	85	125			
			Q2	---	85	125			
C <sub>rss</sub>	Reverse Transfer Capacitance		Q1	---	60	90			
			Q2	---	60	90			
R <sub>g</sub>	Gate resistance		V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, F=1MHz	Q1	---	2.8		5.6	Ω
				Q2	---	2.8		5.6	Ω

### Drain-Source Diode Characteristics

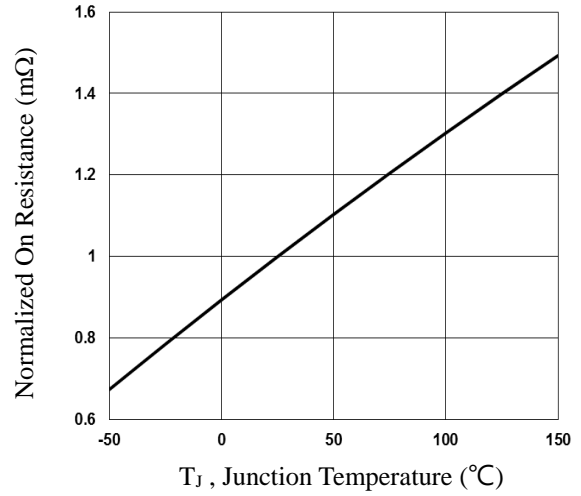
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit		
I <sub>S</sub>	Continuous Source Current	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current	Q1	---	---	19.5	A	
			Q2	---	---	19.5	A	
I <sub>SM</sub>	Pulsed Source Current <sup>3</sup>		Q1	---	---	39	A	
			Q2	---	---	39	A	
V <sub>SD</sub>	Diode Forward Voltage <sup>3</sup>		V <sub>GS</sub> =0V , I <sub>S</sub> =1A , T <sub>J</sub> =25°C	Q1	---	---	1	V
				Q2	---	---	1	V

Note :

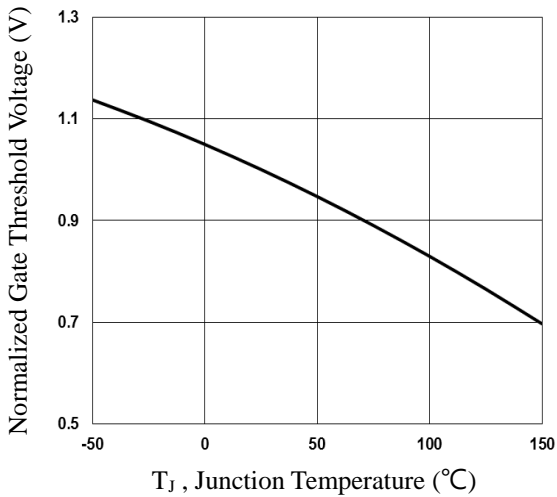
1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. V<sub>DD</sub>=25V, V<sub>GS</sub>=10V, L=0.1mH, Q1: I<sub>AS</sub>=16A, Q2: I<sub>AS</sub>=42A, R<sub>G</sub>=25Ω, Starting T<sub>J</sub>=25°C.
3. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
4. Essentially independent of operating temperature.



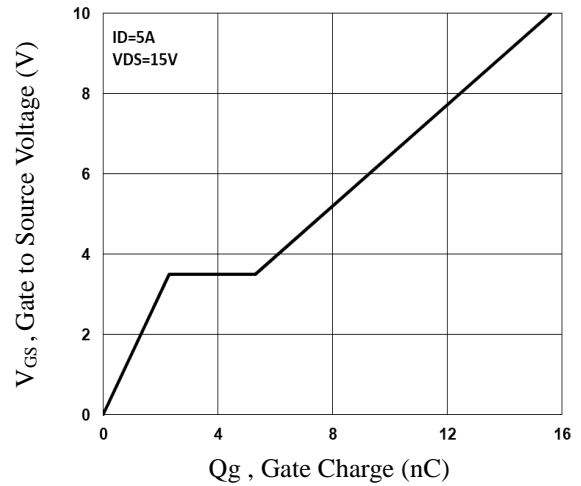
**Fig.1 Q1 Continuous Drain Current vs. T<sub>c</sub>**



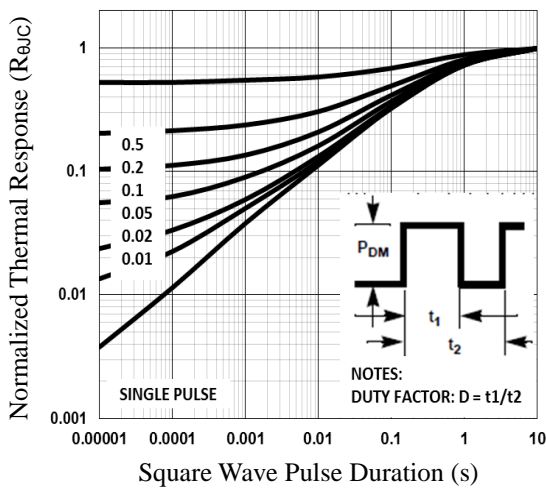
**Fig.2 Q1 Normalized R<sub>DS(on)</sub> vs. T<sub>j</sub>**



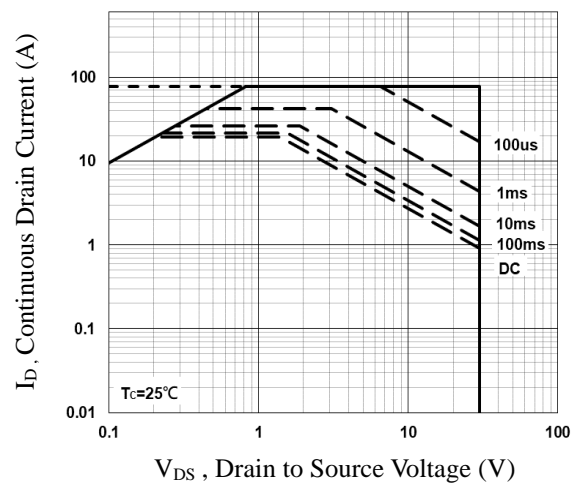
**Fig.3 Q1 Normalized V<sub>th</sub> vs. T<sub>j</sub>**



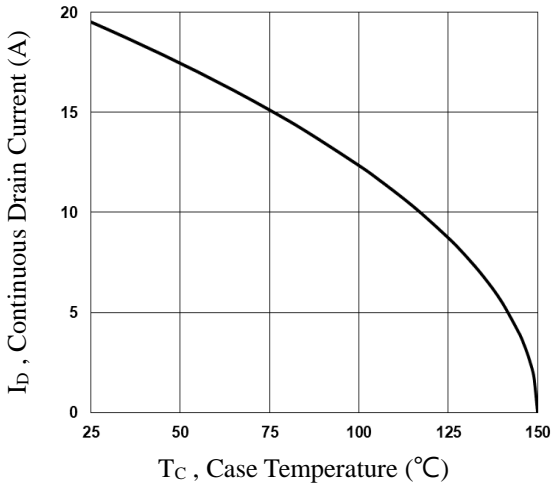
**Fig.4 Q1 Gate Charge Waveform**



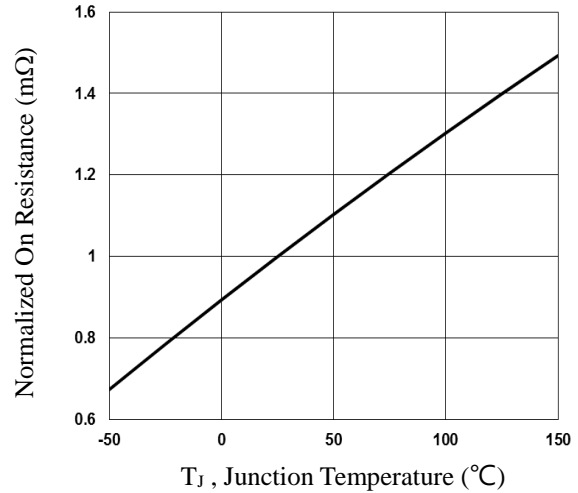
**Fig.5 Q1 Normalized Transient Impedance**



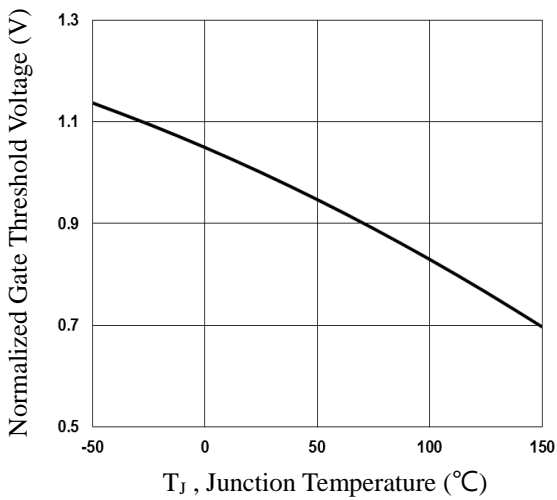
**Fig.6 Q1 Maximum Safe Operation Area**



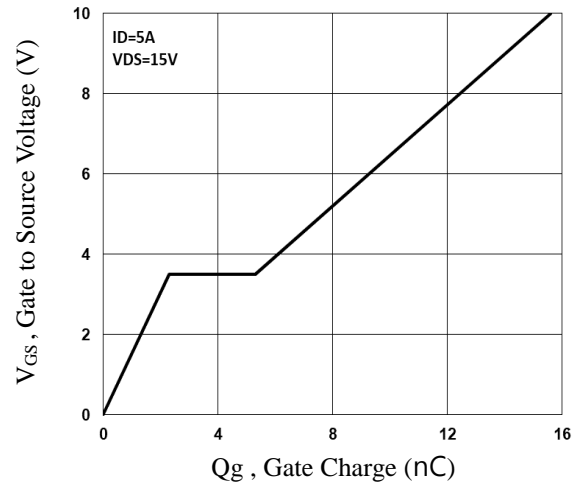
**Fig.7 Q2 Continuous Drain Current vs.  $T_c$**



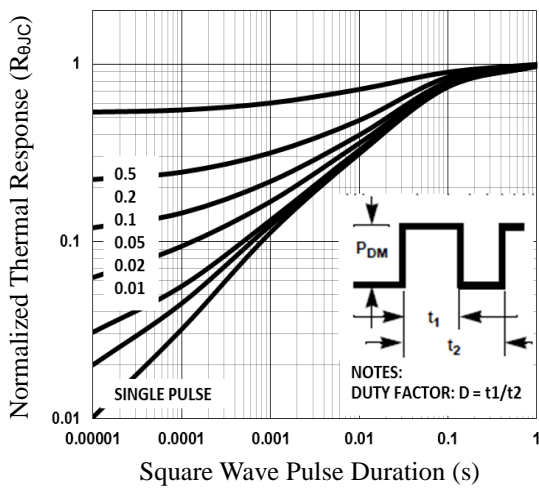
**Fig.8 Q2 Normalized  $R_{DS(on)}$  vs.  $T_j$**



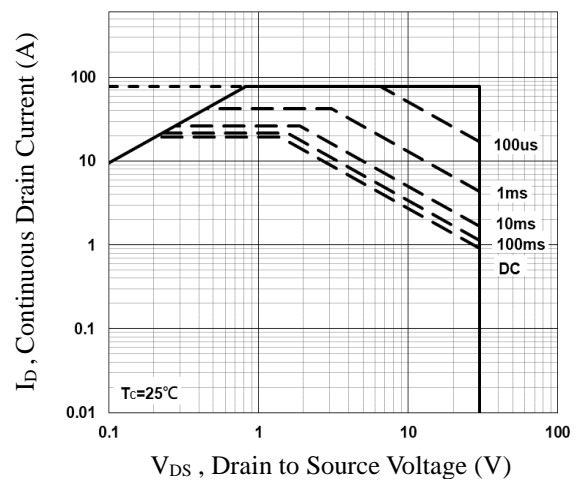
**Fig.9 Q2 Normalized  $V_{th}$  vs.  $T_j$**



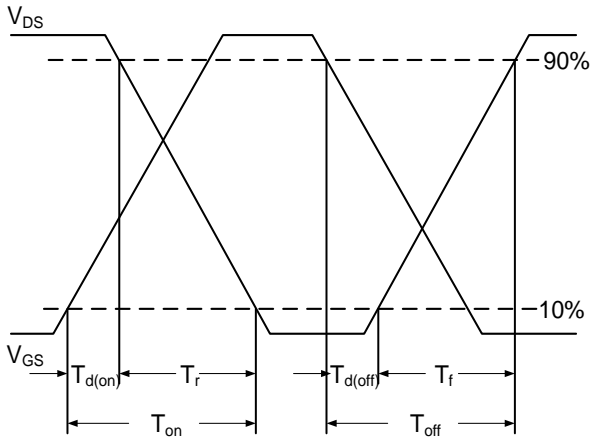
**Fig.10 Q2 Gate Charge Waveform**



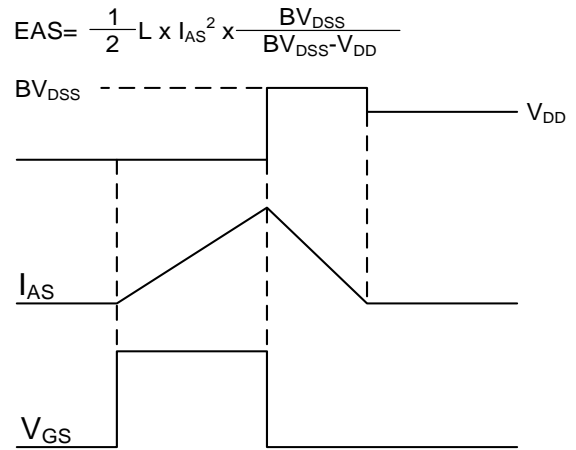
**Fig.11 Q2 Normalized Transient Impedance**



**Fig.12 Q2 Maximum Safe Operation Area**

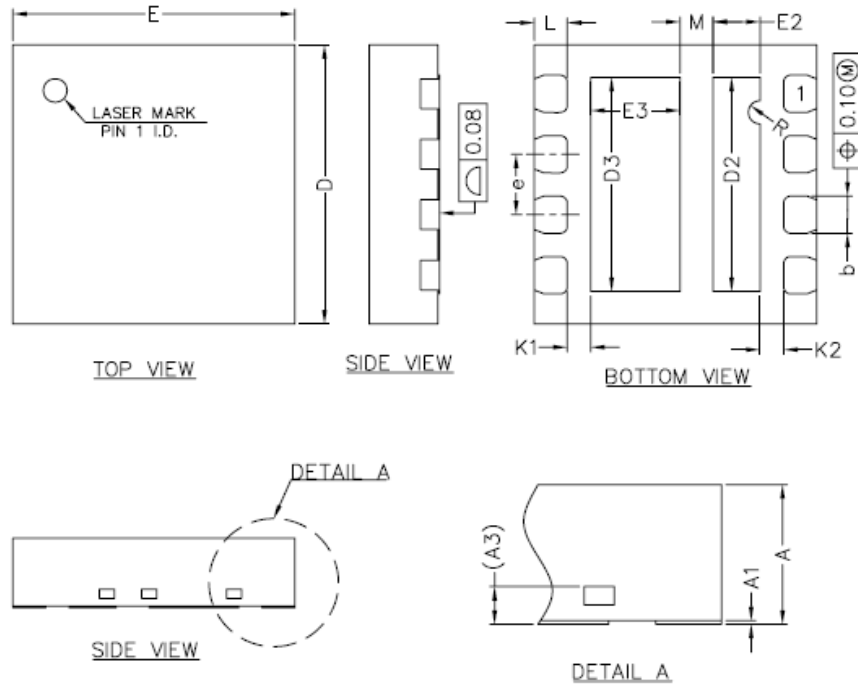


**Fig.13 Switching Time Waveform**



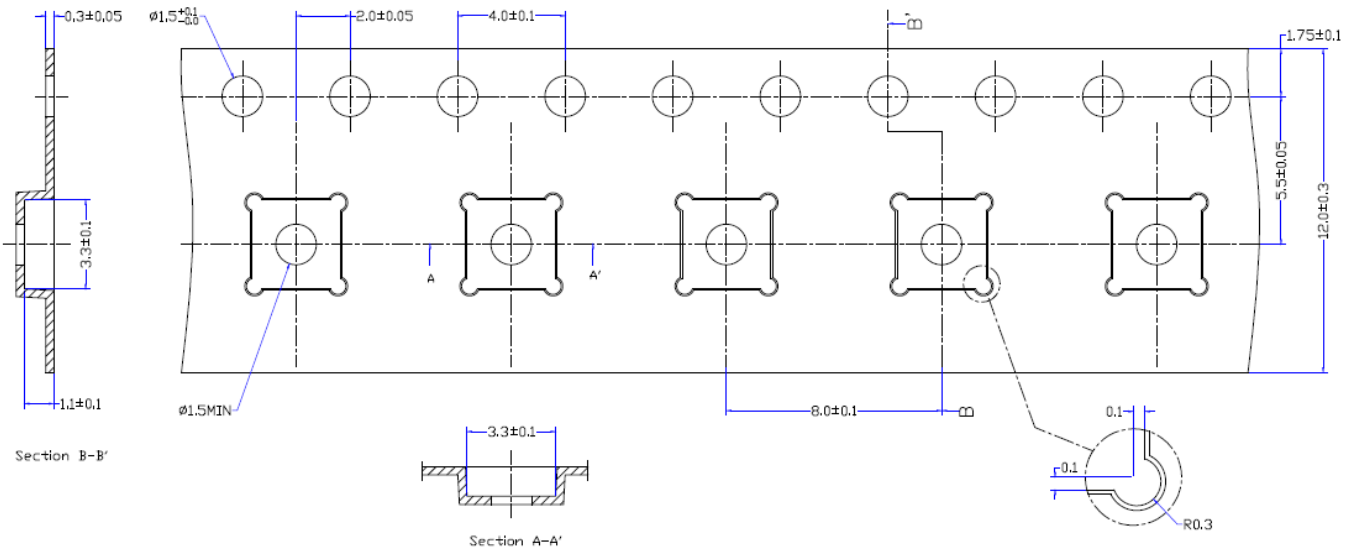
**Fig.14 EAS Waveform**

## DFN3x3 Asymmetric Dual Package Information



Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20REF		
b	0.35	0.40	0.45
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	2.20	2.30	2.40
E2	0.40	0.50	0.60
D3	2.20	2.30	2.40
E3	0.85	0.95	1.05
e	0.55	0.65	0.75
K1	0.15	0.25	0.35
K2	0.15	0.25	0.35
L	0.30	0.35	0.40
M	0.25	0.35	0.45
R	0.125REF		

### TAPE & REEL Information



**NOTES:**

1. 10 procket hole pitch cumulative tolerance  $\pm 0.2$
2. The meander of the tape is assumed with 1mm or less every 100mm between 250mm
3. MATERIAL: CONDUCTIVE POLYSTYRENE
4. ALL DIMS IN MM
5. There must not be foreign body adhesion and the state of the surface must be excellent
6. 17" PAPER-Reel, 77500pockets(620m)
7. Surface resistance  $1 \times 10^5 \sim 1 \times 10^9$  OHMS/SQ



### RECOMMEND FOOTPRINT Information

