DATA SHEET

PDIUSBH11
Universal Serial Bus Hub

Product specification
Supersedes data of 1997 Apr 17

1997 Aug 01

Philips
Semiconductors

PHILIPS

Universal Serial Bus Hub PDIUSBH11

FEATURES

- Complies with the Universal Serial Bus specification Rev. 1.0
- Four downstream ports with per packet connectivity
- Embedded function with two endpoints (control and interrupt)
- Integrated FIFO memory for hub and embedded function
- Automatic protocol handling
- Versatile I^2C interface
- Allows software control of monitor
- Compliant with USB Human Interface and Display Device Class
- Single 3.3V supply with 5V tolerant I/O

DESCRIPTION

The Philips Semiconductors PDIUSBH11 is a compound USB hub IC (hub plus embedded function).

It is used in a microcontroller based system and communicates with the system microcontroller over the I^2C serial bus. This modular approach to implementing a hub and embedded function allows the designer to maintain the system microcontroller of choice and retain existing architecture. This cuts down development time and offers the most cost-effective solution.

Ideal applications for the IC include computer monitors and keyboards.

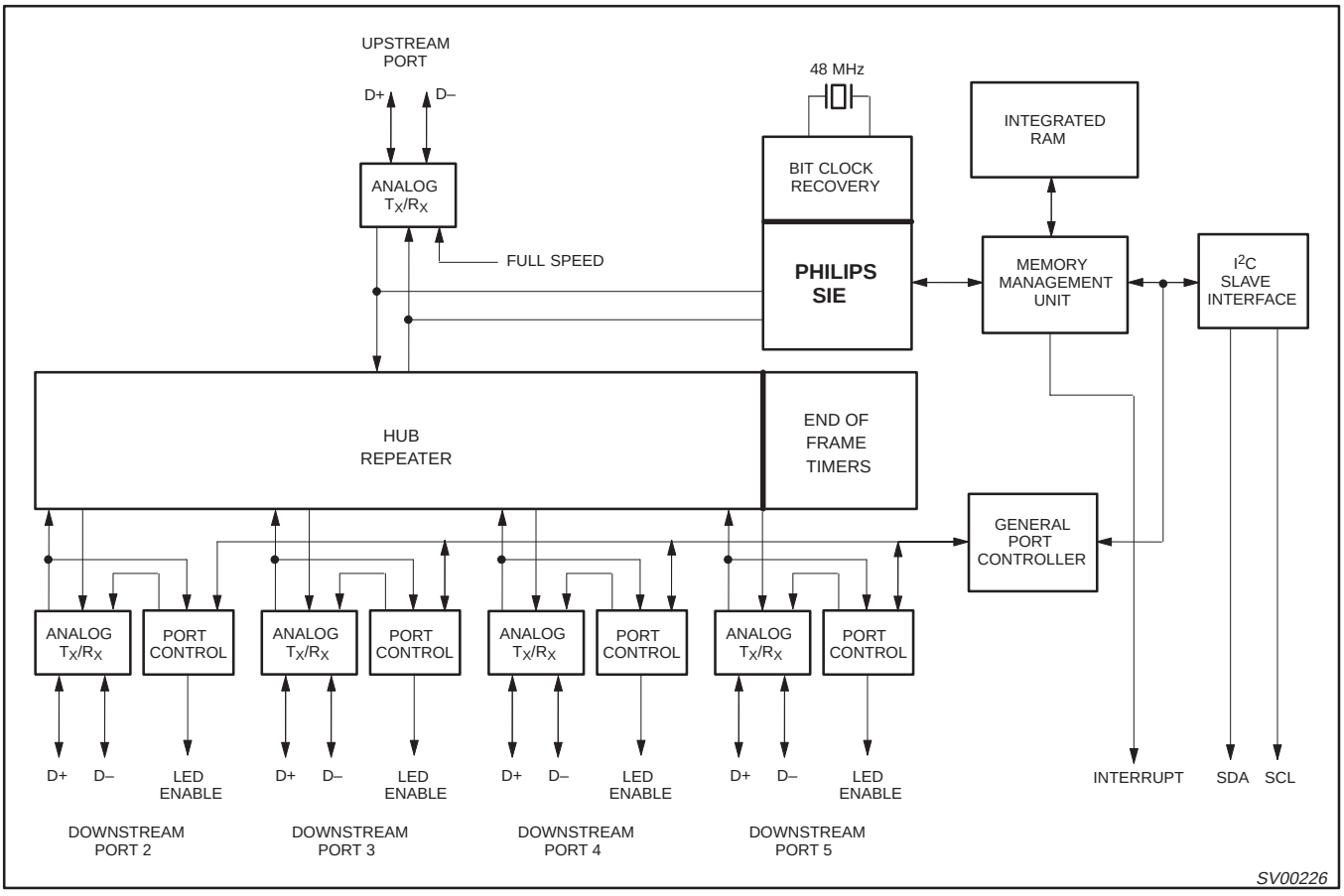
The PDIUSBH11 conforms to the USB specification 1.0 and I^2C serial interface specification. It is also compliant with the USB Human Input Device and Monitor Control Class specifications.

The embedded function of the PDIUSBH11 appears as PORT1 to the host system and the four downstream ports are numbered 2 through 5.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
32-pin plastic SO	0°C to +70°C	PDIUSBH11 D	PDIUSBH11 D	SOT287-1
32-pin plastic SDIP	0°C to +70°C	PDIUSBH11 NB	PDIUSBH11 NB	SOT232-1

BLOCK DIAGRAM



NOTE:

1. This is a conceptual block diagram and does not include each individual signal.

Analog Transceivers
These transceivers interface directly to the USB cables through some termination resistors. They are capable of transmitting and receiving serial data at both “full speed” (12 Mbit/s) and “low speed” (1.5 Mbit/s) data rates.

Hub Repeater
The hub repeater is responsible for managing connectivity on a per packet basis. It implements packet signaling connectivity and resume connectivity.

Low speed devices can be connected to downstream ports since the repeater will not propagate upstream packets to downstream ports, to which low speed devices are connected, unless they are preceded by a PREAMBLE PID.

End of Frame Timers
This block contains the specified EOF1 and EOF2 timers which are used to detect loss-of-activity and babble error conditions in the hub repeater. The timers also maintain the low-speed keep-alive strobe which is sent at the beginning of a frame.

General and Individual Port Controller
The general and individual port controllers together provide status and control of individual downstream ports. Via the I^2C-interface a microcontroller can access the downstream ports and request or change the status of each individual port.

Any change in the status or settings of the individual port will result in an interrupt request. Via an interrupt register, the servicing microcontroller can look up the downstream port which generated the interrupt and request its new status. Any port status change can then be reported to the host via the hub status change (interrupt) endpoint.

Bit Clock Recovery
The bit clock recovery circuit recovers the clock from the incoming USB data stream using (4X) over-sampling principle. It is able to track jitter and frequency drift specified by the USB spec.

Philips Serial Interface Engine (PSIE)
The Philips SIE implements the full USB protocol layer. It is completely hardwired for speed and needs no firmware intervention. The functions of this block include: synchronization pattern recognition, parallel / serial conversion, bit stuffing / destuffing, CRC checking / generation, PID verification / generation, address recognition, handshake evaluation / generation.

Memory Management Unit (MMU) and Integrated RAM
The MMU and the integrated RAM is used to handle the large difference in data-rate between USB, running in burst of 12 Mbit/s and the I^2C interface to the microcontroller, running at 100 kbit/s. This allows the microcontroller to read and write USB packets at its own (low) speed through I^2C.

I^2C Slave Interface
This block implements the necessary I^2C interface protocol. A slave I^2C allows for simple micro-coding. An interrupt is used to alert the microcontroller whenever the PDIUSBH11 needs attention. As a slave I^2C device, the PDIUSBH11 I^2C clock: SCL is an input and is controlled by the microcontroller.

ENDPOINT DESCRIPTIONS

The following table summarizes the endpoints supported by the PDIUSBH11.

FUNCTION	ENDPOINT NUMBER	ENDPOINT TYPE	TRANSFER TYPE	DIRECTION	MAXIMUM PACKET SIZE (bytes)
HUB	0	Default	Control	IN, OUT	8
	1	Status change	Interrupt	IN	1
EMBEDDED	0	Default	Control	IN, OUT	8
	1	Interrupt	Interrupt	IN	8

PIN DESCRIPTION

The PDIUSBH11 has two modes of operation. The first mode (Mode 0) enables the pins DNx_EN_N to power a LED indicating the port is enabled. The second mode (Mode 1) utilizes the LED enable pins as per port overcurrent condition pins.

The voltage level at power up on the TEST1 and TEST2 pins determine the PDIUSBH11 mode of operation. When both of the pins are connected to Ground, Mode 0 is enabled. When pins TEST1 and TEST2 are connected to Vcc, Mode 1 is enabled. Note that in Mode 1 the pin DN2_EN_N remains an LED enable pin. Pin TEST3 should always be connected to Ground at all times.

PIN DESCRIPTION (MODE 0)

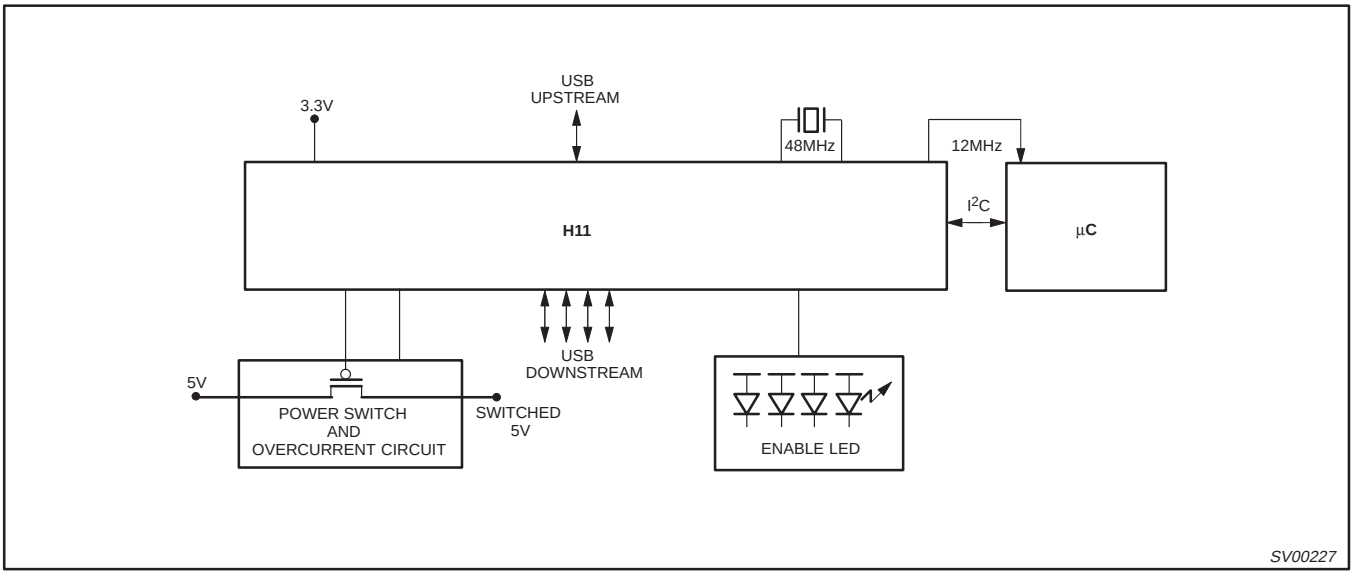
PIN NO	PIN SYMBOL	I/O	DRIVE	NAME AND FUNCTION
1	TEST1	I		Connect to Ground
2	TEST2	I		Connect to Ground
3	TEST3	I		Connect to Ground
4	RESET_N	I	ST	Power-on reset
5	GND	POWER		Ground reference
6	XTAL1	I/O		Crystal connection 1 (48MHz)
7	XTAL2	I/O		Crystal connection 2 (48MHz)
8	CLK12MHZ	O	2mA	12MHz output clock for external devices
9	V_{CC}	POWER		Voltage supply 3.3V ± 0.3V
10	OCURRENT_N	I	ST	Over-current notice to the device
11	SWITCH_N	O	OD8	Enables power to downstream ports
12	SUSPEND	O	4mA	Device is in suspended state
13	DN2_EN_N	O	OD8	Downstream port 2 LED enable indicator
14	DN3_EN_N	O	OD8	Downstream port 3 LED enable indicator
15	DN4_EN_N	O	OD8	Downstream port 4 LED enable indicator
16	DN5_EN_N	O	OD8	Downstream port 5 LED enable indicator
17	INT_N	O	OD4	Connect to microcontroller interrupt
18	SDA	I/O	OD4	I^2C bi-directional data
19	SCL	I/O	OD4	I^2C bit-clock
20	GND	POWER		Ground reference
21	DN5_DP	AI/O		Downstream port 5 D^+ connection
22	DN5_DM	AI/O		Downstream port 5 D^- connection
23	DN4_DP	AI/O		Downstream port 4 D^+ connection
24	DN4_DM	AI/O		Downstream port 4 D^- connection
25	DN3_DP	AI/O		Downstream port 3 D^+ connection
26	DN3_DM	AI/O		Downstream port 3 D^- connection
27	DN2_DP	AI/O		Downstream port 2 D^+ connection
28	DN2_DM	AI/O		Downstream port 2 D^- connection
29	AGND	POWER		Analog Ground reference
30	AV_{CC}	POWER		Analog voltage supply 3.3V ± 0.3V
31	UP_DP	AI/O		Upstream D^+ connection
32	UP_DM	AI/O		Upstream D^- connection

PIN DESCRIPTION (MODE 1)

PIN NO	PIN SYMBOL	I/O	DRIVE	NAME AND FUNCTION
1	TEST1	I		Connect to V_{CC}
2	TEST2	I		Connect to V_{CC}
3	TEST3	I		Connect to Ground
4	RESET_N	I	ST	Power-on reset
5	GND	POWER		Ground reference
6	XTAL1	I/O		Crystal connection 1 (48MHz)
7	XTAL2	I/O		Crystal connection 2 (48MHz)
8	CLK12MHZ	O	2mA	12MHz output clock for external devices
9	V_{CC}	POWER		Voltage supply 3.3V ± 0.3V
10	OCURRENT2_N	I	ST	Downstream port 2 over-current notice
11	SWITCH_N	O	OD8	Enables power to downstream ports
12	SUSPEND	O	4mA	Device is in suspended state
13	DN2_EN_N	O	OD8	Downstream port 2 LED enable indicator
14	OCURRENT3_N	I	ST	Downstream port 3 over-current notice
15	OCURRENT4_N	I	ST	Downstream port 4 over-current notice
16	OCURRENT5_N	I	ST	Downstream port 5 over-current notice
17	INT_N	O	OD4	Connect to microcontroller interrupt
18	SDA	I/O	OD4	I^2C bi-directional data
19	SCL	I/O	OD4	I^2C bit-clock
20	GND	POWER		Ground reference
21	DN5_DP	AI/O		Downstream port 5 D^+ connection
22	DN5_DM	AI/O		Downstream port 5 D^- connection
23	DN4_DP	AI/O		Downstream port 4 D^+ connection
24	DN4_DM	AI/O		Downstream port 4 D^- connection
25	DN3_DP	AI/O		Downstream port 3 D^+ connection
26	DN3_DM	AI/O		Downstream port 3 D^- connection
27	DN2_DP	AI/O		Downstream port 2 D^+ connection
28	DN2_DM	AI/O		Downstream port 2 D^- connection
29	AGND	POWER		Analog Ground reference
30	AV_{CC}	POWER		Analog voltage supply 3.3V ± 0.3V
31	UP_DP	AI/O		Upstream D^+ connection
32	UP_DM	AI/O		Upstream D^- connection

NOTES:
1. Signals ending in _N indicate active low signals.
   ST: Schmitt Trigger
   OD4, OD8: Open Drain with 4 or 8 mA drive
   AI/O: Analog I/O

APPLICATION DIAGRAM



I²C Interface.
The I²C bus is used to interface to an external microcontroller needed to control the operation of the hub. For cost consideration, the target system microcontroller can be shared and utilized for this purpose. The PDIUSBH11 implements a slave I²C interface. When the PDIUSBH11 needs to communicate with the microcontroller it asserts an interrupt signal. The microcontroller services this interrupt by reading the appropriate status register on the PDIUSBH11 through the I²C bus. (For more information about the I²C serial bus, refer to the I²C handbook, Philips order number 9397 750 00013).

The I²C interface on the PDIUSBH11 defines two types of transactions :

1. **command transaction**
   A command transaction is used to define which data (e.g., status byte, buffer data, ...) will be read from / written to the USB interface in the next data transaction. A data transaction usually follows a command transaction.
2. **data transaction**
   A data transaction reads data from / writes data to the USB interface. The meaning of the data is dependent on the command transaction which was sent before the data transaction.

Two addresses are used to differentiate between command and data transactions. Writing to the command address is interpreted as a command, while reading from / writing to the data address is used to transfer data between the PDIUSBH11 and the controller.

ADDRESS TABLE

TYPE OF ADDRESS	PHYSICAL ADDRESS (MSB to LSB)
Command	0011 011 (binary)
Data	0011 010 (binary)

Protocol
An I²C transaction starts with a ‘Start Condition’, followed by an address. When the address matches either the command or data address the transaction starts and runs until a ‘Stop Condition’ or another ‘Start Condition’ (repeated start) occurs.

The command address is write-only and is unable to do a read. The next bytes in the message are interpreted as commands. Several command bytes can be sent after one command address. Each of the command bytes is acknowledged and passed on to the Memory Management Unit inside the PDIUSBH11.

When the start condition address matches the data address, the next bytes are interpreted as data. When the RW bit in the address indicates a ‘master writes data to slave’ (=‘0’) the bytes are received, acknowledged and passed on to the Memory Management Unit. If the RW bit in the address indicates a ‘master reads data from slave’ (=‘1’) the PDIUSBH11 will send data to the master. The I²C-master must acknowledge all data bytes except the last one. In this way the I²C interface knows when the last byte has been transmitted and it then releases the SDA line so that the master controller can generate the STOP condition.

Repeated start support allows another packet to be sent without generating a Stop Condition.

Timing
When the master writes data to the PDIUSBH11, the data is sampled 1 micro-second after the rising edge of SCL. When the PDIUSBH11 writes data to the master, the data is driven 1 micro-second after the falling edge of SCL.

COMMAND SUMMARY

Some commands have the same command code (e.g., Read Buffer and Write Buffer). In these cases, the direction of the Data Phase (read or write) indicates which command is executed.

COMMAND NAME	RECIPIENT	CODING	DATA PHASE
Initialization Commands			
Set Address / Enable	Hub	D0h	Write 1 byte
	Embedded Function	D1h	Write 1 byte
Set Endpoint Enable	Hub + Embedded Function	D8h	Write 1 byte
Data Flow Commands			
Read Interrupt Register		F4h	Read 1 byte
Select Endpoint	Hub Control OUT	00h	Read 1 byte (optional)
	Hub Control IN	01h	Read 1 byte (optional)
	Embedded Function Control OUT	02h	Read 1 byte (optional)
	Embedded Function Control IN	03h	Read 1 byte (optional)
	Embedded Function Interrupt	04h	Read 1 byte (optional)
Read Last Transaction Status	Hub Control OUT	40h	Read 1 byte
	Hub Control IN	41h	Read 1 byte
	Embedded Function Control OUT	42h	Read 1 byte
	Embedded Function Control IN	43h	Read 1 byte
	Embedded Function Interrupt	44h	Read 1 byte
Read Endpoint Status	Hub Control OUT	80h	Read 1 byte
	Hub Control IN	81h	Read 1 byte
	Embedded Function Control OUT	82h	Read 1 byte
	Embedded Function Control IN	83h	Read 1 byte
	Embedded Function Interrupt	84h	Read 1 byte
Read Buffer	Selected Endpoint	F0h	Read n bytes
Write Buffer	Selected Endpoint	F0h	Write n bytes
Set Endpoint Status	Hub Control OUT	40h	Write 1 byte
	Hub Control IN	41h	Write 1 byte
	Embedded Function Control OUT	42h	Write 1 byte
	Embedded Function Control IN	43h	Write 1 byte
	Embedded Function Interrupt	44h	Write 1 byte
Acknowledge Setup	Selected Endpoint	F1h	None
Clear Buffer	Selected Endpoint	F2h	None
Validate Buffer	Selected Endpoint	FAh	None
Hub Commands			
Clear Port Feature	Port 2	E0h	Write 1 byte
	Port 3	E1h	Write 1 byte
	Port 4	E2h	Write 1 byte
	Port 5	E3h	Write 1 byte
Set Port Feature	Port 2	E8h	Write 1 byte
	Port 3	E9h	Write 1 byte
	Port 4	EAh	Write 1 byte
	Port 5	EBh	Write 1 byte
Get Port Status	Port 2	E0h	Read 1 or 2 bytes
	Port 3	E1h	Read 1 or 2 bytes
	Port 4	E2h	Read 1 or 2 bytes
	Port 5	E3h	Read 1 or 2 bytes
Set Status Change Bits		F7h	Write 1 byte
General Commands			
Send Resume		F6h	None
Read Current Frame Number		F5h	Read 1 or 2 bytes

COMMAND DESCRIPTIONS

Command Procedure
There are four basic types of commands: Initialization, Data, Hub Specific and General commands. Respectively, these are used to initialize the hub and embedded function; for data flow between the hub, embedded function and the host; some hub specific commands for controlling individual downstream ports; and some general commands.

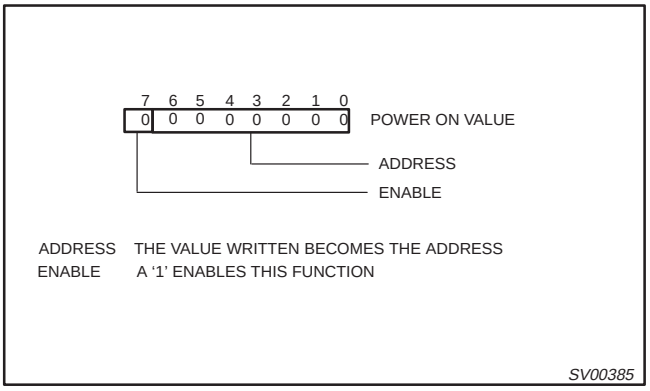
Initialization Commands
Initialization commands are used during the enumeration process of the USB network. These commands are used to enable the hub and embedded function endpoints. They are also used to set the USB assigned address.

Set Address / Enable

Command : D0h (Hub), D1h (Embedded Function)

Data : Write 1 byte

This command is used to set the USB assigned address and enable the hub or embedded function respectively. The hub always powers up disabled and should be enabled after a bus RESET.

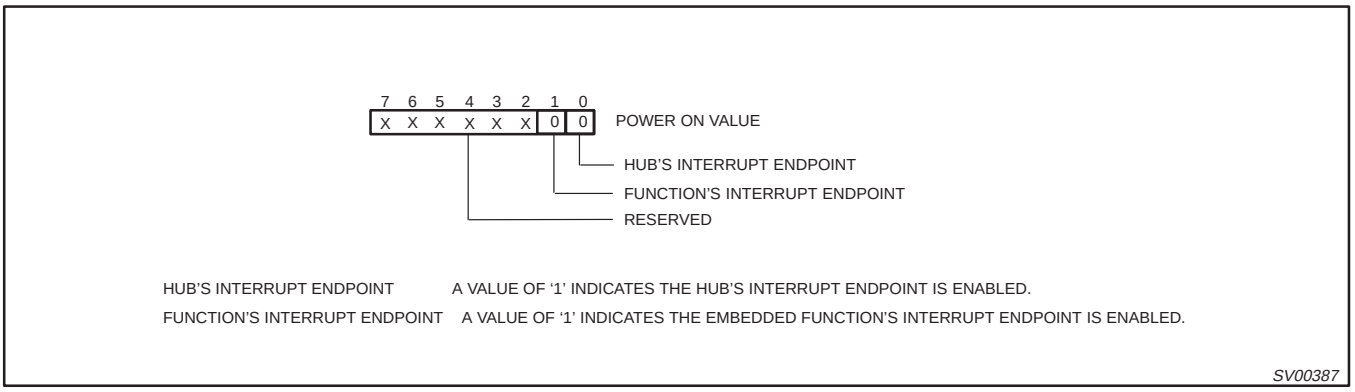


Set Endpoint Enable

Command : D8h

Data : Write 1 byte

Interrupt endpoints can only be enabled when the hub/function is enabled via the Set Address/Enable command.



Data Flow Commands

Data flow commands are used to manage the data transmission between the USB endpoints and the monitor. Much of the data flow is initiated via an interrupt to the microcontroller. The microcontroller utilizes these commands to access and determine whether the endpoint FIFOs have valid data.

Read Interrupt Register

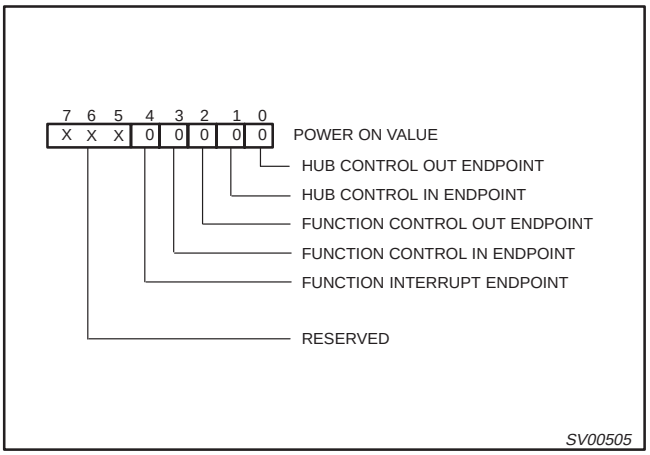
Command : F4h

Data : Read 1 byte

This command indicates the origin of an interrupt. A “1” indicates an interrupt occurred at this endpoint. The bits are cleared by reading the endpoint status register through Read Endpoint Status command.

After a bus reset an interrupt will be generated, however all bits in the interrupt register will be 0. The interrupt is internally cleared by reading the interrupt register. A bus reset is completely identical to the hardware reset through the RESET_N pin with the sole difference of interrupt notification.

The hub interrupt endpoint is handled internally by the PDIUSBH11 hardware without the need of microcontroller intervention.

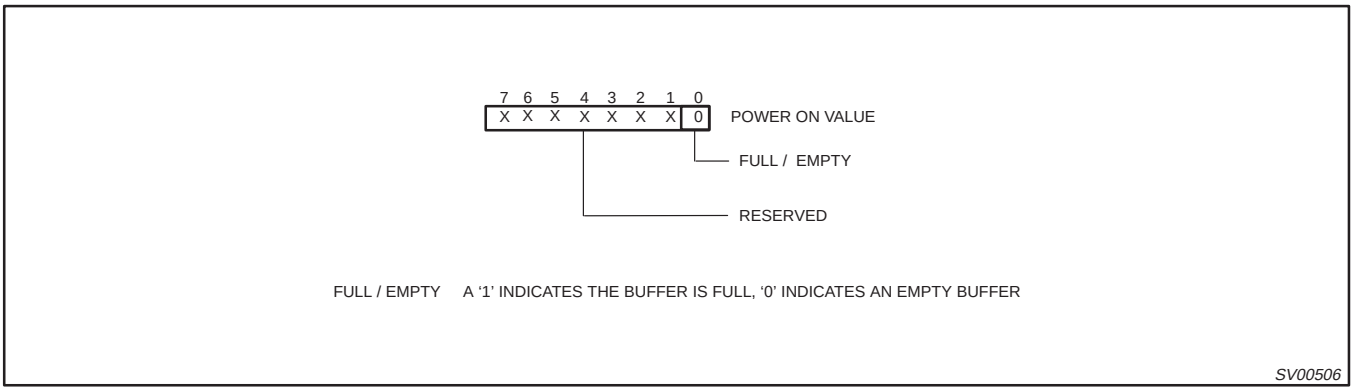


Select Endpoint

Command : 00–04h

Data : Optional Read 1 byte

The Select Endpoint command initializes an internal pointer to the start of the Selected buffer. Optionally, this command can be followed by a data read, which returns 0 if the buffer is empty and 1 if the buffer is full.



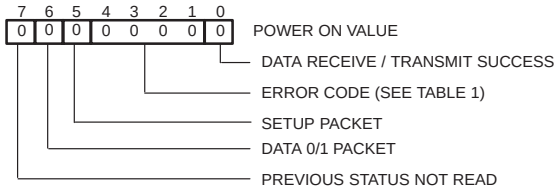
Read Last Transaction Status

Command : 40–44h

Data : Read 1 byte

The *Read Last Transaction Status* command is followed by one data read that returns the status of the last transaction of the endpoint. This command also resets the corresponding interrupt flag in the interrupt register, and clears the status, indicating that it was read.

This command is useful for debugging purposes. Since it keeps track of every transaction, the status information is overwritten for each new transaction.



DATA RECEIVE / TRANSMIT SUCCESS	A '1' INDICATES DATA HAS BEEN RECEIVED OR TRANSMITTED SUCCESSFULLY
ERROR CODE	SEE TABLE 1
SETUP PACKET	A '1' INDICATES THE LAST RECEIVED PACKET HAD A SETUP TOKEN (THIS ALWAYS READ '0' FOR IN BUFFERS.
DATA 0/1 PACKET	A '1' INDICATES THAT THE LAST RECEIVED OR SENT PACKET HAD A DATA1 PID
PREVIOUS STATUS NOT READ	A '1' INDICATES A SECOND EVENT OCCURRED BEFORE THE PREVIOUS STATUS WAS READ.

SV00507

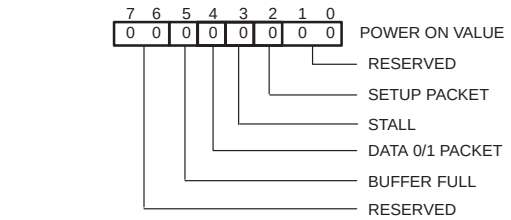
Table 1.

ERROR CODE	RESULT
0000	No Error
0001	PID Encoding Error, Bits 7–4 are not the inversion of bits 3–0
0010	PID Unknown, encoding is valid, but PID does not exist
0011	Unexpected Packet, Packet is not of the type expected (= token, data or acknowledge), or SETUP token to a non-control endpoint
0100	Token CRC Error
0101	Data CRC Error
0110	Time Out Error
0111	Babble Error
1000	Unexpected End of Packet
1001	Sent or Received NAK
1010	Sent Stall, a token was received, but the endpoint was stalled
1011	Overflow Error, the received packet was longer than the available buffer space
1101	Bitstuff Error
1111	Wrong DATA PID, the received DATA PID was not the expected one

Read Endpoint Status

Command : 80–84h

Data : Read 1 byte



SETUP PACKET	A '1' INDICATES THE LAST RECEIVED PACKET WAS A SETUP TOKEN
STALL	A '1' INDICATES THE ENDPOINT IS STALLED
DATA 0/1 PACKET	A '1' INDICATES THAT THE LAST RECEIVED OR SENT PACKET HAD A DATA1 PID
BUFFER FULL	A '1' INDICATES THAT THE BUFFER IS FULL

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Read Buffer

Command : F0h

Data : Read multiple bytes (max 10)

The Read Buffer command is followed by a number of data reads, which return the contents of the selected endpoint data buffer. After each read, the internal buffer pointer is incremented by 1.

The buffer pointer is not reset to the buffer start by the Read Buffer command. This means that reading or writing a buffer can be interrupted by any other command (except for Select Endpoint), or can be done by more than one I2C transaction (read the first 2 bytes to get the number of data bytes, then read the rest in other transactions).

The data in the buffer are organized as follows:

- byte 0: reserved: can have any value
- byte 1: Number / length of data bytes
- byte 2: Data byte 1
- byte 3: Data byte 2

Write Buffer

Command : F0h

Data : Write multiple bytes (max 10)

The Write Buffer command is followed by a number of data writes, which load the endpoints buffer. The data must be organized in the same way as described in the Read Buffer command. The first byte (reserved) should always be 0. As in the Read Buffer command, the data can be split up into different I2C data transactions.

WARNING

There is no protection against writing or reading over a buffer's boundary or against writing into an OUT buffer or reading from an IN buffer. Any of these actions could cause an incorrect operation. Data in an OUT buffer are only meaningful after a successful transaction.

Clear Buffer

Command : F2h

Data : None

When a packet is received completely, an internal endpoint buffer full flag is set. All subsequent packets will be refused by returning a NACK. When the microcontroller has read the data, it should free the buffer by the Clear Buffer command. When the buffer is cleared new packets will be accepted.

Validate Buffer

Command : FAh

Data : None

When the microprocessor has written data into an IN buffer, it should set the buffer full flag by the Validate Buffer command. This indicates that the data in the buffer are valid and can be sent to the host when the next IN token is received.

Set Endpoint Status

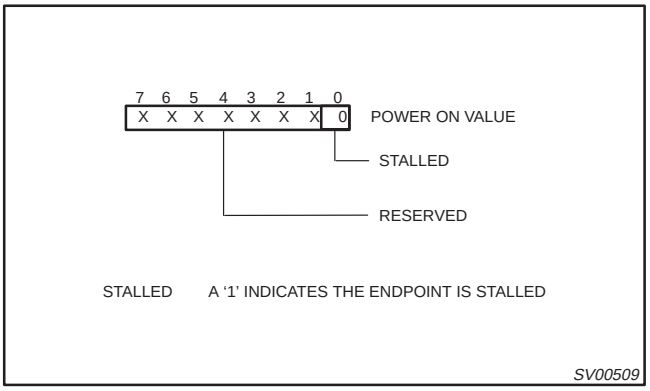
Command : 40–44h

Data : Write 1 byte

A stalled control endpoint is automatically unstalled when it receives a SETUP token, regardless of the content of the packet. If the endpoint should stay in its stalled state, the microcontroller can re–stall it.

When a stalled endpoint is unstalled (either by the Set Endpoint Status command or by receiving a SETUP token), it is also re–initialized. This flushes the buffer and if it is an OUT buffer it waits for a DATA 0 PID, if it is an IN buffer it writes a DATA 0 PID.

Even when unstalled, writing Set Endpoint Status to ‘0’ initializes the endpoint.



Acknowledge Setup

Command : F1h

Data : None

The arrival of a SETUP packet flushes the IN buffer and disables the Validate Buffer and Clear Buffer commands for both IN and OUT endpoints.

The microcontroller needs to re–enable these commands by the Acknowledge Setup command. This ensures that the last SETUP packet stays in the buffer and no packet can be sent back to the host until the microcontroller has acknowledged explicitly that it has seen the SETUP packet.

The microcontroller must send the Acknowledge Setup command to both the IN and OUT endpoints.

Hub Commands
Hub commands are used to report connectivity and power status between the hub and the host. These commands allow the host to enable each port individually and get any change of status such as new connectivity information.

Clear/Set Port Feature

Command : E0–E3h (Clear) and E8h–EBh (Set)

Data : Write 1 byte

When the controller receives a Set Feature or a Clear Feature request, there are two possibilities:

- The request applies to port 1, the embedded port. In this case the request should be handled internally by the controller.
- If the request applies to ports 2 through 5, the controller should translate the request into a Set Feature or Clear Feature command towards the PDIUSBH11.

When the PDIUSBH11 is configured in mode 0, there is only one power switch output and one overcurrent input. This means that the F_PORT_POWER and C_PORT_OVERCURRENT features are not port specific. For these features, any of the Set / Clear Feature commands can be used. The specific port assignment is ignored.

When the PDIUSBH11 is configured in mode 1, there is still only one power switch output but there are four individual overcurrent input pins corresponding to each port. This means that the F_PORT_POWER feature is port specific and the C_PORT_OVERCURRENT feature is not port specific.

Setting the F_PORT_POWER feature turns the power on when it is off and turns the overcurrent detection on only when the power is already on. This allows to have a short period of overcurrent condition at the moment that power is switched on. For this reason, the F_PORT_POWER feature needs to be set twice. Clearing this feature turns both the power and the overcurrent detection off.

The data written in the data phase is the feature code described in Table 2.

Table 2.

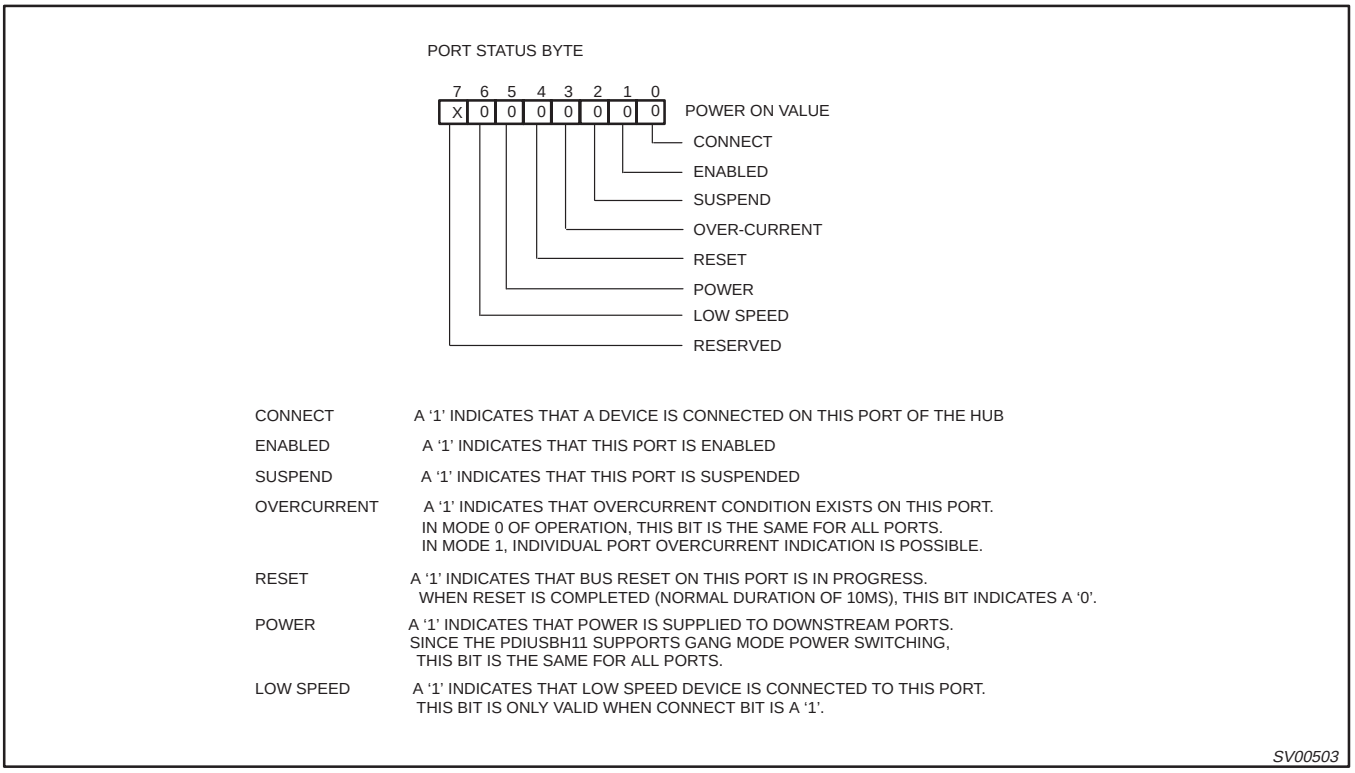
FEATURE	FEATURE CODE	SET	CLEAR
F_PORT_ENABLE	0	Enables a port	Disables a port
F_PORT_SUSPEND	1	Suspends a port	Resumes a port
FC_PORT_RESET	2	Resets a port	Clears a port Reset Change bit
F_PORT_POWER	3	Powers all ports	Unpowers all ports
C_PORT_CONNECTION	4	–	Clears a port Connection Change bit
C_PORT_ENABLE	5	–	Clears a port Enable Change bit
C_PORT_SUSPEND	6	–	Clears a port Suspend Change bit
C_PORT_OVERCURRENT	7	–	Clears a port (Mode 1) or hub (Mode 0) Overcurrent Change bit

Get Port Status

Command : E0h–E3h

Data : Read 1 or 2 bytes

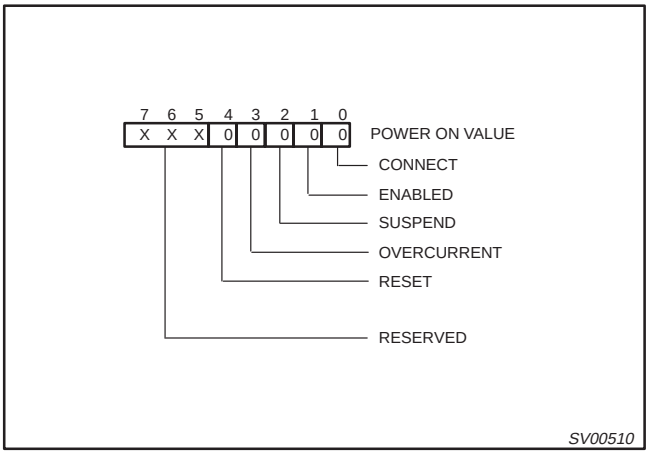
The Get Port Status Command can be followed by one or two data reads. The first byte returned contains the port status. The second byte returned is the port status change byte.



CONNECT	A ‘1’ INDICATES THAT A DEVICE IS CONNECTED ON THIS PORT OF THE HUB
ENABLED	A ‘1’ INDICATES THAT THIS PORT IS ENABLED
SUSPEND	A ‘1’ INDICATES THAT THIS PORT IS SUSPENDED
OVERCURRENT	A ‘1’ INDICATES THAT OVERCURRENT CONDITION EXISTS ON THIS PORT. IN MODE 0 OF OPERATION, THIS BIT IS THE SAME FOR ALL PORTS. IN MODE 1, INDIVIDUAL PORT OVERCURRENT INDICATION IS POSSIBLE.
RESET	A ‘1’ INDICATES THAT BUS RESET ON THIS PORT IS IN PROGRESS. WHEN RESET IS COMPLETED (NORMAL DURATION OF 10MS), THIS BIT INDICATES A ‘0’.
POWER	A ‘1’ INDICATES THAT POWER IS SUPPLIED TO DOWNSTREAM PORTS. SINCE THE PDIUSBH11 SUPPORTS GANG MODE POWER SWITCHING, THIS BIT IS THE SAME FOR ALL PORTS.
LOW SPEED	A ‘1’ INDICATES THAT LOW SPEED DEVICE IS CONNECTED TO THIS PORT. THIS BIT IS ONLY VALID WHEN CONNECT BIT IS A ‘1’.

Port Status Change Byte

The description for the Port Status Change Byte is similar to the Port Status Byte except that the value of the bits are ‘1’ only when a change has occurred.



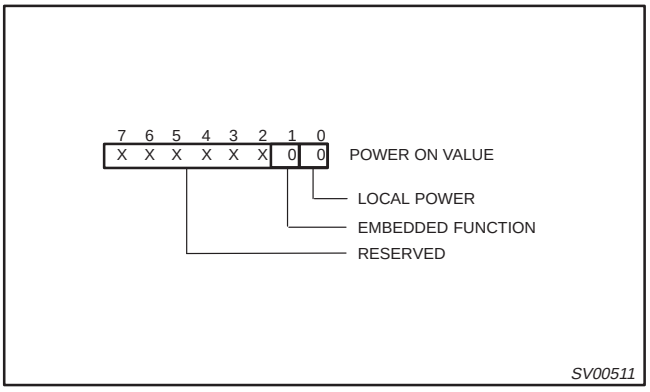
Set Status Change Bits

Command : F7h

Data : Write 1 byte

For assembling the hub's status change register, the device needs some additional information from the controller, i.e. the Local Power Status Change bit and the embedded function Status Change bit.

These are provided by the Set Status Change Bits command. This command is always followed by one data write which contains the Local Power Status Change bit at the LSB and the embedded function Status Change bit at position 1. All other bits should be 0.



GENERAL COMMANDS

Send Resume

Command : F6h

Data : None

Sends an upstream resume signal for 10 ms. This command is normally issued when the device is in suspend. The RESUME command is not followed by a data read or write.

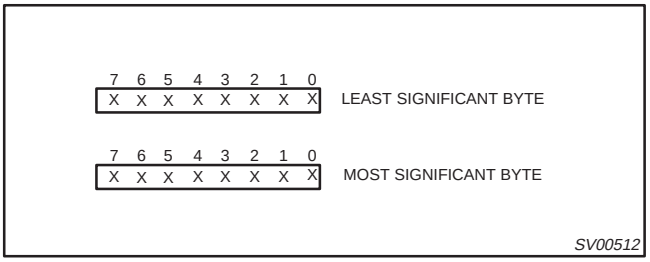
The PDIUSBH11 automatically sends a RESUME command when an event occurs downstream.

Read Current Frame Number

Command : F5h

Data : Read 1 or 2 bytes

This command is followed by one or two data reads and returns the frame number of the last successfully received SOF. The frame number is returned Least Significant Byte first.



EMBEDDED FUNCTION

The USB host sees no difference between the embedded function and a function connected to one of the downstream ports. Some of the port commands sent by the host must be handled appropriately by the embedded function to appear as any other downstream port.

The micro controller maintains a series of status and status change bits for the embedded function as described in the Get Port Status command section. From these bits, the Status Change bit for the embedded function is derived (i.e. the port specific Status Change bits). This Status Change bit is then provided to the PDIUSBH11 by the Set Status Change Bits command.

Host Requests

SetFeature PORT_RESET
Reinitialize the embedded function and set the Reset Change bit to indicate that the reset has completed. Reset the Enable Status bit, enable the embedded function and set its address to 0 by the Set embedded function Address / Enable command. Disable the embedded function interrupt endpoint by the Set Endpoint Enable command.

SetFeature PORT_ENABLE
Enable the function by the Set embedded function Address / Enable command. Set the Enable Status bit.

SetFeature PORT_SUSPEND
Disable the function by the Set embedded function Address / Enable command. Reset the Enable Status bit and set the Suspend Status bit.

ClearFeature PORT_ENABLE
Disable the function by the Set embedded function Address / Enable command. Reset the Enable Status bit.

ClearFeature PORT_SUSPEND
Enable the function by the Set embedded function Address / Enable command. Set the Enable Status bit, reset the Suspend Status bit; set the Resume Status Change bit to indicate that the resume has completed.

ClearFeature any Change Indicator
Clear the corresponding status change bit.

Babbling Condition
When the embedded function causes a babbling condition, the function is automatically disabled by the PDIUSBH11. As soon as the micro controller detects the babbling error, it must set the Enable Status Change bit and reset the Enable Status bit.

Remote WakeUp
There are three scenarios a remote wakeup can occur. The following describes the course of actions for each of the cases:

1. The device is not suspended and the embedded port is suspended
   - Enable back the function by setting the enable bit in the Set Address/Enable register and update the following status bits in the micro–controller program: reset the Suspend Status bit, set the Enable Status bit and set the Suspend Status Change bit.
2. The device is suspended and the embedded port is suspended.
   - Send an upstream Resume using the Send Resume command, enable back the function by setting the enable bit in the Set Address/Enable register and update the following status bits in the micro–controller program: reset the Suspend Status bit, set the Enable Status bit and set the Suspend Status Change bit.
3. The device is suspended and the embedded port is enabled
   - Send an upstream resume using the Send Resume command

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN.	MAX.	
V_{CC}	DC supply voltage		3.0	3.6	V
V_I	DC Input voltage range		0	5.5	V
$V_{I/O}$	DC input range for I/O		0	5.5	V
$V_{AI/O}$	DC input range for analog I/O		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics per device	0	+70	°C

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		–0.5	+4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–	-50	mA
V_I	DC input voltage	Note 2	–0.5	+5.5	V
$V_{I/O}$	DC input voltage range for I/O's		–0.5	V_{CC} +0.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
V_O	DC output voltage	Note 2	–0.5	V_{CC} +0.5	V
I_O	DC output source or sink current for digital pins	V_O = 0 to V_{CC}	–	±15	mA
I_O	DC output source or sink current for D+/D– pins	V_O = 0 to V_{CC}	–	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		–	±100	mA
T_{stg}	Storage temperature range		–60	+150	°C
P_{tot}	Power dissipation per package				mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

DC CHARACTERISTICS (DIGITAL PINS)

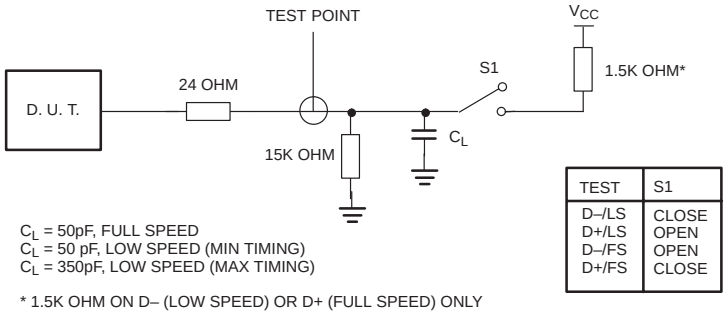
	PARAMETER		LIMITS			
			MIN	TYP	MAX	
Input Levels:						
V_{IL}	LOW level input voltage				0.9	V
V_{IH}	HIGH level input voltage		2.5			V
VTLH	LOW to HIGH threshold voltage	ST (Schmitt Trigger) pins			80	$\%V_{CC}$
VTHL	HIGH to LOW threshold voltage	ST (Schmitt Trigger) pins	20			$\%V_{CC}$
VHYS	Hysteresis voltage	ST (Schmitt Trigger) pins		1.1		V
Output Levels:						
V_{OL}	LOW level output	I_{OL} = rated drive	0.4			V
		I_{OL} = 20µA	0.1			
V_{OH}	HIGH level output	I_{OH} = rated drive			V_{CC} –0.4	V
		I_{OH} = 20µA			V_{CC} –0.1	
Leakage Current:						
I_{OZ}	OFF-state current	OD (Open Drain) pins			±5	µA
I_I	Input leakage current				±1	µA

DC CHARACTERISTICS (AI/O PINS)

	PARAMETER		LIMITS		
			MIN	MAX	
Leakage Current:					
I_{LO}	Hi–Z state data line leakage	0V < V_{IN} < 3.3V		±10	µA
Input Levels:					
VDI	Differential input sensitivity	|(D+) – (D–)|[1]	0.2		V
VCM	Differential common mode range	Includes VDI range	0.8	2.5	V
VSE	Single ended receiver threshold		0.8	2.0	V
Output Levels:					
V_{OL}	Static output LOW	RL of 1.5KΩ to 3.6V		0.3	V
V_{OH}	Static output HIGH	RL of 15KΩ to GND	2.8	3.6	V
Capacitance:					
C_{IN}	Transceiver capacitance	Pin to GND		20	pF
Output Resistance:					
ZDRV[2]	Driver output resistance	Steady state drive	28	43	Ω

NOTES:
1. D+ is the generic symbol for the USB positive data pins: UP_DP, DN2_DP, DN3_DP, DN4_DP, DN5_DP. D– is the generic symbol for the USB negative data pins: UP_DM, DN2_DM, DN3_DM, DN4_DM, DN5_DM.
2. Includes external resistors of 24Ω ±1% each on D+ and D–.

LOAD FOR D+/D–



SV00237

AC CHARACTERISTICS (AI/O PINS. FULL SPEED)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
Driver Characteristics:		C_L = 50pF; R_{pu} = 1.5KΩ on D+ to V_{CC}			
T_R T_F	Transition time: Rise time Fall tIme	Between 10% and 90%	 4 4	 20 20	ns
T_{RFM}	Rise/Fall tIme matching	(T_R/T_F)	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V
Driver Timings:					
T_{EOPT}	Source EOP width	Figure 1	160	175	ns
T_{DEOP}	Differential data to EOP transition skew	Figure 1	–2	5	ns
Receiver Timings:					
T_{JR1} T_{JR2}	Receiver data jitter tolerance To next transition For paired transitions	Characterized and not Tested. Guaranteed by Design.	 –18.5 –9	 18.5 9	ns
T_{EOPR1} T_{EOPR2}	EOP width at receiver Must reject as EOP Must accept	Figure 1	 40 82		ns
Hub Timings:		C_L = 50pF; R_{pu} = 1.5KΩ on D+ to V_{CC}			
T_{HDD}	Hub differential data delay	Figure 2		40	ns
T_{SOP}	Data bit width distortion after SOP	Figure 2	–5	3	ns
T_{EOPDR}	Hub EOP delay relative to T_{HDD}	Figure 3	0	15	ns
T_{HESK}	Hub EOP output width skew	Figure 3	–15	+15	ns

AC CHARACTERISTICS (AI/O PINS. LOW SPEED)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
Driver Characteristics:		C_L = 50pF and 350pF; R_{pu} = 1.5KΩ on D– to V_{CC}			
	Transition time:	Between 10% and 90%			ns
T_{LR}	Rise time	C_L = 50pF	75		
		C_L = 350pF		300	
T_{LF}	Fall tIme	C_L = 50pF	75		
		C_L = 350pF		300	
V_{LCRS}	Output signal crossover voltage		1.3	2.0	V
Driver Timings:					
T_{LEOPT}	Source EOP width	Figure 1	1.25	1.50	ns
T_{LDEOP}	Differential data to EOP transition skew	Figure 1	–40	100	ns
Receiver Timings:					
	EOP width at receiver				ns
T_{LEOPR1}	Must reject as EOP	Figure 1	330		
T_{LEOPR2}	Must accept		675		
Hub Timings:		C_L = 50pF and 350pF; R_{pu} = 1.5KΩ on D– to V_{CC}			
T_{LHDD}	Hub differential data delay	Figure 2		300	ns
T_{LSOP}	Data bit width distortion after SOP	Figure 2	–65	45	ns
T_{LEOPDR}	Hub EOP delay relative to T_{HDD}	Figure 3	0	200	ns
T_{LHESK}	Hub EOP output width skew	Figure 3	–300	+300	ns

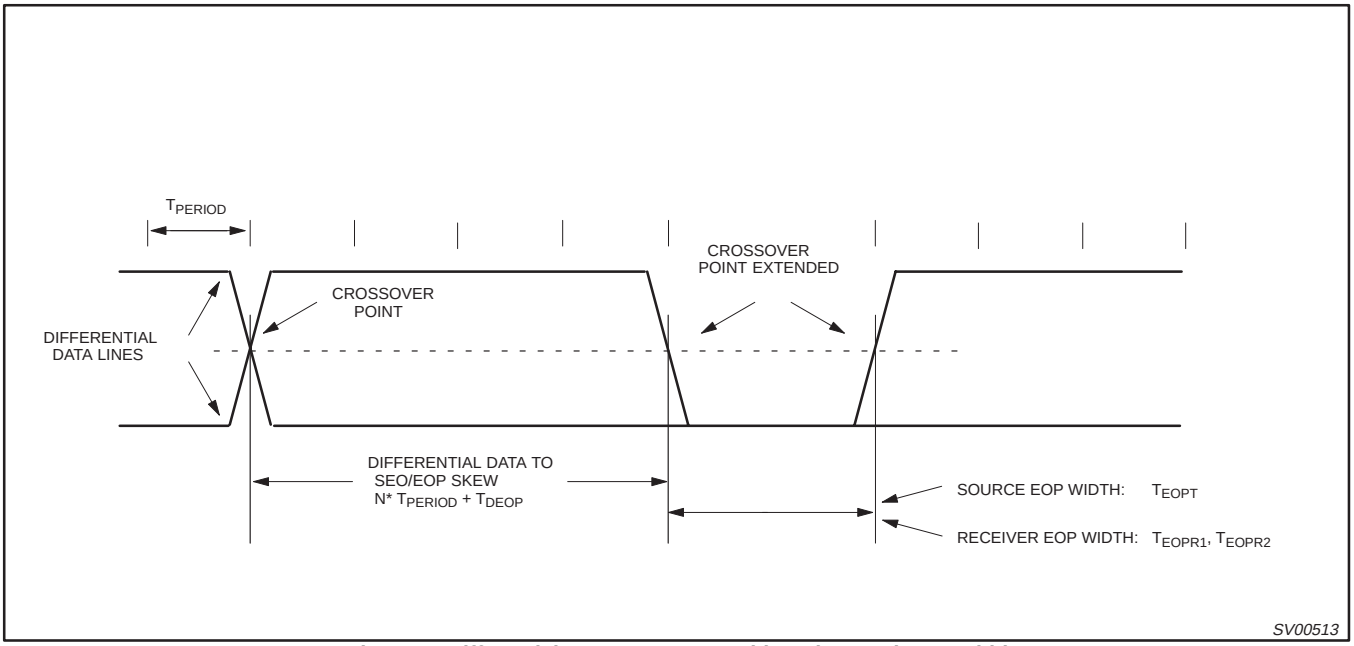


Figure 1. Differential Data to EOP Transition Skew and EOP Width

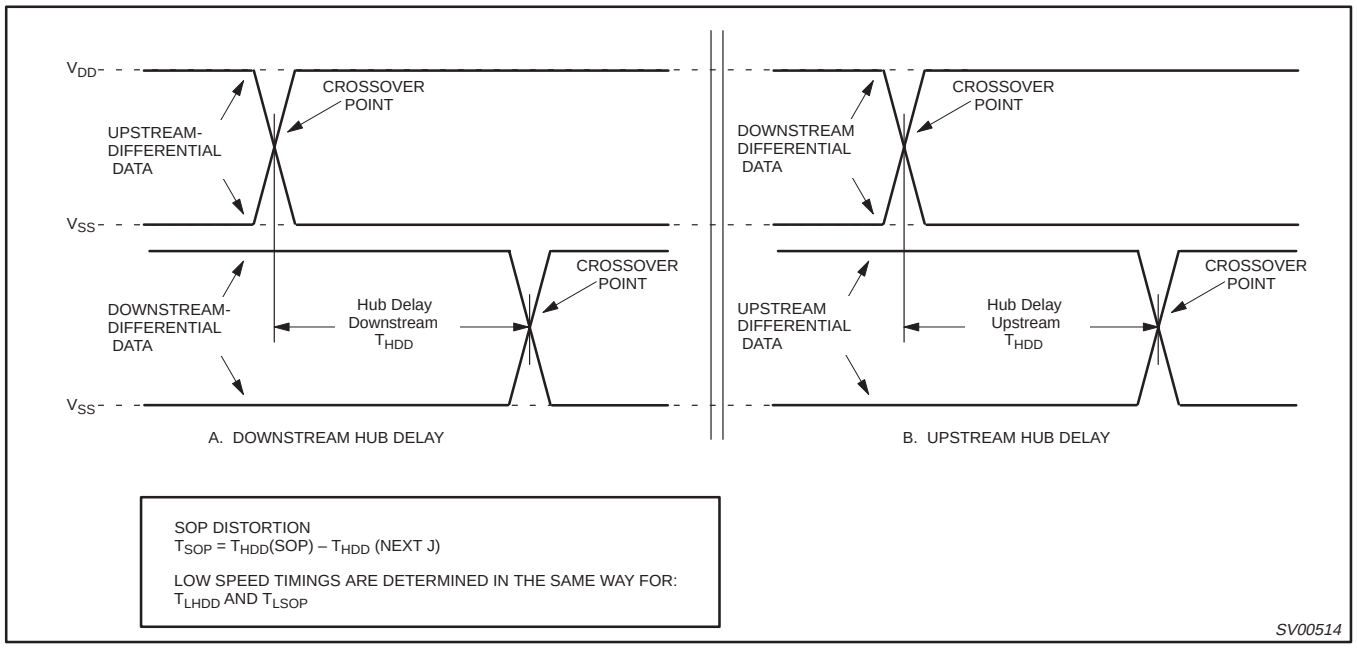


Figure 2. Hub Differential Data Delay and SOP Distortion

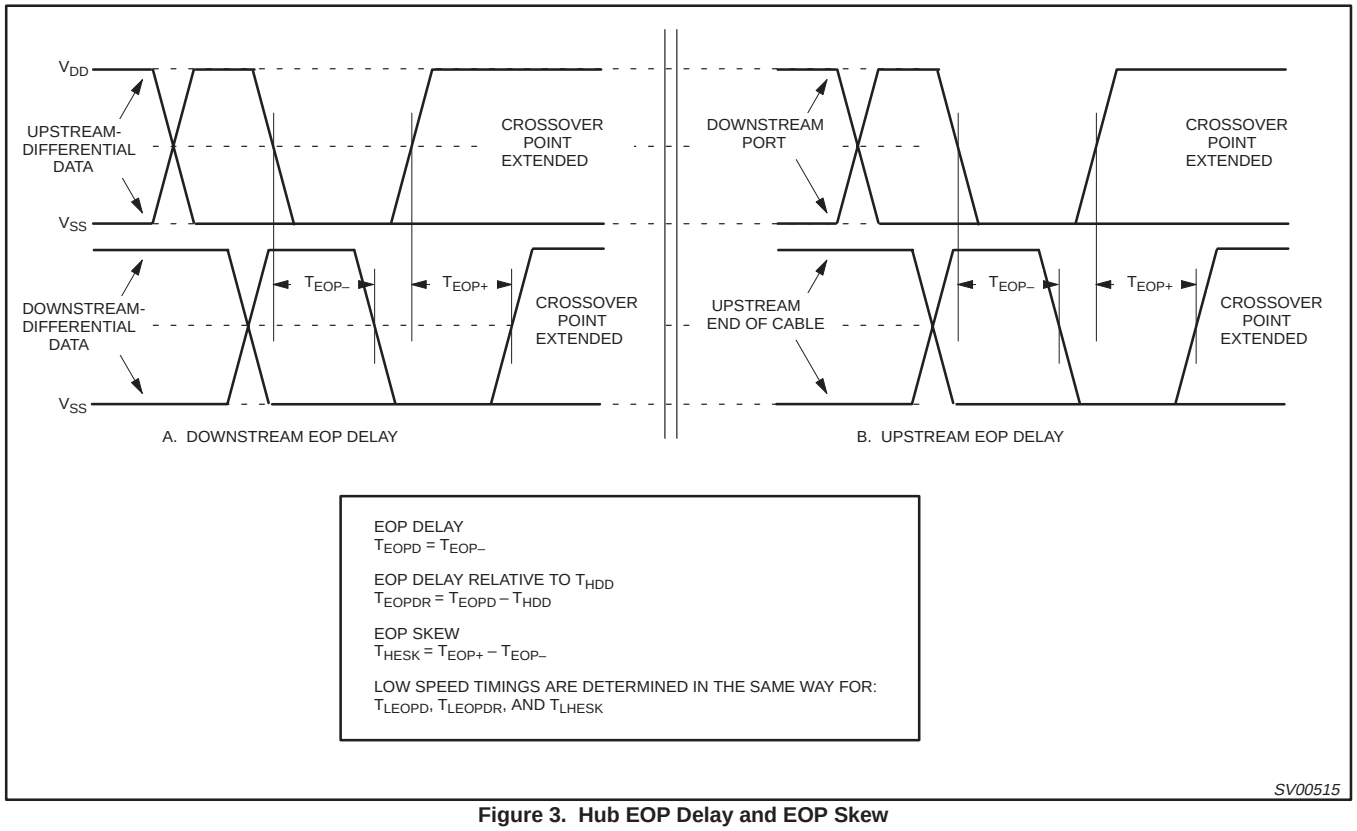


Figure 3. Hub EOP Delay and EOP Skew

AC CHARACTERISTICS (I^2C)

All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} and V_{DD}.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP	MAX	
I^2C-bus timing (see Figure ; Note)					
f_{SCL}	SCL clock frequency	–	–	100	kHZ
t_{SP}	Tolerable spike width on bus	–	–	100	ns
t_{BUF}	Bus free time	4.7	–	–	µs
$t_{SU;STA}$	Start condition set-up time	4.7	–	–	µs
$t_{HD;STA}$	Start condition hold time	4.0	–	–	µs
t_{LOW}	SCL LOW time	4.7	–	–	µs
t_{HIGH}	SCL HIGH time	4.0	–	–	µs
t_r	SCL and SDA rise times	–	–	1.0	µs
t_f	SCL and SDA fall times	–	–	0.3	µs
$t_{SU;DAT}$	Data set-up time	250	–	–	ns
$t_{HD;DAT}$	Data hold time	0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid	–	–	3.4	µs
$t_{SU;STO}$	Stop condition set-up time	4.0	–	–	µs

1. A detailed description of the I^2C-bus specification, with applications, is given in brochure "*The I^2C-bus and how to use it*". This brochure may be ordered using the code 9398 393 40011.

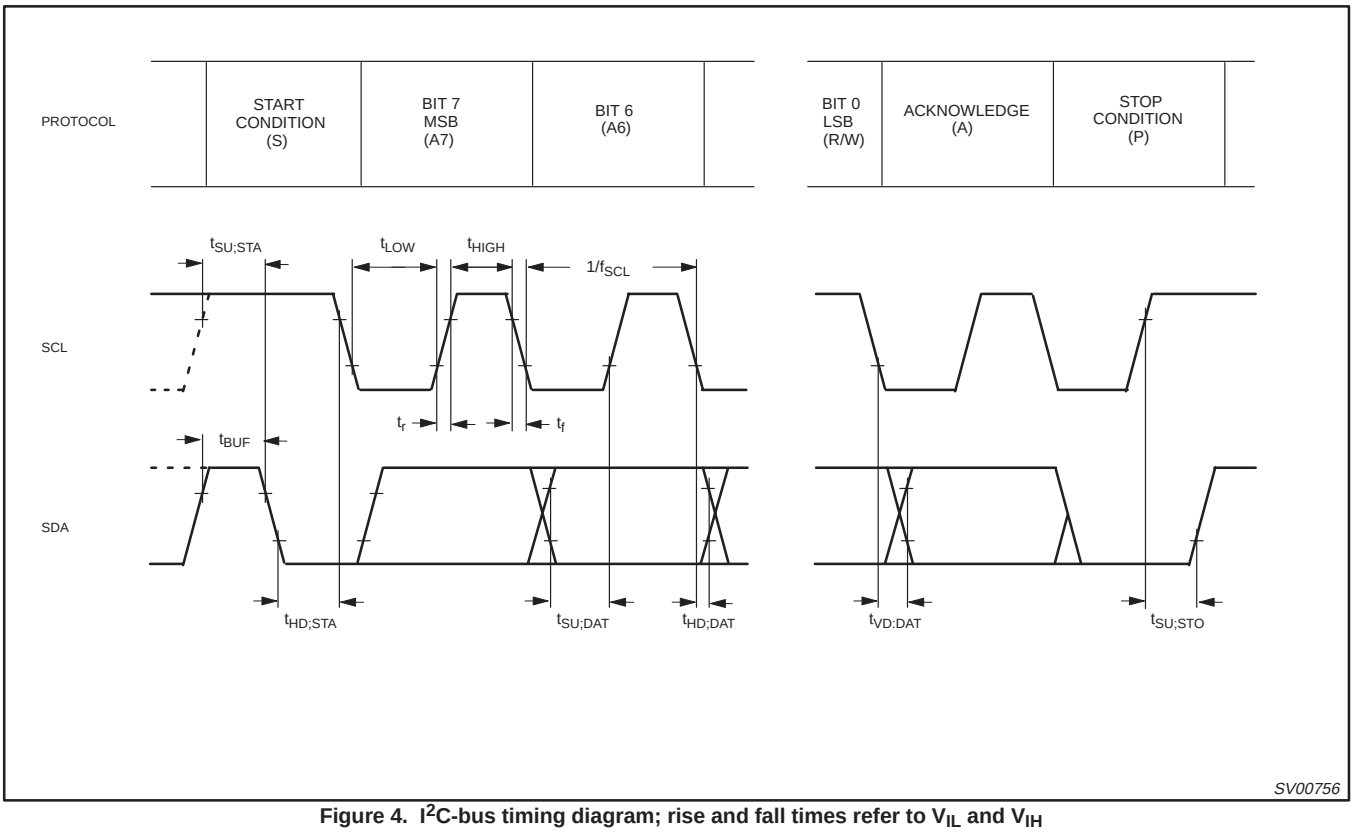
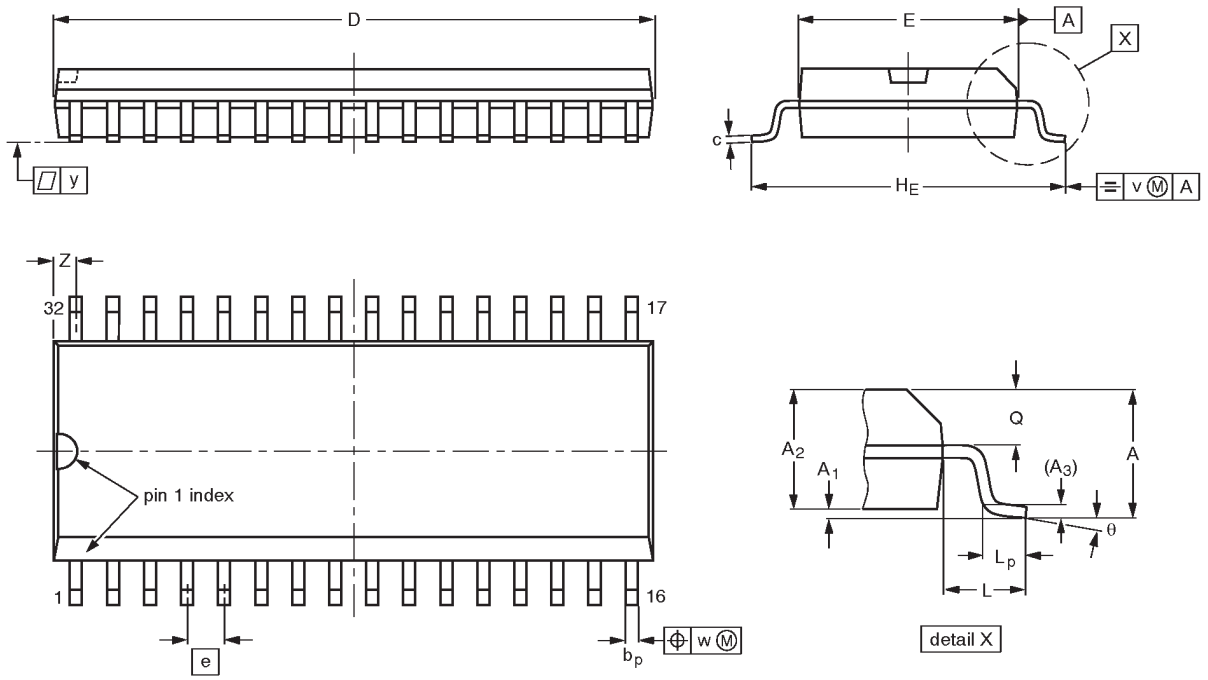
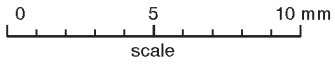


Figure 4. I^2C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}

SO32: plastic small outline package; 32 leads; body width 7.5mm **SOT287-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

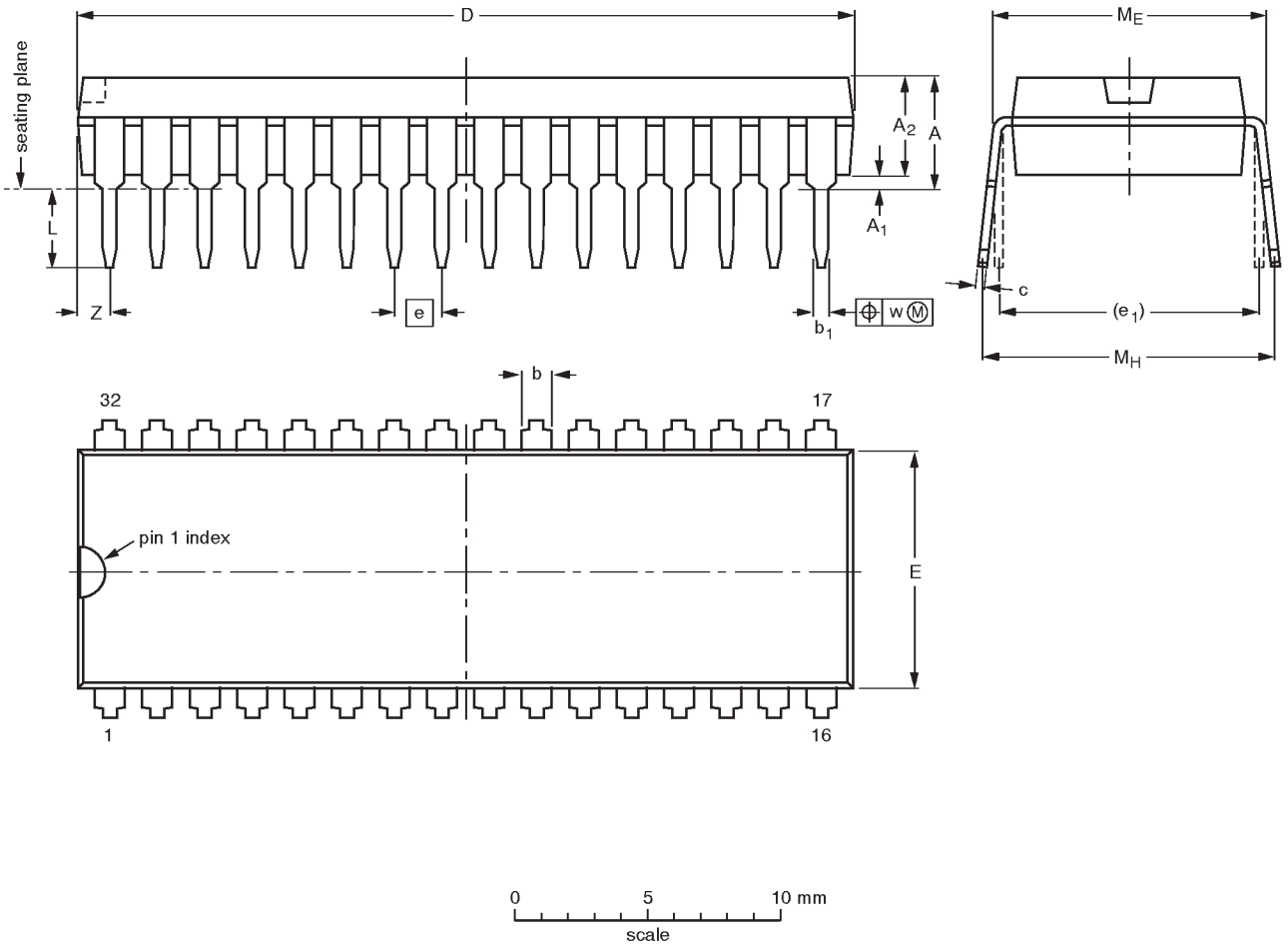
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8° 0°
inches	0.10	0.012 0.004	0.096 0.086	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT287-1						~~92-11-17~~ 95-01-25

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil) **SOT232-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	29.4 28.5	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT232-1						~~92-11-17~~ 95-02-04

NOTES

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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