# 64K x 18 Fast CMOS Synchronous Static SRAM with Linear Burst Counter

## Features

- Interfaces directly with the Motorola 680X0 and PowerPC™ processors (80, 66, 60, 50, 40 MHz)
- High Speed Access Times
  - Clock to data valid times: 8, 9, 10, 12, 14 ns
  - Cycle Times: 12.5, 15, 20, 25 ns
- High Density 64K x 18 Architecture
- Choice of 5V or 3V ±10% Output Vcc for output level compatability
- High Output Drive: 30 pF at Rated Taa
- Asynchronous Output Enable
- Self Timed Write Cycle
- Byte Writeable via Dual Write Strobes
- Internal linear burst read/write address counter
- Internal registers for Address, Data, Controls
- Packages: 52-pin PLCC

## Description

The PDM44028 is a 1,179,648 bit synchronous random access memory organized as 65,536 words by 18 bits. It has burst mode capability and interface controls designed to provide high performance in secondary cache designs for 680X0 and Power PC™ microprocessors. Addresses, write data and all control signals except output enable are controlled through positive edge triggered registers. Write cycles are self timed and are also initiated by the rising edge of the clock. Controls are provided to allow burst reads and writes of up to four words in length. A two-bit burst address counter controls the two least significant bits of the address during burst reads and writes. The burst address counter uses the 2-bit binary counting scheme required by the 680X0 and Power PC™ microprocessors. Individual write strobes provide byte write for the upper and lower 9-bit bytes of data. An asynchronous output enable simplifies interface to high speed buses. Separate output Vcc pins provide user controlled output levels of 5V or 3.3V, for 3.3V TTL compatibility.

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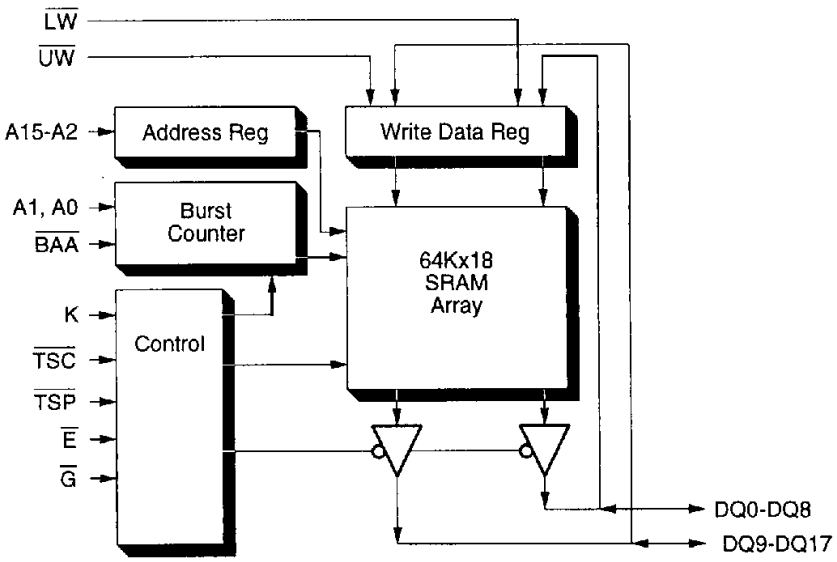
## Functional Block Diagram



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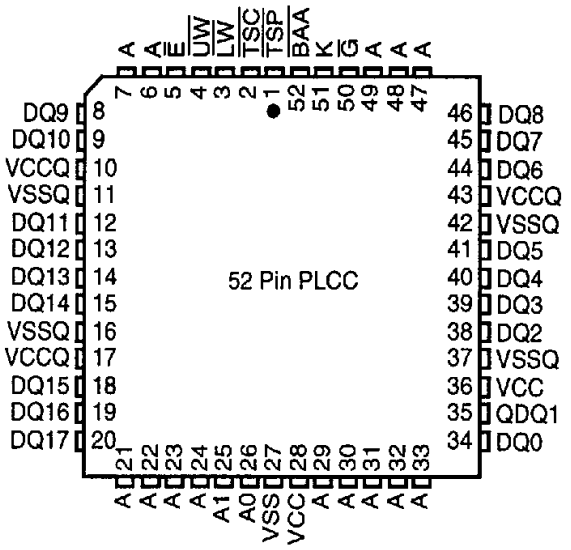
## Pin Assignment




## Pinout

| Name | I/O | Description | Name | I/O | Description |
|---|---|---|---|---|---|
| A | I | Address Inputs A15-A2 | $\overline{LW}$ | I | Low Byte Write Enable, DQ0-DQ8 |
| A1, A0 | I | Address Inputs A1 & A0 | $\overline{UW}$ | I | Upper Byte Write Enable, DQ8-DQ17 |
| DQ0-DQ17 | I/O | Read/Write Data | $\overline{G}$ | I | Output Enable |
| K | I | Clock | VCC | — | Array Power (+5V) |
| $\overline{BAA}$ | I | Burst Counter Advance | VCCQ | — | Output Power for DQ's (+3.3V or +5V) |
| $\overline{TSC}$ | I | Controller Address Status | VSS | — | Array Ground |
| $\overline{TSP}$ | I | Processor Address Status | VSSQ | — | Output Ground for DQ's |
| $\overline{E}$ | I | Chip Enable | | | |

All registers are positive-edge triggered. The state of $\overline{W}$ determines whether the next cycle will be a read or write cycle. The state of $\overline{W}$ is sampled at each clock rising edge. If sampled active (low), a write cycle begins; if sampled inactive (high), a read cycle begins. Read and write cycles begin at the current address, which is the base address loaded by $\overline{TSP}$ or $\overline{TSC}$ and modified by $\overline{BAA}$. $\overline{TSP}$ overrides $\overline{W}$. If $\overline{TSP}$ is active, $\overline{W}$ is internally forced inactive. Therefore, the first cycle following $\overline{TSP}$ is always a read cycle. The $\overline{TSC}$ or $\overline{TSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{TSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{TSC}$) is performed using the new external address. When $\overline{TSC}$ is sampled low (and $\overline{TSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. chip selects (S0, $\overline{S1}$) are sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{W}$ determines whether the next cycle is a read or write cycle, and $\overline{BAA}$ controls the advance of the address counter. When $\overline{BAA}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{BAA}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE FIGURE**.

## Synchronous Truth Table (See Notes 1 through 4)

| E | $\overline{TSP}$ | $\overline{TSC}$ | $\overline{BAA}$ | $\overline{UW}$ or $\overline{LW}$ | K | Address | Operation |
|---|---|---|---|---|---|---|---|
| H | X | L | X | X | ↑ | N/A | Deselected |
| L | L | X | X | X | ↑ | External | Read Cycle, Begin Burst |
| L | H | L | X | L | ↑ | External | Write Cycle, Begin Burst |
| L | H | L | X | H | ↑ | External | Read Cycle, Begin Burst |
| X | H | H | L | L | ↑ | Next | Write Cycle, Continue Burst |
| X | H | H | L | H | ↑ | Next | Read Cycle, Continue Burst |
| X | H | H | H | L | ↑ | Current | Write Cycle, Suspend Burst |
| X | H | H | H | H | ↑ | Current | Read Cycle, Suspend Burst |

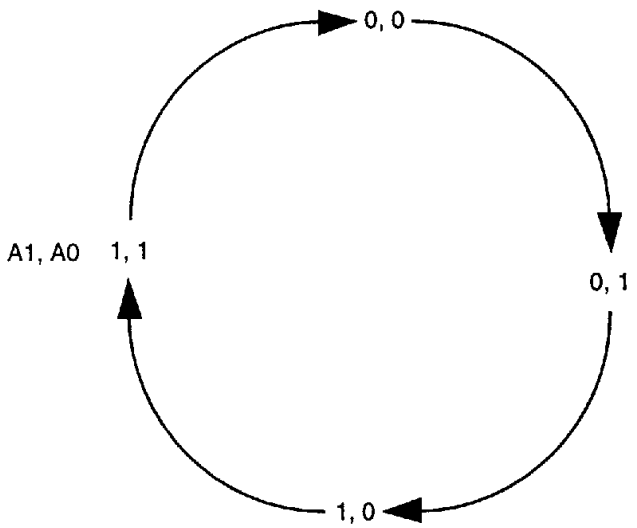
NOTE: 1. X means Don't Care.
2. All inputs except G must meet setup and hold times relative low-to-high transition of clock, K.
3. Wait states are inserted by suspending burst.

## Asynchronous Truth Table

| Operation | $\overline{G}$ | I/O Status |
|---|---|---|
| Read | L | Data Out |
| Read | H | High-Z |
| Write | X | High-Z: Write Data In |
| Deselected | X | High-Z |

NOTE:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup

## Burst Sequence




Base address provided with $\overline{TSP}$ or $\overline{TSC}$. The external two values for A1 and A0 provides the starting point for the burst sequence graph. The burst logic advances A1 and A0 as shown above.

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## Absolute Maximum Ratings

| Symbol | Rating | Com'l. | Unit |
|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | –0.5 to +7.0 | V |
| $T_A$ | Operating Temperature | 0 to +70 | °C |
| $T_{BIAS}$ | Temperature Under Bias | –55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | –55 to +125 | °C |
| $I_{OUT}$ | DC Output Current | 50 | mA |

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended DC Operating Conditions

| Symbol | Description | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 4.75 | 5.0 | 5.25 | V |
| $V_{CCQ}$ | | 5V | 4.5 | 5.0 | 5.5 | V |
| | | 3.3V | 3.0 | 3.3 | 3.6 | V |
| GND | Supply Voltage | | 0 | 0 | 0 | V |
| Industrial | Ambient Temperature | | –40 | 25 | 85 | °C |
| Commercial | Ambient Temperature | | 0 | 25 | 70 | °C |

## DC Electrical Characteristics ($V_{CC}$ = 5.0V ±5%, All Temperature Ranges)

| Symbol | Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $\|I_{LI}\|$ | Input Leakage Current | $V_{CC}$ = MAX., $V_{IN}$ = GND to $V_{CC}$ | — | 1 | µA |
| $\|I_{LO}\|$ | Output Leakage Current | $V_{CC}$= MAX., $V_{OUT}$ = GND to $V_{CC}$ | — | 1 | µA |
| $V_{OL}$ | Output Low Voltage | $V_{CC}$ = Min., $I_{OL}$ = 8 mA | 0 | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $V_{CC}$ = Min., $I_{OH}$ = –4 mA | 2.4 | $V_{CCQ}$ | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.2 | 6 | V |
| $V_{IL}$ | Input LOW Voltage (1) | | –0.5 | 0.8 | V |

NOTE: 1. Undershoots to –1.5 for 10 ns are allowed once per cycle.

## Power Supply Characteristics

| Symbol | Description | Test Conditions | | -8 ns | -9 ns | -10 ns | -12 ns | -14 ns | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $I_{CC1}$ | Active Supply Current: Outputs Open | $V_{CC}$ = Max., Inputs @ 0.0V or 3.0V F = $1/T_{CYC}$ on Rclk & Wclk | Com'l | 380 | 360 | 360 | 340 | 320 | mA |
| $I_{SB}$ | Standby Current: Outputs Open | $V_{CC}$ = Max., Inputs @ 0.0V or 3.0V F = $1/T_{CYC}$, E = $V_{IH}$ | Com'l | 130 | 120 | 120 | 110 | 100 | mA |

## Capacitance ($T_A$ = +25°C, f =1.0 MHz)

| Symbol | Parameter | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 6 | pF |
| $C_{OUT}$ | Output Leakage Current | $V_{OUT}$ = 0V | 8 | pF |

NOTES: 1. Characterized values, not currently tested.
2. With output deselected.

## AC Test Conditions

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input rise and fall times | 3 ns |
| Input timing reference levels | 1.5V |
| Output reference levels | 1.5V |
| Output Load | See Figures 1 and 2 |

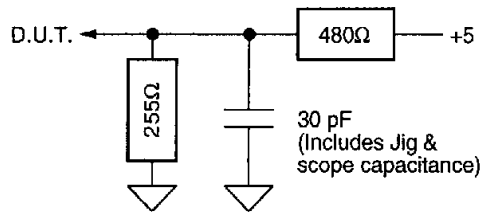



Figure 1a. Output Load

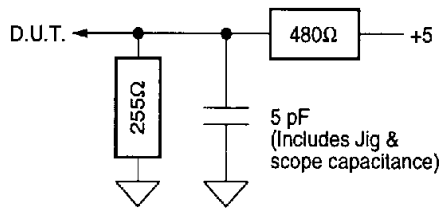


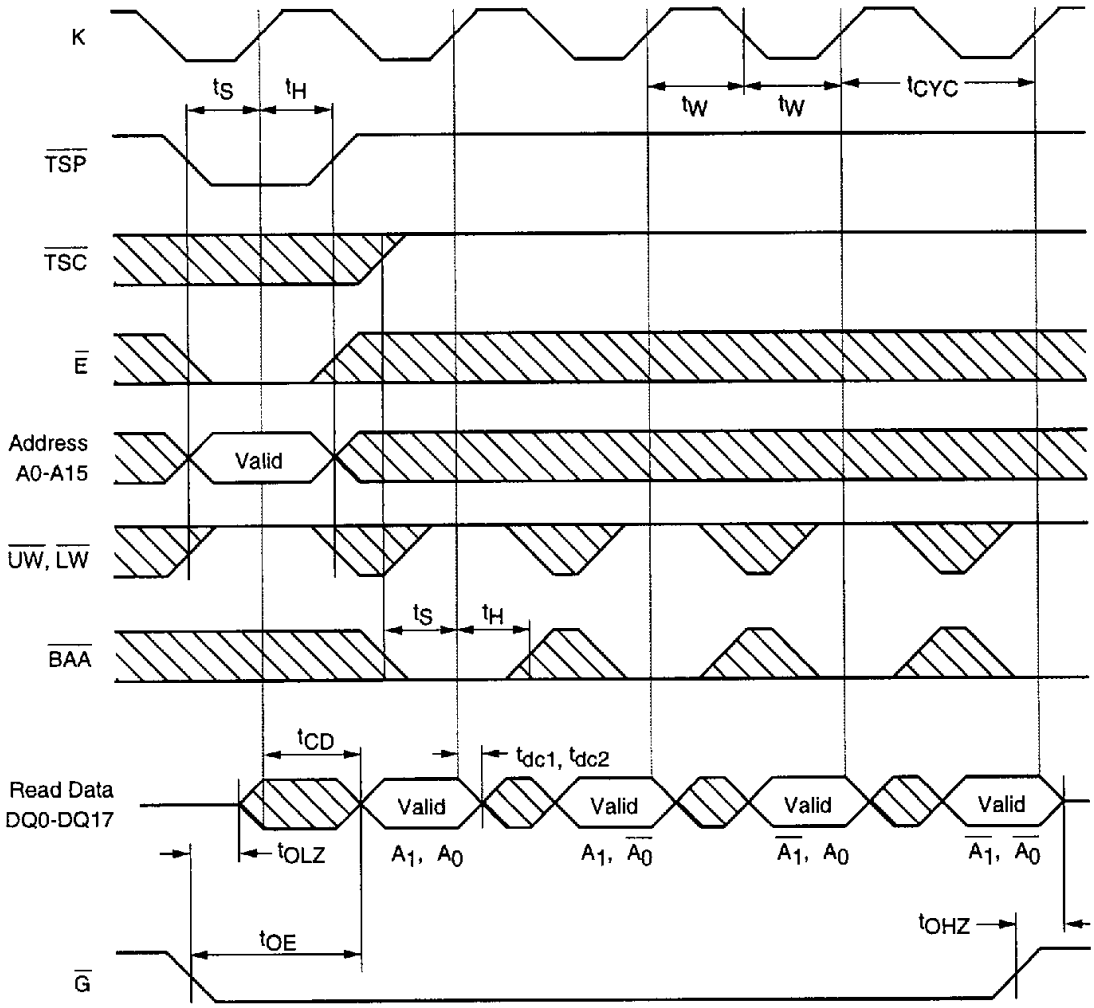

Figure 1b. Output Disable Timing Load

## AC Electrical Characteristics ($V_{CC}$ = 5V ± 5%, All Temperature Ranges)

| Parameter | Symbol | -8 | -9 | -10 | -12 | -14 | Type | Units |
|---|---|---|---|---|---|---|---|---|
| Clock Cycle time | $t_{CYC}$ | 13 | 15 | 15 | 20 | 25 | Min. | ns |
| Clock to Data Valid (Std Load) | $t_{CD}$ | 8 | 9 | 10 | 12 | 14 | Max. | ns |
| Clock to Data Valid (0 pF Load) | $t_{CD0}$ | 7 | 8 | 9 | 11 | 13 | Min. | ns |
| Output Enable | $t_{OE}$ | 5 | 5 | 5 | 6 | 7 | Max. | ns |
| Clock to Data Low-Z | $t_{dc1}$ | 3 | 3 | 3 | 3 | 3 | Min. | ns |
| Clock to Data Hold Time | $t_{dc2}$ | 3 | 3 | 3 | 3 | 3 | Min. | ns |
| OE to Output Low-Z(1) | $t_{OLZ}$ | 0 | 0 | 0 | 0 | 0 | Min. | ns |
| OE to Output High-Z(1) | $t_{OHZ}$ | 2 | 2 | 2 | 2 | 2 | Min. | ns |
| | | 5 | 5 | 5 | 6 | 7 | Max. | ns |
| Clock to Data High-Z | $t_{CZ}$ | 6 | 6 | 6 | 7 | 8 | Max. | ns |
| Clock High/Low | $t_W$ | 4 | 4 | 5 | 6 | 7 | Min. | ns |
| Setup Time | $t_S$ | 2.5 | 2.5 | 2.5 | 3 | 3 | Min. | ns |
| Hold Time | $t_H$ | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | Min. | ns |

NOTES: 1. Values characterized and guaranteed by design, not currently tested.
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{TSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{TSP}$ high for the set up and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible i486 external bus cycles.
6. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, $t_{CHZ}$ max is less than $t_{CLZ}$ min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ALL rising edges of K whenever $\overline{TSP}$ or $\overline{TSC}$ is low, and the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when $\overline{TSP}$ or $\overline{TSC}$ is low) to remain enabled.

## TSP Read Timing Diagram

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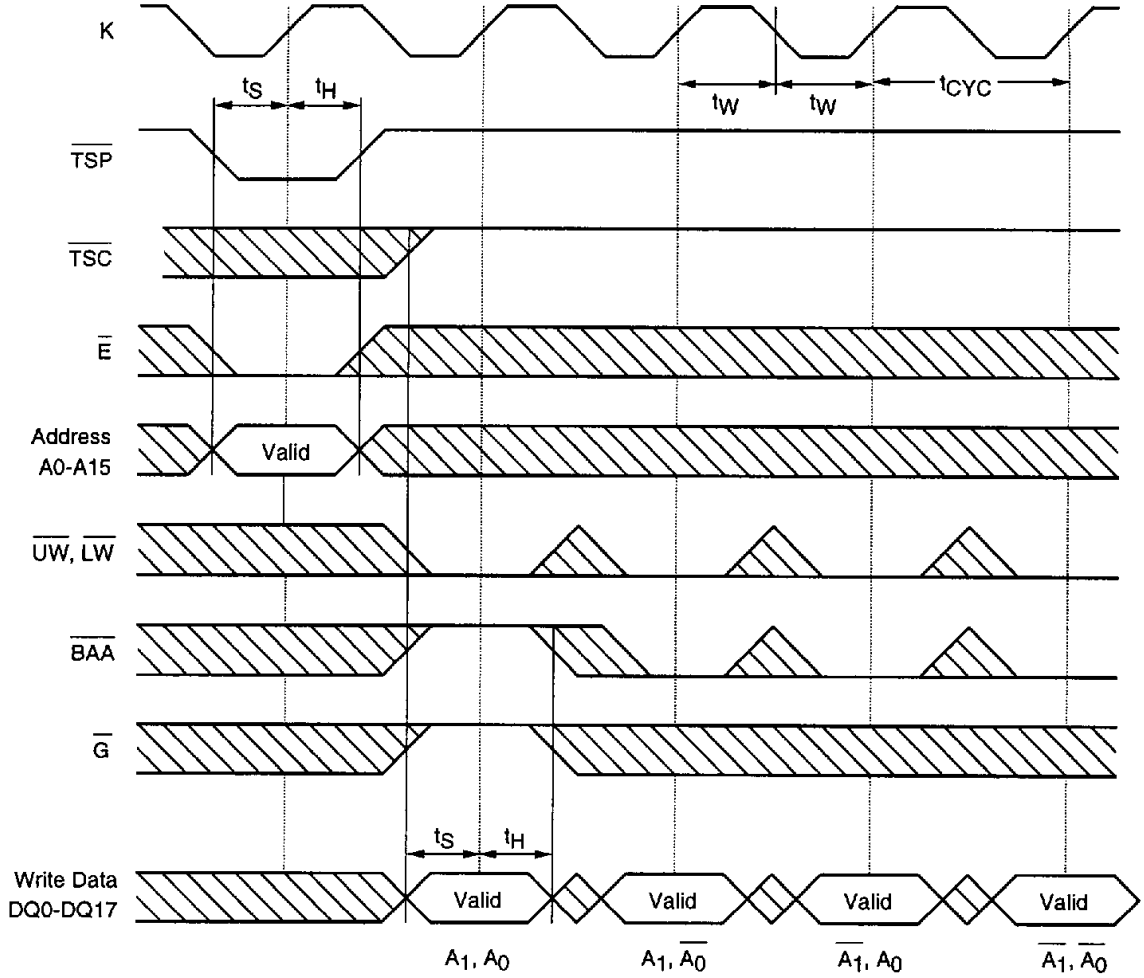
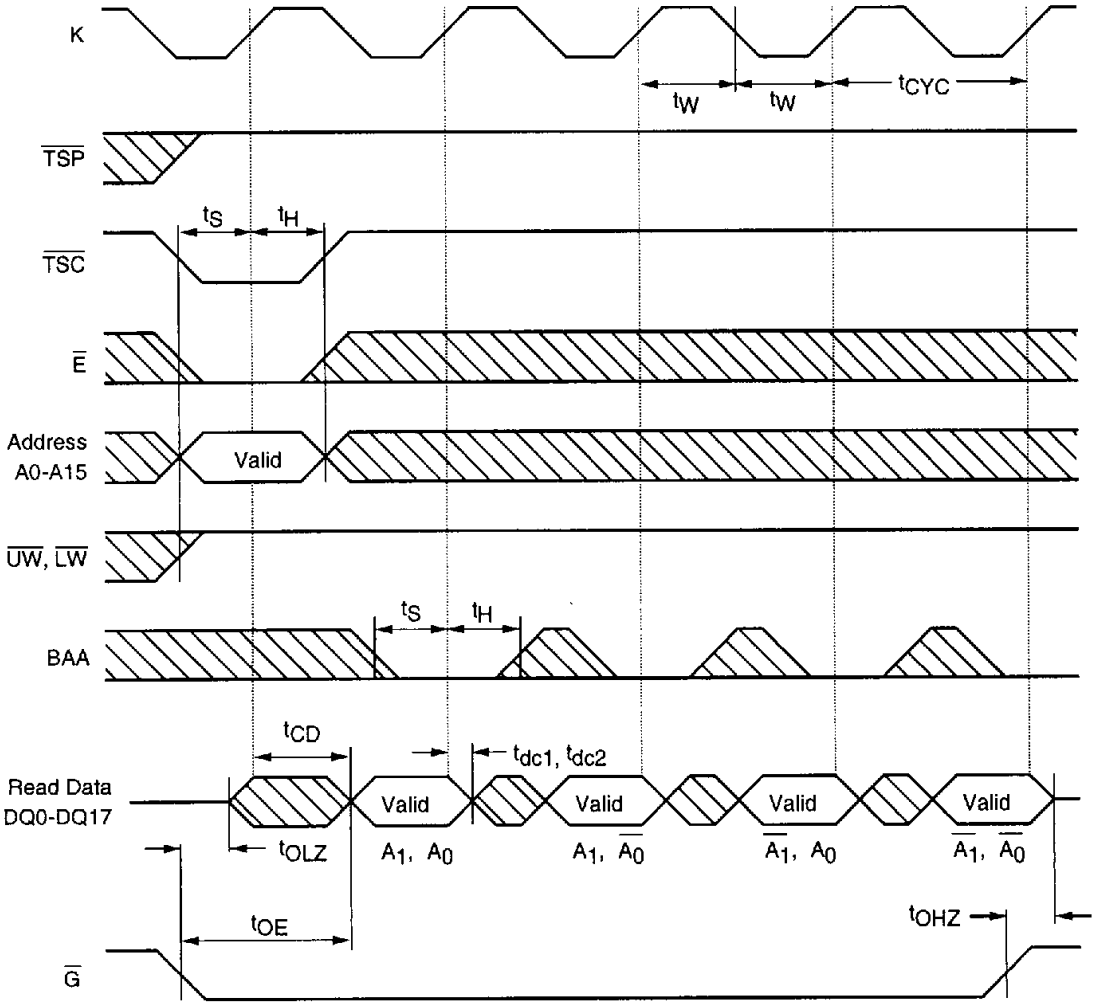
## TSP Write Timing Diagram

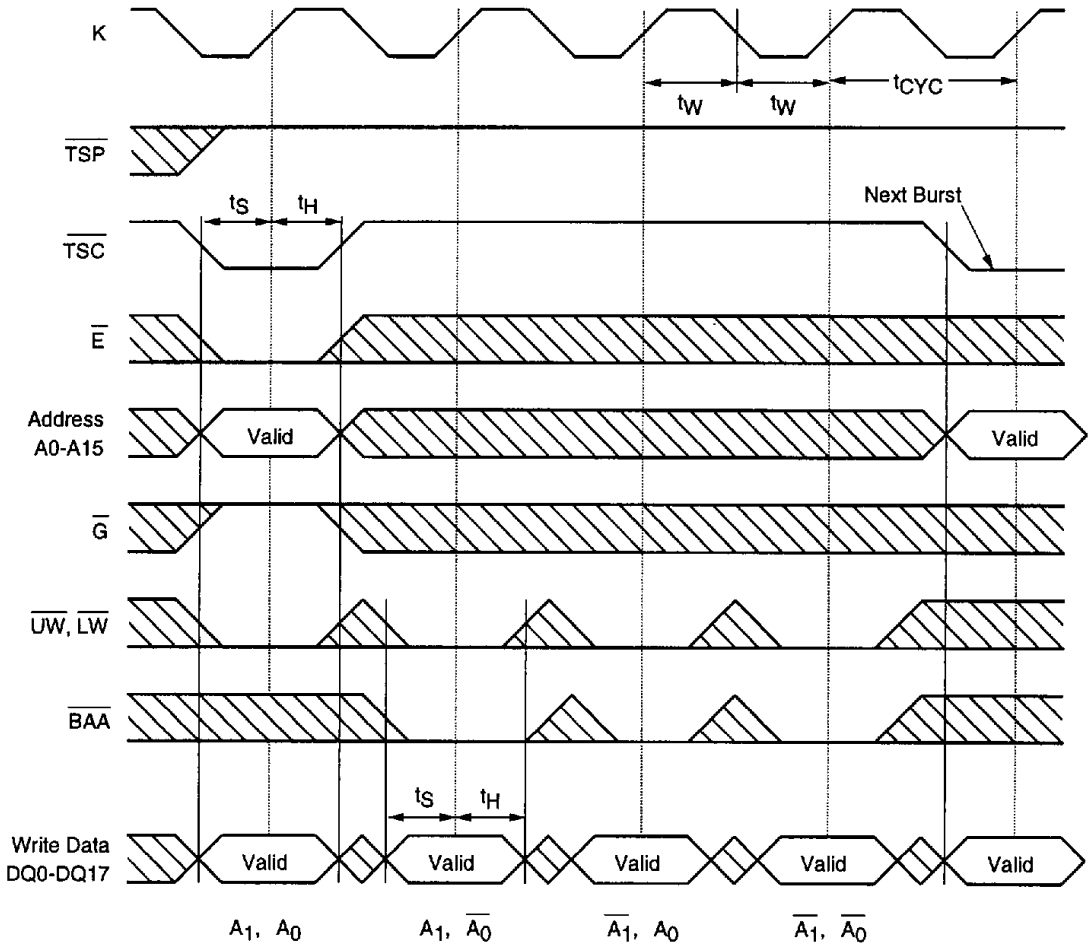



NOTE: UW and LW are ignored for the first cycle when ADSP initiates the burst. ADSP active loads a new address into the address counter and forces the first cycle to be a read cycle.

## TSC Read Timing Diagram

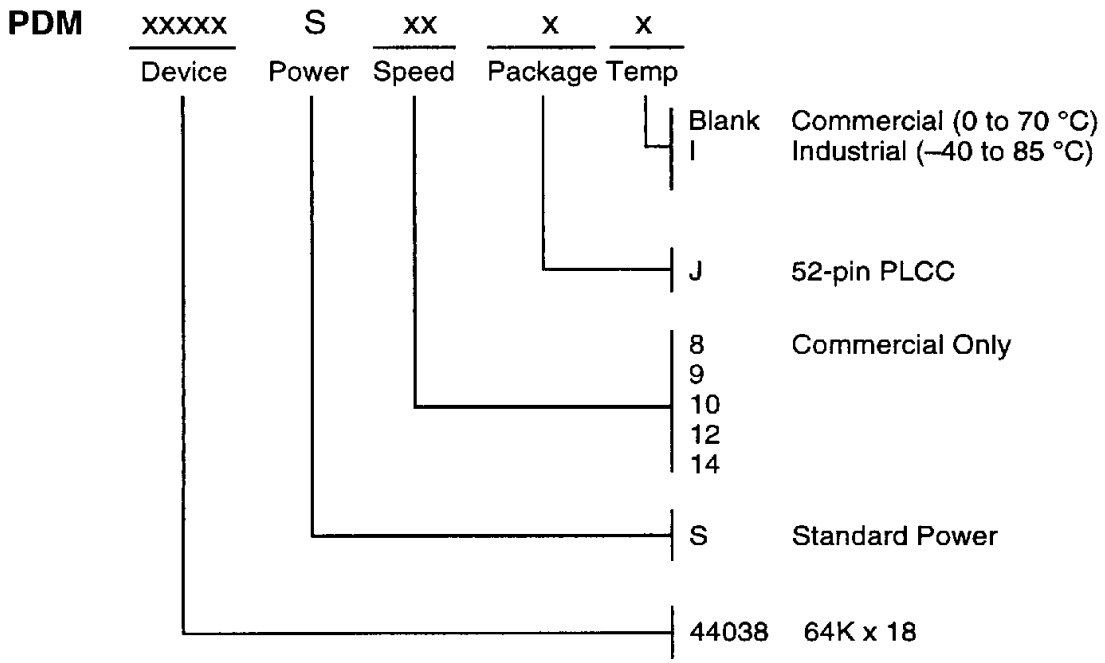


## TSC Write Timing Diagram




NOTE: UW and LW are ignored for the first cycle when ADSP initiates the burst. ADSP active loads a new address into the address counter and forces the first cycle to be a read cycle.

## Ordering Information




| Chip | Description |
|---|---|
| PDM44038 | 52-pin PLCC |