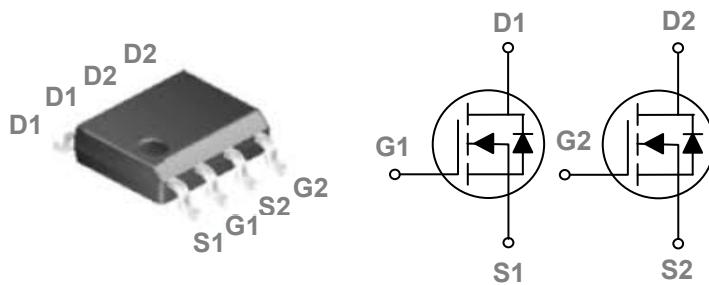


General Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

SOP8 Dual Pin Configuration



BVDSS	RDS(ON)	ID
40V	15mΩ	10A

Features

- 40V, 10A, RDS(ON) = 15mΩ@VGS = 10V
- Improved dv/dt capability
- Fast switching
- 100% EAS Guaranteed
- Green Device Available

Applications

- Motor Drive
- Power Tools
- LED Lighting

Absolute Maximum Ratings $T_c=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current – Continuous ($T_c=25^\circ\text{C}$)	10	A
	Drain Current – Continuous ($T_c=100^\circ\text{C}$)	6.3	A
I_{DM}	Drain Current – Pulsed ¹	40	A
EAS	Single Pulse Avalanche Energy ²	76	mJ
IAS	Single Pulse Avalanche Current ²	39	A
P_D	Power Dissipation ($T_c=25^\circ\text{C}$)	2.1	W
	Power Dissipation – Derate above 25°C	0.017	W/°C
T_{STG}	Storage Temperature Range	-50 to 150	°C
T_J	Operating Junction Temperature Range	-50 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction to ambient	---	60	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)
Off Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$	40	---	---	V
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=40\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{\text{DS}}=32\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=125^\circ\text{C}$	---	---	10	μA
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 100	nA

On Characteristics

$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance	$V_{\text{GS}}=10\text{V}$, $I_D=8\text{A}$	---	12	15	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}$, $I_D=6\text{A}$	---	15	20	$\text{m}\Omega$
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}$, $I_D = 250\mu\text{A}$	1.2	1.8	2.5	V
g_{fs}	Forward Transconductance	$V_{\text{DS}}=10\text{V}$, $I_D=1\text{A}$	---	5	---	S

Dynamic and switching Characteristics

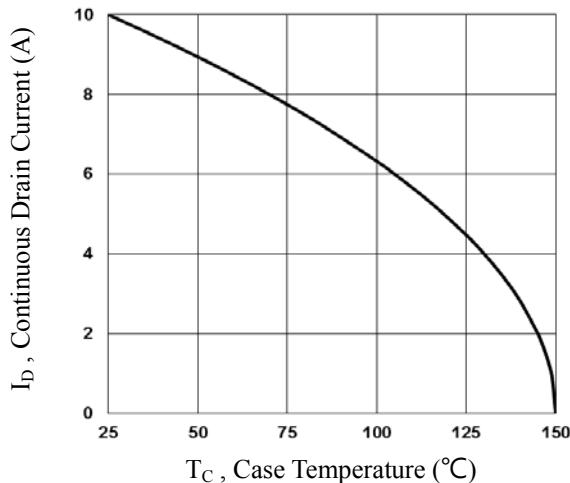
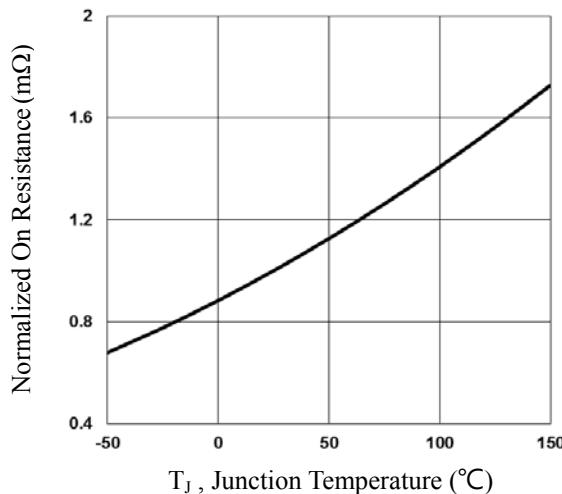
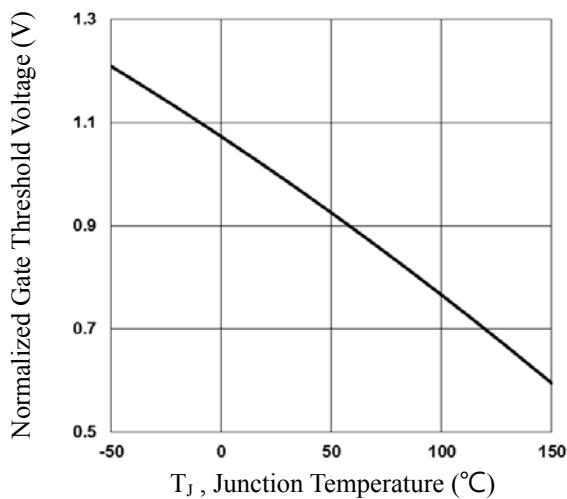
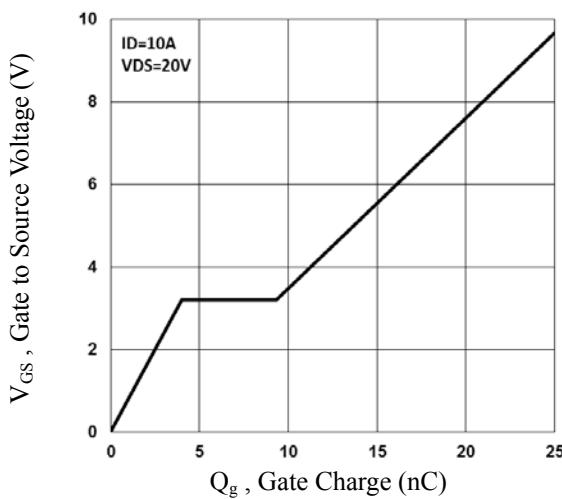
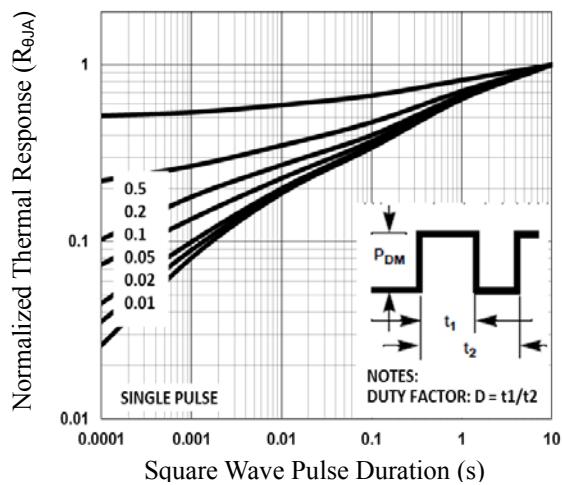
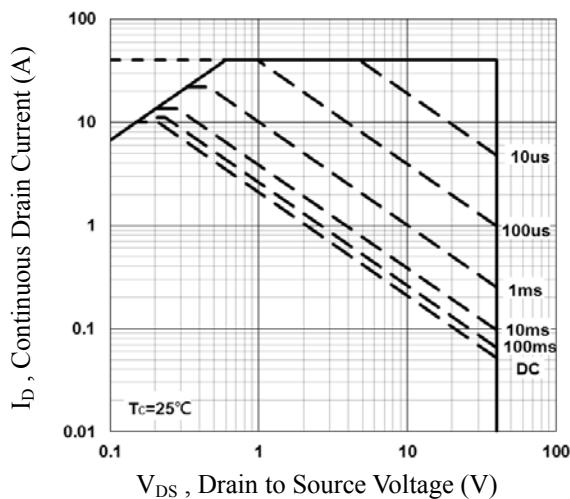
Q_g	Total Gate Charge ^{3, 4}	$V_{\text{DS}}=20\text{V}$, $V_{\text{GS}}=4.5\text{V}$, $I_D=10\text{A}$	---	13	26	nC
Q_{gs}	Gate-Source Charge ^{3, 4}		---	4	8	
Q_{gd}	Gate-Drain Charge ^{3, 4}		---	5.3	10	
$T_{\text{d(on)}}$	Turn-On Delay Time ^{3, 4}	$V_{\text{DD}}=20\text{V}$, $V_{\text{GS}}=10\text{V}$, $R_G=6\Omega$ $I_D=1\text{A}$	---	8	16	ns
T_r	Rise Time ^{3, 4}		---	3.2	8	
$T_{\text{d(off)}}$	Turn-Off Delay Time ^{3, 4}		---	26.4	52	
T_f	Fall Time ^{3, 4}		---	3.8	8	
C_{iss}	Input Capacitance	$V_{\text{DS}}=20\text{V}$, $V_{\text{GS}}=0\text{V}$, $F=1\text{MHz}$	---	1088	2000	pF
C_{oss}	Output Capacitance		---	110	200	
C_{rss}	Reverse Transfer Capacitance		---	80	160	
R_g	Gate resistance	$V_{\text{GS}}=0\text{V}$, $V_{\text{DS}}=0\text{V}$, $F=1\text{MHz}$	---	3	6	Ω

Drain-Source Diode Characteristics and Maximum Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_s	Continuous Source Current	$V_G=V_D=0\text{V}$, Force Current	---	---	10	A
			---	---	20	A
V_{SD}	Diode Forward Voltage	$V_{\text{GS}}=0\text{V}$, $I_s=1\text{A}$, $T_J=25^\circ\text{C}$	---	---	1	V

Note :

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. $V_{\text{DD}}=25\text{V}$, $V_{\text{GS}}=10\text{V}$, $L=0.1\text{mH}$, $I_{\text{AS}}=39\text{A}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$.
3. The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
4. Essentially independent of operating temperature.


Fig.1 Continuous Drain Current vs. T_C

Fig.2 Normalized RD_{SON} vs. T_J

Fig.3 Normalized V_{th} vs. T_J

Fig.4 Gate Charge Waveform

Fig.5 Normalized Transient Impedance

Fig.6 Maximum Safe Operation Area

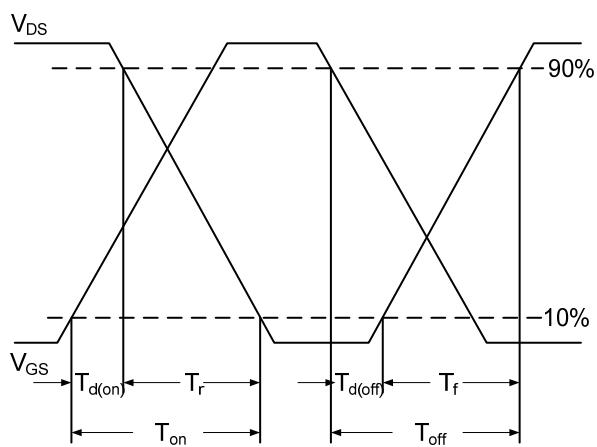


Fig.7 Switching Time Waveform

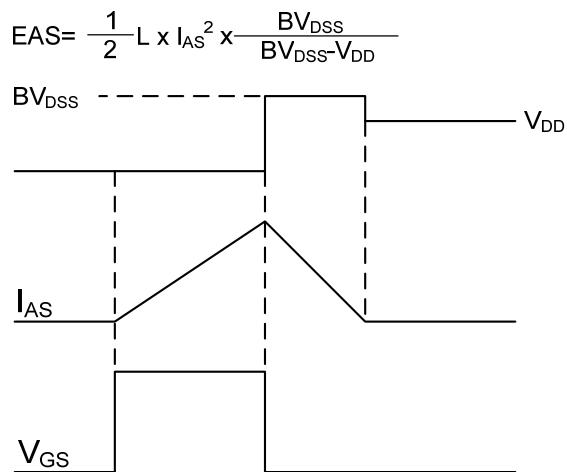
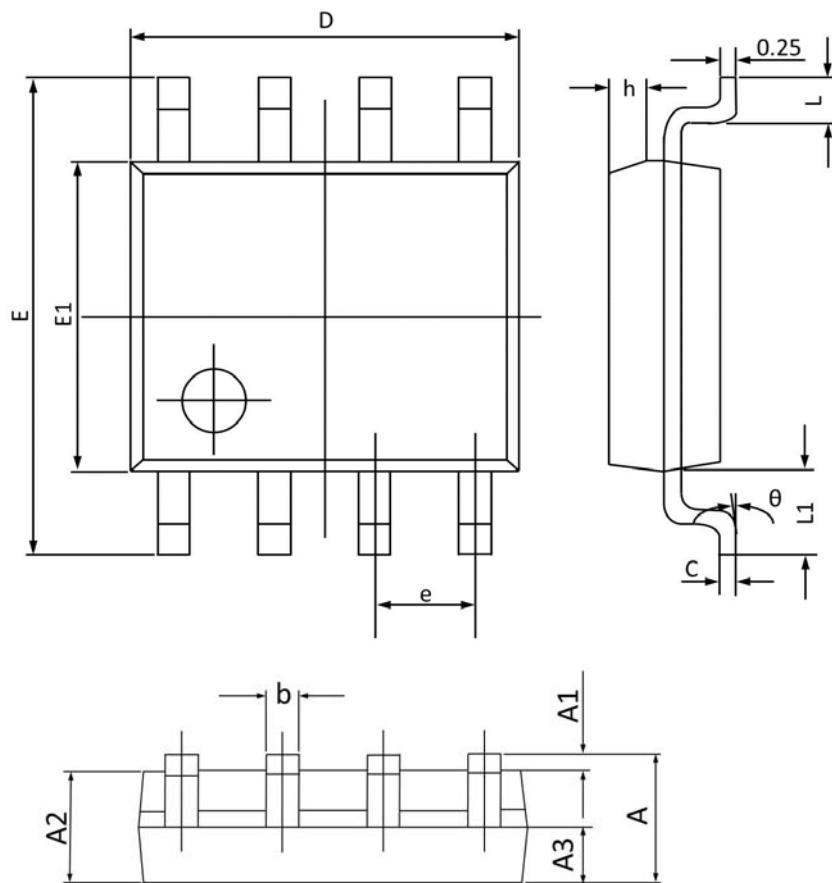


Fig.8 EAS Waveform

SOP8 PACKAGE INFORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.068
A1	0.100	0.250	0.004	0.009
A2	1.300	1.500	0.052	0.059
A3	0.600	0.700	0.024	0.027
b	0.390	0.480	0.016	0.018
c	0.210	0.260	0.009	0.010
D	4.700	5.100	0.186	0.200
E	5.800	6.200	0.229	0.244
E1	3.700	4.100	0.146	0.161
e	1.270(BSC)		0.050(BSC)	
h	0.250	0.500	0.010	0.019
L	0.500	0.800	0.019	0.031
L1	1.050(BSC)		0.041(BSC)	
θ	0°	8°	0°	8°