

This product is obsolete.

This information is available for your convenience only.

For more information on Zarlink's obsolete products and replacement product lists, please visit

http://products.zarlink.com/obsolete_products/



PDSP16112/PDSP16112A

16 x 12 BIT COMPLEX MULTIPLIER

(Supersedes version in December 1993 Digital Video & Video Digital Signal Processing IC Handbook, HB3923-1)

The PDSP16112/PDSP16112A will multiply a complex (16 + 16) bit word by a complex (12 + 12) bit coefficient word and produce a complex (17 + 17) bit rounded product. The input data format is two's complement. The device consists of four 16 x 12 multiplier sections based on Booth's '2 bits at a time' algorithm and is pipelined to achieve a 20MHz (PDSP16112A) or 10MHz (PDSP16112) throughput.

FEATURES

- 20MHz Complex Number (16 + 16) x (12 + 12) Multiplication
- Pipeline Architecture
- Power Dissipation only 500mW
- TTL Compatible Inputs
- 120 pin PGA or QFP packages

APPLICATIONS

- Digital Filtering
- Fast Fourier Transforms
- Radar and Sonar Processing
- Instrumentation
- Automation
- Image Processing

ASSOCIATED PRODUCTS

PDSP1601	Arithmetic Logic Unit
PDSP16318	40MHz Address Generator
PDSP16330	Pythagoras Processor

	A INDEX OP SUR 1			3	4	5	6	7	8	9	10	11	12	13	
	VC	0	GND	P107	PI10	P113	PI16	IC	GND	PR15	PR12	PR09	PR06	VCC	٦
Α	0 P10		O NC	O P106	O P109	0 PI12	O PI15	O CLK	0	O PR 14	O PR11	O PR08	O GND	O PR03	
в	0		0	0	0	0	0	0	0	0	0	0	0	0	
с	PIO O	-	P105 O		P108 0	Р 11 О	0 0	GND O	PR 16 0	PR 13	PR10 O	PR07	PR05	PR02 O	
D	PIO O		P101 O	P104	Q							PR04 O	PR01 O	PR00 O	
Е	×10 O		vcc 0	GND O			OITAC		NC)				GND O	V00 0	
F	X10 O		X 102	X101 O		LO	Ano		110,			GND O	XROO O	XR01 O	
G			X 104									XROS O	XR04 O	XR02	
н	XIO O		X 107	X108 O		PIN			RR/	١Y		XR07 O		XR05	
J	хю		x110 O	XI11 O				C12				XR 10 0	XRO9	XR08	
к	XI1 O	2	XI13 O	YI11 O					-			XR15	XR12	XR11 O	
L	XI1	4		YI10	Y107 O	Y104 O	Y101 O	CLK O		YR04 O	YR07 Ö	YR10	YR11	XR13	
-	XI1	5	NC	Y109	YI06	Y 103	Y 100	GND	YR00	YR 03	YR06	YR09	NC	XR14	
M		0		O YI08	O YI05	0 YI02	GND	GND	GND	O YR02	O YR05	O YR08	GND	o voc	
Ν	0		0	0	0	0	0	0	0	0	0	0	0	0	
XRxx : X REAL INPUTS XIxx : X IMAGINARY INPUTS YRxx : Y REAL INPUTS YIxx : Y IMAGINARY INPUTS PRxx : PRODUCT REAL OUTPUTS PIxx : PRODUCT IMAGINARY OUTPUTS															
AC12	\ <u>C120</u>														

Fig.1 Pin connections - top view (AC120 - PGA)

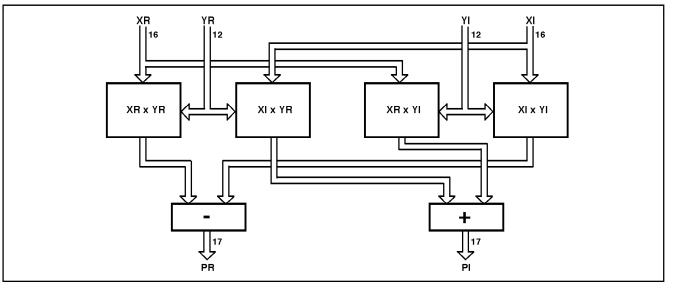


Fig. 2 Multiplier block diagram

PDSP16112/A

Symbol	Pin No.						
PR00	D13	PR09	A11	P100	D1	P109	B4
PR01	D12	PR10	C10	PI01	D2	PI10	A4
PR02	C13	PR11	B10	PI02	C1	PI11	C5
PR03	B13	PR12	A10	PI03	B1	PI12	B5
PR04	D11	PR13	C9	PI04	D3	PI13	A5
PR05	C12	PR14	B9	PI05	C2	PI14	C6
PR06	A12	PR15	A9	P106	B3	PI15	B6
PR07	C11	PR16	C8	PI07	A3	PI16	A6
PR08	B11	CLK	L7	PI08	C4	CLK	B7
XR00	F12	X100	E1	YR00	M8	Y100	M6
XR01	F13	XI01	F3	YR01	L8	YI01	L6
XR02	G13	X102	F2	YR02	N9	Y102	N5
XR03	G11	X103	F1	YR03	M9	Y103	M5
XR04	G12	X104	G2	YR04	L9	YI04	L5
XR05	H13	X105	G1	YR05	N10	Y105	N4
XR06	H12	X106	H1	YR06	M10	Y106	M4
XR07	H11	X107	H2	YR07	L10	Y107	L4
XR08	J13	X108	НЗ	YR08	N11	Y108	N3
XR09	J12	X109	J1	YR09	M11	Y109	МЗ
XR10	J11	XI10	J2	YR10	L11	YI10	L3
XR11	K13	XI11	J3	YR11	L12	YI11	КЗ
XR12	K12	XI12	K1	NC	B2	NC	M12
XR13	L13	XI13	K2	NC	L2	NC	M2
XR14	M13	XI14	L1	VCC	A1	NC	E11
XR15	K11	XI15	M1	VCC	G3	NC	СЗ
GND	N12	GND	C7	VCC	E2	GND	N8
GND	N7	GND	A2	VCC	A13	GND	N6
GND	M7	GND	E12	VCC	E13	GND	F11
GND	N2	GND	E3	VCC	N1	IC	B8
GND	A8	GND	B12	VCC	N13	IC	A7

PIN OUT - FUNCTION TO PIN (PGA Package - AC120)

NOTE

IC = Internally connected - do not connect to these pins.

All inputs are internally connected to Vcc by 10k (nominal) resistors.

PIN OUT - PIN TO FUNCTION (PGA Package - AC120)

	1	2	3	4	5	6	7	8	9	10	11	12	13
Α	VCC	GND	P107	PI10	PI13	P116	IC	GND	PR15	PR12	PR09	PR06	VCC
в	P103	NC	P106	P109	PI12	PI15	CLK	IC	PR14	PR11	PR08	GND	PR03
С	P102	P105	NC	P108	PI11	PI14	GND	PR16	PR13	PR10	PR07	PR05	PR02
D	P100	PI01	P104								PR04	PR01	PR00
Е	X100	VCC	GND								NC	GND	VCC
F	X103	X102	XI01								GND	XR00	XR01
G	XI05	XI04	VCC								XR03	XR04	XR02
н	X106	X107	X108								XR07	XR06	XR05
J	X109	XI10	XI11								XR10	XR09	XR08
κ	XI12	XI13	YI11								XR15	XR12	XR11
L	XI14	NC	YI10	YI07	YI04	YI01	CLK	YR01	YR04	YR07	YR10	YR11	XR13
м	XI15	NC	YI09	Y106	YI03	YI00	GND	YR00	YR03	YR06	YR09	NC	XR14
Ν	VCC	GND	Y108	YI05	YI02	GND	GND	GND	YR02	YR05	YR08	GND	VCC

GG SIG SIG SIG GG GG GG SIG 84 **PR00 PR09** PI00 P109 95 8 115 85 **PR01** 96 **PR10** 7 PI01 114 PI10 86 **PR02** 97 PR11 6 PI02 113 PI11 87 **PR03** 98 **PR12** 5 PI03 112 PI12 88 **PR04** 99 **PR13** 4 PI04 **PI13** 111 89 **PR05** 100 **PR14** 3 PI05 110 PI14 92 **PR06** 101 **PR15** 118 PI06 109 PI15 93 **PR07 PR16** PI07 102 117 108 PI16 94 **PR08** CLK 46 116 PI08 105 CLK 79 X100 XR00 11 49 **YR00** 43 Y100 78 XR01 12 XI01 50 YR01 42 YI01 77 XI02 YI02 XR02 13 51 YR02 41 76 XI03 YI03 XR03 14 52 YR03 40 www.DataSheet4U.com 75 15 XI04 53 YI04 XR04 YR04 39 74 XR05 XI05 54 **YR05** YI05 17 38 73 XR06 18 XI06 55 **YR06** 37 YI06 72 XR07 XI07 56 YI07 19 YR07 36 71 XR08 20 X108 57 **YR08** 35 Y108 70 XI09 XR09 YR09 Y109 21 58 34 69 **XR10** XI10 **YR10** YI10 22 59 33 68 XR11 XI11 **YR11** 23 63 28 YI11 N/C 67 XR12 24 XI12 N/C 29 1 XR13 25 XI13 N/C N/C 66 16 31 65 XR14 XI14 VCC N/C 26 2 61 VCC 64 XR15 27 XI15 10 N/C 83 VCC 9 GND 45 GND 30 GND 44 32 GND 47 GND VCC GND 62 48 104 VCC 60 GND GND 81 80 GND VCC 82 GND 106 GND 90 103 I/C 91 GND 120 GND N/C I/C 119 107

PIN OUT - PIN TO FUNCTION (PGA Package - AC120)

N/C = Not connected - leave open circuit

I/C = Internally connected - leave open circuit

All GND and VDD pins must be used

PIN DESCRIPTION

XR00 - XR15	X Real Inputs : Two's Complement Format XR15 = MSB (Sign) XR00 = LSB For Fractional Arithmetic the Weighting of XR15 = 1 i.e. $-1 \le XR < 1$	PR00 - PR16	P Real Inputs : Two's Complement Format PR16 = MSB (Sign) PR00 = LSB For Fractional Arithmetic the Weighting of PR16 = 2 i.e. $-2 \le PR < 2$
XI00 - XI15	X Imag Inputs : Two's Complement Format XI15 = MSB (Sign) XI00 = LSB For Fractional Arithmetic the Weighting of XI15 = 1 i.e. $-1 \le XI \le 1$	Pl00 - Pl16	P Imag Outputs : Two's Complement Format PI16 = MSB (Sign) PI00 = LSB For Fractional Arithmetic the Weighting of PI16 = 2 i.e. $-2 \le PI \le 2$
YR00 - YR11	Y Real Inputs ∶ Two's Complement Format YR11 = MSB (Sign) YR00 = LSB For Fractional Arithmetic the Weighting of YR11 = 1 i.e1 ≤YR<1	CLK pin B7 and Pin L7 VCC GND	Common Clock to all on chip registers, both pins must be connected All VCC and GND pins must be connected
YI00 - YI11 Sheet4U.com	Y Imag Inputs : Two's Complement Format YI11 = MSB (Sign) YI00 = LSB For Fractional Arithmetic the Weighting of YI11 = 1 i.e. $-1 \le YI \le 1$	IC	Internally connected - do not use

FUNCTIONAL DESCRIPTION

The PDSP16112 Complex Multiplier contains four pipeline 16 x 12 Array Multipliers, a 17-bit adder and a 17-bit subtractor.

The multipliers accept data from the XR, XI, YR, and YI inputs and perform the four multiplies necessary to implement a Complex Multiply Operation.

(XR x YR, XR x YI, XI x YR, XI x YI).

The 28-bit results from these operations are rounded to the most significant 16-bits before being passed to the adder and subtractor. The subtractor calculates

 $(XR \times YR) - (XI \times YI)$

to form a 17-bit result representing the real result of the complex multiplication. The adder calculates

 $(XR \times YI) + (XI \times YR)$

to form a 17-bit result that represents the imaginary result of the complex multiplication. These real and imaginary results are passed to the PR and PI outputs respectively.

The add and subtract operations may (depending upon the data) cause the multiplier results to grow by one bit hence requiring 17-bit outputs to represent the results. The PDSP16112 is designed to operate with two's complement arithmetic, hence if the Fractional two's complement format is used the outputs will lie in the range

-2 ≤P<2

for inputs in the range

-1 ≤X or Y<1

If the output magnitude lies in the range

-1 ≤P<1,

then the 17th (MSB) bit of the outputs will duplicate the 16th (Sign) bit of the output.

In common with other Array multipliers, the operation

-1 x -1

will yield an incorrect result for fractional two's complement formats, and hence should be avoided.

Both X and Y inputs are registered as are the PR and PI outputs. On the rising edge of CLK data present on the XR, XI, YR and YI inputs is clocked into the input registers. At the same time a new result is clocked into the output registers and made available on the PR and PI output ports.

Pipelined Operation

The internal Multiply and Add operations are divided into stages by six internal pipeline registers giving a total latency through the device of eight clock cycles. This means that the result from data loaded into the device on the first clock cycle appears at the outputs during the seventh clock cycle, and may be loaded into another device on the eight clock cycle.

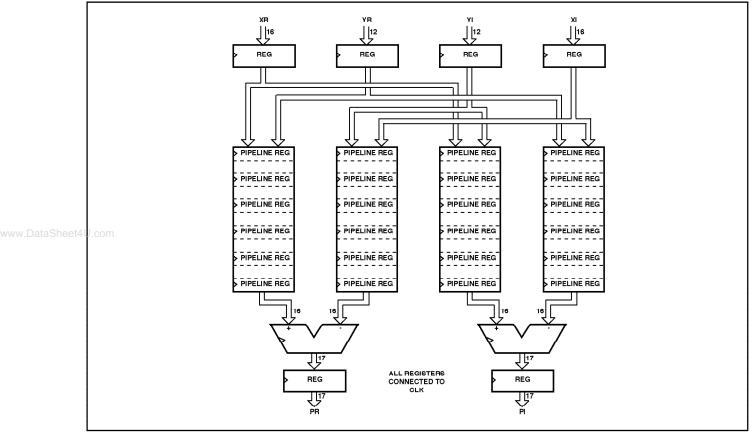


Fig.3 Pipeline multiplier structure

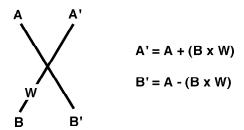
TYPICAL APPLICATION

The PDSP16112A may be configured as the main arithmetic element in the FFT Butterfly calculation. A single PDSP16112A together with two PDSP16318As will produce an arithmetic processor capable of executing a new Radix 2 DIT Butterfly every 50ns using 16-bit data and 12-bit coefficients. The PDSP16318A provides flags that monitor the magnitude of the output data, together with on chip shift circuits.

A single Butterfly processor of this type will allow the following FFT benchmarks.

1024 point complex radix 2 transform in 256µsecs 512 point complex radix 2 transform in 115µsecs 256 point complex radix 2 transform in 51µsecs

The arithmetic operation required to realise a radix 2 decimation in time algorithm is as follows.



Where A and B are the data inputs, A' and B' are the data outputs, and W is the coefficient. A,B,A',B' and W are all complex numbers i.e. they all have real and imaginary components. The Butterfly therefore requires one complex multiply and two complex adds to execute, which is equivalent to four real multiplies and six real adds.

Fig.4 illustrates the interconnection of the PDSP16112A with the two PDSP16318A Complex Accumulators. The PDSP16112A performs the complex multiply operation at the full 20MHz rate to provide the real and imaginary components of the (B x W) to the two ALUs. The PDSP16318A is capable of 16-bit operations at 20MHz and has on chip register storage and Shifter. In every 20MHz cycle each PDSP16318A performs two arithmetic operations to calculate the real or imaginary parts of A + (B x W) and A - (B x W). One of the PDSP16318As calculates the real parts and the other calculates the imaginary parts.

For greater throughput one chip-set mat be allocated to each column of the FFT. For example, a 1K complex FFT could be calculated by 10 chip-sets every $26\mu s$.

PDSP16112/A

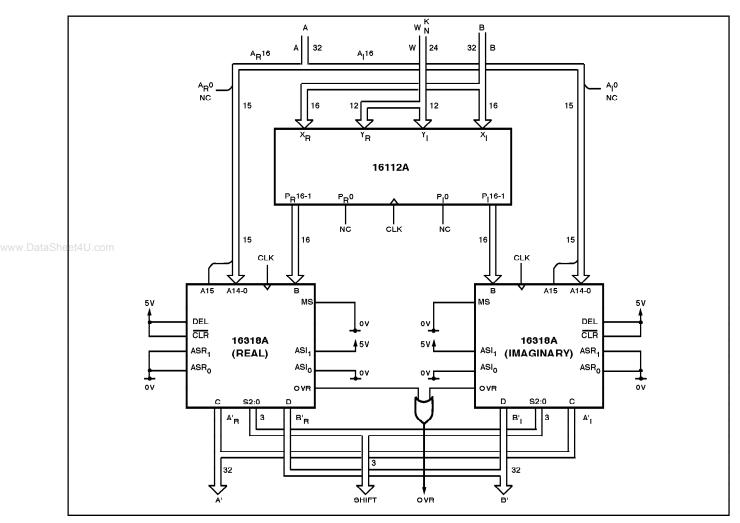


Fig.4 Radix 2 DIT butterfly processor

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): T_{amb} (Industrial) =-40°C to +85°C, Vcc = 5.0V ± 10%, GND = 0V

- $\mathsf{T}_{\mathsf{amb}} \; (\mathsf{Military}) = -55^\circ \mathsf{C} \; \mathsf{to} \; + 125^\circ \mathsf{C}, \; \mathsf{Vcc} = 5.0 \mathsf{V} \pm 10\%, \; \mathsf{GND} = \mathsf{0V}$
- ${\rm T}_{\rm amb}$ (Commercial) = 0°C to +70°C, Vcc = 5.0V \pm 5%, GND = 0V

Static Characteristics

				Val	lue				
Characteristics	Symbol	P	DSP16	112	PC	SP1611	2A	Units	Conditions
		Min.	Тур.	Max.	Min.	Тур.	Max.		
Output high voltage Output low voltage Input high voltage Input low voltage Input leakage current * Output short circuit current Input capacitance	V _{oh} V _{ol} ^H V ^H L _l C ₁	2.4 2.8 -1.2 30	10	0.6 0.8 +0.01 200	2.4 2.8 -1.2 40	10	0.6 0.8 +0.01 200	V V MA pF	$I_{OH} = 4mA$ $I_{OL} = -4mA$ $GND \le V_{IN} \le V_{CC}$ $V_{CC} = max$

* All inputs have a nominal 10K pull resistor to Vcc.

AC Characteristics

					lue strial				lue tary		
Characteristic	Symbol	PD	SP161	12	PDS	SP161 ⁻	2A			Units	Conditions
	5	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.		
Vcc current	lcc			90			170		90	mA	Vcc = max Outputs unloaded f _{ськ} = max
Max. CLK frequency	fc∟ĸ	10			20			10		MHz	I _{CLK} – max
Min. CLK frequency				DC			DC		DC		
Input setup time	tsu			30			20		30	ns	
Input hold time	tin			5			5		5	ns	
CLK to output delay	ta	5		50	5		30	5	50	ns	
CLK Mark/Space ratio		40		60	40		60	40	60	%	
Drive capability					2 x LS	TTL +2	20pF				

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply voltage Vcc	-0.5V to 7.0V
Input voltage VIN	-0.5V to Vcc +0.5V
Output voltage Vout	-0.5V to Vcc +0.5V
Clamp diode current per lk (see Note	e 2) ±18mA
Static discharge voltage	500V
Storage temperature range Ts	-65°C to +150°C
Junction temperature	150°C
Ambient temperature with	
power applied Tamb	
Commercial	0°C
	to +70°C
Industrial	-

	44°C to +85°C
Military	-55°C to
-	+125°C
Package power dissipation PTOT	1000mW

NOTES

1. Exceeding these ratings may cause permanent damage.

Functional operation under these conditions is not implied.

2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.

3. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Package Type	<i>θ</i> JC ° C/W	<i>θ</i> ja ° C/W
AC	12	35

ORDERING INFORMATION

Commercial (0°C to +70°C)

PDSP16112 C0 AC (10MHz - PGA) PDSP16112A C0 AC (20MHz - PGA) PDSP16112A C0 GG (20MHz - QFP)

Industrial (-40°C to +85°C)

PDSP16112 B0 AC (10MHz - PGA) PDSP16112A B0 AC (20MHz - PGA) PDSP16112A B0 GG (20MHz - QFP) **Military** $(-55^{\circ}C \text{ to } + 125^{\circ}C)$

PDSP16112 A0 AC (10MHz - PGA) PDSP16112A A0 AC (20MHz - PGA) PDSP16112A A0 GG (20MHz - QFP)

Call for availability on High Reliability parts and MIL-883C screening.



www.DataSheet4U.com

For more information about all Zarlink products visit our Web Site at

www.zarlink.com

Information relating to products and services furnished herein by Zarlink Semiconductor Inc. or its subsidiaries (collectively "Zarlink") is believed to be reliable. However, Zarlink assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Zarlink or licensed from third parties by Zarlink, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Zarlink, or non-Zarlink furnished goods or services may infringe patents or other intellectual property rights owned by Zarlink or licensed from third parties by Zarlink.

This publication is issued to provide information only and (unless agreed by Zarlink in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Zarlink without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Zarlink's conditions of sale which are available on request.

Purchase of Zarlink's I²C components conveys a licence under the Philips I²C Patent rights to use these components in and I²C System, provided that the system conforms to the I²C Standard Specification as defined by Philips.

Zarlink, ZL and the Zarlink Semiconductor logo are trademarks of Zarlink Semiconductor Inc.

Copyright Zarlink Semiconductor Inc. All Rights Reserved.

TECHNICAL DOCUMENTATION - NOT FOR RESALE